Microchip

27HC1616

256K (16K x 16) High Speed CMOS Erasable PROM

FEATURES

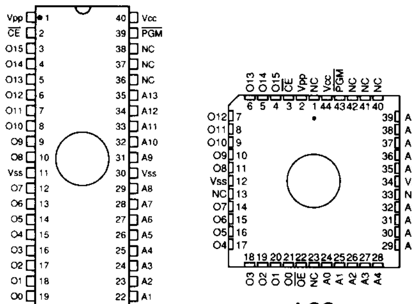
- 16 bit configuration
- High speed performance
  - —55ns access time available
- CMOS Technology for low power consumption
  - —90mA Active current
  - —50mA Standby current
- WordWide architecture offers space saving over Bytewide memories
- Organized 16K x 16: JEDEC standard pinouts
  - —40-Pin ceramic dual in line package
  - —44-Pin ceramic leadless chip carrier
- Temperature range available:
  - —Commercial: 0°C to +70°C
  - —Industrial: -40°C to +85°C

DESCRIPTION

The Microchip Technology Inc. 27HC1616 is a CMOS 16K x 16 (256K) Programmable Read Only Memory. The device operates at Bipolar PROM speeds but uses far less current than any Bipolar PROM. The 27HC1616 is an excellent choice for any application requiring blazing speeds and low power consumption. The word wide (16 bit) architecture can replace two 8 bit EPROMS in any 16 bit application saving valuable printed circuit space and components costs. Typical applications for the 27HC1616 include automotive systems control, high speed modems, digital signal processing, or any application that uses the 80386, 68030, 29000, etc. high performance microprocessors.

PIN CONFIGURATION

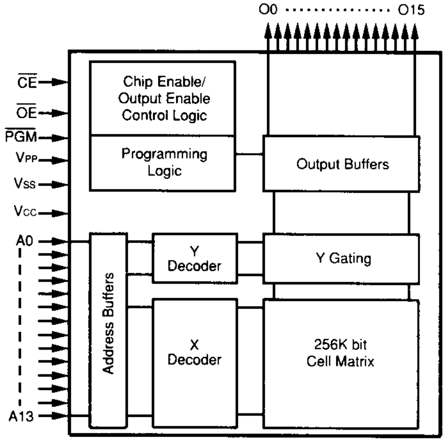
Top View



LCC

DIP

BLOCK DIAGRAM



PIN FUNCTION TABLE

Name	Function
A0 - A13	Address Inputs
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
PGM	Program Enable
VPP	Programming Voltage
O0 - O15	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ....-0.6V to +14.0V
Voltage on A9 w.r.t. VSS ....-0.6V to +13.5V
Output voltage w.r.t. VSS ....-0.6V to VCC +1.0V
Temperature under bias ....-65°C to 125° C
Storage temperature ....-65°C to 150° C
ESD protection on all pins 2KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C

Parameter	Part	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1"	VIH	2.0	VCC+1	V	
		Logic "0"	VIL	-0.1	0.8	V	
Input Leakage	all		ILI	-10	10	µA	VIN = -0.1 to VCC + 1.0V
Output Voltages	all	Logic "1"	VOH	2.4		V	IOH = - 2mA
		Logic "0"	VOL		0.45	V	IOL = 8mA
Output Leakage	all		ILO	-10	10	µA	VOUT = -0.1 to VCC + 0.1V
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb= 25° C; f = 1MHz
Power Supply Current, Active	all	TTL input	ICC		90	mA	VCC = 5.5V; VPP = VCC f = 2MHz; $\overline{\text{OE}}$ = $\overline{\text{CE}}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	all		ICC		50	mA	
IPP Read Current	all	Read Mode	IPP		100	µA	VPP = 5.5V
VPP Read Voltage	all	Read Mode	VPP	VCC-0.7	VCC	V	Note 2

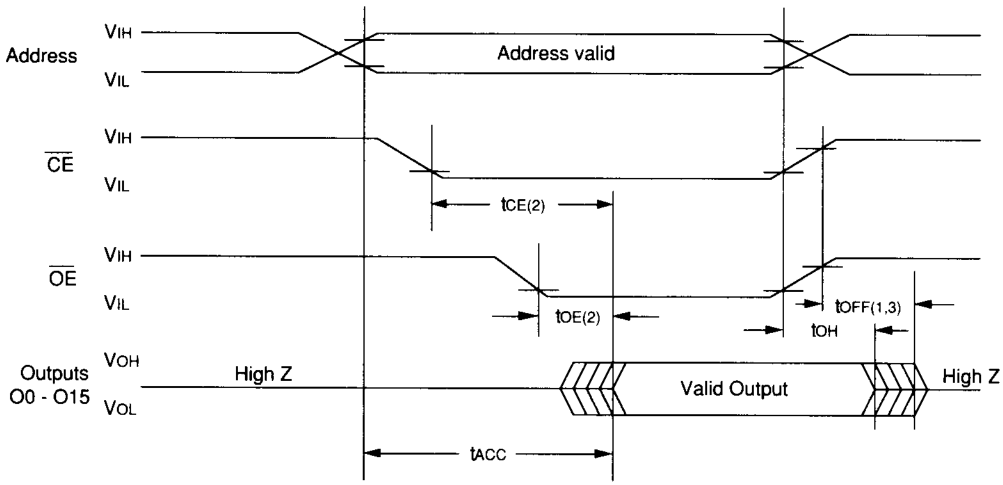
Notes: (1) Active current increases 2 mA per MHz up to operating frequency.
(2) VCC must be applied simultaneously or before VPP and be removed simultaneously or after VPP.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 3.0 V and V_{IL} = 0.0 V; V_{OH} = V_{OL} = 1.5 V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 nsec
Ambient Temperature: Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C

Parameter	Part	Sym	27HC1616-55		27HC1616-70		Units	Conditions
			Min	Max	Min	Max		
Address to Output Delay	all	t_{ACC}		55		70	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	all	t_{CE2}		35		45	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	all	t_{OE}		30		35	ns	$\overline{CE} = V_{IL}$
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	all	t_{OFF}	0	20	0	25	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	all	t_{OH}	0		0		ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

PROGRAMMING
DC Characteristics

Ambient Temperature: 25° C ±5° C
For V_{PP} and V_{CC} Voltages refer to Programming Algorithm

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = -.1V to V_{CC} + 1.0V
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = - 2mA I_{OL} = 8mA
V_{CC} Current, program & verify		I_{CC}		90	mA	Note 1
V_{PP} Current,program		I_{PP}		50	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

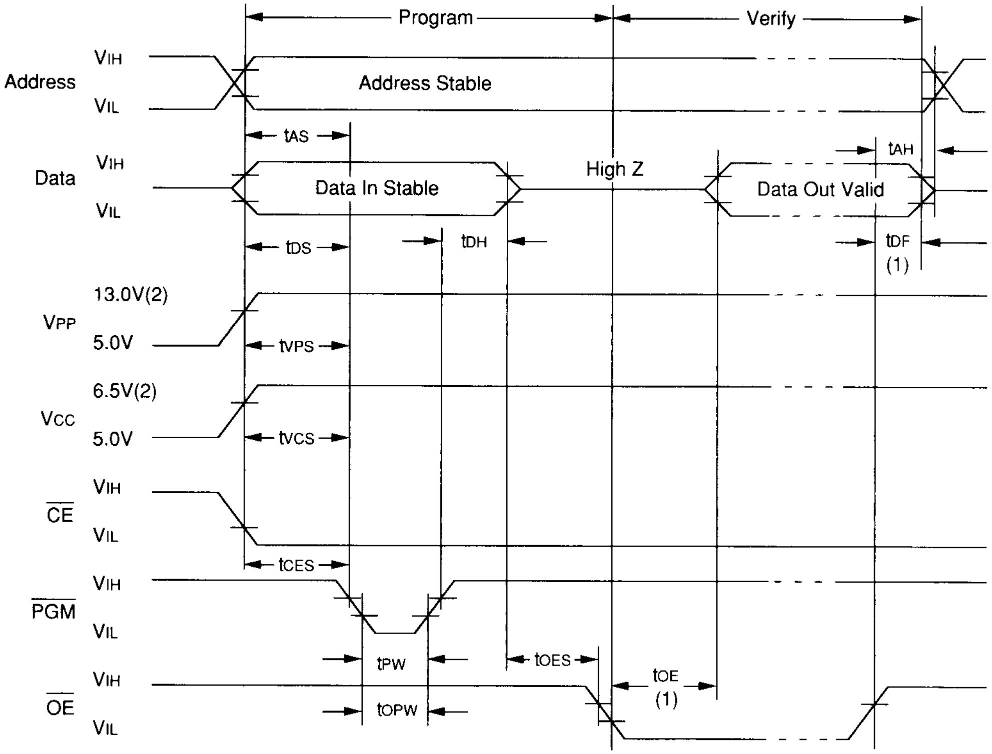
PROGRAMMING
AC Characteristics
for Program, Program Verify
and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V and V_{OL} = 0.8V
Ambient Temperature: 25° C ±5° C
For V_{PP} and V_{CC} Voltages, refer to Programming Algorithm

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µsec ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING Waveforms



Notes: (1) t_{DF} and t_{OE} are characteristics of the device but must be accomodated by the programmer
(2) V_{CC} = 6.5V ±0.25V, V_{PP} = V_H = 13.0V ±0.25V for express algorithm

FUNCTIONAL DESCRIPTION

The 27HC1616 has the following functional modes:

—Operation: The 27HC1616 can be activated for data read, be put in standby mode to lower its power consumption, or have the outputs disabled.

—Programming: To receive its permanent data, the 27HC1616 must be programmed. Both a program and program/verify procedure is available. The Express programming algorithm is recommended.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

For the general characteristics in these operation and programming modes, refer to the table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	A9	O0 - O15
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	X	D_{out}
Program	V_{IL}	V_{IH}	V_{IL}	V_H	X	D_{in}
Program Verify	V_{IH}	V_{IL}	V_{IH}	V_H	X	D_{out}
Program Inhibit	V_{IH}	X	X	V_H	X	High Z
Standby	V_{IH}	X	X	V_{CC}	X	High Z
Output Disable	X	V_{IH}	V_{IH}	V_{CC}	X	High Z
Identity	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_H	Identity Code

X = Don't Care
V_H = 12.0 ±0.5V

OPERATION

Read Mode

For timing and AC characteristics refer to the tables Read Waveforms and Read Operation AC Characteristics.

The 27HC1616's memory data is accessed when

—the chip is enabled by setting the $\overline{\text{CE}}$ pin low.
—the data is gated to the output pins by setting the $\overline{\text{OE}}$ pin low.

Standby Mode

The standby mode is entered when the $\overline{\text{CE}}$ pin is high, and the program mode is not defined. When these conditions are met, the supply current will drop from 90mA to 50mA.

Output Disable

This feature eliminates bus contention in multiple bus microprocessor systems. The outputs go to a high impedance when the $\overline{\text{OE}}$ pin is high, and the program mode is not defined.

Programming/Verification

The 27HC1616 has to be programmed, and afterward the programmed information verified. Before these operations, the Identity Code can be read to properly set up automated equipment. Multiple devices in parallel can be programmed using the programming and inhibit modes.

Programming Algorithm

The "Express" algorithm has been developed to improve programming through-put times in a production environment. Up to 10 pulses of 100µsec each are applied until the byte is verified. No overprogramming is required. A flowchart of this algorithm is shown in Figure 2.

The programming mode is entered when:

a) V_{CC} is brought to the proper level
b) V_{PP} is brought to the proper V_H level
c) the $\overline{\text{OE}}$ pin is high
d) the $\overline{\text{CE}}$ pin is low, and
e) the $\overline{\text{PGM}}$ pin is pulsed low.

Since the erased state is "1" in the array, programming of "0" is required. The address of the memory location to be programmed is set via pins A0 - A13, and the data is presented to pins O0 - O15. When data and address are stable, a low going pulse on the $\overline{\text{CE}}$ line programs that memory location.

Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level
c) the $\overline{\text{OE}}$ line is low
d) the $\overline{\text{CE}}$ pin is low, and
e) the $\overline{\text{PGM}}$ line is high.

Inhibit Mode

When Programming multiple devices in parallel with different data only $\overline{\text{PGM}}$ needs to be under separate control to each device. By pulsing the $\overline{\text{PGM}}$ line low on a particular device, that device will be programmed, and all other devices with corresponding $\overline{\text{PGM}}$ or $\overline{\text{CE}}$ held high will not be programmed with the data although address and data are available on their input pins.

Identity Mode

In this mode specific data is read from the device that identifies the manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to VH (11.5V to 12.5V). The $\overline{\text{CE}}$ and $\overline{\text{OE}}$ pins must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 - O7.

Pin →	Input	Output*								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	1	0	1	1	1	97

*Code subject to change.
Note: O15 - O8 are 00 for the manufacturer and device type code.

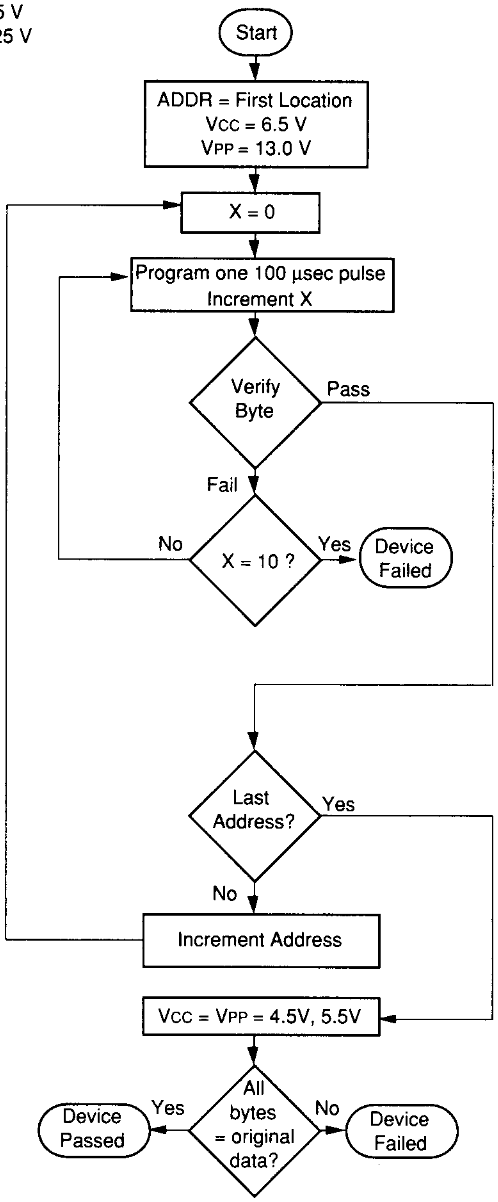
Erasure

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state as a result of being exposed to ultra-violet light at wavelengths ≤ 4000 Angstroms (Å). The recommended procedure is to expose the erasure window of device to a commercial UV source emitting at 2537Å with an intensity of 12,000µW/cm² at 1". The erasure time at that distance is about 15 to 20 min.

Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

Conditions:
Tamb = 25° C ±5° C
VCC = 6.5 ±0.25 V
VPP = 13.0 ±0.25 V



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27HC1616 - 55 I / P

Package:	J	Cerdip DIP
	K	Ceramic Leadless Chip Carrier
Temperature Range:	-	0° C to 70° C
Access Time:	55	55 nsec
	70	70 nsec
Device:	27HC1616	256K (16K x 16) High Speed CMOS EPROM