LG Electronics

LG4573A Datasheet

Mobile Display Driver IC
for a 16M-Color WVGA TFT LCD Panel

Version 1.1.5
2010-09-03

1 General Description

The LG4573 is a 16M-color single-chip controller driver IC for a-Si TFT liquid crystal display with supporting various resolutions of max 480RGB x 1024 dots GIP[1] panels.

The driver supports MIPI[2] DBI[3] and DPI[4] interfaces. The LG4573 supports dot inversion for higher image quality and moving flicker free image realizations with low power driving.

The LG4573 supports BLU[5] control functionality by analyzing the display data properties and it helps to get lower power consumptions without image losses.

The LG4573 can operate with low I/O interface power supply down to 1.65V, with an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The driver also supports function such as ~~8-color displays and~~ shut down. And these features make the LG4573 an ideal LCD driver for medium or small sized portable products supporting WWW full browsers such as smart phones or PDAs, where long battery life is a major concern.

[1] GIP – Gate In Panel
[2] MIPI – Mobile Industrial Processor Interface
[3] DBI – Display Bus Interface
[4] DPI – Display Pixel Interface
[5] BLU – Backlight Unit

2 Features

- A single-chip controller driver incorporating a GIP gate circuit and a power supply circuit for maximum 480RGB x 1024 dots graphics display on a-Si TFT panel in 16M colors. It supports 4N row resolutions of gate outputs in panel. In case of 854 row resolution, it is not divided by 4. But 856 row resolution could be chosen to support 854 row resolution by using 2 dummy rows.
- System interface
  - MIPI DBI Type C
  - MIPI DPI (RGB Interface)
  - SPI
- The 240RGB, 320RGB, 360RGB, and 480RGB source channels can be chosen for some applications. For those cases, the unused source outputs are made floating.
- Abundant color display
  - Programmable gamma correction function for 16M color display
- N-dot inversion and column inversion, where N can be 1, 2, or 3.
- Internal R, G, B independent gamma reference voltages generation function
- Content adaptive backlight control function for optimal power consumption
- Cst structure is only supported.
- Reversible source output shift direction by internal register setting
- Internal level shifter for GIP gate controls
- Internal power supply generations. The DC-DC charge pumping circuitry and PFM Booster with external inductor and external NMOS transistors.
- Internal NVM for VCOM level adjustment : 7bits with 4 times rewritable
- Low power consumption architecture
  - Standby function (Logic VDD is alive)
  - Deep standby function (Logic VDD is dead to be 0volt)
- Input power supply voltage ranges
  - Interface power supply: IOVCC = 1.65 to 3.3V
  - Logic power supply: VCC = 2.6 to 3.3V
    But make sure that internally generated logic voltage (VDD) will not exceed 1.98V.
  - Analog power supply: VCI = 2.6 to 3.3V
    But make sure that voltage difference between VGH and LVGL will not exceed 31.0V.
- Generated power supply voltage ranges
  - Logic VDD voltage : 1.62 to 1.98V
  - Source driver power supply positive voltage: DDVDH = 4.5 to 5.5V
  - Source driver power supply negative voltage: DDVDL = -4.0 to -5.0V
  - Gate on voltage: VGH
  - Gate off voltage: VGL
  - GIP most negative reference voltage: LVGL (VGL-VCI)
  - VGH-LVGL < 31.0V (operation maximum), VGH-GND < 18V (absolute maximum)
  - VCOM voltage: 0V, -0.5V to -3.5V

3 Block Diagram

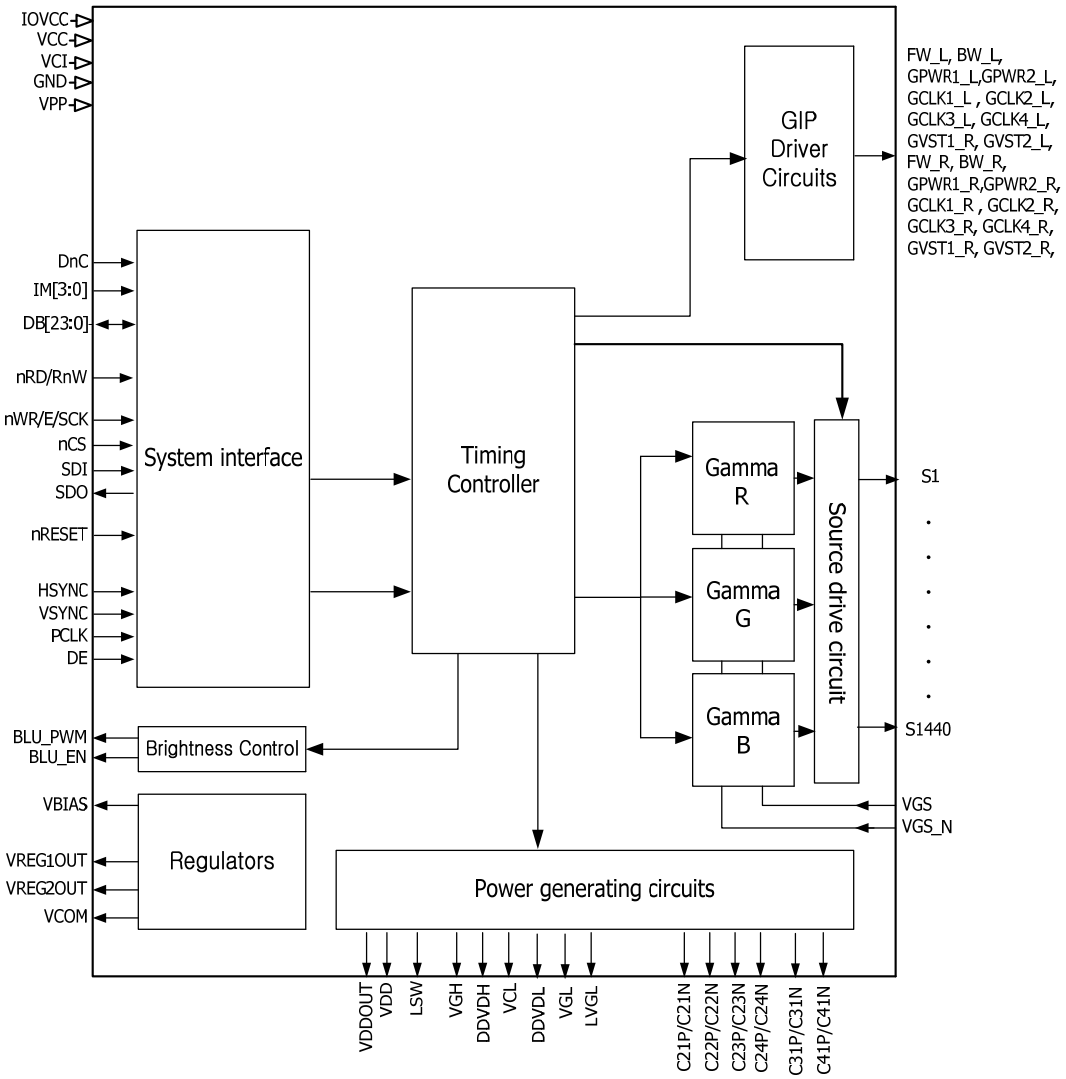


Figure 1

4 Pin Description

4.1 Pin List

Name	# of pins	I/O	Connected to	Description
IM3 IM2 IM1 IM0/ID	4	I	MPU	MPU interface mode selection signal IM[3:0] / Register Access / Pixel Data 0100 / MIPI DBI Type C / MIPI DPI (RGB) 110X / SPI / MIPI DPI (RGB)
nRESET	1	I	MPU or external RC circuit	Reset pin (active low) Be sure to execute a power-on reset after supplying power.
nCS	1	I	MPU	Chip select (active low)
DnC	1	I	MPU	Data (1) or command (0) select
DB[23:0]	24	I/O	MPU	Parallel data bus Unused pins must be fixed either to IOVCC or GND level.
nRD/RnW	1	I	MPU	(I80 interface) nRD - Read strobe (active low) (M68 interface) RnW - Read (1) or write (0) select
nWR/E/SCK	1	I	MPU	(I80 interface) nWR - Write strobe (active low) (M68 interface) E - Enable (SPI interface) SCK - Serial clock
SDI	1	I	MPU	(SPI interface) Serial data input This pin should be fixed either to IOVCC or GND level when not in use.
SDO	1	O	MPU	(SPI interface) Serial data output This pin should be made floating when not in use.
PCLK	1	I	MPU	Pixel clock
VSYNC	1	I	MPU	Frame synchronization signal. It is Vsync input pin when DPI pixel data interface mode.
HSYNC	1	I	MPU	Line synchronization signal. It is Vsync input pin when DPI pixel data interface mode. Fix to either IOVCC or GND level when not in use.
DE	1	I	MPU	Data enable signal in RGB interface mode. Fix to either IOVCC or GND level when not in use.
CLKP CLKN	2	I	MPU	Fix to GND.
DATA0P DATA0N DATA1P DATA1N	4	I/O	MPU	Fix to GND.
V12_SEL	1	I	GND or IOVCC	It is only for MIPI DSI interface. LG4573 does not support MIPI DSI interface anymore, so this pin should be set to fixed level of IOVCC or GND but not to be floating.
TEST1	1	I	GND	Test pin Fix to GND level in normal operation mode
TEST2	1	I	GND	Test pin Fix to GND level in normal operation mode
BLU_EN	1	O	BLU	BLU enable (active HIGH) If not used, leave this pin open.
BLU_PWM	1	O	BLU	BLU PWM signal If not used, leave this pin open.
S1 to S1440	1440	O	LCD	Source driver output pins

Name	# of pins	I/O	Connected to	Description
FW_L BW_L GVST1_L GVST2_L GCLK#_L where #=1,2,3,4	8	O	GIP	Signals for right side GIP on panel view (Left side in IC bump view) Unused pins should be left open.
FW_R BW_R GVST1_R GVST2_R GCLK#_R where #=1,2,3,4	8	O	GIP	Signals for Right side GIP on panel view (Right side in IC bump view) Unused pins should be left open.
VBIAS	1	O	GIP	Bias voltage for some special GIP circuits. If not used, leave this pin open.
LVGL	1	I	GIP	Most negative voltage for some special GIP circuits. If not used, connect to VGL
VGL	1	I		A supply voltage to drive gate lines of the TFT panel.
VGH	1	I		A supply voltage to drive gate lines of the TFT panel.
DDVDL	1	I		Power supply for the source driver's LCD output unit
DDVDH	1	I		Power supply for the source driver's LCD output unit and an input voltage to generate DDVDL voltage.
VCL	1	I		Power supply voltage for the level shifter circuits.
IOVCC	1	I	Power supply	Power supply to the interface pins: IOVCC = 1.65 to 3.3V.
VCC	1	I	Power supply	Power supply to generate the internal logic power supply VDD. VCC = 2.6 to 3.3V
VDD	1	I	Power supply	Generated power supply for the internal logic.
VDDOUT	1	I/O	Stabilizing capacitor and VDD	Internal logic regulator output. Connect VDD to a stabilizing capacitor.
VSS	1	I	Power supply	VSS=0.
VCI	1	I	Power supply	Supply voltage to the analog circuit. Connect to an external power supply of 2.6 to 3.3V.
VCOM	1	O	TFT panel common electrode	Supply voltage to the common electrode of TFT panel.
VCOMR	1	I	Variable resistor or open	Reference level to generate the VCOM level with an externally connected variable resistor. Leave it open when not in use. The VREG2OUT voltage level could be a reference voltage to generate VCOMR.
CREG	1	O	Stabilizing capacitor	Regulator output that needs to be connected with stabilizing capacitor for MIPI block. Leave it open when MIPI were not used.
GND_SH	1	I	GND	Fix to GND.
LSW	1	O	Gate terminal of external switching Tr.	External switching transistor's gate on/off control signal for the switching regulator type DC-DC converter to make DDVDH and/or DDVDL. Leave it open when not in use.
VGS	1	I	GND or external resistor	Reference level for the positive grayscale voltage generation circuit. The VGS level can be changed by connecting to an external resistor.

Name	# of pins	I/O	Connected to	Description
VGS_N	1	I	GND or external resistor	Reference level for the negative grayscale voltage generation circuit. The VGS_N level can be changed by connecting to an external resistor.
VREG1OUT	1	O	Stabilizing capacitor	VREG1OUT is a positive source driver grayscale reference voltage.
VREG2OUT	1	O	Stabilizing capacitor	VREG2OUT is a negative source driver grayscale reference voltage.
C21P, C21N C22P, C22N C23P, C23N C24P, C24N	8	I/O	Step-up capacitor	Connect step-up capacitors to generate VGH, VGL, and VCL. Leave them open when not in use.
C31P, C31N	2	I/O	Step-up capacitor	Connect step-up capacitor to generate DDVDL when charge pumping method is used instead of diode inverting. When DDVDH is supplied externally, this capacitor is necessary to generate DDVDL. Leave them open when not in use.
C41P, C41N	2	I/O	Step-up capacitor	Connect step-up capacitor to generate LVGL only for H-type panel. Leave them open when not in use.
VPP	1	I	Power supply	7.5V power supply only for internal OTP programming for VCOM adjustments. Leave it open when not in programming.
GOUT_TEST1 GOUT_TEST2	2		DUMMY	Dummy pads only with bump
DUM_VON	1		DUMMY	Dummy pad only with bump
DUM_DATA1 DUM_DATA2	2		DUMMY	Dummy pads only with bump They are shorted together.
DUM_GOUT	1		DUMMY	Dummy pads only with bump
OSC1 OSC2 OSC3	3	I/O	DUMMY	Dummy pads Leave them open.

4.2 Pin Assignment

- Chip size : 22350um x 900um
  (With seal ring but without scribe line)
- Chip thickness : 250um
- PAD Coordination : PAD center

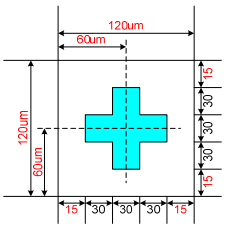
- Au BUMP size
(1) 50.00um x 80.00um
No.1 – No.312

(2) 15.0um x 98.0um
No.313 – No.1756

- Au BUMP pitch : see PAD coordination Table
- Au BUMP height : 15um(typ.)
- No. in the figure corresponds to No. in the PAD coordination Table

- Alignment mark

Alignment mark	X	Y
1-a	-11060	325
1-b	11060	325



4.3 Bump Coordinates

No.	Name	X	Y
1	DUMMY	-10885	-397
2	FW_L	-10815	-397
3	BW_L	-10745	-397
4	GPWR1_L	-10675	-397
5	GPWR2_L	-10605	-397
6	GCLK4_L	-10535	-397
7	GCLK4_L	-10465	-397
8	GCLK3_L	-10395	-397
9	GCLK3_L	-10325	-397
10	GCLK2_L	-10255	-397
11	GCLK2_L	-10185	-397
12	GCLK1_L	-10115	-397
13	GCLK1_L	-10045	-397
14	GVST1_L	-9975	-397
15	GVST2_L	-9905	-397
16	VGL	-9835	-397
17	VGL	-9765	-397
18	VGL	-9695	-397
19	VBIAS	-9625	-397
20	LVGL	-9555	-397
21	LVGL	-9485	-397
22	LVGL	-9415	-397
23	GOUT_TEST1	-9345	-397
24	VCOM	-9275	-397
25	VCOM	-9205	-397
26	VCOM	-9135	-397
27	DUM_VON	-9065	-397
28	DUM_DATA1	-8995	-397
29	DUM_DATA2	-8925	-397
30	DUM_GOUT	-8855	-397
31	VGL	-8785	-397
32	VGL	-8715	-397
33	VGL	-8645	-397
34	LVGL	-8575	-397
35	LVGL	-8505	-397
36	LVGL	-8435	-397
37	LVGL	-8365	-397
38	LVGL	-8295	-397
39	VCOM	-8225	-397
40	VCOM	-8155	-397
41	VCOM	-8085	-397
42	VCOM	-8015	-397
43	C41P	-7945	-397
44	C41P	-7875	-397
45	C41P	-7805	-397
46	C41N	-7735	-397
47	C41N	-7665	-397
48	C41N	-7595	-397
49	VGH	-7525	-397
50	VGH	-7455	-397
51	VGH	-7385	-397
52	VGH	-7315	-397
53	VGH	-7245	-397
54	VGH	-7175	-397
55	C21N	-7105	-397
56	C21N	-7035	-397
57	C21N	-6965	-397
58	C21N	-6895	-397
59	C21P	-6825	-397
60	C21P	-6755	-397
61	C21P	-6685	-397
62	C21P	-6615	-397
63	C23N	-6545	-397
64	C23N	-6475	-397
65	C23N	-6405	-397
66	C23N	-6335	-397
67	C23P	-6265	-397
68	C23P	-6195	-397
69	C23P	-6125	-397
70	C23P	-6055	-397
71	C22P	-5985	-397
72	C22P	-5915	-397
73	C22P	-5845	-397
74	C22P	-5775	-397
75	C22N	-5705	-397
76	C22N	-5635	-397
77	C22N	-5565	-397
78	C22N	-5495	-397
79	C24N	-5425	-397
80	C24N	-5355	-397
81	C24N	-5285	-397
82	C24N	-5215	-397
83	C24P	-5145	-397
84	C24P	-5075	-397
85	C24P	-5005	-397
86	C24P	-4935	-397
87	VPP	-4865	-397
88	VPP	-4795	-397
89	VCL	-4725	-397
90	VCL	-4655	-397
91	VCL	-4585	-397
92	VCL	-4515	-397
93	VCL	-4445	-397
94	VCI	-4375	-397
95	VCI	-4305	-397
96	VCI	-4235	-397
97	VCI	-4165	-397
98	VCI	-4095	-397
99	VCI	-4025	-397
100	LSW	-3955	-397
101	LSW	-3885	-397
102	DDVDH	-3815	-397
103	DDVDH	-3745	-397
104	DDVDH	-3675	-397
105	DDVDH	-3605	-397
106	DDVDH	-3535	-397
107	DDVDH	-3465	-397
108	VSS	-3395	-397
109	VSS	-3325	-397
110	VSS	-3255	-397
111	VSS	-3185	-397
112	VSS	-3115	-397
113	VSS	-3045	-397
114	VSS	-2975	-397
115	VSS	-2905	-397
116	VDD	-2835	-397
117	VDD	-2765	-397
118	VDD	-2695	-397
119	VDD	-2625	-397
120	VDD	-2555	-397
121	VDD	-2485	-397
122	IOVCC	-2415	-397
123	IOVCC	-2345	-397
124	IOVCC	-2275	-397
125	IOVCC	-2205	-397
126	IOVCC	-2135	-397
127	BLU_PWM	-2065	-397
128	BLU_EN	-1995	-397
129	TEST1	-1925	-397
130	TEST2	-1855	-397
131	IM0	-1785	-397
132	IM1	-1715	-397
133	IM2	-1645	-397
134	IM3	-1575	-397
135	nRESET	-1505	-397
136	VSS_DUM	-1435	-397
137	DB<23>	-1365	-397
138	DB<22>	-1295	-397
139	DB<21>	-1225	-397
140	DB<20>	-1155	-397
141	DB<19>	-1085	-397
142	DB<18>	-1015	-397
143	DB<17>	-945	-397
144	DB<16>	-875	-397
145	DB<15>	-805	-397
146	DB<14>	-735	-397
147	DB<13>	-665	-397
148	DB<12>	-595	-397
149	DB<11>	-525	-397
150	DB<10>	-455	-397
151	DB<9>	-385	-397
152	DB<8>	-315	-397
153	DB<7>	-245	-397
154	DB<6>	-175	-397
155	DB<5>	-105	-397
156	DB<4>	-35	-397
157	DB<3>	35	-397
158	DB<2>	105	-397
159	DB<1>	175	-397
160	DB<0>	245	-397
161	VSS_DUM	315	-397
162	nRD/RnW	385	-397
163	nWR/E/SCK	455	-397
164	DnC	525	-397
165	nCS	595	-397
166	VSS_DUM	665	-397
167	SDI	735	-397
168	SDO	805	-397
169	VSYNC	875	-397
170	HSYNC	945	-397
171	DE	1015	-397
172	PCLK	1085	-397
173	V12_SEL	1155	-397
174	DUMMY	1225	-397
175	OSC1	1295	-397
176	OSC2	1365	-397
177	OSC3	1435	-397
178	VSS_SH1	1505	-397
179	DATA0N	1575	-397
180	DATA0N	1645	-397
181	DATA0N	1715	-397
182	DATA0P	1785	-397
183	DATA0P	1855	-397
184	DATA0P	1925	-397
185	VSS_SH2	1995	-397
186	DATA1N	2065	-397
187	DATA1N	2135	-397
188	DATA1N	2205	-397
189	DATA1P	2275	-397
190	DATA1P	2345	-397
191	DATA1P	2415	-397
192	VSS_SH3	2485	-397
193	CLKN	2555	-397
194	CLKN	2625	-397
195	CLKN	2695	-397
196	CLKP	2765	-397
197	CLKP	2835	-397
198	CLKP	2905	-397
199	VSS_SH4	2975	-397
200	CREG	3045	-397
201	CREG	3115	-397
202	VCC	3185	-397
203	VCC	3255	-397
204	VCC	3325	-397
205	VCC	3395	-397
206	VCC	3465	-397
207	VSS	3535	-397
208	VSS	3605	-397
209	VSS	3675	-397
210	VSS	3745	-397
211	VSS	3815	-397
212	VSS	3885	-397
213	VSS	3955	-397
214	VSS	4025	-397
215	VSS	4095	-397
216	VSS	4165	-397

No.	Name	X	Y
217	VSS	4235	-397
218	VSS	4305	-397
219	VSS	4375	-397
220	VSS	4445	-397
221	VSS	4515	-397
222	VDD	4585	-397
223	VDD	4655	-397
224	VDD	4725	-397
225	VDD	4795	-397
226	VDD	4865	-397
227	VDD	4935	-397
228	VDD	5005	-397
229	VDD	5075	-397
230	VDDOUT	5145	-397
231	VDDOUT	5215	-397
232	VDDOUT	5285	-397
233	VDDOUT	5355	-397
234	VDDOUT	5425	-397
235	VREG1OUT	5495	-397
236	VGS	5565	-397
237	DDVDH	5635	-397
238	DDVDH	5705	-397
239	DDVDH	5775	-397
240	DDVDH	5845	-397
241	DDVDH	5915	-397
242	DDVDH	5985	-397
243	DDVDH	6055	-397
244	DDVDH	6125	-397
245	C31P	6195	-397
246	C31P	6265	-397
247	C31P	6335	-397
248	C31P	6405	-397
249	C31N	6475	-397
250	C31N	6545	-397
251	C31N	6615	-397
252	C31N	6685	-397
253	VREG2OUT	6755	-397
254	VGS_N	6825	-397
255	DDVDL	6895	-397
256	DDVDL	6965	-397
257	DDVDL	7035	-397
258	DDVDL	7105	-397
259	DDVDL	7175	-397
260	DDVDL	7245	-397
261	DDVDL	7315	-397
262	VCI	7385	-397
263	VCI	7455	-397
264	VCI	7525	-397
265	VCI	7595	-397
266	VCI	7665	-397
267	VCI	7735	-397
268	VGH	7805	-397
269	VGH	7875	-397
270	VGH	7945	-397
271	VGH	8015	-397
272	VCOM	8085	-397
273	VCOM	8155	-397
274	VCOM	8225	-397
275	VCOM	8295	-397
276	LVGL	8365	-397
277	LVGL	8435	-397
278	LVGL	8505	-397
279	LVGL	8575	-397
280	DUM_GOUT	8645	-397
281	DUMMY	8715	-397
282	VCOMR	8785	-397
283	DUM_VON	8855	-397
284	VCOM	8925	-397
285	VCOM	8995	-397
286	VCOM	9065	-397
287	DUMMY	9135	-397
288	GOUT_TEST2	9205	-397
289	LVGL	9275	-397
290	LVGL	9345	-397
291	LVGL	9415	-397

No.	Name	X	Y
292	VBIAS	9485	-397
293	VGL	9555	-397
294	VGL	9625	-397
295	VGL	9695	-397
296	VGL	9765	-397
297	GVST2_R	9835	-397
298	GVST1_R	9905	-397
299	GCLK1_R	9975	-397
300	GCLK1_R	10045	-397
301	GCLK2_R	10115	-397
302	GCLK2_R	10185	-397
303	GCLK3_R	10255	-397
304	GCLK3_R	10325	-397
305	GCLK4_R	10395	-397
306	GCLK4_R	10465	-397
307	GPWR2_R	10535	-397
308	GPWR1_R	10605	-397
309	BW_R	10675	-397
310	FW_R	10745	-397
311	DUMMY	10815	-397
312	DUMMY	10885	-397
	DUMMY	10935	338
313	S1	10920	225
314	S2	10905	338
315	S3	10890	225
316	S4	10875	338
317	S5	10860	225
318	S6	10845	338
319	S7	10830	225
320	S8	10815	338
321	S9	10800	225
322	S10	10785	338
323	S11	10770	225
324	S12	10755	338
325	S13	10740	225
326	S14	10725	338
327	S15	10710	225
328	S16	10695	338
329	S17	10680	225
330	S18	10665	338
331	S19	10650	225
332	S20	10635	338
333	S21	10620	225
334	S22	10605	338
335	S23	10590	225
336	S24	10575	338
337	S25	10560	225
338	S26	10545	338
339	S27	10530	225
340	S28	10515	338
341	S29	10500	225
342	S30	10485	338
343	S31	10470	225
344	S32	10455	338
345	S33	10440	225
346	S34	10425	338
347	S35	10410	225
348	S36	10395	338
349	S37	10380	225
350	S38	10365	338
351	S39	10350	225
352	S40	10335	338
353	S41	10320	225
354	S42	10305	338
355	S43	10290	225
356	S44	10275	338
357	S45	10260	225
358	S46	10245	338
359	S47	10230	225
360	S48	10215	338
361	S49	10200	225
362	S50	10185	338
363	S51	10170	225
364	S52	10155	338
365	S53	10140	225

No.	Name	X	Y
366	S54	10125	338
367	S55	10110	225
368	S56	10095	338
369	S57	10080	225
370	S58	10065	338
371	S59	10050	225
372	S60	10035	338
373	S61	10020	225
374	S62	10005	338
375	S63	9990	225
376	S64	9975	338
377	S65	9960	225
378	S66	9945	338
379	S67	9930	225
380	S68	9915	338
381	S69	9900	225
382	S70	9885	338
383	S71	9870	225
384	S72	9855	338
385	S73	9840	225
386	S74	9825	338
387	S75	9810	225
388	S76	9795	338
389	S77	9780	225
390	S78	9765	338
391	S79	9750	225
392	S80	9735	338
393	S81	9720	225
394	S82	9705	338
395	S83	9690	225
396	S84	9675	338
397	S85	9660	225
398	S86	9645	338
399	S87	9630	225
400	S88	9615	338
401	S89	9600	225
402	S90	9585	338
403	S91	9570	225
404	S92	9555	338
405	S93	9540	225
406	S94	9525	338
407	S95	9510	225
408	S96	9495	338
409	S97	9480	225
410	S98	9465	338
411	S99	9450	225
412	S100	9435	338
413	S101	9420	225
414	S102	9405	338
415	S103	9390	225
416	S104	9375	338
417	S105	9360	225
418	S106	9345	338
419	S107	9330	225
420	S108	9315	338
421	S109	9300	225
422	S110	9285	338
423	S111	9270	225
424	S112	9255	338
425	S113	9240	225
426	S114	9225	338
427	S115	9210	225
428	S116	9195	338
429	S117	9180	225
430	S118	9165	338
431	S119	9150	225
432	S120	9135	338
433	S121	9120	225
434	S122	9105	338
435	S123	9090	225
436	S124	9075	338
437	S125	9060	225
438	S126	9045	338
439	S127	9030	225
440	S128	9015	338

No.	Name	X	Y
441	S129	9000	225
442	S130	8985	338
443	S131	8970	225
444	S132	8955	338
445	S133	8940	225
446	S134	8925	338
447	S135	8910	225
448	S136	8895	338
449	S137	8880	225
450	S138	8865	338
451	S139	8850	225
452	S140	8835	338
453	S141	8820	225
454	S142	8805	338
455	S143	8790	225
456	S144	8775	338
457	S145	8760	225
458	S146	8745	338
459	S147	8730	225
460	S148	8715	338
461	S149	8700	225
462	S150	8685	338
463	S151	8670	225
464	S152	8655	338
465	S153	8640	225
466	S154	8625	338
467	S155	8610	225
468	S156	8595	338
469	S157	8580	225
470	S158	8565	338
471	S159	8550	225
472	S160	8535	338
473	S161	8520	225
474	S162	8505	338
475	S163	8490	225
476	S164	8475	338
477	S165	8460	225
478	S166	8445	338
479	S167	8430	225
480	S168	8415	338
481	S169	8400	225
482	S170	8385	338
483	S171	8370	225
484	S172	8355	338
485	S173	8340	225
486	S174	8325	338
487	S175	8310	225
488	S176	8295	338
489	S177	8280	225
490	S178	8265	338
491	S179	8250	225
492	S180	8235	338
493	S181	8220	225
494	S182	8205	338
495	S183	8190	225
496	S184	8175	338
497	S185	8160	225
498	S186	8145	338
499	S187	8130	225
500	S188	8115	338
501	S189	8100	225
502	S190	8085	338
503	S191	8070	225
504	S192	8055	338
505	S193	8040	225
506	S194	8025	338
507	S195	8010	225
508	S196	7995	338
509	S197	7980	225
510	S198	7965	338
511	S199	7950	225
512	S200	7935	338
513	S201	7920	225
514	S202	7905	338
515	S203	7890	225

No.	Name	X	Y
516	S204	7875	338
517	S205	7860	225
518	S206	7845	338
519	S207	7830	225
520	S208	7815	338
521	S209	7800	225
522	S210	7785	338
523	S211	7770	225
524	S212	7755	338
525	S213	7740	225
526	S214	7725	338
527	S215	7710	225
528	S216	7695	338
529	S217	7680	225
530	S218	7665	338
531	S219	7650	225
532	S220	7635	338
533	S221	7620	225
534	S222	7605	338
535	S223	7590	225
536	S224	7575	338
537	S225	7560	225
538	S226	7545	338
539	S227	7530	225
540	S228	7515	338
541	S229	7500	225
542	S230	7485	338
543	S231	7470	225
544	S232	7455	338
545	S233	7440	225
546	S234	7425	338
547	S235	7410	225
548	S236	7395	338
549	S237	7380	225
550	S238	7365	338
551	S239	7350	225
552	S240	7335	338
553	S241	7320	225
554	S242	7305	338
555	S243	7290	225
556	S244	7275	338
557	S245	7260	225
558	S246	7245	338
559	S247	7230	225
560	S248	7215	338
561	S249	7200	225
562	S250	7185	338
563	S251	7170	225
564	S252	7155	338
565	S253	7140	225
566	S254	7125	338
567	S255	7110	225
568	S256	7095	338
569	S257	7080	225
570	S258	7065	338
571	S259	7050	225
572	S260	7035	338
573	S261	7020	225
574	S262	7005	338
575	S263	6990	225
576	S264	6975	338
577	S265	6960	225
578	S266	6945	338
579	S267	6930	225
580	S268	6915	338
581	S269	6900	225
582	S270	6885	338
583	S271	6870	225
584	S272	6855	338
585	S273	6840	225
586	S274	6825	338
587	S275	6810	225
588	S276	6795	338
589	S277	6780	225
590	S278	6765	338

No.	Name	X	Y
591	S279	6750	225
592	S280	6735	338
593	S281	6720	225
594	S282	6705	338
595	S283	6690	225
596	S284	6675	338
597	S285	6660	225
598	S286	6645	338
599	S287	6630	225
600	S288	6615	338
601	S289	6600	225
602	S290	6585	338
603	S291	6570	225
604	S292	6555	338
605	S293	6540	225
606	S294	6525	338
607	S295	6510	225
608	S296	6495	338
609	S297	6480	225
610	S298	6465	338
611	S299	6450	225
612	S300	6435	338
613	S301	6420	225
614	S302	6405	338
615	S303	6390	225
616	S304	6375	338
617	S305	6360	225
618	S306	6345	338
619	S307	6330	225
620	S308	6315	338
621	S309	6300	225
622	S310	6285	338
623	S311	6270	225
624	S312	6255	338
625	S313	6240	225
626	S314	6225	338
627	S315	6210	225
628	S316	6195	338
629	S317	6180	225
630	S318	6165	338
631	S319	6150	225
632	S320	6135	338
633	S321	6120	225
634	S322	6105	338
635	S323	6090	225
636	S324	6075	338
637	S325	6060	225
638	S326	6045	338
639	S327	6030	225
640	S328	6015	338
641	S329	6000	225
642	S330	5985	338
643	S331	5970	225
644	S332	5955	338
645	S333	5940	225
646	S334	5925	338
647	S335	5910	225
648	S336	5895	338
649	S337	5880	225
650	S338	5865	338
651	S339	5850	225
652	S340	5835	338
653	S341	5820	225
654	S342	5805	338
655	S343	5790	225
656	S344	5775	338
657	S345	5760	225
658	S346	5745	338
659	S347	5730	225
660	S348	5715	338
661	S349	5700	225
662	S350	5685	338
663	S351	5670	225
664	S352	5655	338
665	S353	5640	225

No.	Name	X	Y
666	S354	5625	338
667	S355	5610	225
668	S356	5595	338
669	S357	5580	225
670	S358	5565	338
671	S359	5550	225
672	S360	5535	338
673	S361	5520	225
674	S362	5505	338
675	S363	5490	225
676	S364	5475	338
677	S365	5460	225
678	S366	5445	338
679	S367	5430	225
680	S368	5415	338
681	S369	5400	225
682	S370	5385	338
683	S371	5370	225
684	S372	5355	338
685	S373	5340	225
686	S374	5325	338
687	S375	5310	225
688	S376	5295	338
689	S377	5280	225
690	S378	5265	338
691	S379	5250	225
692	S380	5235	338
693	S381	5220	225
694	S382	5205	338
695	S383	5190	225
696	S384	5175	338
697	S385	5160	225
698	S386	5145	338
699	S387	5130	225
700	S388	5115	338
701	S389	5100	225
702	S390	5085	338
703	S391	5070	225
704	S392	5055	338
705	S393	5040	225
706	S394	5025	338
707	S395	5010	225
708	S396	4995	338
709	S397	4980	225
710	S398	4965	338
711	S399	4950	225
712	S400	4935	338
713	S401	4920	225
714	S402	4905	338
715	S403	4890	225
716	S404	4875	338
717	S405	4860	225
718	S406	4845	338
719	S407	4830	225
720	S408	4815	338
721	S409	4800	225
722	S410	4785	338
723	S411	4770	225
724	S412	4755	338
725	S413	4740	225
726	S414	4725	338
727	S415	4710	225
728	S416	4695	338
729	S417	4680	225
730	S418	4665	338
731	S419	4650	225
732	S420	4635	338
733	S421	4620	225
734	S422	4605	338
735	S423	4590	225
736	S424	4575	338
737	S425	4560	225
738	S426	4545	338
739	S427	4530	225
740	S428	4515	338

No.	Name	X	Y
741	S429	4500	225
742	S430	4485	338
743	S431	4470	225
744	S432	4455	338
745	S433	4440	225
746	S434	4425	338
747	S435	4410	225
748	S436	4395	338
749	S437	4380	225
750	S438	4365	338
751	S439	4350	225
752	S440	4335	338
753	S441	4320	225
754	S442	4305	338
755	S443	4290	225
756	S444	4275	338
757	S445	4260	225
758	S446	4245	338
759	S447	4230	225
760	S448	4215	338
761	S449	4200	225
762	S450	4185	338
763	S451	4170	225
764	S452	4155	338
765	S453	4140	225
766	S454	4125	338
767	S455	4110	225
768	S456	4095	338
769	S457	4080	225
770	S458	4065	338
771	S459	4050	225
772	S460	4035	338
773	S461	4020	225
774	S462	4005	338
775	S463	3990	225
776	S464	3975	338
777	S465	3960	225
778	S466	3945	338
779	S467	3930	225
780	S468	3915	338
781	S469	3900	225
782	S470	3885	338
783	S471	3870	225
784	S472	3855	338
785	S473	3840	225
786	S474	3825	338
787	S475	3810	225
788	S476	3795	338
789	S477	3780	225
790	S478	3765	338
791	S479	3750	225
792	S480	3735	338
793	S481	3720	225
794	S482	3705	338
795	S483	3690	225
796	S484	3675	338
797	S485	3660	225
798	S486	3645	338
799	S487	3630	225
800	S488	3615	338
801	S489	3600	225
802	S490	3585	338
803	S491	3570	225
804	S492	3555	338
805	S493	3540	225
806	S494	3525	338
807	S495	3510	225
808	S496	3495	338
809	S497	3480	225
810	S498	3465	338
811	S499	3450	225
812	S500	3435	338
813	S501	3420	225
814	S502	3405	338
815	S503	3390	225

No.	Name	X	Y
816	S504	3375	338
817	S505	3360	225
818	S506	3345	338
819	S507	3330	225
820	S508	3315	338
821	S509	3300	225
822	S510	3285	338
823	S511	3270	225
824	S512	3255	338
825	S513	3240	225
826	S514	3225	338
827	S515	3210	225
828	S516	3195	338
829	S517	3180	225
830	S518	3165	338
831	S519	3150	225
832	S520	3135	338
833	S521	3120	225
834	S522	3105	338
835	S523	3090	225
836	S524	3075	338
837	S525	3060	225
838	S526	3045	338
839	S527	3030	225
840	S528	3015	338
841	S529	3000	225
842	S530	2985	338
843	S531	2970	225
844	S532	2955	338
845	S533	2940	225
846	S534	2925	338
847	S535	2910	225
848	S536	2895	338
849	S537	2880	225
850	S538	2865	338
851	S539	2850	225
852	S540	2835	338
853	S541	2820	225
854	S542	2805	338
855	S543	2790	225
856	S544	2775	338
857	S545	2760	225
858	S546	2745	338
859	S547	2730	225
860	S548	2715	338
861	S549	2700	225
862	S550	2685	338
863	S551	2670	225
864	S552	2655	338
865	S553	2640	225
866	S554	2625	338
867	S555	2610	225
868	S556	2595	338
869	S557	2580	225
870	S558	2565	338
871	S559	2550	225
872	S560	2535	338
873	S561	2520	225
874	S562	2505	338
875	S563	2490	225
876	S564	2475	338
877	S565	2460	225
878	S566	2445	338
879	S567	2430	225
880	S568	2415	338
881	S569	2400	225
882	S570	2385	338
883	S571	2370	225
884	S572	2355	338
885	S573	2340	225
886	S574	2325	338
887	S575	2310	225
888	S576	2295	338
889	S577	2280	225
890	S578	2265	338

No.	Name	X	Y
891	S579	2250	225
892	S580	2235	338
893	S581	2220	225
894	S582	2205	338
895	S583	2190	225
896	S584	2175	338
897	S585	2160	225
898	S586	2145	338
899	S587	2130	225
900	S588	2115	338
901	S589	2100	225
902	S590	2085	338
903	S591	2070	225
904	S592	2055	338
905	S593	2040	225
906	S594	2025	338
907	S595	2010	225
908	S596	1995	338
909	S597	1980	225
910	S598	1965	338
911	S599	1950	225
912	S600	1935	338
913	S601	1920	225
914	S602	1905	338
915	S603	1890	225
916	S604	1875	338
917	S605	1860	225
918	S606	1845	338
919	S607	1830	225
920	S608	1815	338
921	S609	1800	225
922	S610	1785	338
923	S611	1770	225
924	S612	1755	338
925	S613	1740	225
926	S614	1725	338
927	S615	1710	225
928	S616	1695	338
929	S617	1680	225
930	S618	1665	338
931	S619	1650	225
932	S620	1635	338
933	S621	1620	225
934	S622	1605	338
935	S623	1590	225
936	S624	1575	338
937	S625	1560	225
938	S626	1545	338
939	S627	1530	225
940	S628	1515	338
941	S629	1500	225
942	S630	1485	338
943	S631	1470	225
944	S632	1455	338
945	S633	1440	225
946	S634	1425	338
947	S635	1410	225
948	S636	1395	338
949	S637	1380	225
950	S638	1365	338
951	S639	1350	225
952	S640	1335	338
953	S641	1320	225
954	S642	1305	338
955	S643	1290	225
956	S644	1275	338
957	S645	1260	225
958	S646	1245	338
959	S647	1230	225
960	S648	1215	338
961	S649	1200	225
962	S650	1185	338
963	S651	1170	225
964	S652	1155	338
965	S653	1140	225

No.	Name	X	Y
966	S654	1125	338
967	S655	1110	225
968	S656	1095	338
969	S657	1080	225
970	S658	1065	338
971	S659	1050	225
972	S660	1035	338
973	S661	1020	225
974	S662	1005	338
975	S663	990	225
976	S664	975	338
977	S665	960	225
978	S666	945	338
979	S667	930	225
980	S668	915	338
981	S669	900	225
982	S670	885	338
983	S671	870	225
984	S672	855	338
985	S673	840	225
986	S674	825	338
987	S675	810	225
988	S676	795	338
989	S677	780	225
990	S678	765	338
991	S679	750	225
992	S680	735	338
993	S681	720	225
994	S682	705	338
995	S683	690	225
996	S684	675	338
997	S685	660	225
998	S686	645	338
999	S687	630	225
1000	S688	615	338
1001	S689	600	225
1002	S690	585	338
1003	S691	570	225
1004	S692	555	338
1005	S693	540	225
1006	S694	525	338
1007	S695	510	225
1008	S696	495	338
1009	S697	480	225
1010	S698	465	338
1011	S699	450	225
1012	S700	435	338
1013	S701	420	225
1014	S702	405	338
1015	S703	390	225
1016	S704	375	338
1017	S705	360	225
1018	S706	345	338
1019	S707	330	225
1020	S708	315	338
1021	S709	300	225
1022	S710	285	338
1023	S711	270	225
1024	S712	255	338
1025	S713	240	225
1026	S714	225	338
1027	S715	210	225
1028	S716	195	338
1029	S717	180	225
1030	S718	165	338
1031	S719	150	225
1032	S720	135	338
1033	DUMMY	90	338
1034	DUMMY	30	338
1035	DUMMY	-30	338
1036	DUMMY	-90	338
1037	S721	-135	338
1038	S722	-150	225
1039	S723	-165	338
1040	S724	-180	225

No.	Name	X	Y
1041	S725	-195	338
1042	S726	-210	225
1043	S727	-225	338
1044	S728	-240	225
1045	S729	-255	338
1046	S730	-270	225
1047	S731	-285	338
1048	S732	-300	225
1049	S733	-315	338
1050	S734	-330	225
1051	S735	-345	338
1052	S736	-360	225
1053	S737	-375	338
1054	S738	-390	225
1055	S739	-405	338
1056	S740	-420	225
1057	S741	-435	338
1058	S742	-450	225
1059	S743	-465	338
1060	S744	-480	225
1061	S745	-495	338
1062	S746	-510	225
1063	S747	-525	338
1064	S748	-540	225
1065	S749	-555	338
1066	S750	-570	225
1067	S751	-585	338
1068	S752	-600	225
1069	S753	-615	338
1070	S754	-630	225
1071	S755	-645	338
1072	S756	-660	225
1073	S757	-675	338
1074	S758	-690	225
1075	S759	-705	338
1076	S760	-720	225
1077	S761	-735	338
1078	S762	-750	225
1079	S763	-765	338
1080	S764	-780	225
1081	S765	-795	338
1082	S766	-810	225
1083	S767	-825	338
1084	S768	-840	225
1085	S769	-855	338
1086	S770	-870	225
1087	S771	-885	338
1088	S772	-900	225
1089	S773	-915	338
1090	S774	-930	225
1091	S775	-945	338
1092	S776	-960	225
1093	S777	-975	338
1094	S778	-990	225
1095	S779	-1005	338
1096	S780	-1020	225
1097	S781	-1035	338
1098	S782	-1050	225
1099	S783	-1065	338
1100	S784	-1080	225
1101	S785	-1095	338
1102	S786	-1110	225
1103	S787	-1125	338
1104	S788	-1140	225
1105	S789	-1155	338
1106	S790	-1170	225
1107	S791	-1185	338
1108	S792	-1200	225
1109	S793	-1215	338
1110	S794	-1230	225
1111	S795	-1245	338
1112	S796	-1260	225
1113	S797	-1275	338
1114	S798	-1290	225
1115	S799	-1305	338

No.	Name	X	Y
1116	S800	-1320	225
1117	S801	-1335	338
1118	S802	-1350	225
1119	S803	-1365	338
1120	S804	-1380	225
1121	S805	-1395	338
1122	S806	-1410	225
1123	S807	-1425	338
1124	S808	-1440	225
1125	S809	-1455	338
1126	S810	-1470	225
1127	S811	-1485	338
1128	S812	-1500	225
1129	S813	-1515	338
1130	S814	-1530	225
1131	S815	-1545	338
1132	S816	-1560	225
1133	S817	-1575	338
1134	S818	-1590	225
1135	S819	-1605	338
1136	S820	-1620	225
1137	S821	-1635	338
1138	S822	-1650	225
1139	S823	-1665	338
1140	S824	-1680	225
1141	S825	-1695	338
1142	S826	-1710	225
1143	S827	-1725	338
1144	S828	-1740	225
1145	S829	-1755	338
1146	S830	-1770	225
1147	S831	-1785	338
1148	S832	-1800	225
1149	S833	-1815	338
1150	S834	-1830	225
1151	S835	-1845	338
1152	S836	-1860	225
1153	S837	-1875	338
1154	S838	-1890	225
1155	S839	-1905	338
1156	S840	-1920	225
1157	S841	-1935	338
1158	S842	-1950	225
1159	S843	-1965	338
1160	S844	-1980	225
1161	S845	-1995	338
1162	S846	-2010	225
1163	S847	-2025	338
1164	S848	-2040	225
1165	S849	-2055	338
1166	S850	-2070	225
1167	S851	-2085	338
1168	S852	-2100	225
1169	S853	-2115	338
1170	S854	-2130	225
1171	S855	-2145	338
1172	S856	-2160	225
1173	S857	-2175	338
1174	S858	-2190	225
1175	S859	-2205	338
1176	S860	-2220	225
1177	S861	-2235	338
1178	S862	-2250	225
1179	S863	-2265	338
1180	S864	-2280	225
1181	S865	-2295	338
1182	S866	-2310	225
1183	S867	-2325	338
1184	S868	-2340	225
1185	S869	-2355	338
1186	S870	-2370	225
1187	S871	-2385	338
1188	S872	-2400	225
1189	S873	-2415	338
1190	S874	-2430	225

No.	Name	X	Y
1191	S875	-2445	338
1192	S876	-2460	225
1193	S877	-2475	338
1194	S878	-2490	225
1195	S879	-2505	338
1196	S880	-2520	225
1197	S881	-2535	338
1198	S882	-2550	225
1199	S883	-2565	338
1200	S884	-2580	225
1201	S885	-2595	338
1202	S886	-2610	225
1203	S887	-2625	338
1204	S888	-2640	225
1205	S889	-2655	338
1206	S890	-2670	225
1207	S891	-2685	338
1208	S892	-2700	225
1209	S893	-2715	338
1210	S894	-2730	225
1211	S895	-2745	338
1212	S896	-2760	225
1213	S897	-2775	338
1214	S898	-2790	225
1215	S899	-2805	338
1216	S900	-2820	225
1217	S901	-2835	338
1218	S902	-2850	225
1219	S903	-2865	338
1220	S904	-2880	225
1221	S905	-2895	338
1222	S906	-2910	225
1223	S907	-2925	338
1224	S908	-2940	225
1225	S909	-2955	338
1226	S910	-2970	225
1227	S911	-2985	338
1228	S912	-3000	225
1229	S913	-3015	338
1230	S914	-3030	225
1231	S915	-3045	338
1232	S916	-3060	225
1233	S917	-3075	338
1234	S918	-3090	225
1235	S919	-3105	338
1236	S920	-3120	225
1237	S921	-3135	338
1238	S922	-3150	225
1239	S923	-3165	338
1240	S924	-3180	225
1241	S925	-3195	338
1242	S926	-3210	225
1243	S927	-3225	338
1244	S928	-3240	225
1245	S929	-3255	338
1246	S930	-3270	225
1247	S931	-3285	338
1248	S932	-3300	225
1249	S933	-3315	338
1250	S934	-3330	225
1251	S935	-3345	338
1252	S936	-3360	225
1253	S937	-3375	338
1254	S938	-3390	225
1255	S939	-3405	338
1256	S940	-3420	225
1257	S941	-3435	338
1258	S942	-3450	225
1259	S943	-3465	338
1260	S944	-3480	225
1261	S945	-3495	338
1262	S946	-3510	225
1263	S947	-3525	338
1264	S948	-3540	225
1265	S949	-3555	338

No.	Name	X	Y
1266	S950	-3570	225
1267	S951	-3585	338
1268	S952	-3600	225
1269	S953	-3615	338
1270	S954	-3630	225
1271	S955	-3645	338
1272	S956	-3660	225
1273	S957	-3675	338
1274	S958	-3690	225
1275	S959	-3705	338
1276	S960	-3720	225
1277	S961	-3735	338
1278	S962	-3750	225
1279	S963	-3765	338
1280	S964	-3780	225
1281	S965	-3795	338
1282	S966	-3810	225
1283	S967	-3825	338
1284	S968	-3840	225
1285	S969	-3855	338
1286	S970	-3870	225
1287	S971	-3885	338
1288	S972	-3900	225
1289	S973	-3915	338
1290	S974	-3930	225
1291	S975	-3945	338
1292	S976	-3960	225
1293	S977	-3975	338
1294	S978	-3990	225
1295	S979	-4005	338
1296	S980	-4020	225
1297	S981	-4035	338
1298	S982	-4050	225
1299	S983	-4065	338
1300	S984	-4080	225
1301	S985	-4095	338
1302	S986	-4110	225
1303	S987	-4125	338
1304	S988	-4140	225
1305	S989	-4155	338
1306	S990	-4170	225
1307	S991	-4185	338
1308	S992	-4200	225
1309	S993	-4215	338
1310	S994	-4230	225
1311	S995	-4245	338
1312	S996	-4260	225
1313	S997	-4275	338
1314	S998	-4290	225
1315	S999	-4305	338
1316	S1000	-4320	225
1317	S1001	-4335	338
1318	S1002	-4350	225
1319	S1003	-4365	338
1320	S1004	-4380	225
1321	S1005	-4395	338
1322	S1006	-4410	225
1323	S1007	-4425	338
1324	S1008	-4440	225
1325	S1009	-4455	338
1326	S1010	-4470	225
1327	S1011	-4485	338
1328	S1012	-4500	225
1329	S1013	-4515	338
1330	S1014	-4530	225
1331	S1015	-4545	338
1332	S1016	-4560	225
1333	S1017	-4575	338
1334	S1018	-4590	225
1335	S1019	-4605	338
1336	S1020	-4620	225
1337	S1021	-4635	338
1338	S1022	-4650	225
1339	S1023	-4665	338
1340	S1024	-4680	225

No.	Name	X	Y
1341	S1025	-4695	338
1342	S1026	-4710	225
1343	S1027	-4725	338
1344	S1028	-4740	225
1345	S1029	-4755	338
1346	S1030	-4770	225
1347	S1031	-4785	338
1348	S1032	-4800	225
1349	S1033	-4815	338
1350	S1034	-4830	225
1351	S1035	-4845	338
1352	S1036	-4860	225
1353	S1037	-4875	338
1354	S1038	-4890	225
1355	S1039	-4905	338
1356	S1040	-4920	225
1357	S1041	-4935	338
1358	S1042	-4950	225
1359	S1043	-4965	338
1360	S1044	-4980	225
1361	S1045	-4995	338
1362	S1046	-5010	225
1363	S1047	-5025	338
1364	S1048	-5040	225
1365	S1049	-5055	338
1366	S1050	-5070	225
1367	S1051	-5085	338
1368	S1052	-5100	225
1369	S1053	-5115	338
1370	S1054	-5130	225
1371	S1055	-5145	338
1372	S1056	-5160	225
1373	S1057	-5175	338
1374	S1058	-5190	225
1375	S1059	-5205	338
1376	S1060	-5220	225
1377	S1061	-5235	338
1378	S1062	-5250	225
1379	S1063	-5265	338
1380	S1064	-5280	225
1381	S1065	-5295	338
1382	S1066	-5310	225
1383	S1067	-5325	338
1384	S1068	-5340	225
1385	S1069	-5355	338
1386	S1070	-5370	225
1387	S1071	-5385	338
1388	S1072	-5400	225
1389	S1073	-5415	338
1390	S1074	-5430	225
1391	S1075	-5445	338
1392	S1076	-5460	225
1393	S1077	-5475	338
1394	S1078	-5490	225
1395	S1079	-5505	338
1396	S1080	-5520	225
1397	S1081	-5535	338
1398	S1082	-5550	225
1399	S1083	-5565	338
1400	S1084	-5580	225
1401	S1085	-5595	338
1402	S1086	-5610	225
1403	S1087	-5625	338
1404	S1088	-5640	225
1405	S1089	-5655	338
1406	S1090	-5670	225
1407	S1091	-5685	338
1408	S1092	-5700	225
1409	S1093	-5715	338
1410	S1094	-5730	225
1411	S1095	-5745	338
1412	S1096	-5760	225
1413	S1097	-5775	338
1414	S1098	-5790	225
1415	S1099	-5805	338

No.	Name	X	Y
1416	S1100	-5820	225
1417	S1101	-5835	338
1418	S1102	-5850	225
1419	S1103	-5865	338
1420	S1104	-5880	225
1421	S1105	-5895	338
1422	S1106	-5910	225
1423	S1107	-5925	338
1424	S1108	-5940	225
1425	S1109	-5955	338
1426	S1110	-5970	225
1427	S1111	-5985	338
1428	S1112	-6000	225
1429	S1113	-6015	338
1430	S1114	-6030	225
1431	S1115	-6045	338
1432	S1116	-6060	225
1433	S1117	-6075	338
1434	S1118	-6090	225
1435	S1119	-6105	338
1436	S1120	-6120	225
1437	S1121	-6135	338
1438	S1122	-6150	225
1439	S1123	-6165	338
1440	S1124	-6180	225
1441	S1125	-6195	338
1442	S1126	-6210	225
1443	S1127	-6225	338
1444	S1128	-6240	225
1445	S1129	-6255	338
1446	S1130	-6270	225
1447	S1131	-6285	338
1448	S1132	-6300	225
1449	S1133	-6315	338
1450	S1134	-6330	225
1451	S1135	-6345	338
1452	S1136	-6360	225
1453	S1137	-6375	338
1454	S1138	-6390	225
1455	S1139	-6405	338
1456	S1140	-6420	225
1457	S1141	-6435	338
1458	S1142	-6450	225
1459	S1143	-6465	338
1460	S1144	-6480	225
1461	S1145	-6495	338
1462	S1146	-6510	225
1463	S1147	-6525	338
1464	S1148	-6540	225
1465	S1149	-6555	338
1466	S1150	-6570	225
1467	S1151	-6585	338
1468	S1152	-6600	225
1469	S1153	-6615	338
1470	S1154	-6630	225
1471	S1155	-6645	338
1472	S1156	-6660	225
1473	S1157	-6675	338
1474	S1158	-6690	225
1475	S1159	-6705	338
1476	S1160	-6720	225
1477	S1161	-6735	338
1478	S1162	-6750	225
1479	S1163	-6765	338
1480	S1164	-6780	225
1481	S1165	-6795	338
1482	S1166	-6810	225
1483	S1167	-6825	338
1484	S1168	-6840	225
1485	S1169	-6855	338
1486	S1170	-6870	225
1487	S1171	-6885	338
1488	S1172	-6900	225
1489	S1173	-6915	338
1490	S1174	-6930	225

No.	Name	X	Y
1491	S1175	-6945	338
1492	S1176	-6960	225
1493	S1177	-6975	338
1494	S1178	-6990	225
1495	S1179	-7005	338
1496	S1180	-7020	225
1497	S1181	-7035	338
1498	S1182	-7050	225
1499	S1183	-7065	338
1500	S1184	-7080	225
1501	S1185	-7095	338
1502	S1186	-7110	225
1503	S1187	-7125	338
1504	S1188	-7140	225
1505	S1189	-7155	338
1506	S1190	-7170	225
1507	S1191	-7185	338
1508	S1192	-7200	225
1509	S1193	-7215	338
1510	S1194	-7230	225
1511	S1195	-7245	338
1512	S1196	-7260	225
1513	S1197	-7275	338
1514	S1198	-7290	225
1515	S1199	-7305	338
1516	S1200	-7320	225
1517	S1201	-7335	338
1518	S1202	-7350	225
1519	S1203	-7365	338
1520	S1204	-7380	225
1521	S1205	-7395	338
1522	S1206	-7410	225
1523	S1207	-7425	338
1524	S1208	-7440	225
1525	S1209	-7455	338
1526	S1210	-7470	225
1527	S1211	-7485	338
1528	S1212	-7500	225
1529	S1213	-7515	338
1530	S1214	-7530	225
1531	S1215	-7545	338
1532	S1216	-7560	225
1533	S1217	-7575	338
1534	S1218	-7590	225
1535	S1219	-7605	338
1536	S1220	-7620	225
1537	S1221	-7635	338
1538	S1222	-7650	225
1539	S1223	-7665	338
1540	S1224	-7680	225
1541	S1225	-7695	338
1542	S1226	-7710	225
1543	S1227	-7725	338
1544	S1228	-7740	225
1545	S1229	-7755	338
1546	S1230	-7770	225
1547	S1231	-7785	338
1548	S1232	-7800	225
1549	S1233	-7815	338
1550	S1234	-7830	225
1551	S1235	-7845	338
1552	S1236	-7860	225
1553	S1237	-7875	338
1554	S1238	-7890	225
1555	S1239	-7905	338
1556	S1240	-7920	225
1557	S1241	-7935	338
1558	S1242	-7950	225
1559	S1243	-7965	338
1560	S1244	-7980	225
1561	S1245	-7995	338
1562	S1246	-8010	225
1563	S1247	-8025	338
1564	S1248	-8040	225
1565	S1249	-8055	338

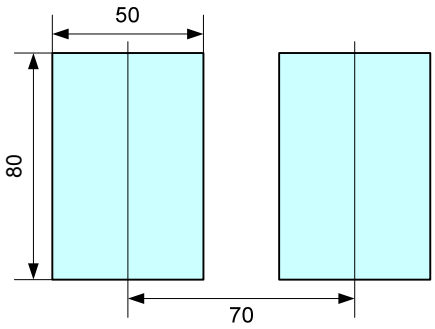
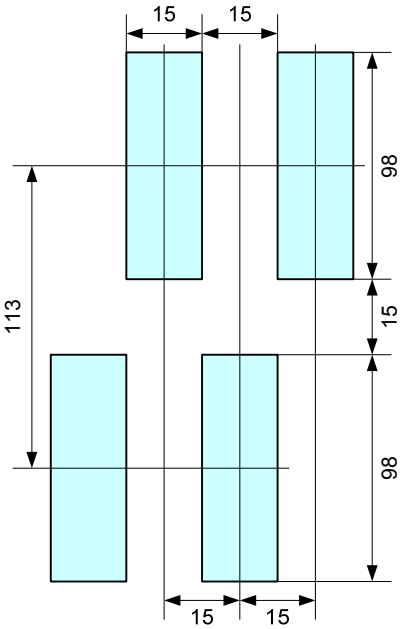
No.	Name	X	Y
1566	S1250	-8070	225
1567	S1251	-8085	338
1568	S1252	-8100	225
1569	S1253	-8115	338
1570	S1254	-8130	225
1571	S1255	-8145	338
1572	S1256	-8160	225
1573	S1257	-8175	338
1574	S1258	-8190	225
1575	S1259	-8205	338
1576	S1260	-8220	225
1577	S1261	-8235	338
1578	S1262	-8250	225
1579	S1263	-8265	338
1580	S1264	-8280	225
1581	S1265	-8295	338
1582	S1266	-8310	225
1583	S1267	-8325	338
1584	S1268	-8340	225
1585	S1269	-8355	338
1586	S1270	-8370	225
1587	S1271	-8385	338
1588	S1272	-8400	225
1589	S1273	-8415	338
1590	S1274	-8430	225
1591	S1275	-8445	338
1592	S1276	-8460	225
1593	S1277	-8475	338
1594	S1278	-8490	225
1595	S1279	-8505	338
1596	S1280	-8520	225
1597	S1281	-8535	338
1598	S1282	-8550	225
1599	S1283	-8565	338
1600	S1284	-8580	225
1601	S1285	-8595	338
1602	S1286	-8610	225
1603	S1287	-8625	338
1604	S1288	-8640	225
1605	S1289	-8655	338
1606	S1290	-8670	225
1607	S1291	-8685	338
1608	S1292	-8700	225
1609	S1293	-8715	338
1610	S1294	-8730	225
1611	S1295	-8745	338
1612	S1296	-8760	225
1613	S1297	-8775	338
1614	S1298	-8790	225
1615	S1299	-8805	338
1616	S1300	-8820	225
1617	S1301	-8835	338
1618	S1302	-8850	225
1619	S1303	-8865	338
1620	S1304	-8880	225
1621	S1305	-8895	338
1622	S1306	-8910	225
1623	S1307	-8925	338
1624	S1308	-8940	225
1625	S1309	-8955	338
1626	S1310	-8970	225
1627	S1311	-8985	338
1628	S1312	-9000	225
1629	S1313	-9015	338
1630	S1314	-9030	225
1631	S1315	-9045	338
1632	S1316	-9060	225
1633	S1317	-9075	338
1634	S1318	-9090	225
1635	S1319	-9105	338
1636	S1320	-9120	225
1637	S1321	-9135	338
1638	S1322	-9150	225
1639	S1323	-9165	338
1640	S1324	-9180	225

No.	Name	X	Y
1641	S1325	-9195	338
1642	S1326	-9210	225
1643	S1327	-9225	338
1644	S1328	-9240	225
1645	S1329	-9255	338
1646	S1330	-9270	225
1647	S1331	-9285	338
1648	S1332	-9300	225
1649	S1333	-9315	338
1650	S1334	-9330	225
1651	S1335	-9345	338
1652	S1336	-9360	225
1653	S1337	-9375	338
1654	S1338	-9390	225
1655	S1339	-9405	338
1656	S1340	-9420	225
1657	S1341	-9435	338
1658	S1342	-9450	225
1659	S1343	-9465	338
1660	S1344	-9480	225
1661	S1345	-9495	338
1662	S1346	-9510	225
1663	S1347	-9525	338
1664	S1348	-9540	225
1665	S1349	-9555	338
1666	S1350	-9570	225
1667	S1351	-9585	338
1668	S1352	-9600	225
1669	S1353	-9615	338
1670	S1354	-9630	225
1671	S1355	-9645	338
1672	S1356	-9660	225
1673	S1357	-9675	338
1674	S1358	-9690	225
1675	S1359	-9705	338
1676	S1360	-9720	225
1677	S1361	-9735	338
1678	S1362	-9750	225
1679	S1363	-9765	338
1680	S1364	-9780	225
1681	S1365	-9795	338
1682	S1366	-9810	225
1683	S1367	-9825	338
1684	S1368	-9840	225
1685	S1369	-9855	338
1686	S1370	-9870	225
1687	S1371	-9885	338
1688	S1372	-9900	225
1689	S1373	-9915	338
1690	S1374	-9930	225
1691	S1375	-9945	338
1692	S1376	-9960	225
1693	S1377	-9975	338
1694	S1378	-9990	225
1695	S1379	-10005	338
1696	S1380	-10020	225
1697	S1381	-10035	338
1698	S1382	-10050	225
1699	S1383	-10065	338
1700	S1384	-10080	225
1701	S1385	-10095	338
1702	S1386	-10110	225
1703	S1387	-10125	338
1704	S1388	-10140	225
1705	S1389	-10155	338
1706	S1390	-10170	225
1707	S1391	-10185	338
1708	S1392	-10200	225
1709	S1393	-10215	338
1710	S1394	-10230	225
1711	S1395	-10245	338
1712	S1396	-10260	225
1713	S1397	-10275	338
1714	S1398	-10290	225
1715	S1399	-10305	338

No.	Name	X	Y
1716	S1400	-10320	225
1717	S1401	-10335	338
1718	S1402	-10350	225
1719	S1403	-10365	338
1720	S1404	-10380	225
1721	S1405	-10395	338
1722	S1406	-10410	225
1723	S1407	-10425	338
1724	S1408	-10440	225
1725	S1409	-10455	338
1726	S1410	-10470	225
1727	S1411	-10485	338
1728	S1412	-10500	225
1729	S1413	-10515	338
1730	S1414	-10530	225
1731	S1415	-10545	338
1732	S1416	-10560	225
1733	S1417	-10575	338
1734	S1418	-10590	225
1735	S1419	-10605	338
1736	S1420	-10620	225
1737	S1421	-10635	338
1738	S1422	-10650	225
1739	S1423	-10665	338
1740	S1424	-10680	225
1741	S1425	-10695	338
1742	S1426	-10710	225
1743	S1427	-10725	338
1744	S1428	-10740	225
1745	S1429	-10755	338
1746	S1430	-10770	225
1747	S1431	-10785	338
1748	S1432	-10800	225
1749	S1433	-10815	338
1750	S1434	-10830	225
1751	S1435	-10845	338
1752	S1436	-10860	225
1753	S1437	-10875	338
1754	S1438	-10890	225
1755	S1439	-10905	338
1756	S1440	-10920	225
	DUMMY	-10935	338

Alignment mark	X	Y
✚ (1-a)	-11060	325
✚ (1-b)	11060	325

4.4 Bump Arrangement

In-Line bumps (No. 1 to 312)	 Area = 4000 um^2
Staggered bumps (No. 313 to 1756)	 Area = 1470 um^2

5 Functional Description

5.1 SPI (Serial Peripheral Interface)

The serial interface is selected by setting the IM[2:0] = 110x for register access while MIPI DPI is used for pixel data streaming in LG4573. The data is transferred via chip select line (nCS), serial transfer clock line (SCK), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM[0] pin functions as the ID pin, and the DB[23:0] pins, not used in this mode, must be fixed at either IOVCC or GND level. When nCS is high, SCK clock pulse or serial input (SDI) and output (SDO) have no effect. A falling edge on nCS enables the serial interface and indicate the start of data transmission.

The LG4573 recognizes the start of data transfer on the falling edge of nCS input and starts transferring the start byte. It recognizes the data transferd on the rising edge of nCS input. The LG4573 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the LG4573 are compared and both 6-bit data match, and then the LG4573 starts taking in data. The least significant bit of the device identification code is set with the ID pin. "The seventh bit of the start byte is assigned to the register select bit (RS). When RS = 0, an index register write operation is executed. When RS = 1, an instruction write operation is executed. The eighth bit of the start byte is to select read or write operation (R/W bit). The LG4573 receives data when the R/W = 0, and transfers data when the R/W = 1.

After receiving the start byte, the LG4573 starts transferring or receiving data. The LG4573 executes data transfer from the MSB.

Table 1 Start Byte Format

Transferred bits	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Device ID code						RS	R/W
	0	1	1	1	0	IM[0]		

Note: ID bit is selected by setting the IM0/ID pin.

Table 2

RS	**R/W**	**Function**
0	0	Set an index register
~~0~~	~~1~~	~~Read a status~~
1	0	Write an instruction
1	1	Read an instruction

5.1.1 Write/ Read Cycle Sequence

As shown in the following figure, on the rising edge of SCK the SDI data start being transferred to LG4573. But the serial reading operation through SDO happens on the falling edge of SCK.

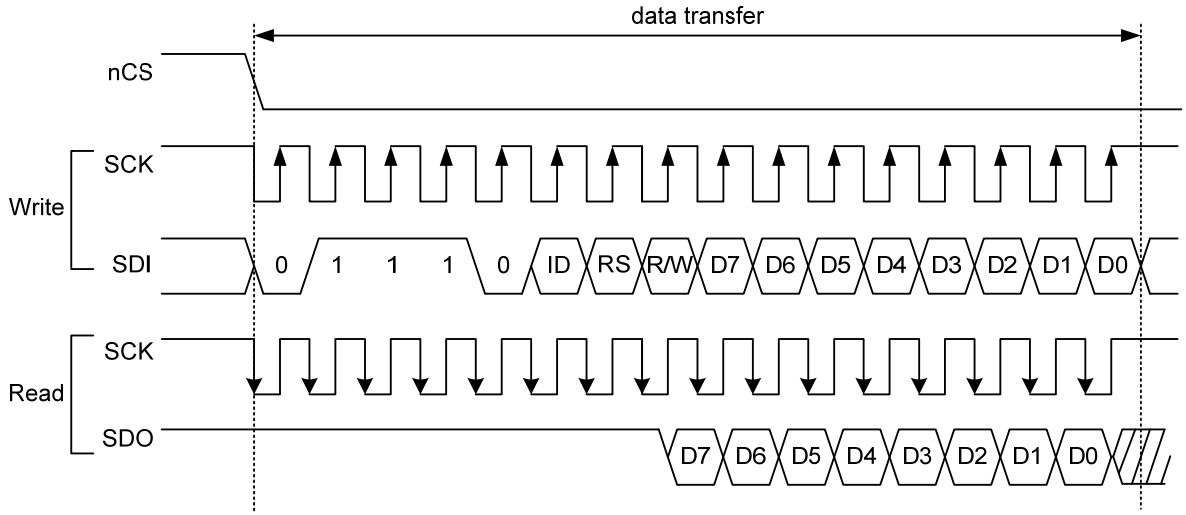


Figure 2. SPI Interface

The following figures demonstrate the serial reading operation in the FAh register for example.

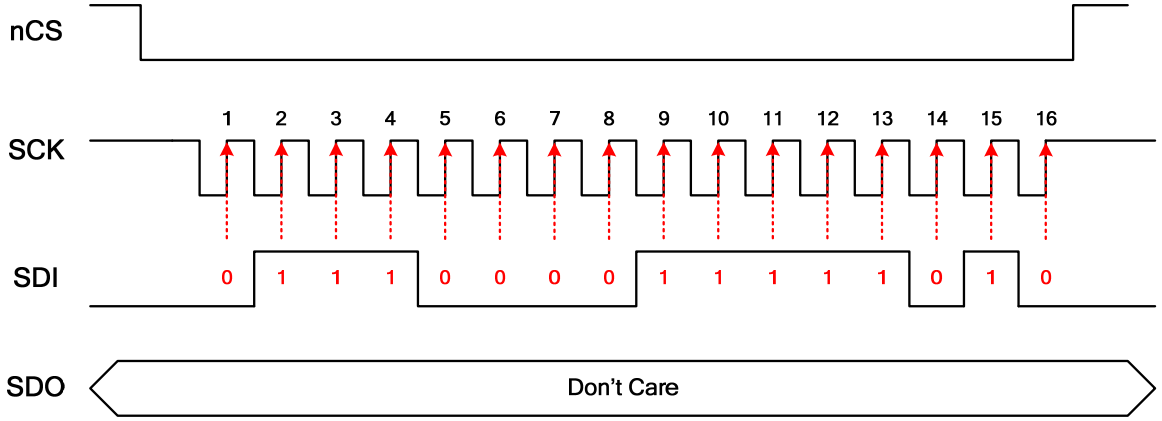


Figure 3. Example for serial data reading

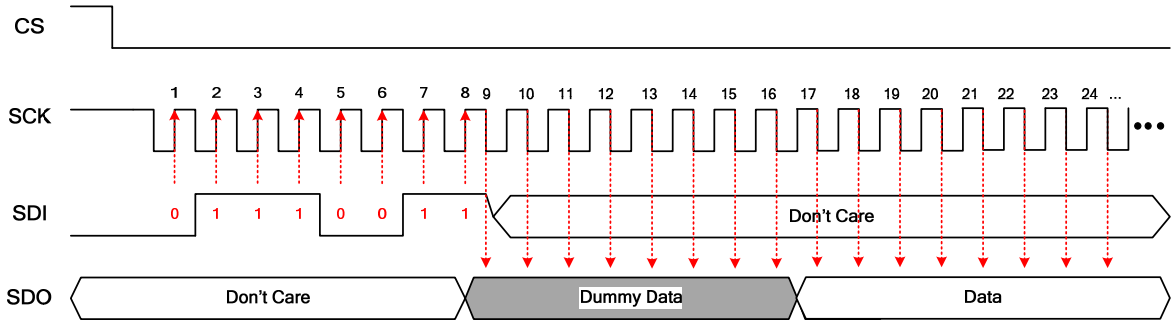


Figure 4. Example for serial data reading – continued

5.2 MIPI DBI Type C

The LG4573 supports MIPI DBI type C (4-wire 9-bit serial interface).

5.2.1 Write Cycle Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The type C interface utilizes nCS, SCK and SDI signals. SCK is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCK.

The following figure shows the write cycle for the type C interface.

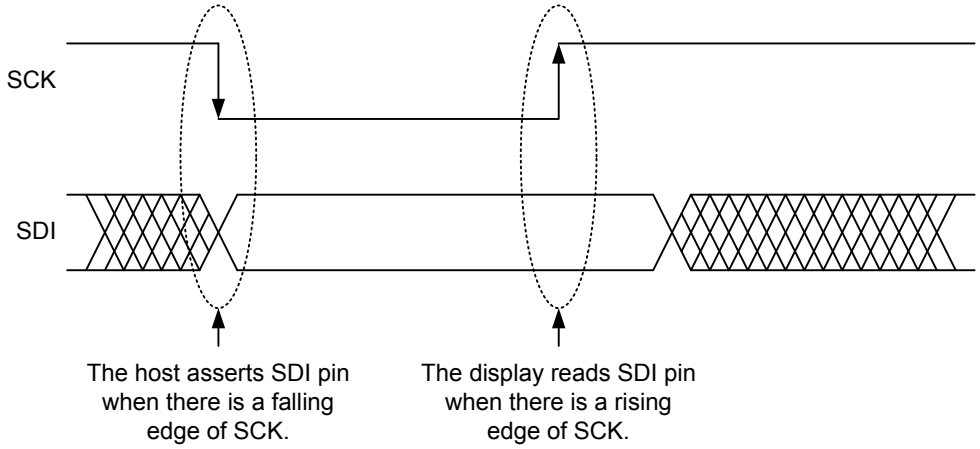


Figure 5. DBI Type C Interface Write Cycle

Note: SCK is an unsynchronized signal; it can be stopped.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when nCS is driven from high to low and ends when nCS is pulled high. Each byte is nine write cycles in length.

The type C interface write sequences is described in Figure 6.

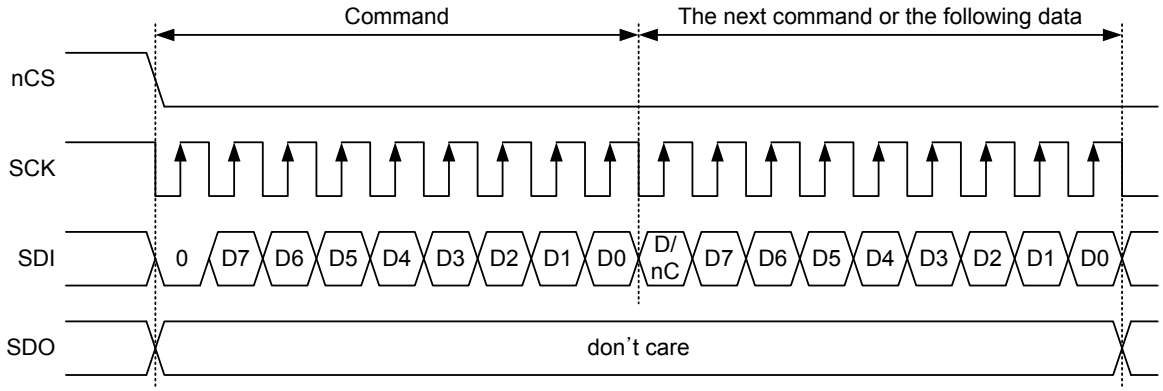


Figure 6. DBI Type C Interface Write Sequence

5.2.2 Read Cycle Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The type C interface utilizes nCS, SCK and SDO signals. SCK is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCK.

Figure 7 shows the read cycle for the type C interface.

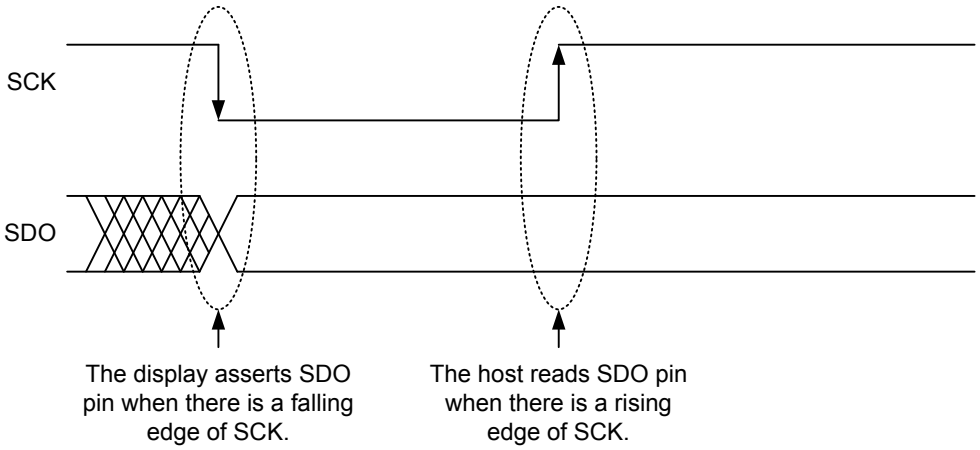


Figure 7. DBI Type C Interface Read Cycle

Note: SCK is an unsynchronized signal; it can be stopped.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when nCS is driven from high to low and ends when nCS is pulled high. Each byte is nine read cycles in length.

The type C interface read sequence is shown in Figure 8.

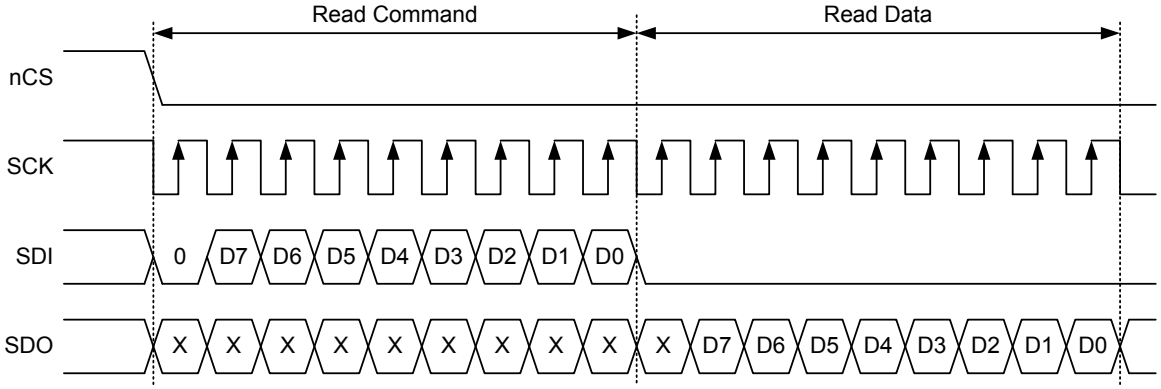


Figure 8. DBI Type C Interface Read Sequence

5.2.3 Break and Pause of Sequences

The host processor can break a read or write sequence by pulling the nCS signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when nCS is again driven low.

The host processor can pause a read or write sequence by pulling the nCS signal high between command or data bytes. The display module shall wait for the host processor to drive nCS low before continuing the read or write sequence at the point where the sequence was paused.

5.3 MIPI DPI-2

5.3.1 Interface Signals

Table 3. Interface Signals for DPI

Symbol	Name	I/O	Description
VSYNC	Vertical sync	I	Vertical synchronization timing signal
HSYNC	Horizontal sync	I	Horizontal synchronization timing signal
DE	Data enable	I	Data enable signal (assertion indicates valid pixels)
PCLK	Pixel Clock	I	Pixel clock for capturing pixels at display interface
DB[15:0], DB[17:0] or DB[23:0]	Pixel Data	I	Pixel data in 16-bit, 18-bit, or 24-bit format

5.3.2 Interface Color Coding

Table 4 specifies the mapping of data bits, as components of primary pixel color values R, G, and B, to signal lines at the interface.

Note: LG4573 supports configuration 3 for 16-bit pixels, configuration 2 for 18-bit pixels and 24-bit pixels.

Table 4. Interface Color Coding

Signal Line	16-bit			18-bit		24-bit
	Configuration 1	Configuration 2	Configuration 3	Configuration 1	Configuration 2	
D23	~~(not used)~~	~~(not used)~~	(not used)	~~(not used)~~	(not used)	R7
D22	~~(not used)~~	~~(not used)~~	(not used)	~~(not used)~~	(not used)	R6
D21	~~(not used)~~	~~(not used)~~	R4	~~(not used)~~	R5	R5
D20	~~(not used)~~	~~R4~~	R3	~~(not used)~~	R4	R4
D19	~~(not used)~~	~~R3~~	R2	~~(not used)~~	R3	R3
D18	~~(not used)~~	~~R2~~	R1	~~(not used)~~	R2	R2
D17	~~(not used)~~	~~R1~~	R0	~~R5~~	R1	R1
D16	~~(not used)~~	~~R0~~	(not used)	~~R4~~	R0	R0
D15	~~R4~~	~~(not used)~~	(not used)	~~R3~~	(not used)	G7
D14	~~R3~~	~~(not used)~~	(not used)	~~R2~~	(not used)	G6
D13	~~R2~~	~~G5~~	G5	~~R1~~	G5	G5
D12	~~R1~~	~~G4~~	G4	~~R0~~	G4	G4
D11	~~R0~~	~~G3~~	G3	~~G5~~	G3	G3
D10	~~G5~~	~~G2~~	G2	~~G4~~	G2	G2
D9	~~G4~~	~~G1~~	G1	~~G3~~	G1	G1
D8	~~G3~~	~~G0~~	G0	~~G2~~	G0	G0
D7	~~G2~~	~~(not used)~~	(not used)	~~G1~~	(not used)	B7
D6	~~G1~~	~~(not used)~~	(not used)	~~G0~~	(not used)	B6
D5	~~G0~~	~~(not used)~~	B4	~~B5~~	B5	B5
D4	~~B4~~	~~B4~~	B3	~~B4~~	B4	B4
D3	~~B3~~	~~B3~~	B2	~~B3~~	B3	B3
D2	~~B2~~	~~B2~~	B1	~~B2~~	B2	B2
D1	~~B1~~	~~B1~~	B0	~~B1~~	B1	B1
D0	~~B0~~	~~B0~~	(not used)	~~B0~~	B0	B0

There are three mappings for 16-bit pixels to data signals, two mapping for 18-bit pixels to data signals, and one mapping for 24-bit pixels to data signals.

5.4 Backlight Control Function

5.4.1 CABC (Content Adaptive Brightness Control)

The LG4573 supports "Content Adaptive Brightness Control" function which can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depend on the content of the image.

The following figure shows that how the CABC algorithm works. The CABC block accumulates the gray levels for each pixels of the image and thus CABC block becomes to know the histograms about the gray levels of the image. Next, CABC block modify the original image data to have more widely spread shape while it makes the back light luminance lower so that the image luminance perceived by human becomes almost same.

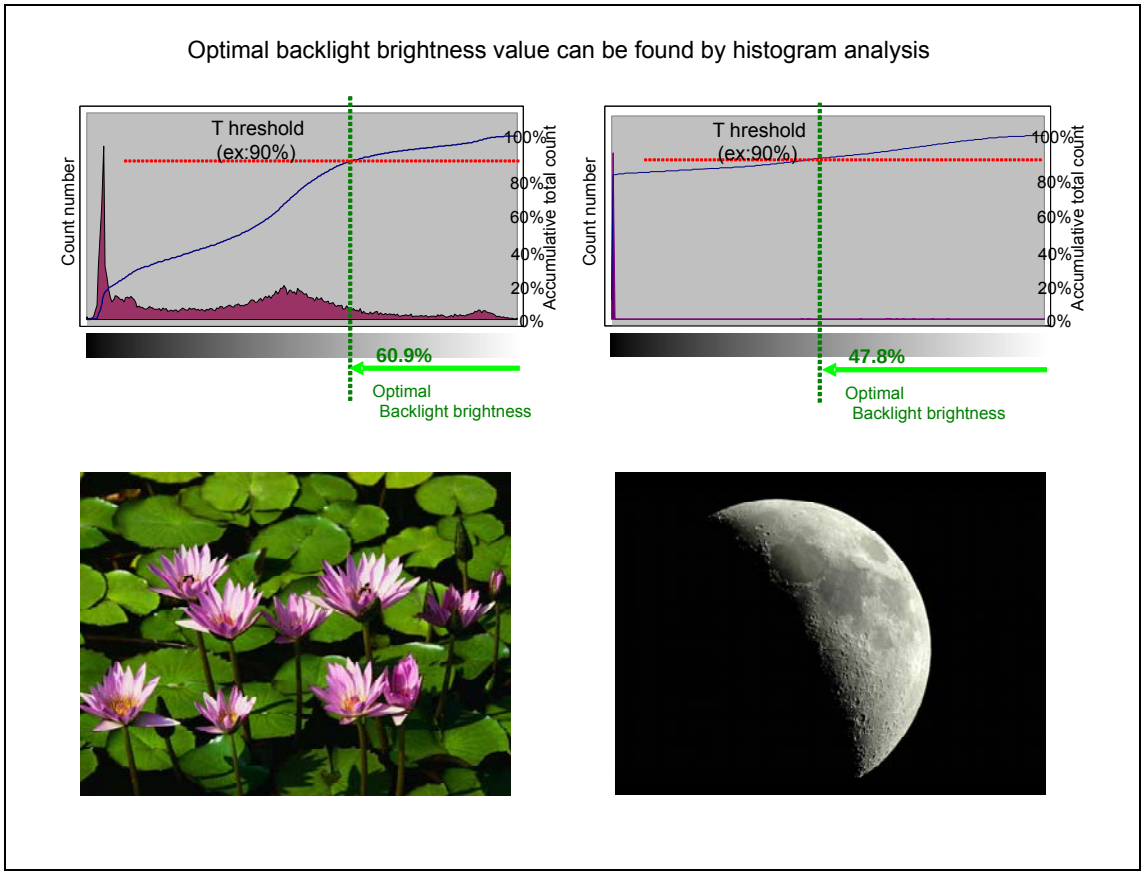


Figure 9. Simple Explanation of Content Adaptive Brightness Control

5.4.2 Brightness Control Block and CABC Block

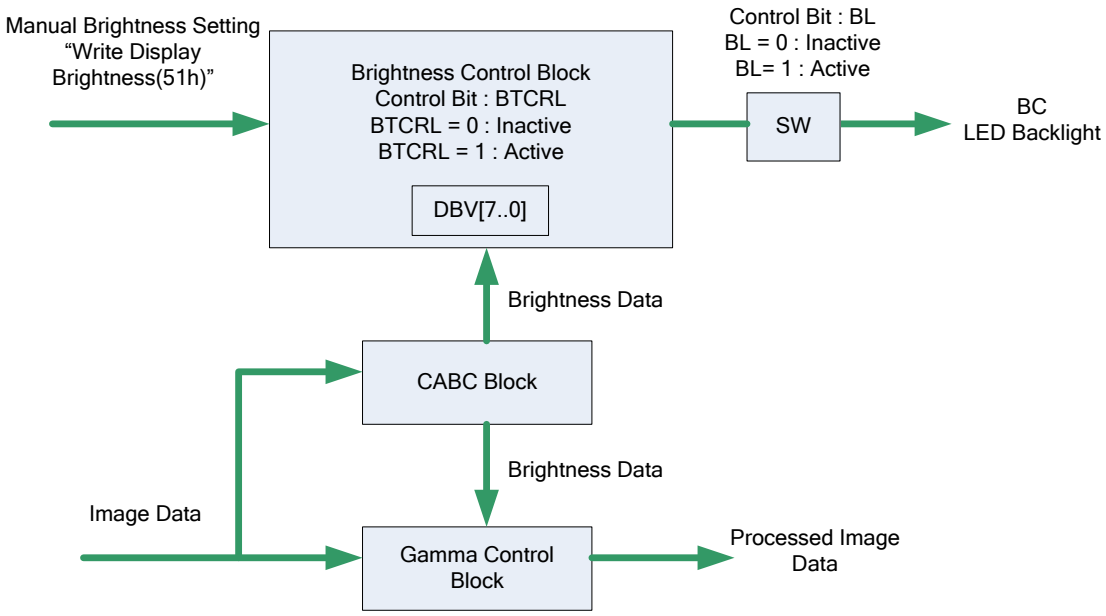


Figure 10. Block Diagram for Brightness Control Block and CABC Block

Brightness control block is used to control the display brightness as follows:

There is a resister, DBV: 8 bit, for display brightness of manual brightness setting and CABC in the display module. There is a PWM output signal, BC line, to control the LED driver IC in order to control display brightness. The brightness control method should be taken into account to avoid abnormal visible effect related with scanning frame frequency.

The brightness control block can be used in manual brightness mode and CABC mode, see "Write CTRL Display (53h)" and "Write Content Adaptive Brightness Control (55h)".

The user can adjust brightness, see "Write Display Brightness (51h)" for the display.

	WRCABC(55h)	Function	RDCABCMB(5Fh)	Image
CABC Off	00b	Disable	WRCABCMB(5Eh)	Original
CABC On	01b /10b /11b	Enable	WRCABCMB(5Eh)	CABC modified

Brightness level calculates with the following formula.

Display Output Brightness = Manual brightness setting * CABC brightness ratio

Below drawing is for the explanation of the CABC minimum brightness setting.

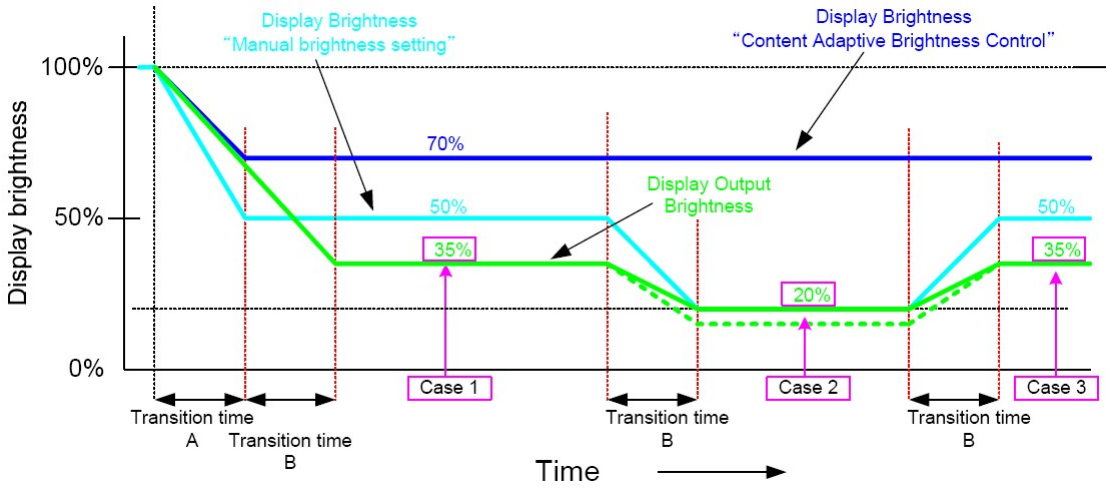


Figure 11. Controlled Display Brightness by LABC and CABC Algorithm

CABC minimum brightness value = 51 (33h: 20% display brightness)

	Display Brightness [manual setting]	**Brightness Ratio[CABC]**	**Calculation result of the display brightness formula**	**Display Output Brightness**	**Image**
Case 1	50%	70%	35%	35%	CABC modified
Case 2	20%	70%	14%	20%	CABC modified
Case 3	50%	70%	35%	35%	CABC modified

At the case 2, the calculation result of the display brightness is 14%. CABC minimum brightness value is set to 20% brightness. Actual display brightness is 20% as the CABC minimum brightness setting.

To get more easy understandings and control of this CABC function, the below conceptual control flow diagram would be a help. In the following diagram, the DD, BCTRL, and BL are control parameter in 53h register. They control the CABC paths. If DD=0, then CABC function is disabled and the manual brightness setting by DBV[7:0] in 51h register is available. If DD=1, CABC function will start to work with the maximum and minimum brightness settings respectively by DBV[7:0] and CMB[7:0] in 5Eh register. If BCTRL=1, the CABC function will go through to next path. But if BCTRL=0, GND level for BLU_PWM would be forced. If BL=1, the CABC function will go though with BCTRL=1 and controls the duties of PWM (Pulse Width Modulated) waveforms through BLU_PWM pad. Finally, the PWMP parameter in C8h register can change the polarity of BLU_PWM output. If PWMP=0, BLU_PWM waveform works as active high but if 1, then the BLU_PWM waveform works as active low.

The not-shown parameter in the following diagram to control CABC function are CDSP[3:0], CDMP[3:0], and FPWM[1:0] in C8h register, where CDSP and CDMP parameter control the dimming levels of still images and moving images, respectively. If CDSP=8, then the duties of BLU_PWM are increased or decreased by 8 levels per frame, whose total levels of this is 255, after comparing the differences between predetermined threshold value and the calculated histogram value for still images. And if CDMP=4, then the duties of BLU_PWM are increased or decreased by 4 levels per frame, whose total levels of this is 255, after comparing the differences between predetermined threshold value and the calculated histogram value for moving images. The last parameter FPWM controls the frequencies of BLU_PWM output. The setting 0 means 2 times of frame frequency, 1 means 4 times, 2 means 8

times, and 3 means 16 times of frame frequency. It goes faster according to the increased FPWM values. The tables for them are shown in C8h register description section.

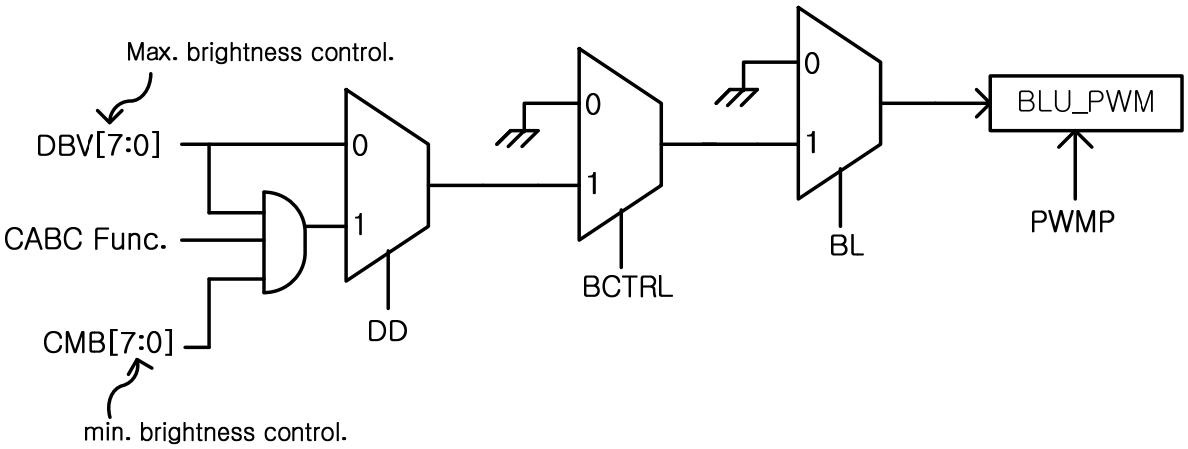


Figure 12. Conceptual control flow diagram of CABC function.

5.5 LCD Power Supply Circuit

The LCD power supply circuit generates the voltage levels of DDVDH, DDVDL, VCL, VREG1OUT, VREG2OUT, VGH, VGL, LVGL and VCOM for driving an LCD.

The internal logic power supply regulator generates internal logic power supply VDD.

5.5.1 Voltage Setting Pattern Diagram

The pattern diagram of voltage setting and waveforms of the liquid crystal application voltages are as follows.

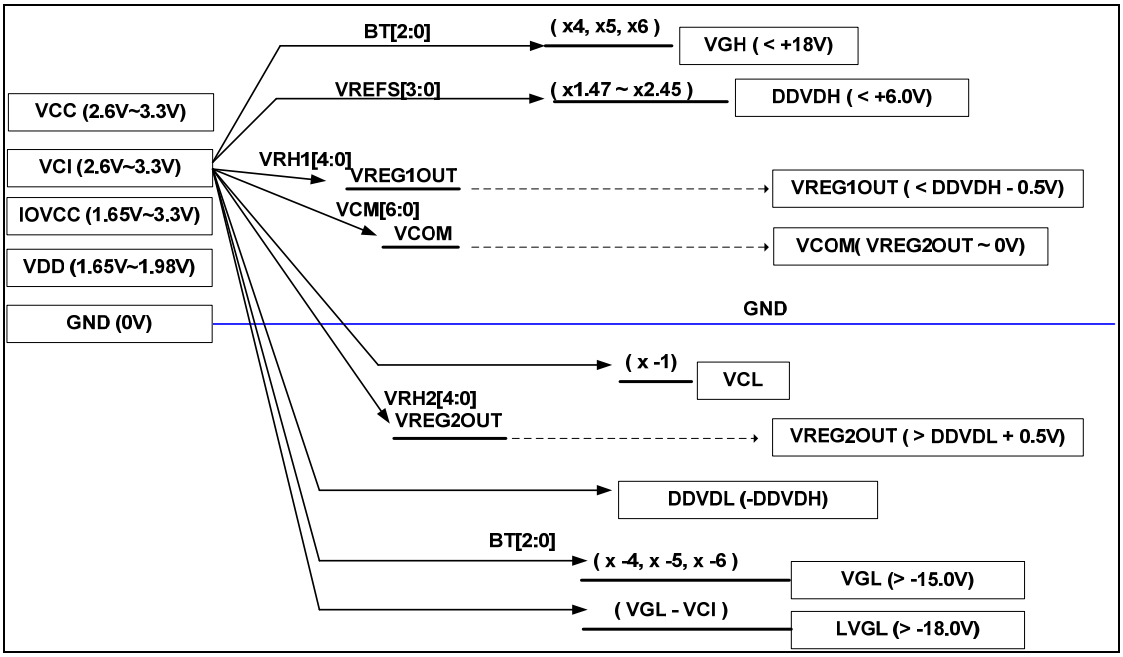
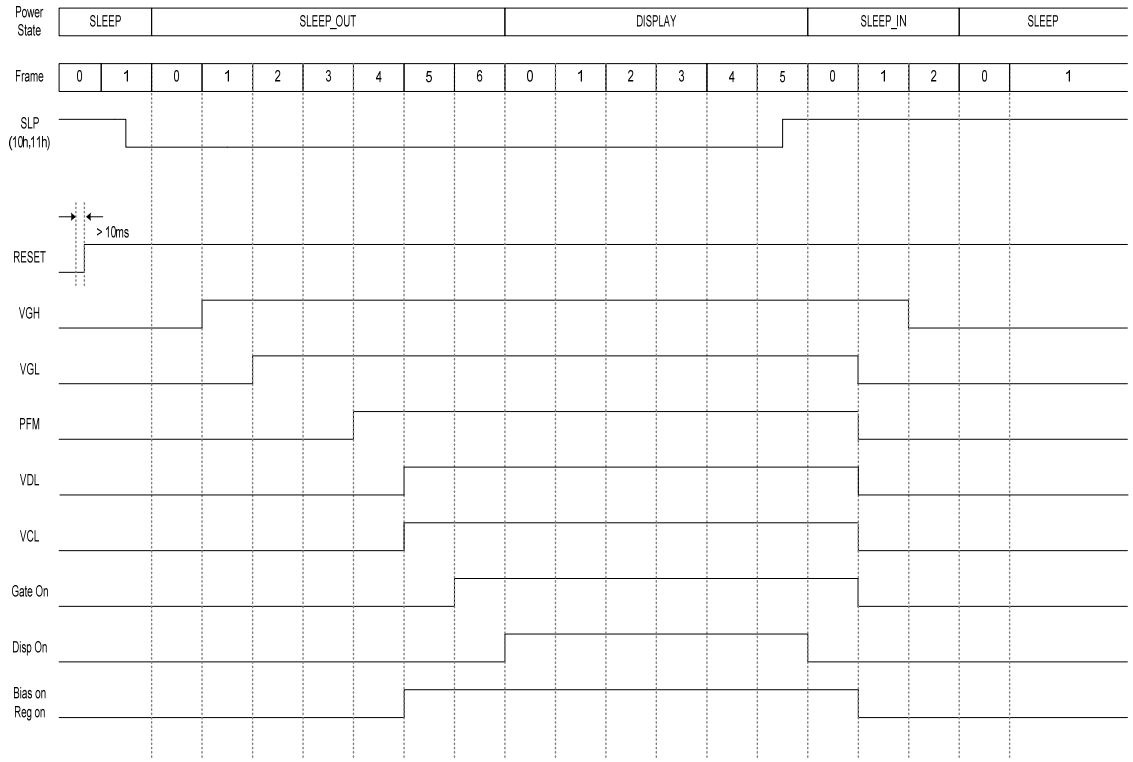


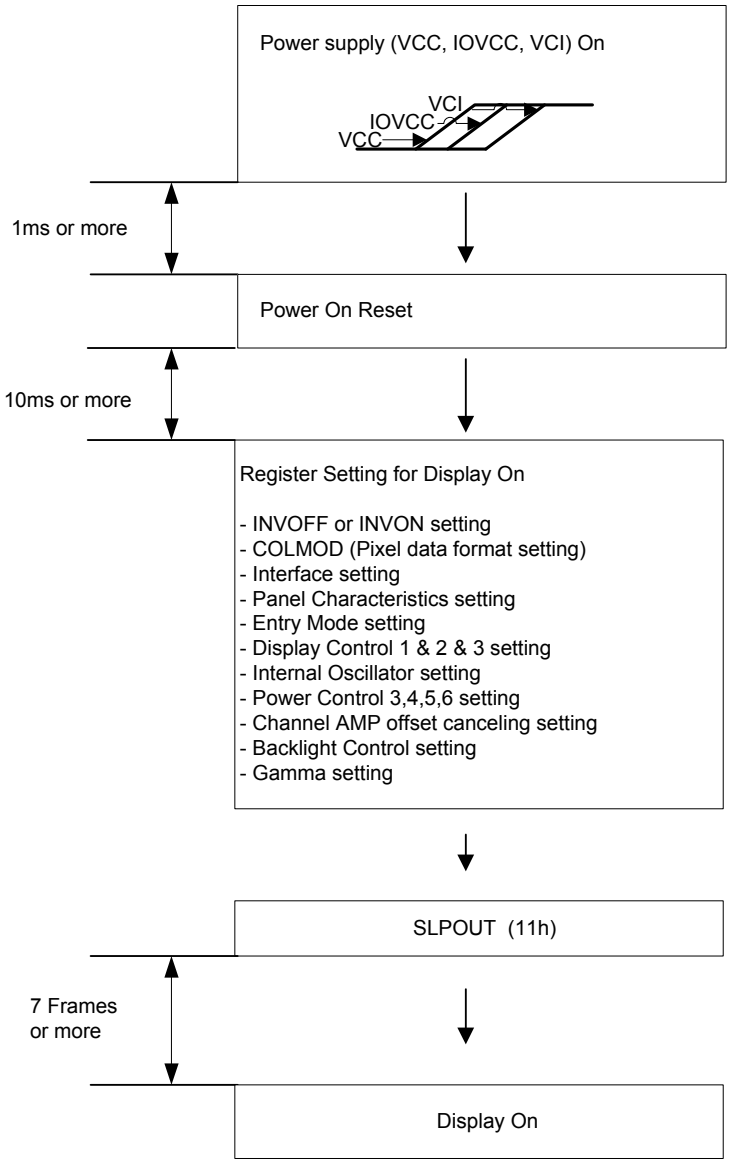
Figure 13. Pattern Diagram for Voltage Setting

5.5.2 Power On/Off Sequence



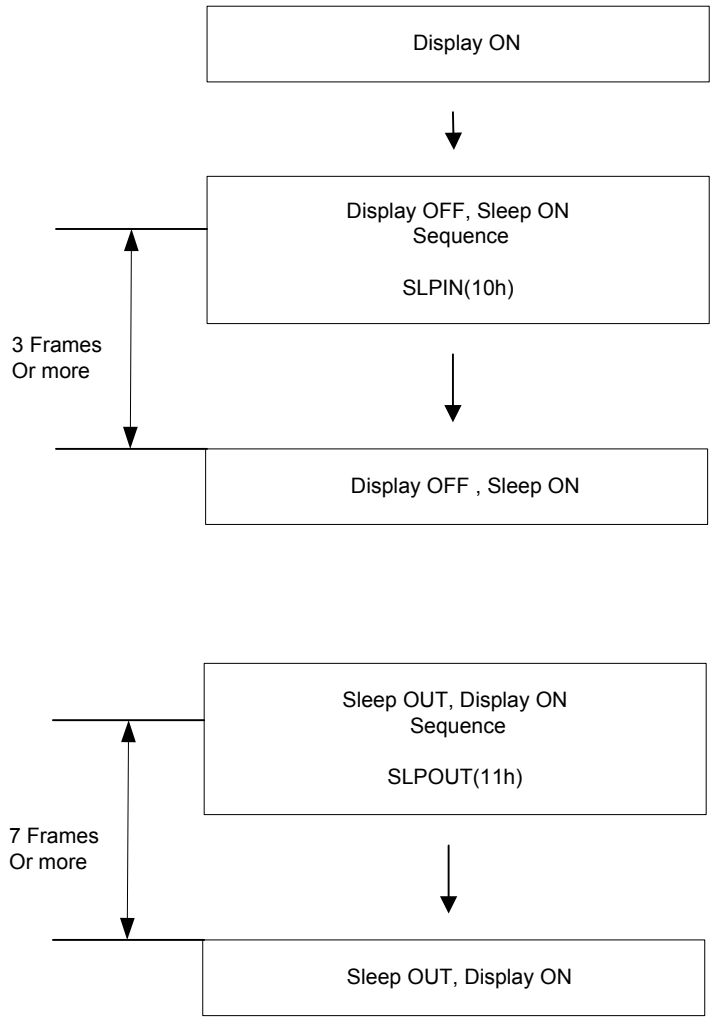
5.5.3 Display On Sequence

Display On Sequence



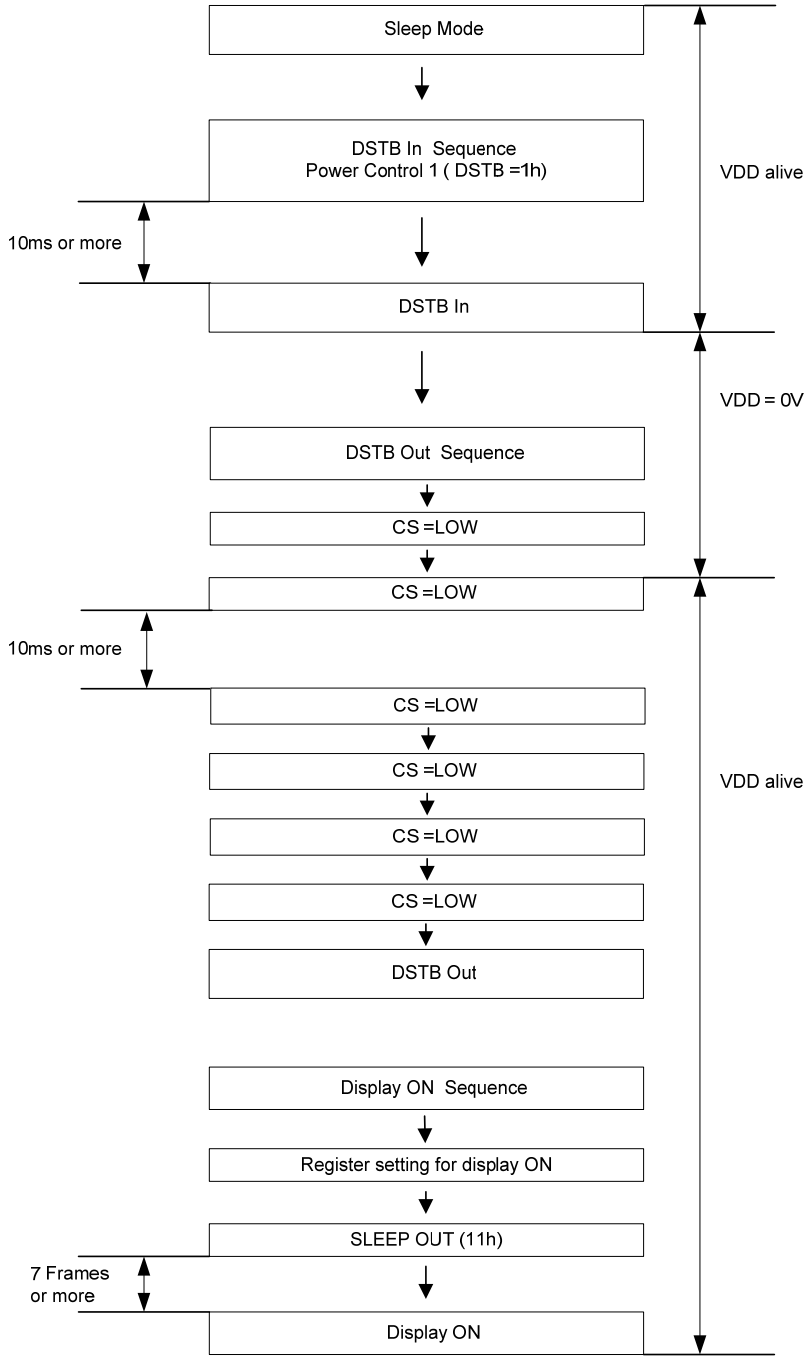
5.5.4 Sleep In, Out Sequence

Sleep In, Out Sequence



5.5.5 DSTB IN, DSTB OUT, Display On Sequence

DSTB IN, DSTB OUT, Display ON Sequences



5.6 Gamma Correction Function

The LG4573 has the gamma correction function to display in 16M colors simultaneously. The gamma correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers. Each register groups further consists of register groups of positive and negative polarities. Each register group is set independently to other register groups, making the LG4573 available with liquid crystal panels of various characteristics.

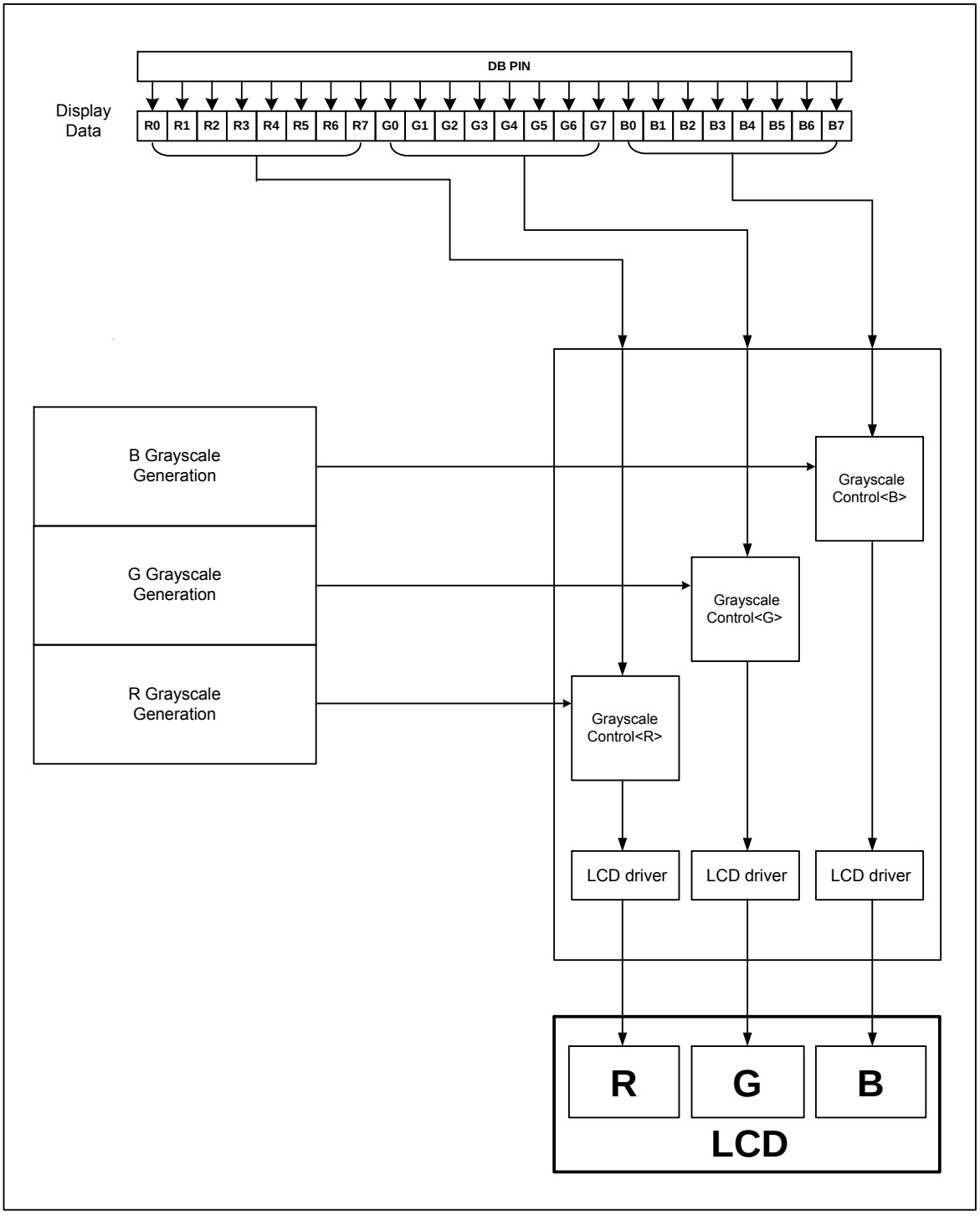


Figure 14. Grayscale Control

5.6.1 Grayscale Generation Unit Configuration

The following figure illustrates the grayscale generation unit of the LG4573.

To generate 64 grayscale voltages (V0 to V63), the LG4573 first generates eight reference grayscale voltages (VINP0-7/VINN0-7). The grayscale generation unit then divides eight reference grayscale voltages with the ladder resistors incorporated therein.

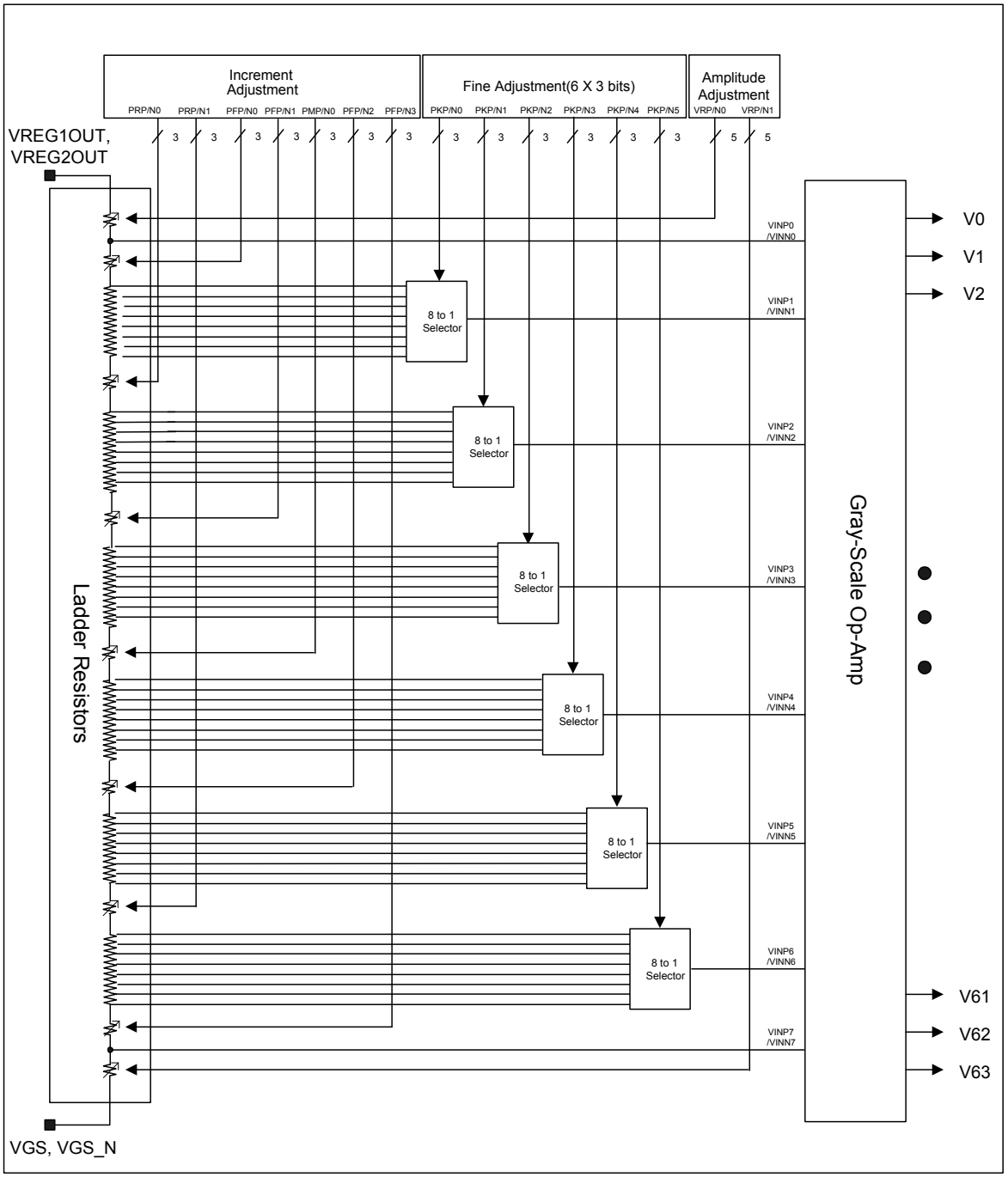


Figure 15. Grayscale Generation unit

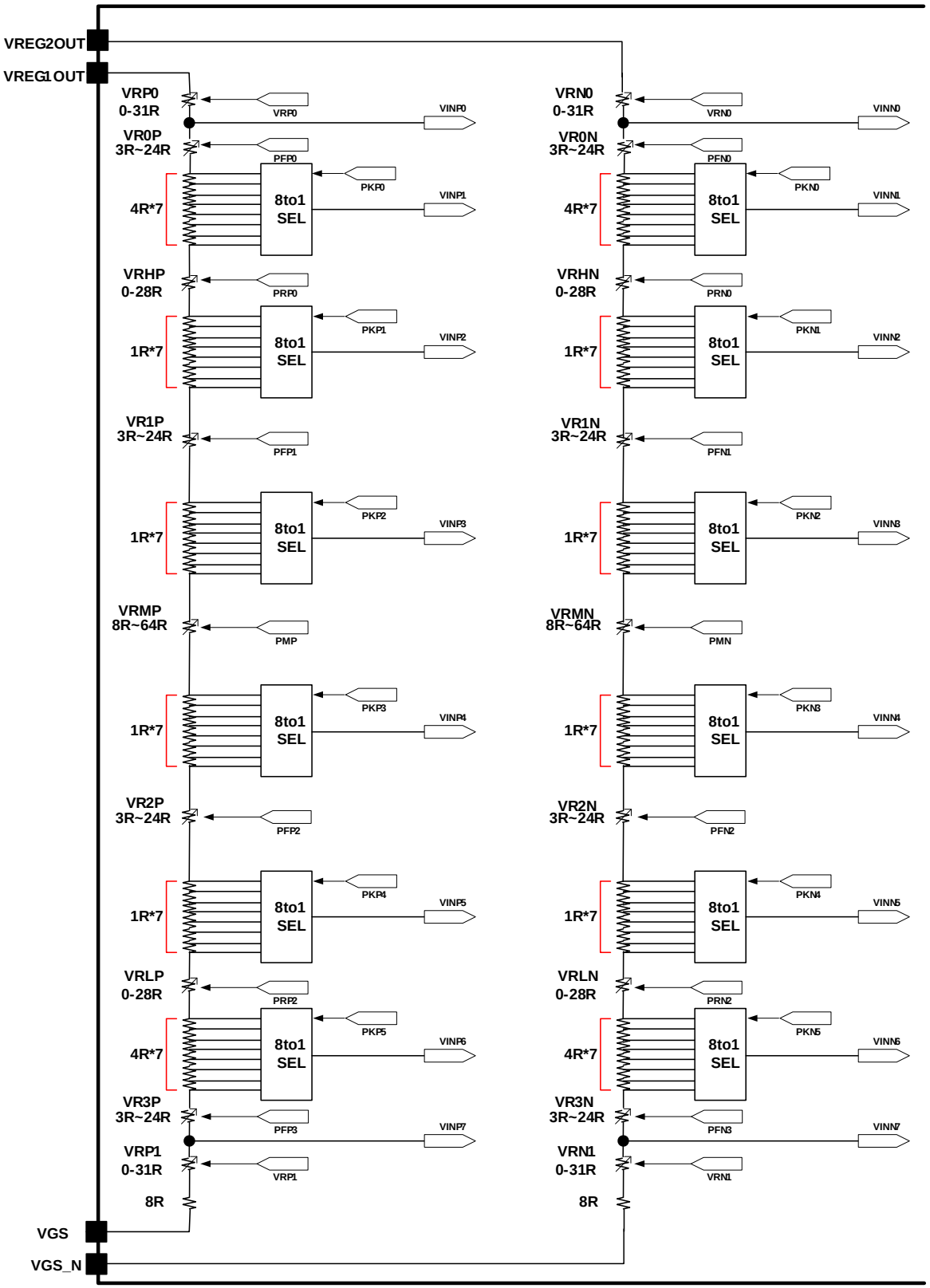


Figure 16. Ladder resistor units and 8-to-1 selectors

5.6.2 Gamma Correction Register

The gamma correction registers of the LG4573 consist of gradient adjustment, amplitude adjustment, and fine adjustment registers, each of which has registers of positive and negative polarities. Each

different register group can be set independently to others, enabling adjustment of grayscale voltage levels in relation to grayscales set optimally for gamma characteristics of a liquid crystal panel. These gamma correction register settings and the reference levels of the 64 grayscales to which the three kinds of adjustments are made (bold lines in the following figure) are common to all RGB dots.

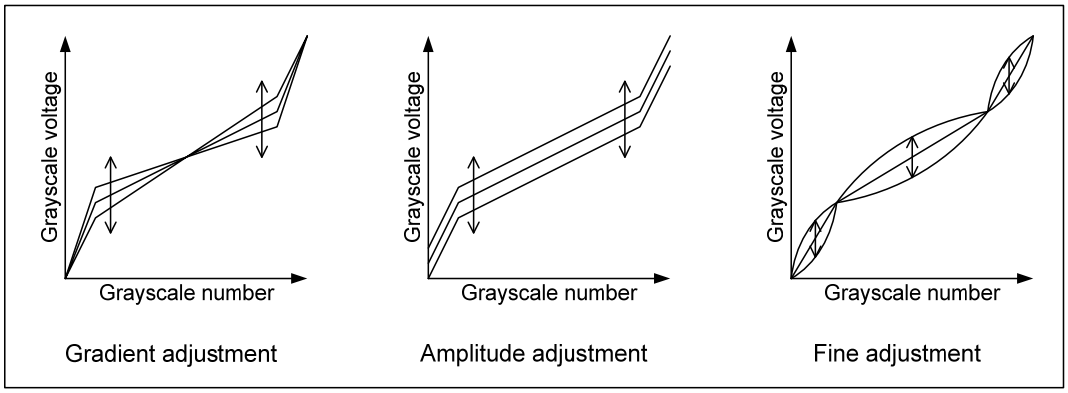


Figure 17

Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale voltage level around middle grayscales without changing the dynamic range. To adjust the gradient, the resistance values of grayscale reference voltage generating variable resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit are adjusted. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of the grayscale voltage generating variable resistors (VRP(N)1/0) at the top and bottom of the ladder resistor unit are adjusted. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor unit, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Table 5. List of registers

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRHP(N)
	PFP0[2:0]	PFN0[2:0]	Variable resistor VR0P(N)
	PFP1[2:0]	PFN1[2:0]	Variable resistor VR1P(N)
	PFP2[2:0]	PFN2[2:0]	Variable resistor VR2P(N)
	PFP3[2:0]	PFN3[2:0]	Variable resistor VR3P(N)
	PMP[2:0]	PMN[2:0]	Variable resistor VRMP(N)
Amplitude adjustment	VRP0[4:0]	VRN0[4:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Fine adjustment	PKP0[2:0]	PKN0[2:0]	8-to-1 selector (voltage level of grayscale 1)
	PKP1[2:0]	PKN1[2:0]	8-to-1 selector (voltage level of grayscale 8)
	PKP2[2:0]	PKN2[2:0]	8-to-1 selector (voltage level of grayscale 20)

	PKP3[2:0]	PKN3[2:0]	8-to-1 selector (voltage level of grayscale 43)
	PKP4[2:0]	PKN4[2:0]	8-to-1 selector (voltage level of grayscale 53)
	PKP5[2:0]	PKN5[2:0]	8-to-1 selector (voltage level of grayscale 62)

5.6.3 Ladder Resistors and 8-to-1 Selector

Block Configuration

The grayscale generation unit as illustrated in Figure 16 consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the gamma correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable Resistors

The LG4573 uses variable resistors of the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)/VR0~4P(N)/VRMP(N)) and amplitude adjustment (VRP(N)0~1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Table 6. Amplitude adjustment

Contents of register VRP(N)0[4:0]	Resistance VRP(N)0 VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 Selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register, and output the selected voltage level as a reference grayscale voltage (VINP(N)1~ VINP(N 6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Table 7. Fine adjustment registers and selected voltage

PKP(N)[2:0]	Selected Voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
3'h0	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
3'h1	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
3'h2	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
3'h3	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
3'h4	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
3'h5	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
3'h6	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
3'h7	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale voltage levels for V0~V63 grayscales are calculated from the following formula.

Table 8. Formula for calculating voltage (1)

Pin	Formula	Fine adjustment register value	Reference voltage
KVP0	VREG1OUT - ΔV x VRP0/SUMRP	-	VINP0
KVP1	VREG1OUT - ΔV x (VRP0+VR0P+0R)/SUMRP	PKP0= 3'h0	VINP1
KVP2	VREG1OUT - ΔV x (VRP0+VR0P+4R)/SUMRP	PKP0= 3'h1	
KVP3	VREG1OUT - ΔV x (VRP0+VR0P+8R)/SUMRP	PKP0= 3'h2	
KVP4	VREG1OUT - ΔV x (VRP0+VR0P+12R)/SUMRP	PKP0= 3'h3	
KVP5	VREG1OUT - ΔV x (VRP0+VR0P+16R)/SUMRP	PKP0= 3'h4	
KVP6	VREG1OUT - ΔV x (VRP0+VR0P+20R)/SUMRP	PKP0= 3'h5	
KVP7	VREG1OUT - ΔV x (VRP0+VR0P+24R)/SUMRP	PKP0= 3'h6	
KVP8	VREG1OUT - ΔV x (VRP0+VR0P+28R)/SUMRP	PKP0= 3'h7	
KVP9	VREG1OUT - ΔV x (VRP0+VR0P+28R+VRHP)/SUMRP	PKP1= 3'h0	VINP2
KVP10	VREG1OUT - ΔV x (VRP0+VR0P+29R+VRHP)/SUMRP	PKP1= 3'h1	
KVP11	VREG1OUT - ΔV x (VRP0+VR0P+30R+VRHP)/SUMRP	PKP1= 3'h2	
KVP12	VREG1OUT - ΔV x (VRP0+VR0P+31R+VRHP)/SUMRP	PKP1= 3'h3	
KVP13	VREG1OUT - ΔV x (VRP0+VR0P+32R+VRHP)/SUMRP	PKP1= 3'h4	
KVP14	VREG1OUT - ΔV x (VRP0+VR0P+33R+VRHP)/SUMRP	PKP1= 3'h5	
KVP15	VREG1OUT - ΔV x (VRP0+VR0P+34R+VRHP)/SUMRP	PKP1= 3'h6	
KVP16	VREG1OUT - ΔV x (VRP0+VR0P+35R+VRHP)/SUMRP	PKP1= 3'h7	
KVP17	VREG1OUT - ΔV x (VRP0+VR0/1P+35R+VRHP)/SUMRP	PKP2= 3'h0	VINP3
KVP18	VREG1OUT - ΔV x (VRP0+VR0/1P+36R+VRHP)/SUMRP	PKP2= 3'h1	
KVP19	VREG1OUT - ΔV x (VRP0+VR0/1P+37R+VRHP)/SUMRP	PKP2= 3'h2	
KVP20	VREG1OUT - ΔV x (VRP0+VR0/1P+38R+VRHP)/SUMRP	PKP2= 3'h3	
KVP21	VREG1OUT - ΔV x (VRP0+VR0/1P+39R+VRHP)/SUMRP	PKP2= 3'h4	
KVP22	VREG1OUT - ΔV x (VRP0+VR0/1P+40R+VRHP)/SUMRP	PKP2= 3'h5	
KVP23	VREG1OUT - ΔV x (VRP0+VR0/1P+41R+VRHP)/SUMRP	PKP2= 3'h6	
KVP24	VREG1OUT - ΔV x (VRP0+VR0/1P+42R+VRHP)/SUMRP	PKP2= 3'h7	
KVP25	VREG1OUT - ΔV x (VRP0+VR0/1P+42R+VRHP +VRMP)/SUMRP	PKP3= 3'h0	VINP4
KVP26	VREG1OUT - ΔV x (VRP0+VR0/1P+43R+VRHP +VRMP)/SUMRP	PKP3= 3'h1	
KVP27	VREG1OUT - ΔV x (VRP0+VR0/1P+44R+VRHP +VRMP)/SUMRP	PKP3= 3'h2	
KVP28	VREG1OUT - ΔV x (VRP0+VR0/1P+45R+VRHP +VRMP)/SUMRP	PKP3= 3'h3	
KVP29	VREG1OUT - ΔV x (VRP0+VR0/1P+46R+VRHP +VRMP)/SUMRP	PKP3= 3'h4	
KVP30	VREG1OUT - ΔV x (VRP0+VR0/1P+47R+VRHP +VRMP)/SUMRP	PKP3= 3'h5	
KVP31	VREG1OUT - ΔV x (VRP0+VR0/1P+48R+VRHP +VRMP)/SUMRP	PKP3= 3'h6	
KVP32	VREG1OUT - ΔV x (VRP0+VR0/1P+49R+VRHP +VRMP)/SUMRP	PKP3= 3'h7	
KVP33	VREG1OUT - ΔV x (VRP0+VR0/1/2P+49R+VRHP +VRMP)/SUMRP	PKP4= 3'h0	VINP5
KVP34	VREG1OUT - ΔV x (VRP0+VR0/1/2P+50R+VRHP +VRMP)/SUMRP	PKP4= 3'h1	
KVP35	VREG1OUT - ΔV x (VRP0+VR0/1/2P+51R+VRHP +VRMP)/SUMRP	PKP4= 3'h2	
KVP36	VREG1OUT - ΔV x (VRP0+VR0/1/2P+52R+VRHP +VRMP)/SUMRP	PKP4= 3'h3	
KVP37	VREG1OUT - ΔV x (VRP0+VR0/1/2P+53R+VRHP +VRMP)/SUMRP	PKP4= 3'h4	
KVP38	VREG1OUT - ΔV x (VRP0+VR0/1/2P+54+VRHP +VRMP)/SUMRP	PKP4= 3'h5	
KVP39	VREG1OUT - ΔV x (VRP0+VR0/1/2P+55R+VRHP +VRMP)/SUMRP	PKP4= 3'h6	
KVP40	VREG1OUT - ΔV x (VRP0+VR0/1/2P+56R+VRHP +VRMP)/SUMRP	PKP4= 3'h7	

Pin	Formula	Fine adjustment register value	Reference voltage
KVP41	VREG1OUT - ΔV x (VRP0+VR0/1/2P+56R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h0	VINP6
KVP42	VREG1OUT - ΔV x (VRP0+VR0/1/2P+60R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h1	
KVP43	VREG1OUT - ΔV x (VRP0+VR0/1/2P+64R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h2	
KVP44	VREG1OUT - ΔV x (VRP0+VR0/1/2P+68R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h3	
KVP45	VREG1OUT - ΔV x (VRP0+VR0/1/2P+72R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h4	
KVP46	VREG1OUT - ΔV x (VRP0+VR0/1/2P+76R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h5	
KVP47	VREG1OUT - ΔV x (VRP0+VR0/1/2P+80R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h6	
KVP48	VREG1OUT - ΔV x (VRP0+VR0/1/2P+84R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h7	
KVP49	VREG1OUT - ΔV x (VRP0+VR0/1/2/3P+84R+VRHP+VRMP +VRLP)/SUMRP	-	VINP7

SUMRP: Sum of positive ladder resistors =
92R+VRHP+VRLP+VRP0+VRP1+VR0P+VR1P+VR2P+VR3P+VRMP
ΔV: Difference in electrical potential between VREG1OUT and VGS

Table 9. Formula for calculating voltage (2)

Grayscale voltage	Formula
V0	VINP0
V1	VINP1
V2	VINP2+(VINP1-VINP2) x (30/48)
V3	VINP2+(VINP1-VINP2) x (23/48)
V4	VINP2+(VINP1-VINP2) x (16/48)
V5	VINP2+(VINP1-VINP2) x (12/48)
V6	VINP2+(VINP1-VINP2) x (8/48)
V7	VINP2+(VINP1-VINP2) x (4/48)
V8	VINP2
V9	VINP3+(VINP2-VINP3) x (22/24)
V10	VINP3+(VINP2-VINP3) x (20/24)
V11	VINP3+(VINP2-VINP3) x (18/24)
V12	VINP3+(VINP2-VINP3) x (16/24)
V13	VINP3+(VINP2-VINP3) x (14/24)
V14	VINP3+(VINP2-VINP3) x (12/24)
V15	VINP3+(VINP2-VINP3) x (10/24)
V16	VINP3+(VINP2-VINP3) x (8/24)
V17	VINP3+(VINP2-VINP3) x (6/24)
V18	VINP3+(VINP2-VINP3) x (4/24)
V19	VINP3+(VINP2-VINP3) x (2/24)
V20	VINP3
V21	VINP4+(VINP3-VINP4) x (22/23)
V22	VINP4+(VINP3-VINP4) x (21/23)
V23	VINP4+(VINP3-VINP4) x (20/23)
V24	VINP4+(VINP3-VINP4) x (19/23)
V25	VINP4+(VINP3-VINP4) x (18/23)
V26	VINP4+(VINP3-VINP4) x (17/23)
V27	VINP4+(VINP3-VINP4) x (16/23)
V28	VINP4+(VINP3-VINP4) x (15/23)
V29	VINP4+(VINP3-VINP4) x (14/23)
V30	VINP4+(VINP3-VINP4) x (13/23)
V31	VINP4+(VINP3-VINP4) x (12/23)
V32	VINP4+(VINP3-VINP4) x (11/23)
V33	VINP4+(VINP3-VINP4) x (10/23)
V34	VINP4+(VINP3-VINP4) x (9/23)
V35	VINP4+(VINP3-VINP4) x (8/23)
V36	VINP4+(VINP3-VINP4) x (7/23)
V37	VINP4+(VINP3-VINP4) x (6/23)
V38	VINP4+(VINP3-VINP4) x (5/23)
V39	VINP4+(VINP3-VINP4) x (4/23)
V40	VINP4+(VINP3-VINP4) x (3/23)
V41	VINP4+(VINP3-VINP4) x (2/23)
V42	VINP4+(VINP3-VINP4) x (1/23)
V43	VINP4
V44	VINP5+(VINP4-VINP5) x (22/24)

Grayscale voltage	Formula
V45	VINP5+(VINP4-VINP5) x (20/24)
V46	VINP5+(VINP4-VINP5) x (18/24)
V47	VINP5+(VINP4-VINP5) x (16/24)
V48	VINP5+(VINP4-VINP5) x (14/24)
V49	VINP5+(VINP4-VINP5) x (12/24)
V50	VINP5+(VINP4-VINP5) x (10/24)
V51	VINP5+(VINP4-VINP5) x (8/24)
V52	VINP5+(VINP4-VINP5) x (6/24)
V53	VINP5+(VINP4-VINP5) x (4/24)
V54	VINP5+(VINP4-VINP5) x (2/24)
V55	VINP5
V56	VINP6+(VINP5-VINP6) x (44/48)
V57	VINP6+(VINP5-VINP6) x (40/48)
V58	VINP6+(VINP5-VINP6) x (36/48)
V59	VINP6+(VINP5-VINP6) x (32/48)
V60	VINP6+(VINP5-VINP6) x (25/48)
V61	VINP6+(VINP5-VINP6) x (18/48)
V62	VINP6
V63	VINP7

Notes:

1. Make sure DDVDH-V0 > 0.5V
2. Based on the generated 64 gray levels above, interpolated 4 levels are newly generated. Eventually total 253 gray levels are generated to acquire 16.2M color depth.

5.7 Oscillator

LG4573 could generate RC oscillation with an internal oscillation resistor for power boosting circuit, like as step-up and step-down.

5.8 OTP Control

LG4573 has an embedded OTP which is a 32-bit one-time programmable (OTP) IP from eMemory Technology Inc. (EO01X32KCV6).

EO01X32KCV6 is a CMOS, 1bit (1-bit) program OTP logic device. The main memory block is organized as 8-bits by 4 banks. See the data sheet of EO01X32KCV6.

The pins of the embedded OTP can be controlled using the OTP control 1 (C4h) register as shown below.

Table 10.

EO01X32KCV6	Bit fields of register C4h
PTM = 0V/1.8V	PTM[1:0] = 00/11
POR = 0V/1.8V	POR = 0/1
VPP = 1.8V/7.5V	VPP = 0/1
PPROG = 0V/1.8V	PPROG = 0/1
PWE = 0V/1.8V	PWE = 0/1
PA[1:0] = 0V/1.8V	PA[1:0] = 0/1
PDIN[7:0] = 0V/1.8V	PDIN[7:0] = 0/1

The RA[1:0] of register F9h selects one of four OTP bytes.

Accessing OTP control registers, follow the timing requirements of read and program cycles.

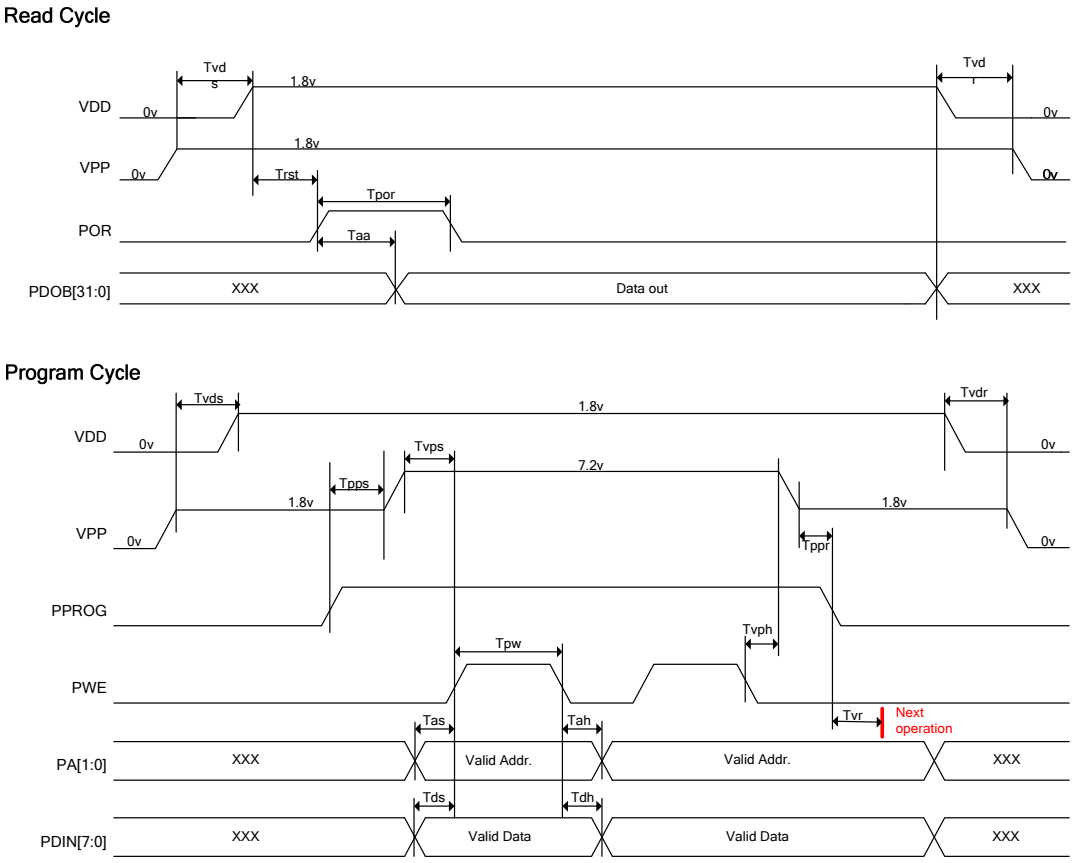


Figure 18. OTP Timing

Table 11.

Parameter	Symbol	EO01X32KCV6	Unit

		Min	Max	
Rising Time / Falling Time	Tr / Tf	-	1	ns
Data Access Time	Taa	-	70	ns
Power-on Pulse Width Time	Tpor	200	-	ns
Address / Data Setup Time	Tas / Tds	4	-	ns
Address / Data Hold Time	Tah / Tdh	9	-	ns
External VPP Setup Time	Tvps	0	-	ns
External VPP Hold Time	Tvph	0	-	ns
Program Recovery Time	Tvr	10	-	μs
Program Pulse Width	Tpw	300	350	μs
VDD Setup Time	Tvds	0	-	ms
VDD Recovery Time	Tvdr	0	-	ms
PPROG Setup Time	Tpps	10	-	ns
PPROG Recovery Time	Tppr	10	-	ns
Power on Read Time	Trst	20	-	ns

Notes:

1. All program signals that align together in the timing diagrams should be derived from the rising clock edge.
2. All timing measurements are from the 50% of the input to 50% of the output.
3. All input waveforms have rising time (tr) and falling time (tf) of 1ns from 10% to 90% of the input waveforms.
4. For capacitive loads greater than 1pF, access time will increase by 1ns per pF of additional loading.
5. Program time means one byte program time in user mode

The following sequences are for writing and reading data into and/or from OTP.

OTP Write Sequence

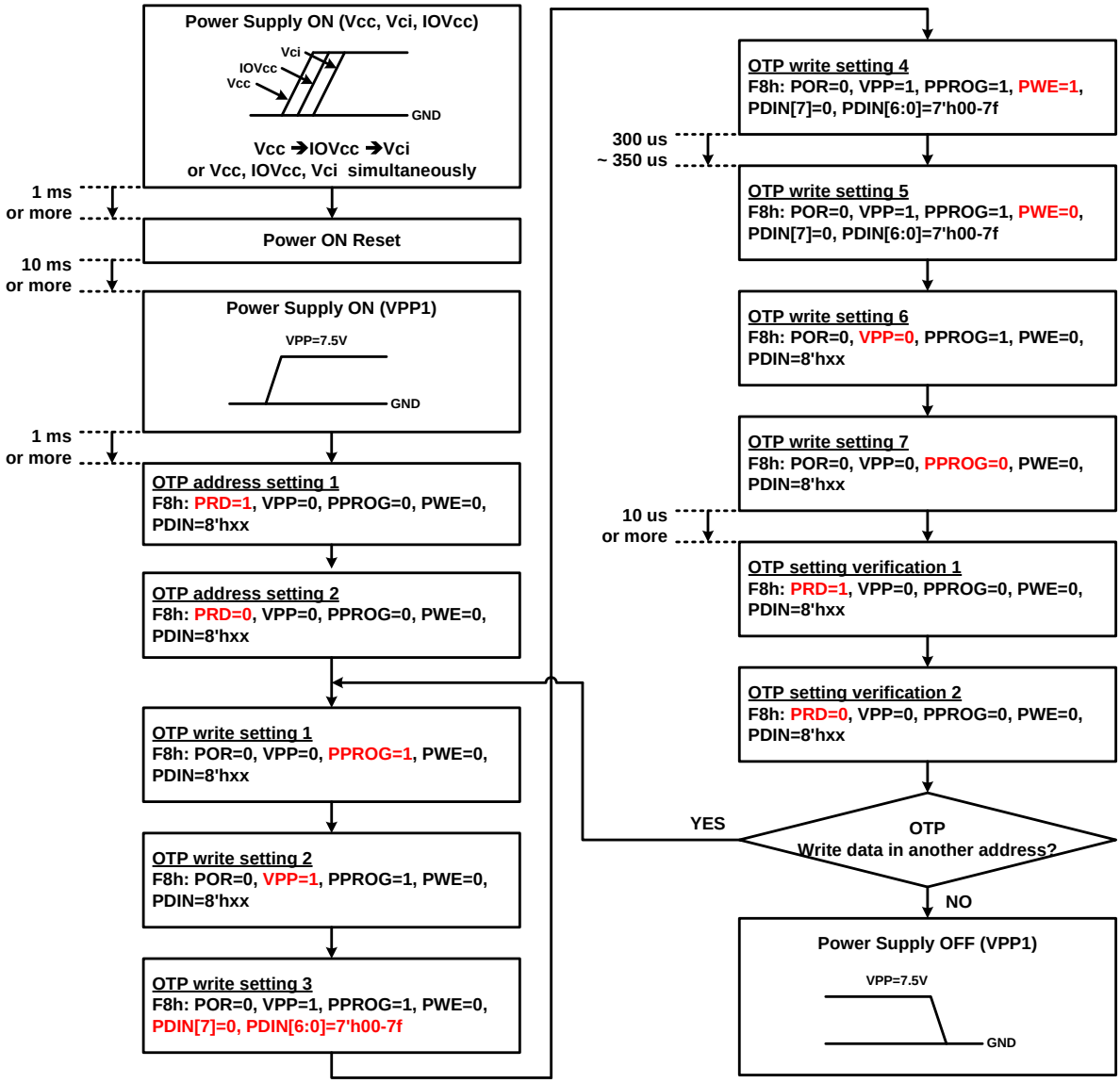


Figure 19. OTP Write Sequence

OTP Read Sequence

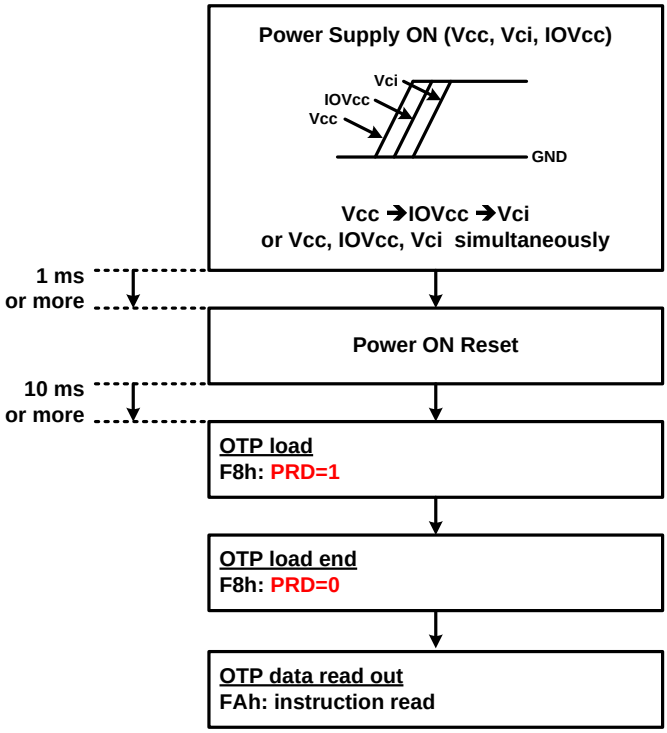


Figure 20. OTP Write Sequence

6 Commands

6.1 Command List

User Command Set

Name	Addr	Size	D/nC	b7	b6	b5	b4	b3	b2	b1	b0	Default
NOP	00h	0										
SWRESET	01h	0		SWRST = 1 (self cleared after a fixed delay)								0
RDDPM	0Ah	1		0	IDM	0	nSLP	1	DISP	0	0	
RDDMADCTL	0Bh	1		0	0	0	0	BGR	0	FH	FV	
RDDCOLMOD	0Ch	1		0	DPIPF[2:0]			0	0	0	0	
RDDIM	0Dh	1		0	0	INV	0	0	0	0	0	
SLPIN	10h	0		nSLP = 0								0
SLPOUT	11h	0		nSLP = 1								
INVOFF	20h	0		INV = 0								0
INVON	21h	0		INV = 1								
DISPOFF	28h	0		DISP = 0								0
DISPON	29h	0		DISP = 1								
~~TEOFF~~	~~34h~~	~~0~~	~~0~~									
~~TEON~~	~~35h~~	~~1~~	~~0~~									
			~~1~~								~~M~~	
MADCTL	36h	1						BGR		FH	FV	00h
~~IDMOFF~~	~~38h~~	~~0~~		~~IDM = 0~~								
~~IDMON~~	~~39h~~	~~0~~		~~IDM = 1~~								
COLMOD	3Ah	1			DPIPF[2:0]							70h
~~TESCAN~~	~~44h~~	~~3~~	~~0~~									
			~~1~~							~~N[9:8]~~		~~00h~~
			~~1~~	~~N[7:0]~~								~~00h~~
			~~1~~	~~TEPW[7:0]~~								~~00h~~
WRDISBV	51h	1	1	DBV[7:0]								00h
RDDISBV	52h	1	1	DBV[7:0]								00h
WRCTRLD	53h	1	1			BCTRL		DD	BL			00h
RDCTRLD	54h	1	1			BCTRL		DD	BL			00h
WRCABC	55h	1	1							CABC[1:0]		00h
RDCABC	56h	1	1							CABC[1:0]		00h
WRCABCMB	5Eh	1	1	CMB[7:0]								00h
RDCABCMB	5Fh	1	1	CMB[7:0]								00h
RDDDB	A1h	52	1	DDB[7:0]								xxh
RDDDBC	A8h	52	1	DDBC[7:0]								xxh

Manufacturer Command Set

Name	Addr	Size	D/nC	b7	b6	b5	b4	b3	b2	b1	b0	Default
RGBIF	B1h	3	0									
			1				SYNC	CKPL	HSPL	VSPL	DEPL	06h
			1		HBP[6:0]							1Eh
			1	VBP[7:0]								0Ch
PANELSET	B2h	2	0									
			1			LR	SELP		HRS[1:0]		REV	11h
			1	VRS[7:0]								D8h
PANELDRV	B3h	1	0									
			1							DINV		02h
DISPMODE	B4h	1	0									
			1						DITH			04h
DISPCTL1	B5h	5	0									
			1	SDT[7:0]								10h
			1		~~SHPN[6:0]~~							10h
			1		~~ENGND[6:0]~~							10h
			1	~~SHIZ[7:0]~~								00h
			1								~~SLT~~	00h
DISPCTL2	B6h	6	0									
			1						ASG	SDM	FHN	01h
			1	CLW[7:0]								18h
			1			GTO[5:0]						02h
			1	GNO[7:0]								40h
			1	FTI[7:0]								10h
			1	GPM[7:0]								00h
OSCSET	C0h	2	0									
			1								OSC	00h
			1				FRS[4:0]					00h
PWRCTL1	C1h	1	0									
			1					DTE		STB	DSTB	02h
PWRCTL2	C2h	1	0									
			1			LVGL	VDL	VCL	VGL	VGH	VDH	00h
PWRCTL3	C3h	5	0									
			1						STMODE[2:0]			00h
			1						DC1[2:0]			04h
			1						DC2[2:0]			03h
			1						DC3[2:0]			03h
			1						DCPFM[2:0]			03h
PWRCTL4	C4h	6	0									
			1			OPB	BMB		BDC[2:0]			00h
			1		GDC[2:0]				AP[2:0]			00h
			1				VRH1[4:0]					00h
			1				VRH2[4:0]					00h
			1			SELOPA	REGPD		BT[2:0]			05h
			1		VBS[2:0]			VREFS[3:0]				0Bh
PWRCTL5	C5h	1	0									
			1		VCM[6:0]							00h
PWRCTL6	C6h	3	0									
			1		RI[2:0]				RV[2:0]			23h
			1		RSET[2:0]				RCONT[2:0]			50h
			1							SBC	GBC	00h
~~OFCCTL~~	~~C7h~~	~~3~~	~~0~~									
			~~1~~								~~OFCEN~~	~~00h~~
			~~1~~	~~OFCTSW[7:0]~~								~~B0h~~
			~~1~~	~~OFCTD2[3:0]~~				~~OFCTD1[3:0]~~				~~40h~~
BLCTL	C8h	2	0									
			1	CDSP[3:0]				CDMP[3:0]				82h
			1	PWMP						FPWM[1:0]		01h

RGAMMAP	D0h	9	0									
			1		PKP1[2:0]				PKP0[2:0]			00h
			1		PKP3[2:0]				PKP2[2:0]			00h
			1		PKP5[2:0]				PKP4[2:0]			00h
			1		PRP1[2:0]				PRP0[2:0]			00h
			1				VRP0[4:0]					00h
			1				VRP1[4:0]					00h
			1		PFP1[2:0]				PFP0[2:0]			00h
			1		PFP3[2:0]				PFP2[2:0]			00h
			1						PMP[2:0]			00h
RGAMMAN	D1h	9	0									
			1		PKN1[2:0]				PKN0[2:0]			00h
			1		PKN3[2:0]				PKN2[2:0]			00h
			1		PKN5[2:0]				PKN4[2:0]			00h
			1		PRN1[2:0]				PRN0[2:0]			00h
			1				VRN0[4:0]					00h
			1				VRN1[4:0]					00h
			1		PFN1[2:0]				PFN0[2:0]			00h
			1		PFN3[2:0]				PFN2[2:0]			00h
			1						PMN[2:0]			00h
GGAMMAP	D2h	9	0									
			1		PKP1[2:0]				PKP0[2:0]			00h
			1		PKP3[2:0]				PKP2[2:0]			00h
			1		PKP5[2:0]				PKP4[2:0]			00h
			1		PRP1[2:0]				PRP0[2:0]			00h
			1				VRP0[4:0]					00h
			1				VRP1[4:0]					00h
			1		PFP1[2:0]				PFP0[2:0]			00h
			1		PFP3[2:0]				PFP2[2:0]			00h
			1						PMP[2:0]			00h
GGAMMAN	D3h	9	0									
			1		PKN1[2:0]				PKN0[2:0]			00h
			1		PKN3[2:0]				PKN2[2:0]			00h
			1		PKN5[2:0]				PKN4[2:0]			00h
			1		PRN1[2:0]				PRN0[2:0]			00h
			1				VRN0[4:0]					00h
			1				VRN1[4:0]					00h
			1		PFN1[2:0]				PFN0[2:0]			00h
			1		PFN3[2:0]				PFN2[2:0]			00h
			1						PMN[2:0]			00h
BGAMMAN	D4h	9	0									
			1		PKP1[2:0]				PKP0[2:0]			00h
			1		PKP3[2:0]				PKP2[2:0]			00h
			1		PKP5[2:0]				PKP4[2:0]			00h
			1		PRP1[2:0]				PRP0[2:0]			00h
			1				VRP0[4:0]					00h
			1				VRP1[4:0]					00h
			1		PFP1[2:0]				PFP0[2:0]			00h
			1		PFP3[2:0]				PFP2[2:0]			00h
			1						PMP[2:0]			00h
BGAMMAN	D5h	9	0									
			1		PKN1[2:0]				PKN0[2:0]			00h
			1		PKN3[2:0]				PKN2[2:0]			00h
			1		PKN5[2:0]				PKN4[2:0]			00h
			1		PRN1[2:0]				PRN0[2:0]			00h
			1				VRN0[4:0]					00h
			1				VRN1[4:0]					00h
			1		PFN1[2:0]				PFN0[2:0]			00h
			1		PFN3[2:0]				PFN2[2:0]			00h
			1						PMN[2:0]			00h
TEST1	F0h	1	0									
			1	HIZ						TPOL[1:0]		00h

OTP1	F8h	3	0									
			1	PTM[1:0]				PRD	PWE	VPP	PPROG	00h
			1	APRG						PA[1:0]		00h
			1	PDIN[7:0]								00h
OTP2	F9h	1	0									
			1	VCMSEL[1:0]						RA[1:0]		00h
OTP3	FAh	4	0									
			1	PDOUT[7:0]								xxh
			1	PDOUT[15:8]								xxh
			1	PDOUT[23:16]								xxh
			1	PDOUT[31:24]								xxh

6.2 Command Description

6.2.1 00h – No Operation

Mnemonic NOP

Type Command

Parameters None

Description

This command is an empty command; it does not have any effect on the display module.

6.2.2 01h – Software Reset

Mnemonic SWRESET

Type Command

Parameters None

Description

When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their default values.

The display becomes to be blank or white immediately, which depends on the panel type.

Restrictions

It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier's factory default values to the registers during this time.

If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command.

Software Reset Command cannot be sent during Sleep Out sequence.

6.2.3 0Ah – Read Display Power Mode

Mnemonic RDDPM

Type Read

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	IDM	-	nSLP	-	DISP	-	-	00h

Description

This command indicates the current status of the display as described below:

IDM - Idle Mode On/Off
0 = Idle Mode Off.
1 = Idle Mode On.

nSLP – Sleep In/Out
0 = Sleep In Mode.
1 = Sleep Out Mode.

DISP – Display On/Off
0 = Display is Off.
1 = Display is On.

6.2.4 0Bh – Read Display MADCTL

Mnemonic RDDMADCTL

Type Read

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	-	-	BGR	-	FH	FV	00h

Description

This command indicates the current status of the display as described below:

BGR – RGB/BGR Order
0 = RGB (When MADCTL.BGR = 0).
1 = BGR (When MADCTL.BGR = 1).

FH – Switching Between Segment Outputs and Host Processor
This bit is not applicable for this project, so it is set to 0.

FV – Switching Between Common Outputs and Host Processor
This bit is not applicable for this project, so it is set to 0.

6.2.5 0Ch – Read Display Pixel Format

Mnemonic RDDCOLMOD

Type Read

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	DPIPF[2:0]			-	-			70h

Description

This command indicates the current status of the display as described below:

DPIPF[2:0] – DPI Pixel Format Definition

The pixel formats are shown below:

DPIPF[2:0]	Pixel Format
101	16 bits/pixel
110	18 bits/pixel
111	24 bits/pixel
Others	Not defined

6.2.6 0Dh – Read Display Image Mode

Mnemonic RDDIM

Type Read

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	INV	-	-	-	-	-	00h

Description

This command indicates the current status of the display as described below:

INV – Inversion On/Off
0 = Inversion Off.
1 = Inversion On.

6.2.7 10h – Sleep In

Mnemonic SLPIN

Type Command

Parameters None

Default Sleep In Mode

Description

This command causes the display module to enter the minimum power consumption mode.

In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.

Host interface is still working.

Backlights, display and keyboard, are off.

Dimming function does not work when there is changing mode from Sleep Out to Sleep In.

Restrictions

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).

It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.

It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

6.2.8 11h – Sleep Out

Mnemonic SLPOUT

Type Command

Parameters None

Default Sleep In Mode

Description

This command turns off sleep mode.

In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.

~~See also section 8.6.2.~~

Restrictions

This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h), SW Reset Command (01h) or HW Reset.

It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this time and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out mode.

The display module is doing self-diagnostic functions during this 5msec.

It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.

6.2.9 13h – Normal Display Mode On

Mnemonic NORON

Type Command

Parameters None

Default Normal Display Mode On

Description

This command returns the display to normal mode.

Restrictions

This command has no effect when Normal Display mode is active.

6.2.10 20h – Display Inversion Off

Mnemonic INVOFF

Type Command

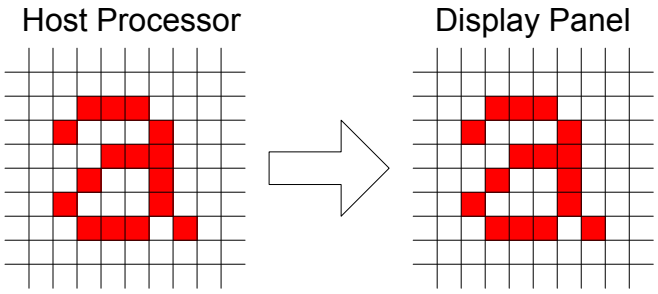
Parameters None

Default Display Inversion Off

Description

This command is used to recover from display inversion mode.

This command does not change any other status.



6.2.11 21h – Display Inversion On

Mnemonic INVOFF

Type Command

Parameters None

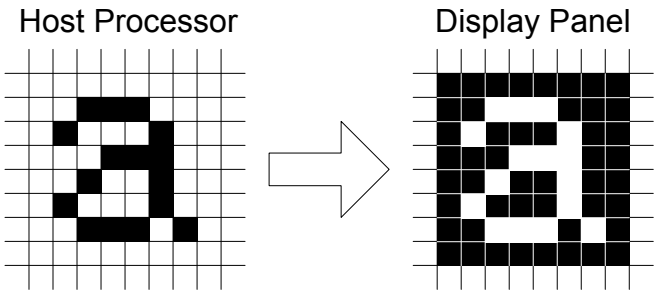
Default Display Inversion Off

Description

This command is used to enter into display inversion mode.

Every bit is inverted from the Host Processor to the display.

This command does not change any other status.



6.2.12 28h – Display Off

Mnemonic DISPOFF

Type Command

Parameters None

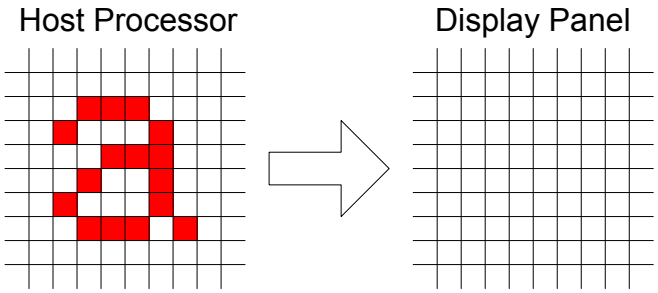
Default Display Off

Description

This command is used to enter into Display Off mode. In this mode, the normal white or normal black image is displayed, which depends on the panel type.

This command does not change any other status.

There will be no abnormal visible effect on the display.



Restrictions

This command has no effect when module is already in display off mode.

6.2.13 29h – Display On

Mnemonic DISPON

Type Command

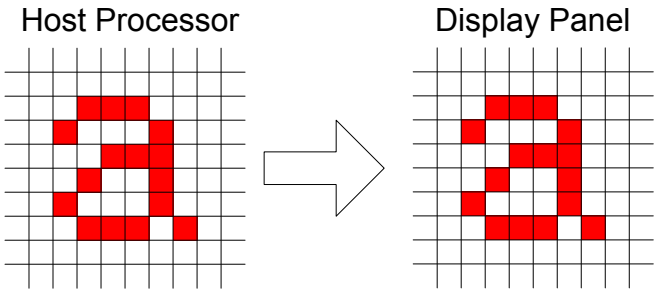
Parameters None

Default Display Off

Description

This command is used to recover from Display Off mode.

This command does not change any other status.



Restrictions

This command has no effect when module is already in display on mode.

6.2.14 36h – Set Address Mode

Mnemonic MADCTL

Type Write

Parameters

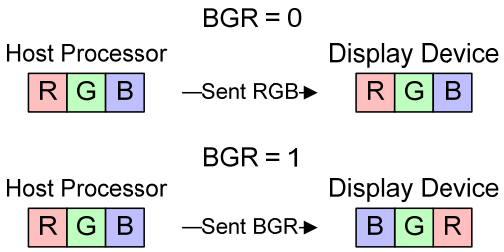
No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	-	-	BGR	-	FH	FV	00h

Description

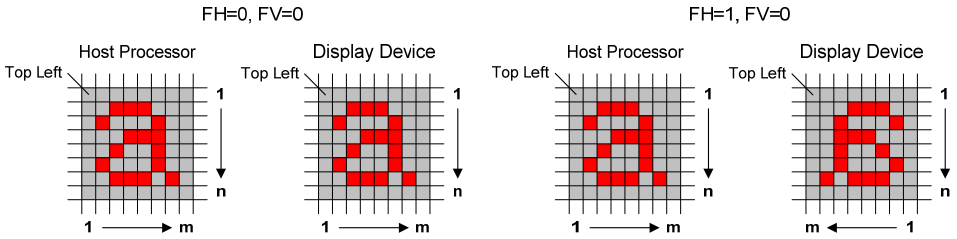
This command defines write scanning direction from the host processor.

This command makes no change on the other driver status.

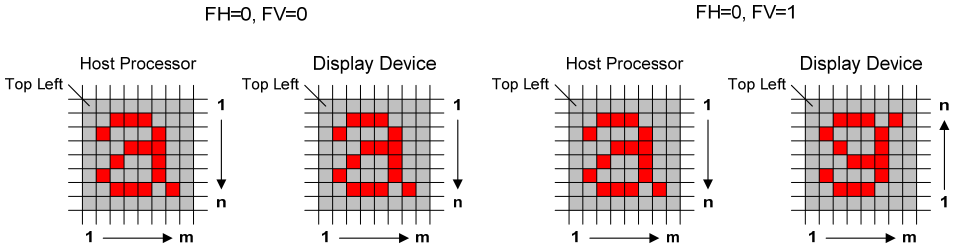
BGR – RGB/BGR Order
0 = Pixels sent in RGB order
1 = Pixels sent in BGR order



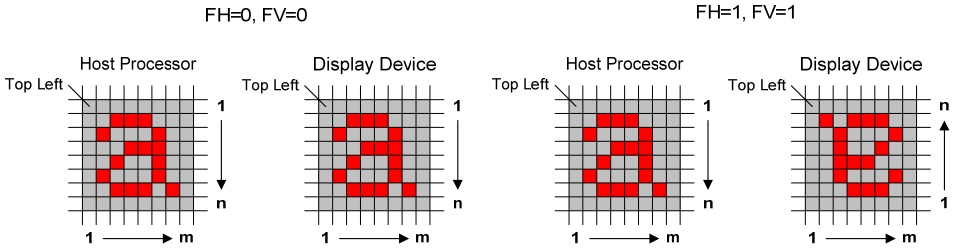
FH – Flip Horizontal
0 = Normal
1 = Flipped



FV – Flip Vertical (Note: For this function, the panel should support bi-directional scanning.)
0 = Normal
1 = Flipped



The remaining flip combination of FH=1 with FV=1 is as follows. For this function, the panel should support bi-directional scanning.



6.2.15 3Ah – Interface Pixel Format

Mnemonic COLMOD

Type Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	DPIPF[2:0]			-	-			70h

Description

This command is used to define the format of RGB picture data, which is to be transferred via the Host interface. The formats are shown below:

DPIPF[2:0] – DPI Pixel Format Definition

The pixel formats are shown below:

DPIPF[2:0]	Pixel Format
101	16 bits/pixel
110	18 bits/pixel
111	24 bits/pixel
Others	Not defined

6.2.16 51h – Write Display Brightness

Mnemonic WRDISBV

Type Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	DBV[7:0]								00h

Description

This command is used to adjust the brightness value of the display.

It should be checked what is the relationship between this written value and output brightness of the display. ~~This relationship is defined on the display module specification.~~

In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

6.2.17 52h – Read Display Brightness Value

Mnemonic RDDISBV

Type Read

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	DBV[7:0]								00h

Description

This command returns the brightness value of the display.

It should be checked what the relationship between this returned value and output brightness of the display. ~~This relationship is defined on the display module specification.~~

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

6.2.18 53h – Write Control Display

Mnemonic WRCTRLD

Type Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	BCTRL	-	DD	BL	-	-	00h

Description

This command is used to control ambient light, brightness and gamma settings.

BCTRL – Brightness Control Block On/Off
This bit is always used to switch brightness for display.
0 = Off (Brightness registers are 00h, DBV[7:0])
1 = On (Brightness registers are active, according to the other parameters.)

DD – Display Dimming
0 = Display Dimming is off
1 = Display Dimming is on

BL – Backlight On/Off
0 = Off (Completely turn off backlight circuit. Control lines must be low.)
1 = On

6.2.19 54h – Read Display Brightness Value

Mnemonic RDCTRLD

Type Read

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	BCTRL	-	DD	BL	-	-	00h

Description

This command returns brightness control values.

BCTRL – Brightness Control Block On/Off
This bit is always used to switch brightness for display.
0 = Off (Brightness registers are 00h, DBV[7:0])
1 = On (Brightness registers are active, according to the other parameters.)

DD – Display Dimming
0 = Display Dimming is off
1 = Display Dimming is on

BL – Backlight On/Off
0 = Off (Completely turn off backlight circuit. Control lines must be low.)
1 = On

6.2.20 55h – Write Content Adaptive Brightness Control

Mnemonic WRCABC

Type Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	-	-	-	-	CABC[1:0]		00h

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

CABC[1:0] – CABC mode
00 = Off
01 = User Interface Image
10 = Still Picture
11 = Moving Image

6.2.21 56h – Read Content Adaptive Brightness Control

Mnemonic WRCABC

Type Read

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	-	-	-	-	CABC[1:0]		00h

Description

This command is used to read the settings for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

CABC[1:0] – CABC mode
00 = Off
01 = User Interface Image
10 = Still Picture
11 = Moving Image

6.2.22 5Eh – Write CABC Minimum Brightness

Mnemonic WRCABCMB

Type Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	CMB[7:0]								00h

Description

This command is used to set the minimum brightness value of the display for CABC function.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

6.2.23 5Fh – Read CABC Minimum Brightness

Mnemonic RDCABCMB

Type Read

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	CMB[7:0]								00h

Description

This command returns the minimum brightness value of CABC function.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

6.2.24 A1h – Read DDB Start

Mnemonic RDDDB

Type Read

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	DDB[7:0] : Revision								10h
2	DDB[7:0] : Level								01h
3	DDB[7:0] : Not used								00h
4	DDB[7:0] : Not used								00h
5	DDB[7:0] : Manufacture ID (MSB)								01h
6	DDB[7:0] : Manufacture ID (LSB)								2Ah
7	DDB[7:0] : Device Code (MSB)								45h
8	DDB[7:0] : Device Code (LSB)								73h
9	DDB[7:0] : Length of DDB Level 2 Data (MSB)								00h
10	DDB[7:0] : Length of DDB Level 2 Data (LSB)								2Ah
…	…								…

Description

This command returns the DDB (Device Descriptor Block) values. For further DDB values in level 2 (larger number than 10) are not described here in detail.

6.2.25 B1h – RGB Interface Setting

Mnemonic RGBIF

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	-	SYNC	CKPL	HSPL	VSPL	DEPL	06h
2	-	HBP[6:0]							1Eh
3	VBP[7:0]								0Ch

Description

This command is used to set registers related with RGB (MIPI DPI) interface.

SYNC – Sync mode
0 = VSYNC+HSYNC+DE
1 = VSYNC+HSYNC
If SYNC is 1, the DE pin is ignored and a corresponding signal is internally generated using the registers HBP and VBP.

CKPL – PCLK pin polarity
0 = Rising edge
1 = Falling edge

HSPL – HSYNC pin polarity
0 = Active high
1 = Active low

VSPL – VSYNC pin polarity
0 = Active high
1 = Active low

DEPL – DE pin polarity
0 = Active high
1 = Active low

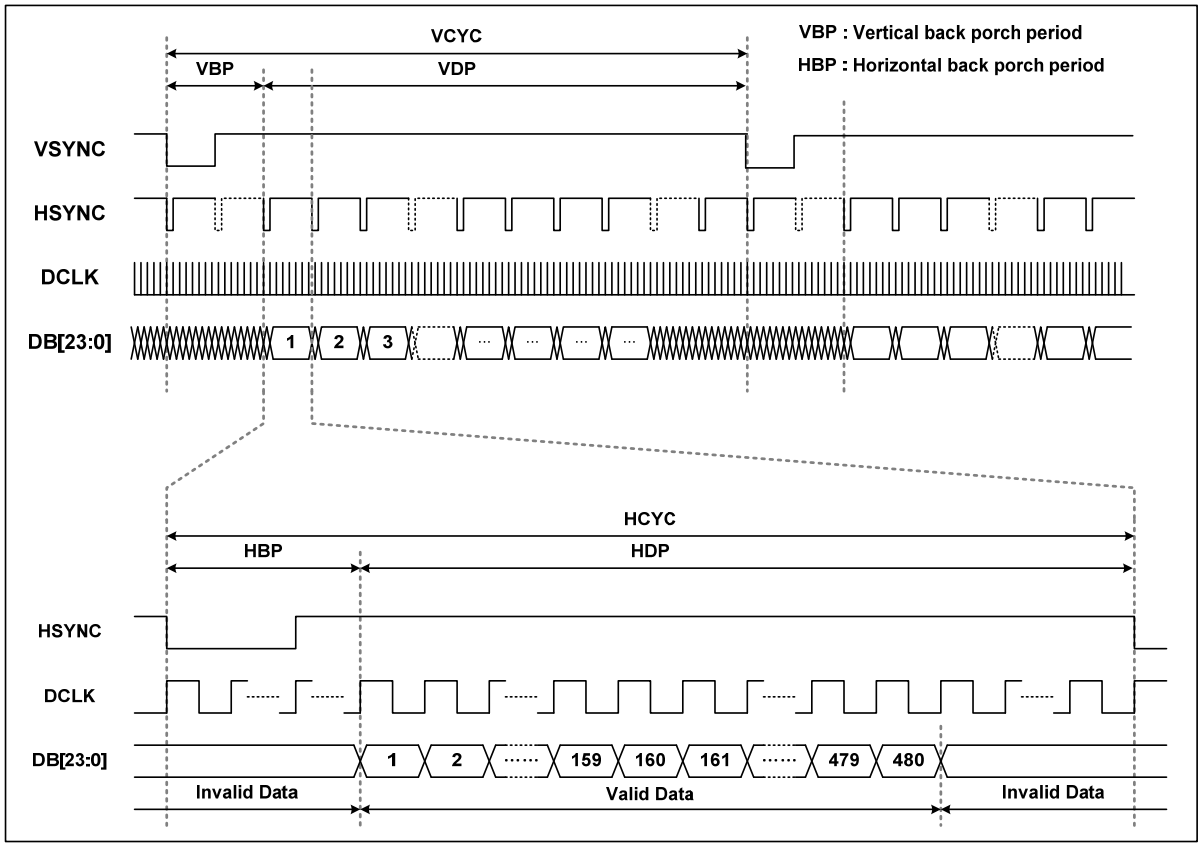
HBP[6:0] – Horizontal backporch in PCLKs

Used only if RGBIF.SYNC = 1 and the relationship of HBP > SDT should always be guaranteed for both DE and SYNC modes.

If HBP[6:0] is 32, then HBP is 32XPLK.

VBP[7:0] – Vertical backporch in lines
Used only if RGBIF.SYNC = 1.

If VBP[6:0] is 32, then VBP is 32x(Line Time).



Restrictions

This command has no effect if RGB interface is not used.

6.2.26 B2h – Panel Characteristics Setting

Mnemonic PANELSET

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	LR	SELP	-	HRS[1:0]		REV	11h
2	VRS[7:0]								D8h

Description

LR – Swap left/right GIP signals
0 = No swap
1 = Swap

SELP – Panel select
0 = L-Typepanel
1 = H-Type panel

HRS[1:0] – Horizontal resolution in pixels
00 = 480 (Valid source outputs = S1 ~ S1440)
01 = 360 (Valid source outputs = S181 ~ S1260)
10 = 320 (Valid source outputs = S241 ~ S1200)
11 = 240 (Valid source outputs = S361 ~ S1080)

REV – Panel type
0 = Normally black panel
1 = Normally white panel

VRS[7:0] – Vertical resolution in lines divided by 4
For example, if VRS is C8h (200 in decimal), vertical resolution is 800.

VRS[7:0]	Supportable Row Resolution
0	1024
1	4
2	8
3	12
…	…
255	1020

6.2.27 B3h – Panel Drive Setting

Mnemonic PANELDRV

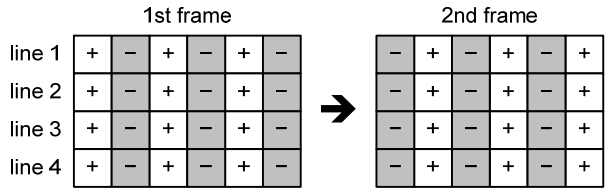
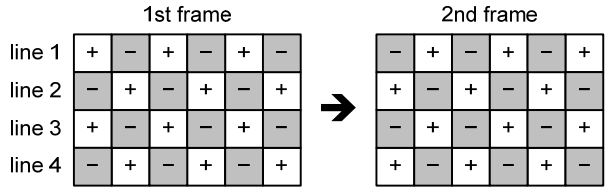
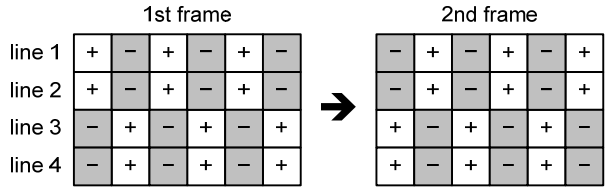
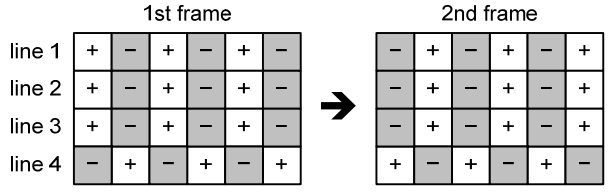
Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	-	-	-	-	DINV[1:0]		02h

Description

DINV[1:0] – Dot inversion mode

DINV[1:0]	Mode	Description
00	Column inversion	
01	1-dot inversion	
10	2-dot inversion	
11	3-dot inversion	

6.2.28 B4h – Display Mode Control

Mnemonic PANELSET

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	-	-	-	DITH	-	-	04h

Description

DITH – Dither block enable
0 = Disable
1 = Enable

6.2.29 B5h – Display Control 1

Mnemonic DISPCTL1

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	SDT[7:0]								10h
2	-	~~SHPN[6:0]~~							10h
3	-	~~ENGND[6:0]~~							10h
4	~~SHIZ[7:0]~~								00h
5	-	-	-	-	-	-	-	~~SLT~~	00h

Description

This command sets registers related with source outputs.

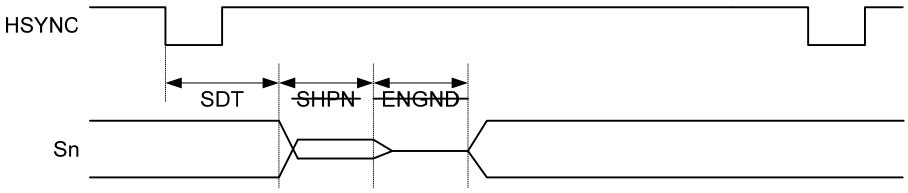
SDT[7:0] – Source output delay; [1..255] pixel clocks

~~**SHPN[6:0]** – Equalization period; [0..127] pixel clocks~~

~~**ENGND[6:0]** – GND level period; [1..127] pixel clocks~~

~~**SHIZ[7:0]** – Source output High-Z period controlled by registers GDC and BDC.~~

~~**SLT** – Spread spectrum source output generation~~
~~0 = Simultaneous drive~~
~~1 = Spread source outputs for several pixel clocks~~



6.2.30 B6h – Display Control 2

Mnemonic DISPCTL2

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	-	-	-	ASG	SDM	FHN	01h
2	CLW[7:0]								18h
3	-	-	GTO[5:0]						02h
4	GNO[7:0]								40h
5	FTI[7:0]								10h
6	GPM[7:0]								00h

Description

This command sets registers related with gate outputs.

ASG – (Amorphous Silicon Gate) Scanning mode only for H-type panel
0 = Dual scan
1 = Single scan

SDM – Number of gate clocking phases only for L-type panel
0 = 4-phase clocking
1 = 8-phase clocking

FHN – Gate signaling mode for both panel types
0 = non-overlapping
1 = overlapping

CLW[7:0] – Non-overlapping interval between GCLKs; [1..255] pixel clocks

GTO[5:0] – GPWR toggling period; [1..63] frames

GNO[7:0] – Non-overlapping interval between GPWRs; [1..255] pixel clocks

FTI[7:0] – GVST output delay; [1..255] pixel clocks

GPM[7:0] – Duration of gate pulse modulation; [0..255] pixel clocks

In case of H-type panel (SELP=1), ASG and FHN are the related registers. According to ASG, dual mode (ASG=0) or single mode (ASG=1) is selected. According to the FHN, non-overlap (FHN=0) or overlap (FHN=1) mode is selected. The FTI determines the delay time of starting signal (STPO or STPE) referring to Hsync. And the CLW determines the non-overlapping time between CLKs.. The following timing diagram and the tables are for them.

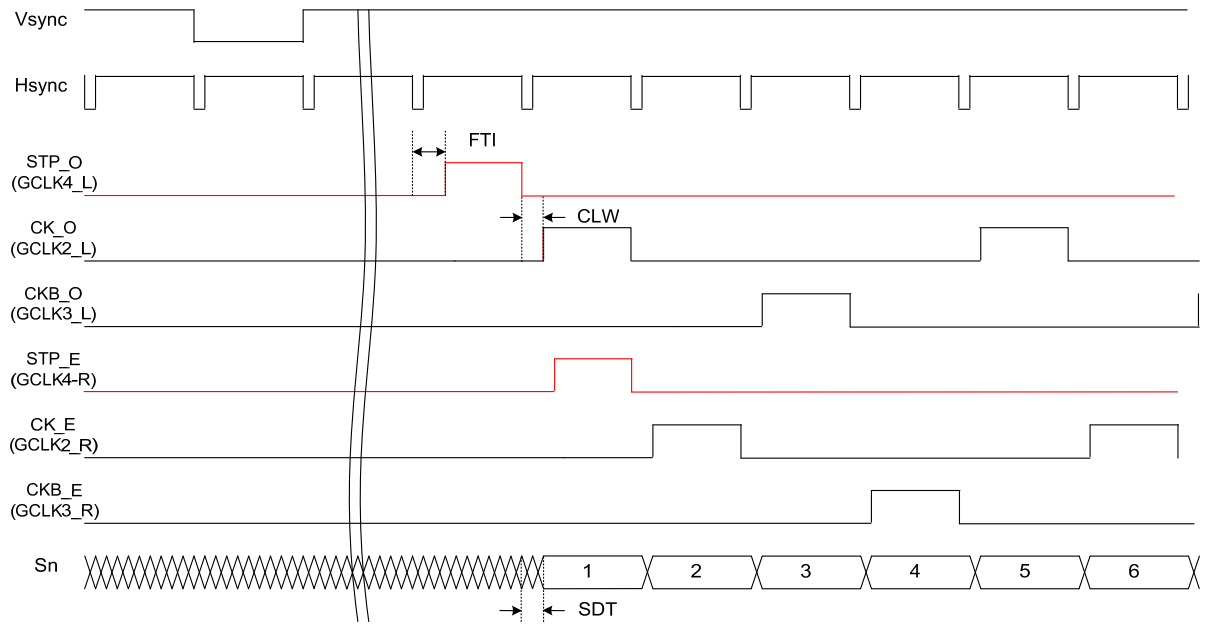


Figure 21. FTI and CLW timing diagram for H-type panel

CLW[7:0] –Non-overlap timing control with CLW register

CLW[7:0]	GCLK non-overlap timing
8'h00	0
8'h01	1 x PCLK
8'h02	2 x PCLK
:	:
:	:
8'hFD	253 x PCLK
8'hFE	254 x PCLK
8'hFF	255 x PCLK

FTI[4:0] – GVST output delay control with FTI register

FTI[7:0]	GVST output delay
7'h00	0
7'h01	1 x PCLK
7'h02	2 x PCLK
:	:
:	:
7'h7D	125 x PCLK
7'h7E	126 x PCLK
7'h7F	127 x PCLK

In case of L-type panel (SELP=0), FHN, SDM, and FV (in 36h) are the related registers. According to the FHN, non-overlapping (FHN=0) or overlapping (FHN=1) mode is selected. According to the SDM, 4-phase (SDM=0) or 8-phase mode (SDM=1) is selected. Finally according to the FV, forward scan

mode (FV=0) or reverse scan mode (FV=1) is selected. This FV setting make flip horizontal image possible. But it should be noted that some L-type panels do not support this bi-directional scanning feature. It means that this flip horizontal image availability depends on the panel feature.

GVSTs output delay timing referred to Hsync can be set by FTI register. And non-overlapping intervals between nearby GCLKs can be set by CLW register. The setting choices are same as above in the H-type panel case. There is a related timing diagram in the following.

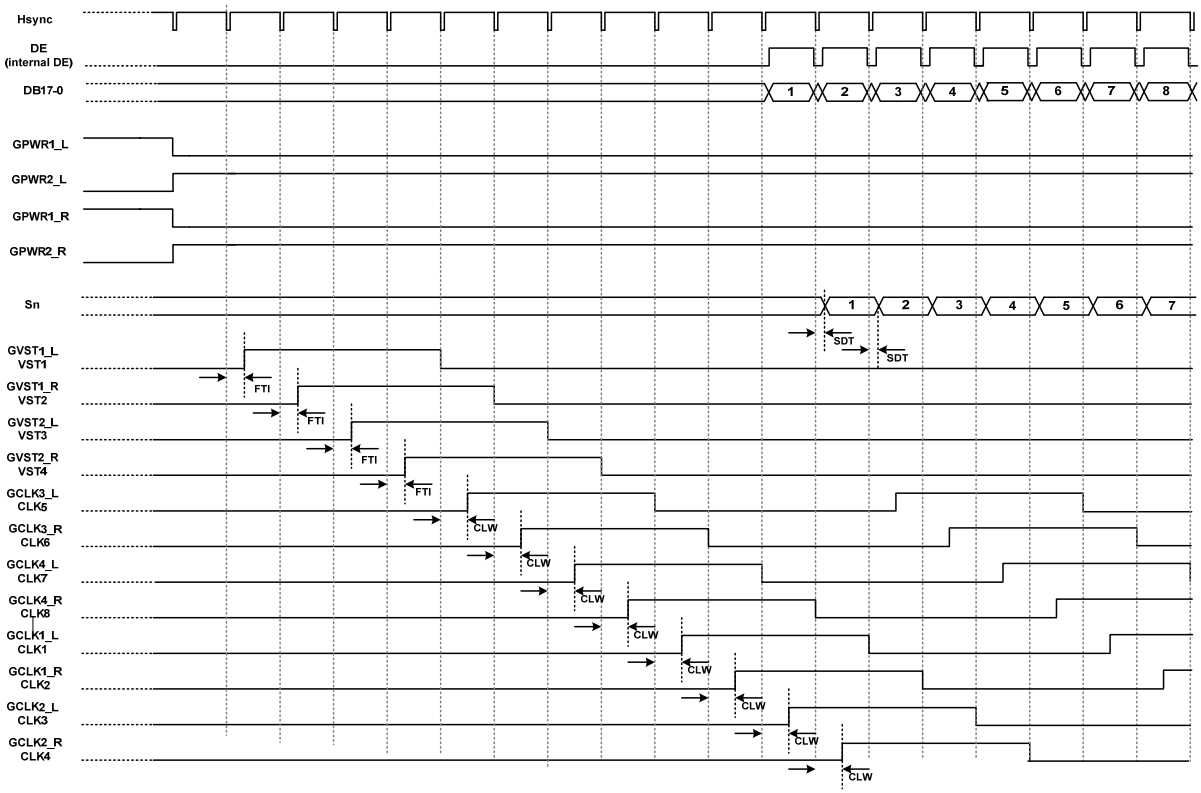


Figure 22. FTI and CLW timing diagram for L-type panel

To get more stable panel electrical characteristics, GNO and GTO registers are used only for the L-type panel. GTO determines GPWRs toggle frequency and the GNO determines the non-overlap timing between nearby GPWRs. The following timing diagram and the tables defines this.

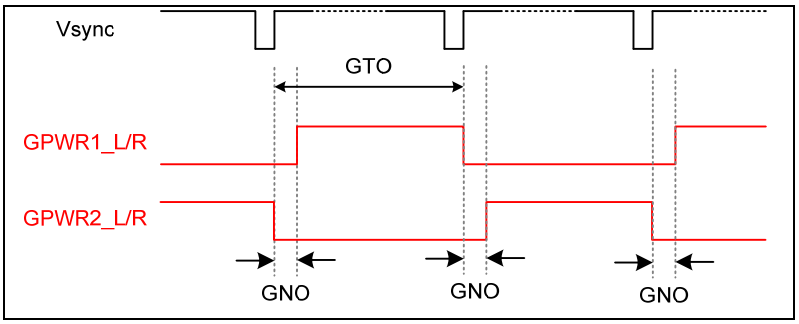


Figure 23. GTO and GNO timing for L-type panel

GTO[5:0] – GPWR toggle frequency with GTO register

GTO[5:0]	GPWR toggle frequency
6'h00	0
6'h01	1 x Frame
6'h02	2 x Frame
:	:
:	:
6'hFD	61 x Frame
6'hFE	62 x Frame
6'h3F	63 x Frame

GNO[7:0] – Non-overlap interval control between GPWRs with GNO register

GNO[7:0]	GPWR non-overlap timing
8'h00	0
8'h01	1 x PCLK
8'h02	2 x PCLK
:	:
:	:
8'hFD	253 x PCLK
8'hFE	254 x PCLK
8'hFF	255 x PCLK

For both H- and L- type panel cases, gate pulse modulation can be adopted to reduce source data sampling errors at the edge of gate falling by reducing the VGH and VGL voltage level difference when pixel data sampling. See the following functional diagram. The gate pulse modulated period (=GPM) can be controlled by using GPM register.

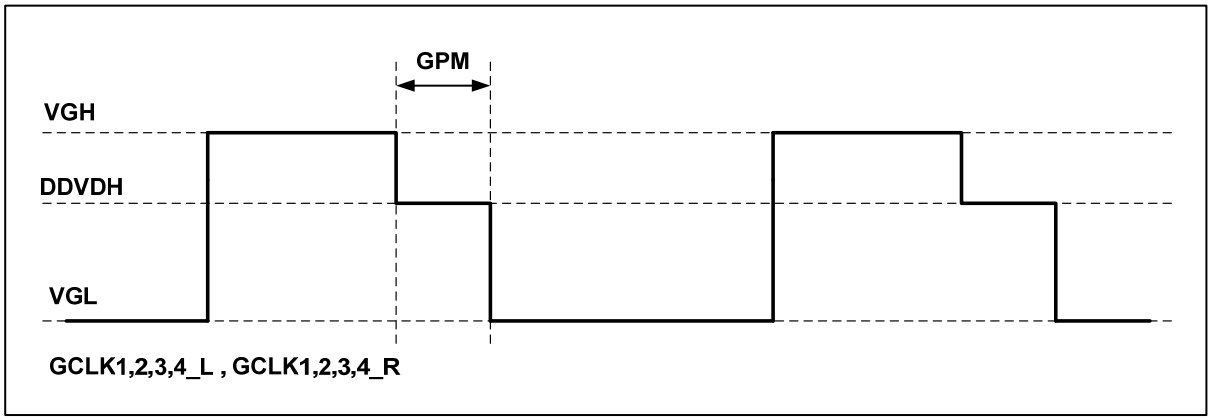


Figure 24. Functional diagram of Gate Pulse Modulation

GPM[7:0] –Gate pulse modulation duration control with GPM register

GPM[7:0]	Duration of gate pulse modulation
8'h00	0
8'h01	1 x PCLK

8'h02	2 x PCLK
8'h03	3 x PCLK
:	:
8'hFD	253 x PCLK
8'hFE	254 x PCLK
8'hFF	255 x PCLK

Detailed waveforms with each cases are illustrated in the following figures. According to SELP setting, either H-type panel (SELP=1) or L-type panel (SELP=0) case is selected.

H-Type Panel (SELP = 1)

The three following figures are for the H-type panel. They vary their waveforms according to the FHN and ASG register settings.

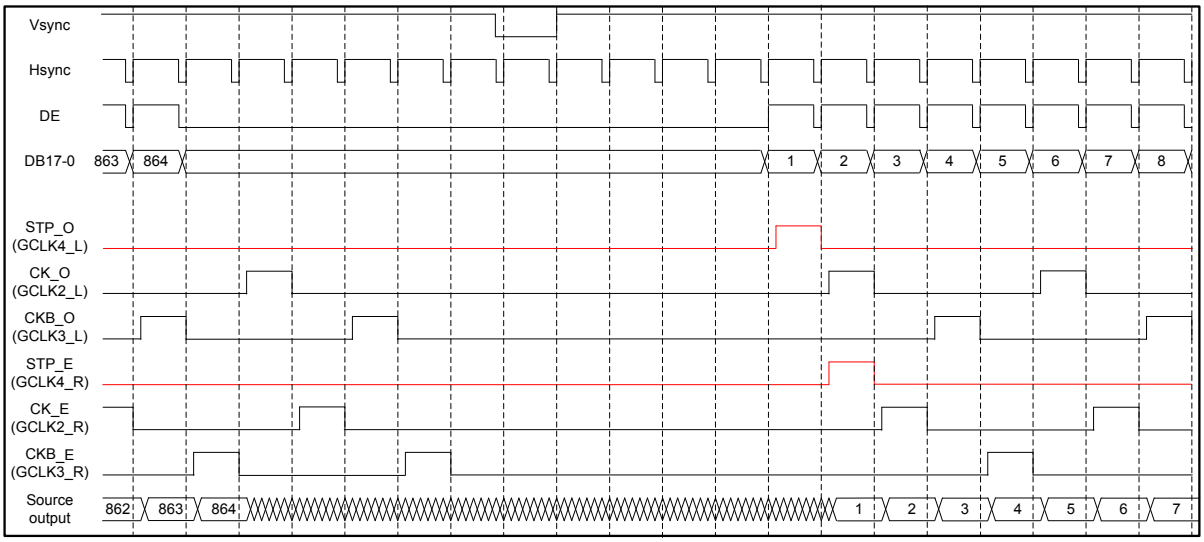


Figure 25. Non-overlap, dual scan (FHN=0, ASG=0)

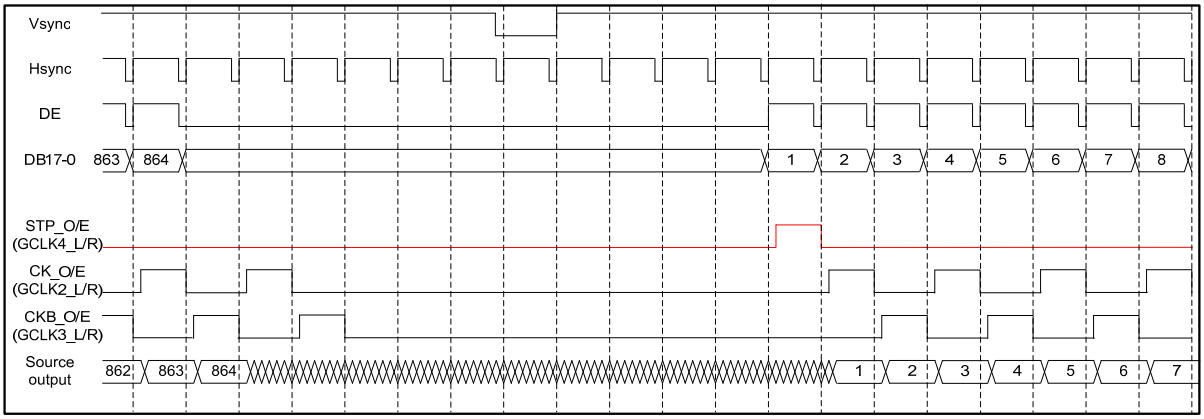


Figure 26. Non-overlap, single scan (FHN=X, ASG=1)

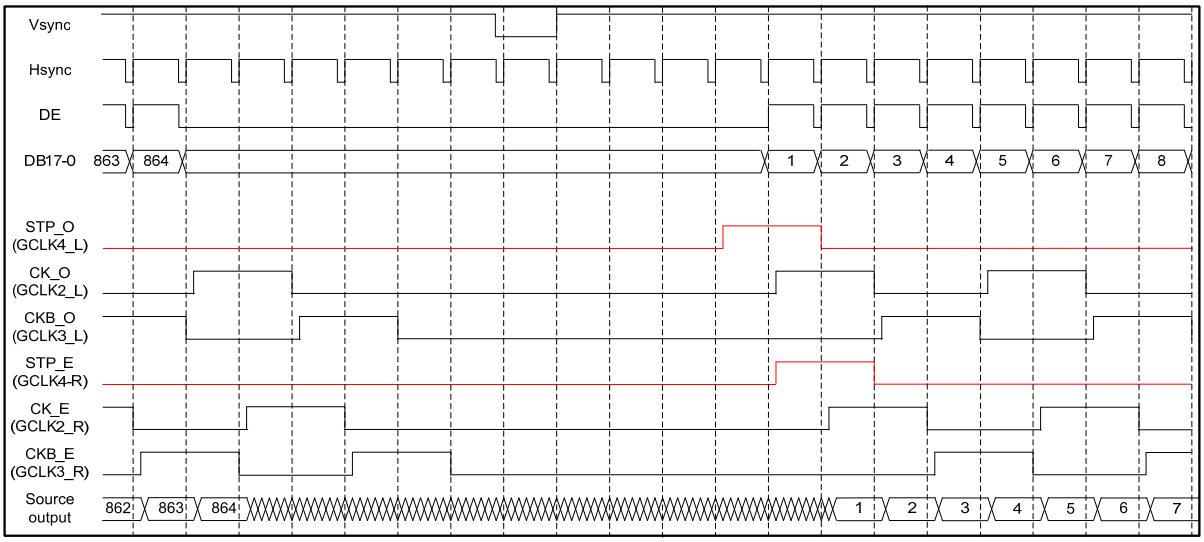


Figure 27. Overlap, dual scan (FHN=1, ASG=0)

L-Type Panel (SELP = 0)

The following figures are for the L-type panel. They vary their waveforms according to the FHN, SDM, FV and FVST register settings. When GSWAP register is set to high, GCLK waveform swapping happens for each modes.

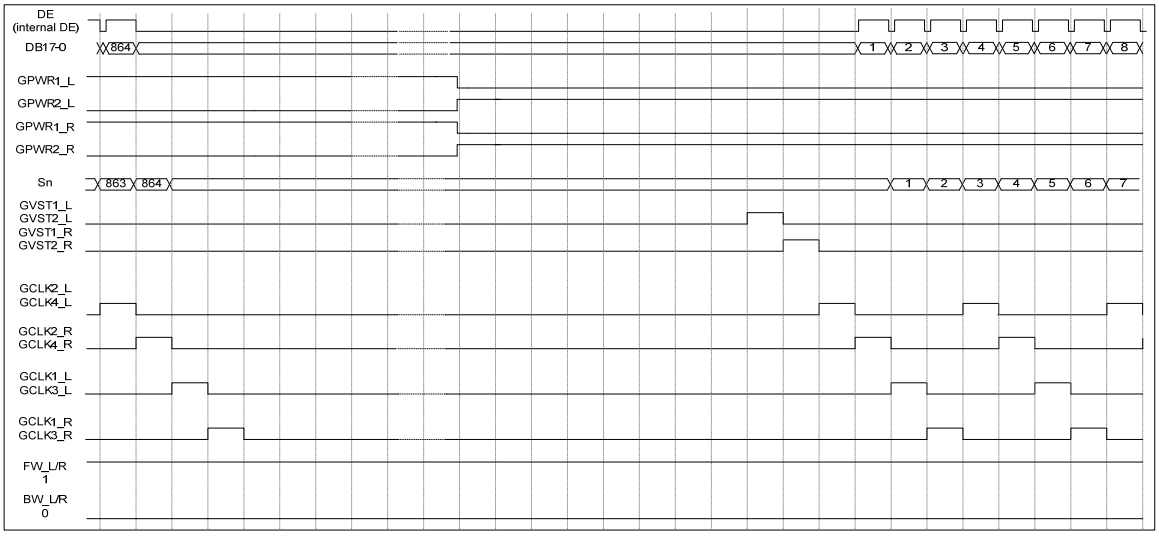


*Figure 28. Non-overlap, 4-phase, forward mode (**FHN=0, SDM=0, FV=0**)*

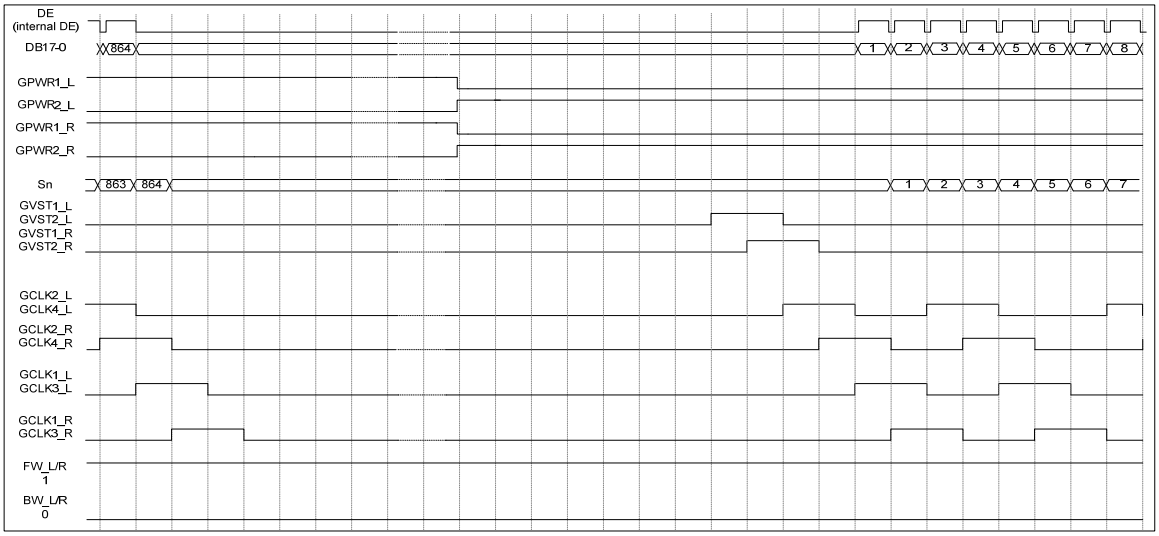


*Figure 29. Overlap, 4-phase, forward mode **(FHN=1, SDM=0, FV=0)***

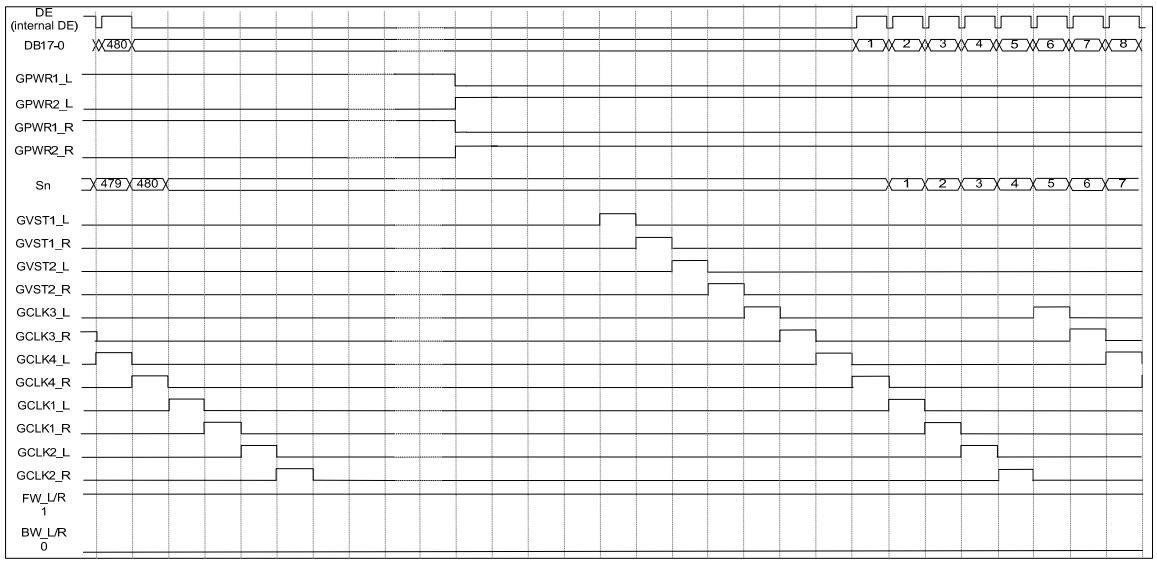


*Figure 30. Non-overlap, 8-phase, forward mode (**FHN=0, SDM=1, FV=0**)*

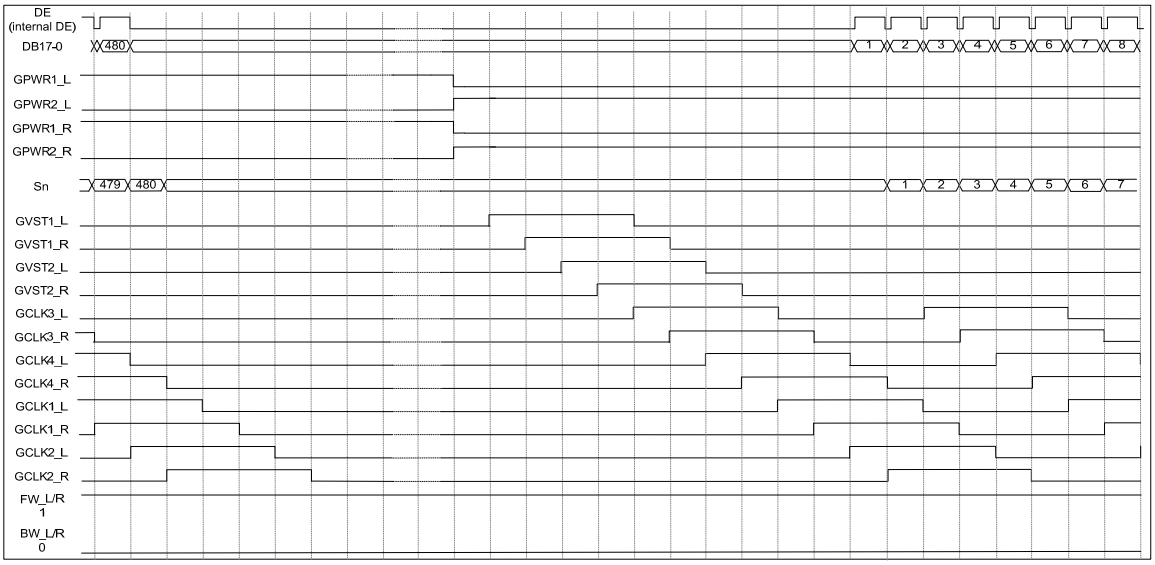


*Figure 31. Overlap, 8-phase, forward mode (**FHN=1, SDM=1, FV=0**)*

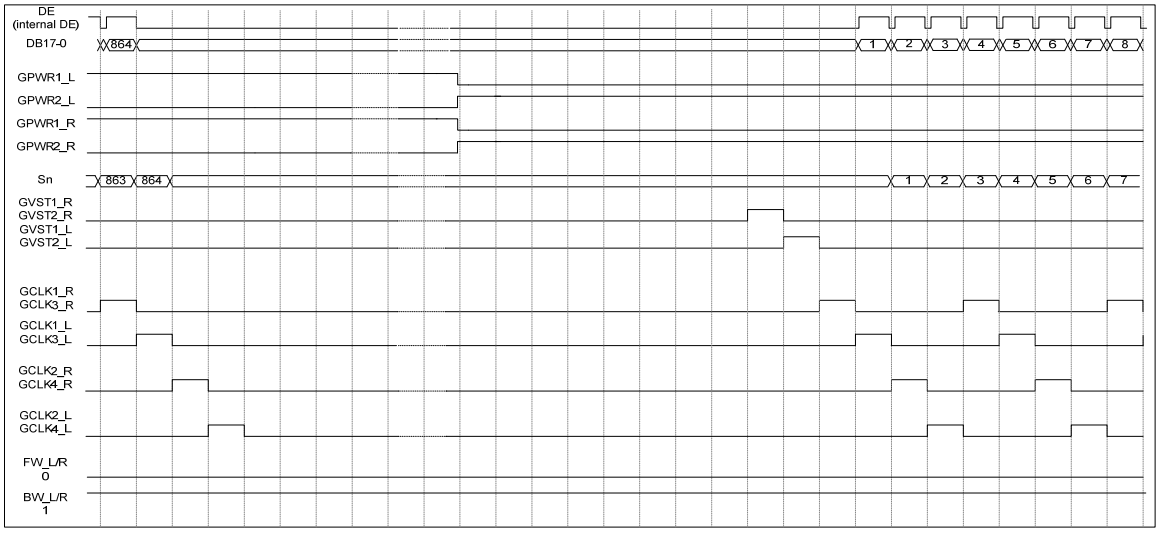


*Figure 32. Non-overlap, 4-phase, backward mode (**FHN=0, SDM=0, FV=1**)*

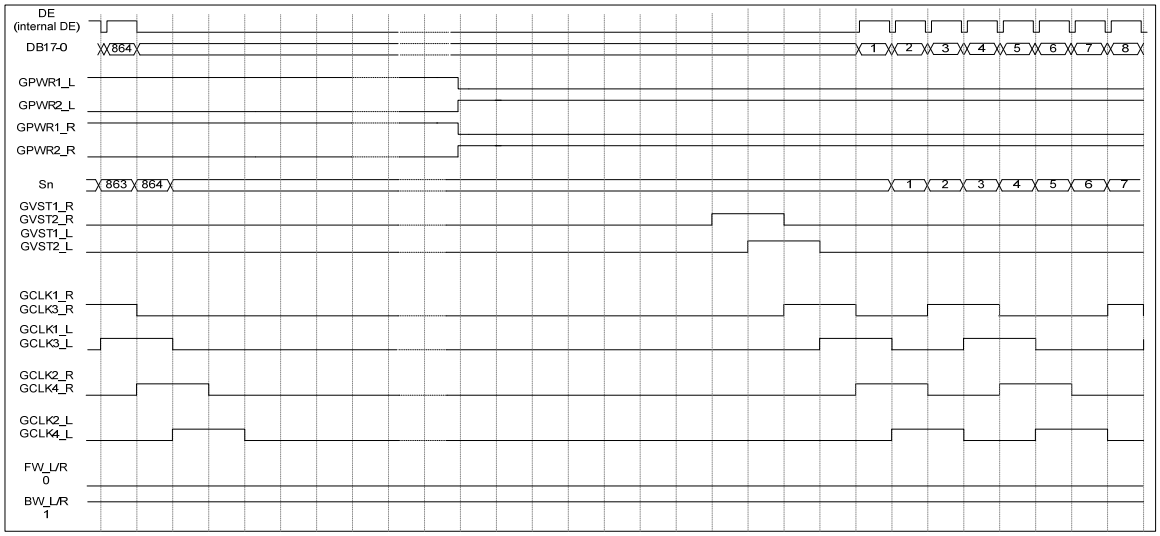


*Figure 33. Overlap, 4-phase, backward mode (**FHN=1, SDM=0, FV=1**)*

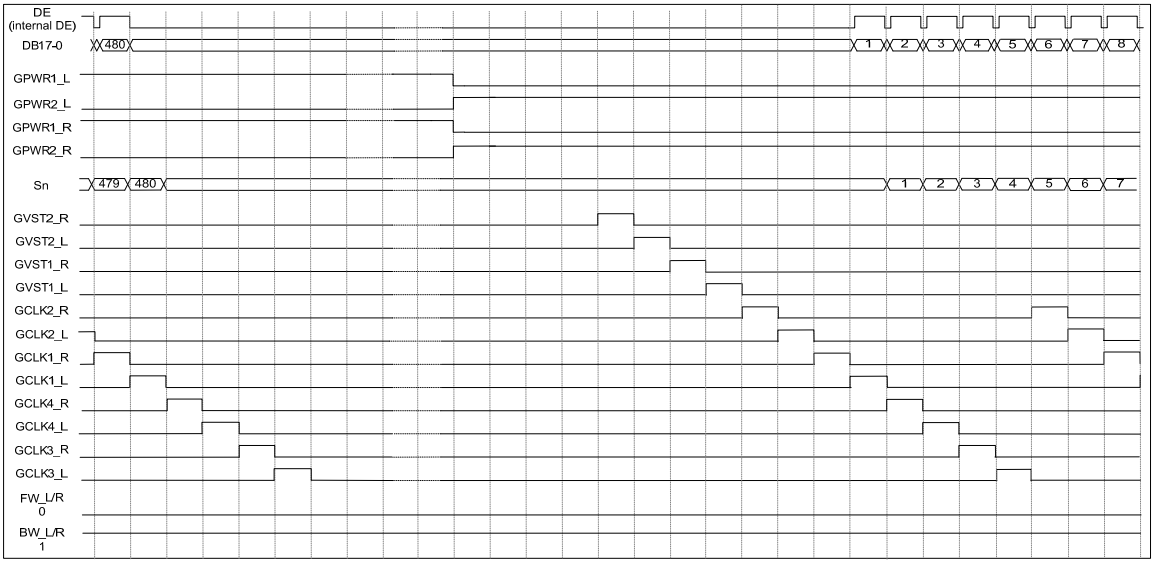


*Figure 34. Non-overlap, 8-phase, backward mode (**FHN=0, SDM=1, FV=1**)*

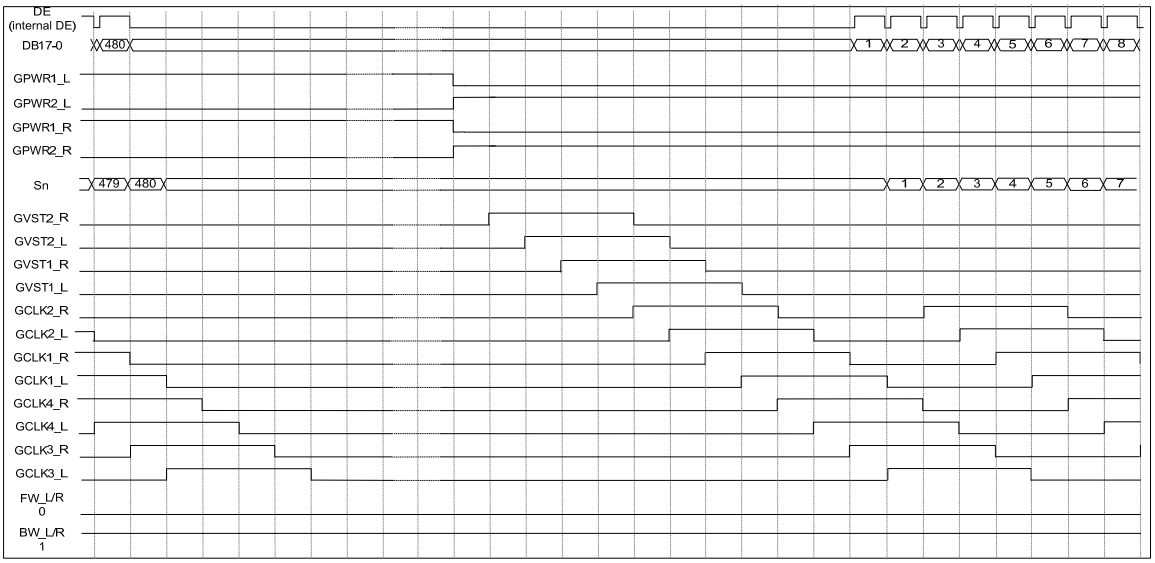


*Figure 35. Overlap, 8-phase, backward mode (**FHN=1, SDM=1, FV=1**)*

6.2.31 C0h – Internal Oscillator Setting

Mnemonic OSCSET

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	-	-	-	-	-	OSC	00h
2	-	-	-	FRS[4:0]					00h

Description

OSC – For step-up circuits, use the internal oscillator instead of PCLK.
0 = Disable
1 = Enable

FRS[4:0] – Oscillator frequency control

FRS[4:0]	Oscillator Frequency
00h	184 kHz
08h	256 kHz
10h	475 kHz
14h	499 kHz
18h	2.06 MHz
1Ah	2.30 MHz
1Ch	2.56 MHz
1Dh	2.94 MHz
1Eh	3.13 MHz
1Fh	3.58 MHz

6.2.32 C1h – Power Control 1

Mnemonic PWRCTL1

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	-	-	DTE	-	STB	DSTB	02h

Description

DTE – Manual gate output enable
0 = Disable
1 = Enable

STB – Standby mode
0 = Normal mode
1 = Standby mode
Standby mode is equivalent with sleep mode except that it does not come up with an automatic power on/off sequence.

DSTB – Deep standby mode
0 = Normal mode
1 = Deep standby mode
In deep standby mode, the internal logic power supply is turned off to reduce power consumption. In this mode, register contents are not retained.

6.2.33 C2h – Power Control 2

Mnemonic PWRCTL2

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	LVGL	VDL	VCL	VGL	VGH	VDH	00h

Description

LVGL – Generate LVGL
0 = Disable
1 = Enable

VDL – Generate DDVDL
0 = Disable
1 = Enable

VCL – Generate VCL
0 = Disable
1 = Enable

VGL – Generate VGL
0 = Disable
1 = Enable

VGH – Generate VGH
0 = Disable
1 = Enable

LVGL – Generate LVGL
0 = Disable
1 = Enable

VDH – Generate DDVDH
0 = Disable
1 = Enable

6.2.34 C3h – Power Control 3

Mnemonic PWRCTL3

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	-	-	-	STMODE[2:0]			00h
2	-	-	-	-	-	DC1[2:0]			04h
3	-	-	-	-	-	DC2[2:0]			03h
4	-	-	-	-	-	DC3[2:0]			03h
5	-	-	-	-	-	DCPFM[2:0]			03h

Description

STMODE[2:0] – These bits set the step-up auto power generation modes. 1~3 are for H-type panel and 5~7 are for L-type panel. 0 and 4 are for manual power generation settings.

STMODE[2:0]	DDVDH circuit	DDVDL circuit	Power Setting
3'h0	Manual	Manual	Manual
3'h1	External DDVDH	STEP-UP3	Auto
3'h2	PFM Boosting	STEP-UP3	Auto
3'h3	PFM Boosting	Diode inverting	Auto
3'h4	Manual	Manual	Manual
3'h5	External DDVDH	STEP-UP3	Auto
3'h6	PFM Boosting	STEP-UP3	Auto
3'h7	PFM Boosting	Diode inverting	Auto

DC1[2:0] – Clock frequency of the step-up circuit 2

DC1[2:0]	Step-up frequency	
	OSC = 1	OSC = 0
000	fosc/2	fpclk/64
001	fosc/4	fpclk/128
010	fosc/8	fpclk/256
011	fosc/16	fpclk/512
100	fosc/32	fpclk/1024
101	fosc/64	fpclk/2048
110	fosc/128	fpclk/4096
111	fosc/256	Setting disabled

DC2[2:0] – Clock frequency of the step-up circuit 3

DC2[2:0]	Step-up frequency	
	OSC = 1	OSC = 0
000	fosc/2	fpclk/64
001	fosc/4	fpclk/128
010	fosc/8	fpclk/256
011	fosc/16	fpclk/512
100	fosc/32	fpclk/1024
101	fosc/64	fpclk/2048
110	fosc/128	fpclk/4096
111	fosc/256	Setting disabled

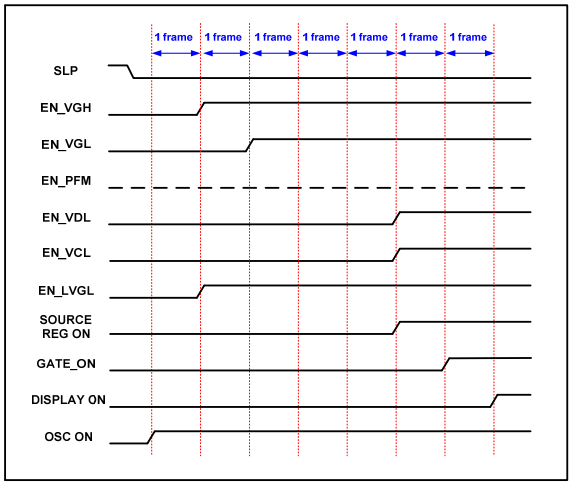
DC3[2:0] – Clock frequency of the step-up circuit 4

DC3[2:0]	Step-up frequency	
	OSC = 1	OSC = 0
000	fosc/2	fpclk/64
001	fosc/4	fpclk/128
010	fosc/8	fpclk/256
011	fosc/16	fpclk/512
100	fosc/32	fpclk/1024
101	fosc/64	fpclk/2048
110	fosc/128	fpclk/4096
111	fosc/256	Setting disabled

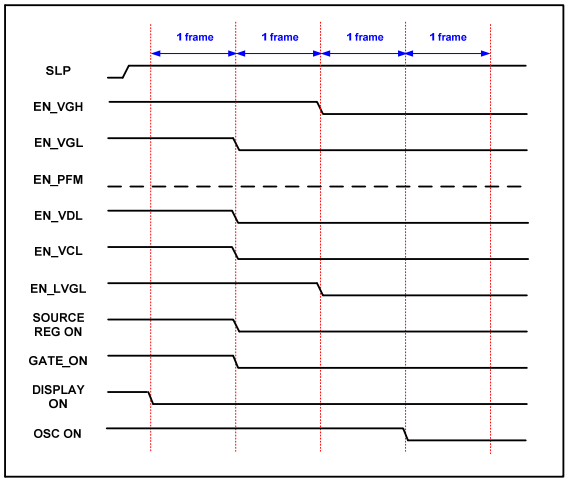
DCPFM[2:0] – Clock frequency of the PFM booster

DCPFM[2:0]	Step-up frequency	
	OSC = 1	OSC = 0
000	fosc/1	fpclk/4
001	fosc/1	fpclk/6
010	fosc/1	fpclk/8
011	fosc/1	fpclk/12
100	fosc/1	fpclk/16
101	fosc/1	fpclk/24
110	fosc/1	fpclk/32
111	fosc/2	fpclk/48

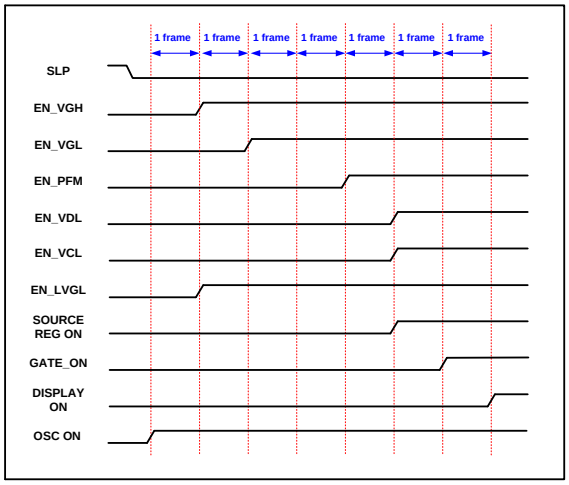
The followings are for understanding the operations of each auto power generation modes.



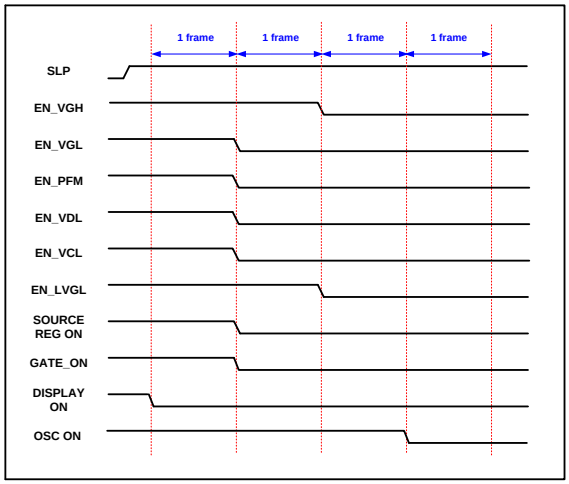
Power ON
STMODE[2:0]=1h



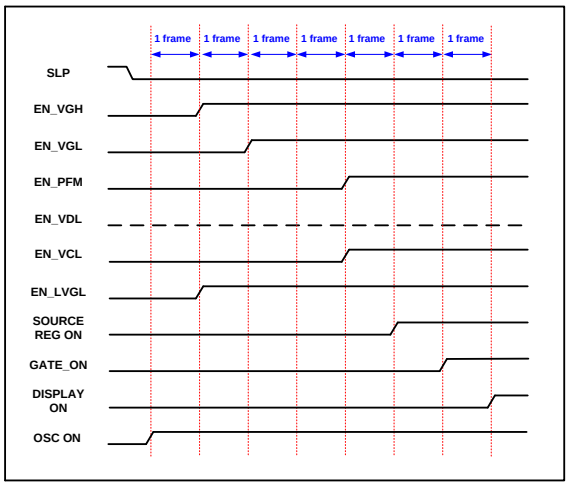
Power OFF
STMODE[2:0]=1h



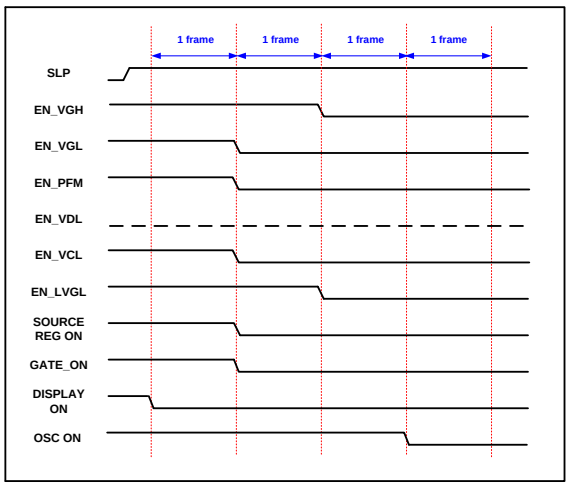
Power ON
STMODE[2:0]=2h



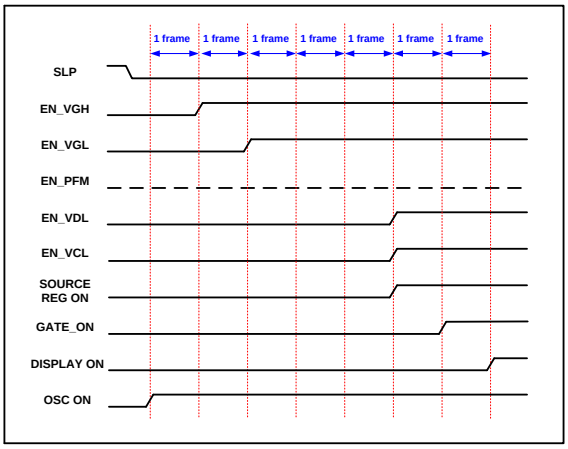
Power OFF
STMODE[2:0]=2h



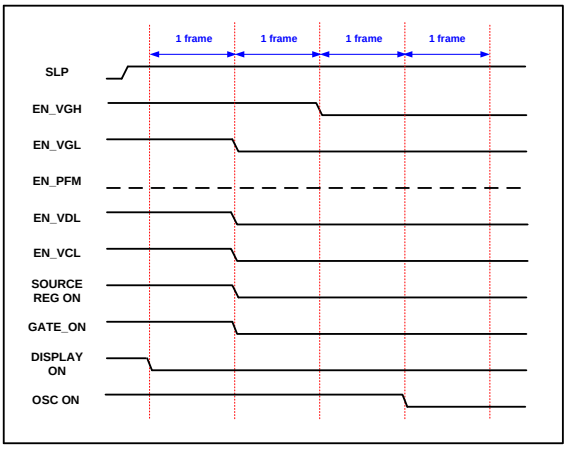
Power ON
STMODE[2:0]=3h



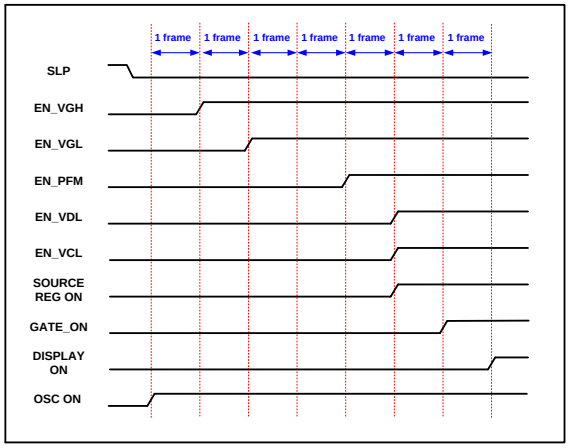
Power OFF
STMODE[2:0]=3h



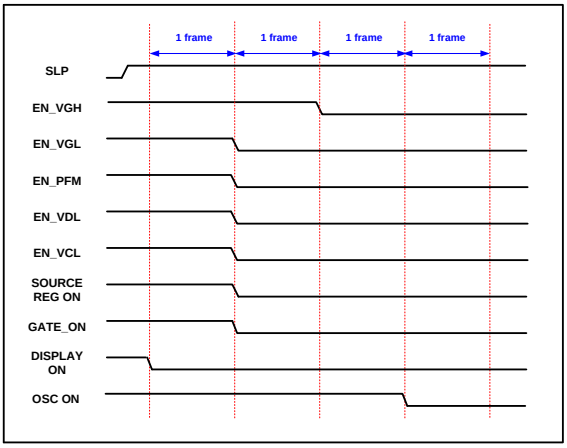
Power ON
STMODE[2:0]=5h



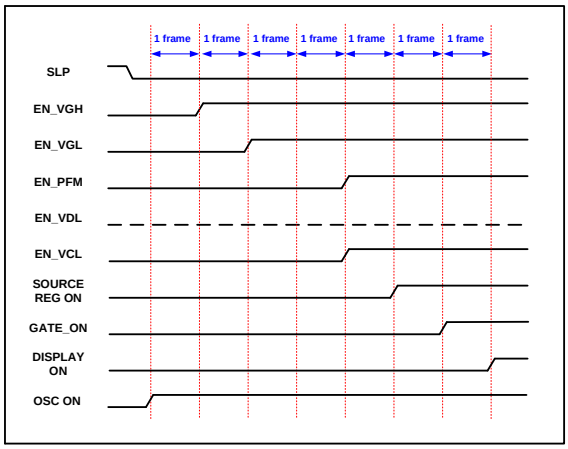
Power OFF
STMODE[2:0]=5h



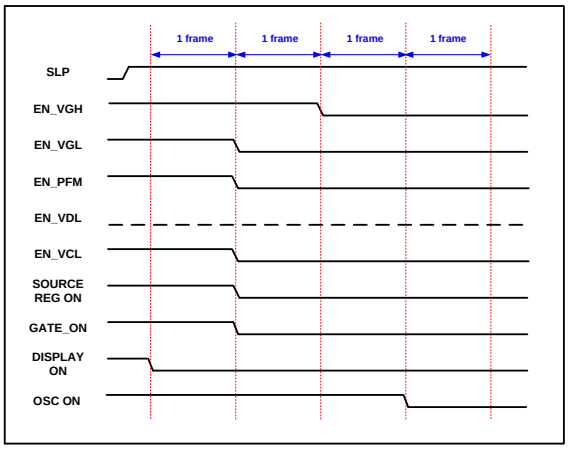
Power ON
STMODE[2:0]=6h



Power OFF
STMODE[2:0]=6h



Power ON
STMODE[2:0]=7h



Power OFF
STMODE[2:0]=7h

6.2.35 C4h – Power Control 4

Mnemonic PWRCTL4

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	OPB	BMB	-	BDC[2:0]			00h
2	-	GDC[2:0]				AP[2:0]			00h
3	-	-	-	VRH1[4:0]					00h
4	-	-	-	VRH2[4:0]					00h
5	-	-	SELOPA	REGPD	-	BT[2:0]			05h
6	-	VBS[2:0]			-	VREFS[2:0]			0Bh

Description

OPB – Bias selection
0 = Buffered bias
1 = Normal Bias

BMB – Bias line current adjustment
0 = 2
1 = 1

BDC[2:0] – Channel amp quiescent current adjustment

BDC[2:0]	Bias Current (μA)
0	Halt
1	0.5
2	1
3	1.5
4	2
5	2.5
6	3
7	3.5

GDC[2:0] – Grayscale amp quiescent current adjustment

GDC[2:0]	Bias Current (μA)
0	Halt
1	0.5
2	1
3	1.5
4	2
5	2.5
6	3
7	3.5

AP[2:0] – Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit.

AP[2:0]	Bias Current (μA)
0	Halt
1	0.25
2	0.5
3	0.75

4	1
5	1.25
6	1.5
7	1.75

VRH1[4:0] – Sets the VREG1 output level, which is a reference level for the grayscale voltage level.

VRH1[4:0]	VREG1 Level
5'h00	Halt (VREG1 = High-Z)
5'h01	VCI x 1.133
5'h02	VCI x 1.160
5'h03	VCI x 1.187
5'h04	VCI x 1.213
5'h05	VCI x 1.240
5'h06	VCI x 1.267
5'h07	VCI x 1.293
5'h08	VCI x 1.320
5'h09	VCI x 1.347
5'h0A	VCI x 1.373
5'h0B	VCI x 1.400
5'h0C	VCI x 1.427
5'h0D	VCI x 1.453
5'h0E	VCI x 1.480
5'h0F	VCI x 1.507

VRH1[4:0]	VREG1 Level
5'h10	VCI x 1.533
5'h11	VCI x 1.560
5'h12	VCI x 1.587
5'h13	VCI x 1.613
5'h14	VCI x 1.640
5'h15	VCI x 1.667
5'h16	VCI x 1.693
5'h17	VCI x 1.720
5'h18	VCI x 1.747
5'h19	VCI x 1.773
5'h1A	VCI x 1.800
5'h1B	VCI x 1.827
5'h1C	VCI x 1.853
5'h1D	VCI x 1.880
5'h1E	VCI x 1.907
5'h1F	VCI x 1.933

VRH2[4:0] – Sets the VREG2 output level, which is a reference level for the grayscale voltage level.

VRH2[4:0]	VREG2 Level
5'h00	Halt (VREG2 = High-Z)
5'h01	-VCI x 1.133
5'h02	-VCI x 1.160
5'h03	-VCI x 1.187
5'h04	-VCI x 1.213
5'h05	-VCI x 1.240
5'h06	-VCI x 1.267
5'h07	-VCI x 1.293
5'h08	-VCI x 1.320
5'h09	-VCI x 1.347
5'h0A	-VCI x 1.373
5'h0B	-VCI x 1.400
5'h0C	-VCI x 1.427
5'h0D	-VCI x 1.453
5'h0E	-VCI x 1.480
5'h0F	-VCI x 1.507

VRH2[4:0]	VREG2 Level
5'h10	-VCI x 1.533
5'h11	-VCI x 1.560
5'h12	-VCI x 1.587
5'h13	-VCI x 1.613
5'h14	-VCI x 1.640
5'h15	-VCI x 1.667
5'h16	-VCI x 1.693
5'h17	-VCI x 1.720
5'h18	-VCI x 1.747
5'h19	-VCI x 1.773
5'h1A	-VCI x 1.800
5'h1B	-VCI x 1.827
5'h1C	-VCI x 1.853
5'h1D	-VCI x 1.880
5'h1E	-VCI x 1.907
5'h1F	-VCI x 1.933

SELOPA – Vcom amp select

REGPD – Regulator power down

BT[2:0] – Changes the rate applied to the step-up circuit. Adjust the step-up rate according to the voltage in use. To reduce current consumption, set a smaller step-up rate.

BT[2:0]	DDVDH	DDVDL	VGH	VGL
3'h0			DDVDH x 3 [x 6]	−(DDVDH x 3) [x −6]
3'h1				−(VCI + DDVDH x 2) [x −5]
3'h2				−(DDVDH x 2) [x −4]
3'h3			VCI + DDVDH x 2 [x 5]	−(DDVDH x 3) [x −6]
~~3'h4~~				~~−(VCI + DDVDH x 2) [x −5]~~
3'h5				−(DDVDH x 2) [x −4]
3'h6			DDVDH x 2 [x 4]	−(VCI + DDVDH x 2) [x −5]
3'h7				−(DDVDH x 2) [x −4]

Notes:

1. The step-up rate from the VCI level is shown in the bracket [ ] in the above table.
2. When using the DDVDH, DDVDL, VCL, VGH and VGL voltage levels, connect a capacitor to each capacitor connection pin. Set the following voltages within the limits: DDVDH = max 6V, VCL = min -3V, VGH = max 18V, VGL = min -18V.
3. BT[2:0]=3'h4 mode is not recommended in auto power generation mode. If this mode is needed, manual power setting should be used.

VBS[2:0] – Sets the VBIAS level. The VBS bits can set the VBIAS level 1.3 to 1.9 times the VCI level.

VBS[2:0]	VBIAS
0	Halt
1	VCI x 1.30
2	VCI x 1.36
3	VCI x 1.44
4	VCI x 1.50
5	VCI x 1.56
6	VCI x 1.64
7	VCI x 1.90

VREFS[3:0] – Selects the reference voltage of the switching regulator circuit. Adjust the reference voltage according to the VCI voltage in use.

VREFS[3:0]	DDVDH voltage
0	VCI x 2.45
1	VCI x 2.40
2	VCI x 2.35
3	VCI x 2.30
4	VCI x 2.25
5	VCI x 2.20
6	VCI x 2.15
7	VCI x 2.10
8	VCI x 2.05
9	VCI x 2.00
10	VCI x 1.95

11	VCI x 1.90
12	VCI x 1.85
13	VCI x 1.80
14	VCI x 1.75
15	VCI x 1.70

6.2.36 C5h – Power Control 5

Mnemonic PWRCTL5

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	VCM[6:0]							00h

Description

Note: Set the VCOML voltage from VREG2OUT level to 0V.

VCM[6:0] – Sets the VCOM level. VCM[6:0] specifies the voltage by VREG2OUT x n, where n can change from 0.1 to 1 as shown in the table below. To halt internal setting and adjust VCOM through VCOMR pad, set VCM[6:0] = "1111111". Then, VCOM level follows VCOMR level.

VCM[6:0]	VCOM
7'h00	Halt(VCOM=GND)
7'h01	VREG2OUT x 1
7'h02	VREG2OUT x 0.993
7'h03	VREG2OUT x 0.986
7'h04	VREG2OUT x 0.979
7'h05	VREG2OUT x 0.971
7'h06	VREG2OUT x 0.964
7'h07	VREG2OUT x 0.957
7'h08	VREG2OUT x 0.950
7'h09	VREG2OUT x 0.943
7'h0A	VREG2OUT x 0.936
7'h0B	VREG2OUT x 0.929
7'h0C	VREG2OUT x 0.921
7'h0D	VREG2OUT x 0.914
7'h0E	VREG2OUT x 0.907
7'h0F	VREG2OUT x 0.9
7'h10	VREG2OUT x 0.893
7'h11	VREG2OUT x 0.886
7'h12	VREG2OUT x 0.879
7'h13	VREG2OUT x 0.871
7'h14	VREG2OUT x 0.864
7'h15	VREG2OUT x 0.857
7'h16	VREG2OUT x 0.850
7'h17	VREG2OUT x 0.843
7'h18	VREG2OUT x 0.836
7'h19	VREG2OUT x 0.829
7'h0A	VREG2OUT x 0.821
7'h0B	VREG2OUT x 0.814
7'h0C	VREG2OUT x 0.807
7'h0D	VREG2OUT x 0.8
7'h0E	VREG2OUT x 0.793
7'h0F	VREG2OUT x 0.786
7'h20	VREG2OUT x 0.779
7'h21	VREG2OUT x 0.771
7'h22	VREG2OUT x 0.764
7'h23	VREG2OUT x 0.757
7'h24	VREG2OUT x 0.750
7'h25	VREG2OUT x 0.743

VCM[6:0]	VCOM
7'h26	VREG2OUT x 0.736
7'h27	VREG2OUT x 0.729
7'h28	VREG2OUT x 0.721
7'h29	VREG2OUT x 0.714
7'h2A	VREG2OUT x 0.707
7'h2B	VREG2OUT x 0.7
7'h2C	VREG2OUT x 0.693
7'h2D	VREG2OUT x 0.686
7'h2E	VREG2OUT x 0.679
7'h2F	VREG2OUT x 0.671
7'h30	VREG2OUT x 0.664
7'h31	VREG2OUT x 0.657
7'h32	VREG2OUT x 0.650
7'h33	VREG2OUT x 0.643
7'h34	VREG2OUT x 0.636
7'h35	VREG2OUT x 0.629
7'h36	VREG2OUT x 0.621
7'h37	VREG2OUT x 0.614
7'h38	VREG2OUT x 0.607
7'h39	VREG2OUT x 0.6
7'h3A	VREG2OUT x 0.593
7'h3B	VREG2OUT x 0.586
7'h3C	VREG2OUT x 0.579
7'h3D	VREG2OUT x 0.571
7'h3E	VREG2OUT x 0.564
7'h3F	VREG2OUT x 0.557
7'h40	VREG2OUT x 0.550
7'h41	VREG2OUT x 0.543
7'h42	VREG2OUT x 0.536
7'h43	VREG2OUT x 0.529
7'h44	VREG2OUT x 0.521
7'h45	VREG2OUT x 0.514
7'h46	VREG2OUT x 0.507
7'h47	VREG2OUT x 0.5
7'h48	VREG2OUT x 0.493
7'h49	VREG2OUT x 0.486
7'h4A	VREG2OUT x 0.479
7'h4B	VREG2OUT x 0.471

VCM[6:0]	VCOM
7'h4C	VREG2OUT x 0.464
7'h4D	VREG2OUT x 0.457
7'h4E	VREG2OUT x 0.450
7'h4F	VREG2OUT x 0.443
7'h50	VREG2OUT x 0.436
7'h51	VREG2OUT x 0.429
7'h52	VREG2OUT x 0.421
7'h53	VREG2OUT x 0.414
7'h54	VREG2OUT x 0.407
7'h55	VREG2OUT x 0.4
7'h56	VREG2OUT x 0.393
7'h57	VREG2OUT x 0.386
7'h58	VREG2OUT x 0.379
7'h59	VREG2OUT x 0.371
7'h5A	VREG2OUT x 0.364
7'h5B	VREG2OUT x 0.357
7'h5C	VREG2OUT x 0.350
7'h5D	VREG2OUT x 0.343
7'h5E	VREG2OUT x 0.336
7'h5F	VREG2OUT x 0.329
7'h60	VREG2OUT x 0.321
7'h61	VREG2OUT x 0.314
7'h62	VREG2OUT x 0.307
7'h63	VREG2OUT x 0.3
7'h64	VREG2OUT x 0.293
7'h65	VREG2OUT x 0.286
7'h66	VREG2OUT x 0.279
7'h67	VREG2OUT x 0.271
7'h68	VREG2OUT x 0.264
7'h69	VREG2OUT x 0.257
7'h6A	VREG2OUT x 0.250
7'h6B	VREG2OUT x 0.243
7'h6C	VREG2OUT x 0.236
7'h6D	VREG2OUT x 0.229
7'h6E	VREG2OUT x 0.221
7'h6F	VREG2OUT x 0.214
7'h70	VREG2OUT x 0.207
7'h71	VREG2OUT x 0.2

VCM[6:0]	VCOM
7'h72	VREG2OUT x 0.193
7'h73	VREG2OUT x 0.186
7'h74	VREG2OUT x 0.179
7'h75	VREG2OUT x 0.171
7'h76	VREG2OUT x 0.164
7'h77	VREG2OUT x 0.157
7'h78	VREG2OUT x 0.150
7'h79	VREG2OUT x 0.143
7'h7A	VREG2OUT x 0.136
7'h7B	VREG2OUT x 0.129
7'h7C	VREG2OUT x 0.121
7'h7D	VREG2OUT x 0.114
7'h7E	VREG2OUT x 0.107
7'h7F	VCOMR

6.2.37 C6h – Power Control 6

Mnemonic PWRCTL4

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	RI[2:0]			-	RV[2:0]			23h
2	-	RSET[2:0]			-	RCONT[2:0]			50h
3	-	-	-	-	-	-	SBC	GBC	00h

Description

RI[2:0] – These bits control the bias current of internal logic regulator.

RI[2:0]	Logic Regulator Bias Current
0	x 0.2
1	x 1
2	x 2
3	x 3
4	x 3
5	x 4
6	x 5
7	x 6

RV[2:0] – These bits control the output voltage of internal logic regulator.

RV[2:0]	VDD Voltage
0	VCI x 0.80
1	VCI x 0.75
2	VCI x 0.70
3	VCI x 0.65
4	VCI x 0.60
5	VCI x 0.55
6	VCI x 0.50
7	VCI x 0.45

RSET[2:0] – These bits control the main bias.

RSET[2:0]	Main Bias Current
0	x 0.39
1	x 0.43
2	x 0.48
3	x 0.56
4	x 0.65
5	x 0.79
6	x 1.00 (default)
7	x 1.36

RCONT[2:0] – These bits control the input voltage of main bias opamp.

RCONT[2:0]	Main Bias Voltage
0	VCI x 0.25
1	Setting disabled

2	Open
3	VCI x 0.30
4	Setting disabled
5	Setting disabled
6	VCI x 0.20
7	Setting disabled

SBC – Source Channel AMP bias control.

GBC – Grayscale AMP bias control.

6.2.38 C7h – Offset Cancelling Control

Mnemonic OFCCTL

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	-	-	-	-	-	-	OFCEN	00h
2	OFCTSW[7:0]								B0h
3	OFCTD2[3:0]				OFCTD1[3:0]				40h

Description

OFCEN – Offset cancelling enable/disable
0 = disable
1 = enable

OFCTSW[7:0] – Offset sampling period in 2*PCLKs

OFCTSW[7:0]	Sampling Period in PCLKs
0	0
1	2
2	4
3	6
…	…
253	506
254	508
255	510

OFCTD1[3:0] – Delay of the offset sampling start time in 2*PCLKs

OFCTD2[3:0] – Interval between offset sampling period and compensation period in 2*PCLKs

6.2.39 C8h – Backlight Control

Mnemonic BLCTL

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	CDSP[3:0]				CDMP[3:0]				82h
2	PWMP	-	-	-	-	-	FPWM[1:0]		01h

Description

CDSP[3:0] – Dimming control of still image

CDSP[3:0]	Dimming Control Steps	CDSP[3:0]	Dimming Control Steps
4'h0	0	4'h8	8
4'h1	1	4'h9	9
4'h2	2	4'hA	10
4'h3	3	4'hB	11
4'h4	4	4'hC	12
4'h5	5	4'hD	13
4'h6	6	4'hE	14
4'h7	7	4'hF	15

CDMP[3:0] – Dimming control of moving picture

CDMP[3:0]	Dimming Control Steps	CDMP[3:0]	Dimming Control Steps
4'h0	0	4'h8	8
4'h1	1	4'h9	9
4'h2	2	4'hA	10
4'h3	3	4'hB	11
4'h4	4	4'hC	12
4'h5	5	4'hD	13
4'h6	6	4'hE	14
4'h7	7	4'hF	15

PWMP – PWM output polarity
0 = Active high
1 = Active low

FPWM[1:0] – PWM frequency

FPWM[1:0]	PWM Frequency
0	Frame frequency x 2
1	Frame frequency x 4
2	Frame frequency x 8
3	Frame frequency x 16

6.2.40 D0h – Positive Gamma Curve for Red

Mnemonic RGAMMAP

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	PKP1[2:0]			-	PKP0[2:0]			00h
2	-	PKP3[2:0]			-	PKP2[2:0]			00h
3	-	PKP5[2:0]			-	PKP4[2:0]			00h
4	-	PRP1[2:0]			-	PRP0[2:0]			00h
5	-	-	-	VRP0[4:0]					00h
6	-	-	-	VRP1[4:0]					00h
7	-	PFP1[2:0]			-	PFP0[2:0]			00h
8	-	PFP3[2:0]			-	PFP2[2:0]			00h
9	-	-	-	-	-	PMP[2:0]			00h

Description

PKP0-5[2:0] – Gamma fine-adjustment register for positive polarity

PRP0-1[2:0] – Gamma gradient-adjustment register for positive polarity

VRP0-1[3:0] – Gamma amplitude-adjustment register for positive polarity

PFP0-3[2:0] – Gamma fine adjustment register bits for positive polarity

PMP[2:0] – Gamma fine adjustment register bits for positive polarity

For details, see "Gamma Correction Function" section.

6.2.41 D1h – Negative Gamma Curve for Red

Mnemonic RGAMMAN

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	PKN1[2:0]			-	PKN0[2:0]			00h
2	-	PKN3[2:0]			-	PKN2[2:0]			00h
3	-	PKN5[2:0]			-	PKN4[2:0]			00h
4	-	PRN1[2:0]			-	PRN0[2:0]			00h
5	-	-	-	VRN0[4:0]					00h
6	-	-	-	VRN1[4:0]					00h
7	-	PFN1[2:0]			-	PFN0[2:0]			00h
8	-	PFN3[2:0]			-	PFN2[2:0]			00h
9	-	-	-	-	-	PMN[2:0]			00h

Description

PKN0-5[2:0] – Gamma fine-adjustment register for negative polarity

PRN0-1[2:0] – Gamma gradient-adjustment register for negative polarity

VRN0-1[3:0] – Gamma amplitude-adjustment register for negative polarity

PFN0-3[2:0] – Gamma fine adjustment register bits for negative polarity

PMN[2:0] – Gamma fine adjustment register bits for negative polarity

For details, see "Gamma Correction Function" section.

6.2.42 D2h – Positive Gamma Curve for Green

Mnemonic GGAMMAP

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	PKP1[2:0]			-	PKP0[2:0]			00h
2	-	PKP3[2:0]			-	PKP2[2:0]			00h
3	-	PKP5[2:0]			-	PKP4[2:0]			00h
4	-	PRP1[2:0]			-	PRP0[2:0]			00h
5	-	-	-	VRP0[4:0]					00h
6	-	-	-	VRP1[4:0]					00h
7	-	PFP1[2:0]			-	PFP0[2:0]			00h
8	-	PFP3[2:0]			-	PFP2[2:0]			00h
9	-	-	-	-	-	PMP[2:0]			00h

Description

PKP0-5[2:0] – Gamma fine-adjustment register for positive polarity

PRP0-1[2:0] – Gamma gradient-adjustment register for positive polarity

VRP0-1[3:0] – Gamma amplitude-adjustment register for positive polarity

PFP0-3[2:0] – Gamma fine adjustment register bits for positive polarity

PMP[2:0] – Gamma fine adjustment register bits for positive polarity

For details, see "Gamma Correction Function" section.

6.2.43 D3h – Negative Gamma Curve for Green

Mnemonic GGAMMAN

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	PKN1[2:0]			-	PKN0[2:0]			00h
2	-	PKN3[2:0]			-	PKN2[2:0]			00h
3	-	PKN5[2:0]			-	PKN4[2:0]			00h
4	-	PRN1[2:0]			-	PRN0[2:0]			00h
5	-	-	-	VRN0[4:0]					00h
6	-	-	-	VRN1[4:0]					00h
7	-	PFN1[2:0]			-	PFN0[2:0]			00h
8	-	PFN3[2:0]			-	PFN2[2:0]			00h
9	-	-	-	-	-	PMN[2:0]			00h

Description

PKN0-5[2:0] – Gamma fine-adjustment register for negative polarity

PRN0-1[2:0] – Gamma gradient-adjustment register for negative polarity

VRN0-1[3:0] – Gamma amplitude-adjustment register for negative polarity

PFN0-3[2:0] – Gamma fine adjustment register bits for negative polarity

PMN[2:0] – Gamma fine adjustment register bits for negative polarity

For details, see "Gamma Correction Function" section.

6.2.44 D4h – Positive Gamma Curve for Blue

Mnemonic BGAMMAP

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	PKP1[2:0]			-	PKP0[2:0]			00h
2	-	PKP3[2:0]			-	PKP2[2:0]			00h
3	-	PKP5[2:0]			-	PKP4[2:0]			00h
4	-	PRP1[2:0]			-	PRP0[2:0]			00h
5	-	-	-	VRP0[4:0]					00h
6	-	-	-	VRP1[4:0]					00h
7	-	PFP1[2:0]			-	PFP0[2:0]			00h
8	-	PFP3[2:0]			-	PFP2[2:0]			00h
9	-	-	-	-	-	PMP[2:0]			00h

Description

PKP0-5[2:0] – Gamma fine-adjustment register for positive polarity

PRP0-1[2:0] – Gamma gradient-adjustment register for positive polarity

VRP0-1[3:0] – Gamma amplitude-adjustment register for positive polarity

PFP0-3[2:0] – Gamma fine adjustment register bits for positive polarity

PMP[2:0] – Gamma fine adjustment register bits for positive polarity

For details, see "Gamma Correction Function" section.

6.2.45 D5h – Negative Gamma Curve for Blue

Mnemonic BGAMMAN

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	-	PKN1[2:0]			-	PKN0[2:0]			00h
2	-	PKNP3[2:0]			-	PKN2[2:0]			00h
3	-	PKN5[2:0]			-	PKN4[2:0]			00h
4	-	PRN1[2:0]			-	PRN0[2:0]			00h
5	-	-	-	VRN0[4:0]					00h
6	-	-	-	VRN1[4:0]					00h
7	-	PFN1[2:0]			-	PFN0[2:0]			00h
8	-	PFN3[2:0]			-	PFN2[2:0]			00h
9	-	-	-	-	-	PMN[2:0]			00h

Description

PKN0-5[2:0] – Gamma fine-adjustment register for negative polarity

PRN0-1[2:0] – Gamma gradient-adjustment register for negative polarity

VRN0-1[3:0] – Gamma amplitude-adjustment register for negative polarity

PFN0-3[2:0] – Gamma fine adjustment register bits for negative polarity

PMN[2:0] – Gamma fine adjustment register bits for negative polarity

For details, see "Gamma Correction Function" section.

6.2.46 F0h – Test Register 1

Mnemonic TEST1

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	HIZ	-	-	-	-	-	TPOL[1:0]		00h

Description

6.2.47 F8h – OTP 1

Mnemonic OTP1

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	PTM[1:0]		-	-	PRD	PWE	VPP	PPROG	00h
2	APRG	-	-	-	-	-	PA[1:0]		00h
3	PDIN[7:0]								00h

Description

PPROG : Program mode enable.

VPP : Power switch control for the VPP pin of the embedded OTP. When VPP = "1", the internal VPP is set to 7.5V; otherwise it is set to 1.8V. This VPP register parameter is different from VPP in PAD.

PWE : Write enable.

PRD: Pin for power-on rest.

PTM[1:0]: Pins for enabling test mode.

PA[1:0] : Address input. This selects one of four banks of the OTP as bellows.

PA[1:0]	Write Data Input	Write OPT Cell
2'h0	PDIN[6:0]	Cell[6:0]
2'h1	PDIN[6:0]	Cell[14:8]
2'h2	PDIN[6:0]	Cell[22:16]
2'h3	PDIN[6:0]	Cell[30:24]

APRG : Select the method of write operation as bellows.

APRG	**Write Operation**
1'h0	Write address is PA.
1'h0	Write address is auto select address.

PDIN[7:0] : Data input.

More details can be referenced at 5.8 OTP Control section.

6.2.48 F9h – OTP 2

Mnemonic OTP2

Type Read/Write

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	VCMSEL		-	-	-	-	RA[1:0]		00h

Description

RA[1:0] : Read address input. This selects one of four banks of the OTP as bellows.

RA[1:0]	Read Data Input	Read OPT Cell
2'h0	PDOUT [6:0]	Cell[6:0]
2'h1	PDOUT [6:0]	Cell[14:8]
2'h2	PDOUT [6:0]	Cell[22:16]
2'h3	PDOUT[6:0]	Cell[30:24]

VCMSEL[1:0] : Sets Vcom level from either the register C5h or the OTP as bellows.

VCMSEL[1:0]	**Vcom Level adjustment**
2'h0	VCM[6:0] of the register C5h
2'h1	OTP data at first if OTP has data. Otherwise,VCM[6:0] of the register C5h
2'h2	OTP data selected by RA[1:0]
2'h3	OTP data selected by RA[1:0]

More details can be referenced at 5.8 OTP Control section.

6.2.49 FAh – OTP 3

Mnemonic OTP3

Type Read

Parameters

No.	b7	b6	b5	b4	b3	b2	b1	b0	Reset
1	PDOUT[7:0]								xxh
2	PDOUT[15:8]								xxh
3	PDOUT[23:16]								xxh
4	PDOUT[31:24]								xxh

Description

PDOUT[31:0] : Read OTP Data

More details can be referenced at 5.8 OTP Control section.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 12. Absolute Maximum Ratings

Item	Symbol	Unit	Min	Max	Notes
Power supply voltage (1)	VDD	V	-0.3	3.0	1
Power supply voltage (2)	VCC, IOVCC – GND	V	-0.3	4.5	1, 2
Power supply voltage (3)	VCI – GND	V	-0.3	4.5	1, 2
Power supply voltage (4)	DDVDH	V	-0.3	8.0	1, 3, 4
Power supply voltage (5)	VGND – VCL	V	-0.3	4.5	1
Power supply voltage (6)	VGH – AGND	V	-0.3	18	1, 5
Power supply voltage (7)	AGND – VGL (or LVGL)	V	-0.3	18	1, 6
Input voltage	Vt	V	-0.3	IOVCC+0.3	1
Operating temperature	Topr	°C	-40	85	1, 7
Storage temperature	Tstg	°C	-55	125	1

Notes:

1. If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI at a condition within the electrical characteristics for normal operation. Exposure to a condition not within the electrical characteristics may affect device reliability.
2. Make sure (High) VCI ≥ GND (Low). (High) IOVCC ≥ GND (Low). (High) VCC ≥ GND (Low).
3. Make sure (High) DDVDH ≥ AGND (Low).
4. Make sure (High) DDVDH ≥ VCI (Low).
5. Make sure (High) VGH ≥ GND (Low).
6. Make sure (High) GND ≥ VGL (or LVGL) (Low).
7. The DC/AC characteristics of die and wafer products is guaranteed at 85°C.
8. Make sure (High) VGH – VGL (or LVGL) < 31V (operation maximum).

7.2 Power Supply Specifications

Table 13. Power Supply Specifications

No.	Item		LG4573
1	TFT source lines		1440 pins (480 x RGB)
2	GIP control signals		FW_L, BW_L, GPWR1_L, GPWR2_L, GCLK4_L, GCLK3_L, GCLK2_L, GCLK1_L, GVST1_L, GVST2_L, FW_R, BW_R, GPWR1_R, GPWR2_R, GCLK4_R, GCLK3_R, GCLK2_R, GCLK1_R, GVST1_R, GVST2_R,
3	Input voltages	IOVCC	1.65 to 3.30 V
		VCC	2.60 to 3.30 V
		VCI	2.60 to 3.30 V
4	Internal logic voltages	VDD	1.62 to 1.98 V
5	Internal step-up circuits	DDVDH	VCI x (1.47 to 2.45)
		DDVDL	-DDVDH
		VGH	DDVDH x 2, DDVDH x 2 + VCI, DDVDH x 3
		VGL	-(DDVDH x 2), -(DDVDH x 2 + VCI), -(DDVDH x 3)
		LVGL	VGL - VCI
		VCL	VCI x -1

7.3 DC Characteristics

Table 14. DC Characteristics

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
Input high voltage	V_{IH}	V	IOVCC = 1.65~3.3	0.8*IOVCC	-	IOVCC	
Input low voltage	V_{IL}	V	IOVCC = 1.65~3.3	-0.3	-	0.2*IOVCC	
Output high voltage (1) (DB17-0, SDO)	V_{OH1}	V	IOVCC = 1.65~3.3 IOH = 0.1mA	0.8*IOVCC	-	-	
Output low voltage (1) (DB17-0, SDO)	V_{OL1}	V	IOVCC = 1.65~3.3 IOL = 0.1mA	-	-	0.2*IOVCC	
I/O leakage current	I_{Li}	µA	Vin = 0~IOVCC	-1	-	1	
Current consumption during standby mode: (IOVCC - GND) + (VCC - GND)	I_{ST}	µA	IOVCC = VCC = VCI = 2.8V Ta = 25°C	-	1.4	10	

7.4 AC Characteristics

7.4.1 Serial Peripheral Interface Characteristics

Table 15. (Condition: IOVCC = 1.65 to 3.30V, VCC = 2.60 to 3.30V)

Item		Symbol	Unit	Min	Typ	Max
Serial clock cycle time	Write (received)	tSCYC	ns	20	-	-
	Read (transmitted)			100	-	-
Serial clock "High" level pulse width	Write (received)	tSCH	ns	10	-	-
	Read (transmitted)			50	-	-
Serial clock "Low" level pulse width	Write (received)	tSCL	ns	10	-	-
	Read (transmitted)			50	-	-
Serial clock rise/fall time		tscr, tscf	ns	-	-	20
Chip select setup time		tCSU	ns	20	-	-
Chip select hold time		tCH	ns	10	-	-
Serial input data setup time		tSISU	ns	5	-	-
Serial input data hold time		tSIH	ns	10	-	-
Serial output data setup time		tSOD	ns	80	-	150
Serial output data hold time		tSOH	ns	-	-	80

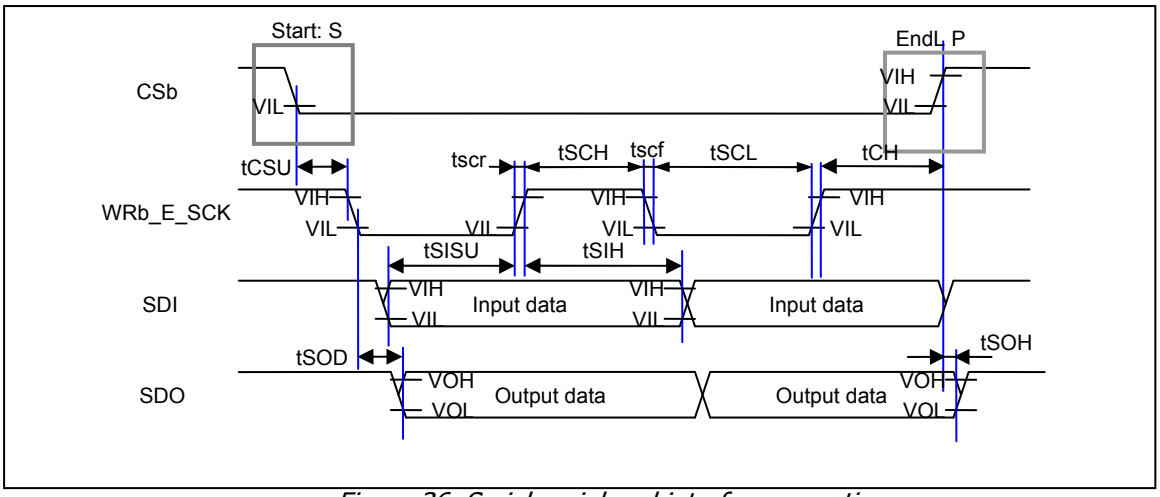


Figure 36. Serial peripheral interface operation

7.4.2 Reset Characteristics

Table 16. (Condition: IOVCC = 1.65 to 3.30V, VCC = 2.60 to 3.30V)

Item	Symbol	Unit	Min	Typ	Max
Reset "Low" level width	tRES	ms	1	-	-
Reset rise time	trRES	µs	-	-	10

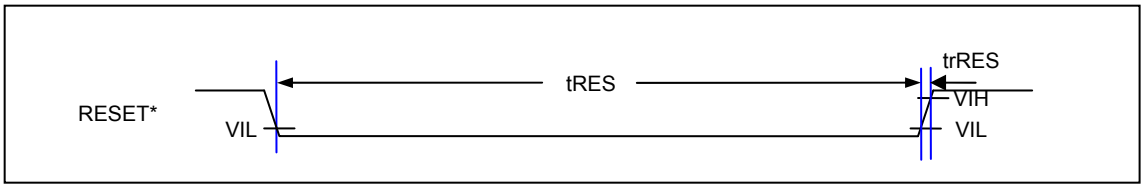


Figure 37. Reset operation

7.4.3 RGB Interface Timing Characteristics

Table 17. (24/18/16-bit I/F, IOVCC = 1.65 to 3.30V, VCC = 2.60 to 3.30V)

Item	Symbol	Unit	Min	Typ	Max
VSYNC/HSYNC setup time	tSYNCS	ns	5	-	-
VSYNC/HSYNC hold time	tSYNCH	ns	5	-	-
DE setup time	tENS	ns	5	-	-
DE hold time	tENH	ns	5	-	-
PCLK "Low" level pulse width	PWDL	ns	10	-	-
PCLK "High" level pulse width	PWDH	ns	10	-	-
PCLK cycle time	tCYCD	ns	20	-	-
Data setup time	tPDS	ns	6	-	-
Date hold time	tPDH	ns	6	-	-
PCLK, VSYNC, HSYNC, DE rise/fall time	trgbr, trgbf	ns	-	-	13

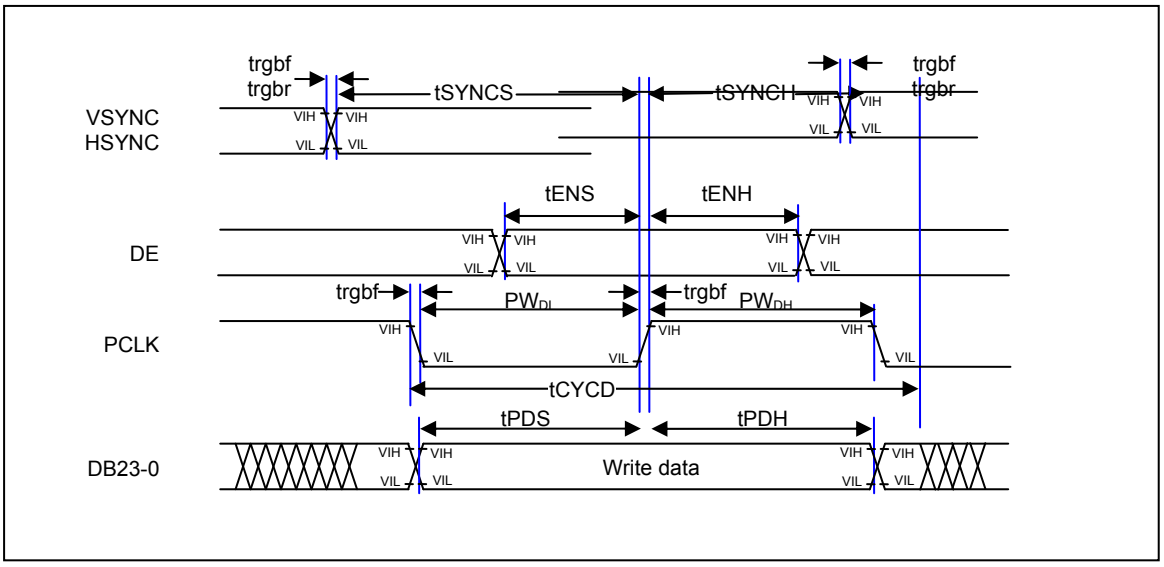


Figure 38. RGB interface

8 Reference Applications

8.1 Configuration of Power Supply Circuit

Figure 39 is one of the configurations of power supply circuits to generate liquid crystal panel drive levels.

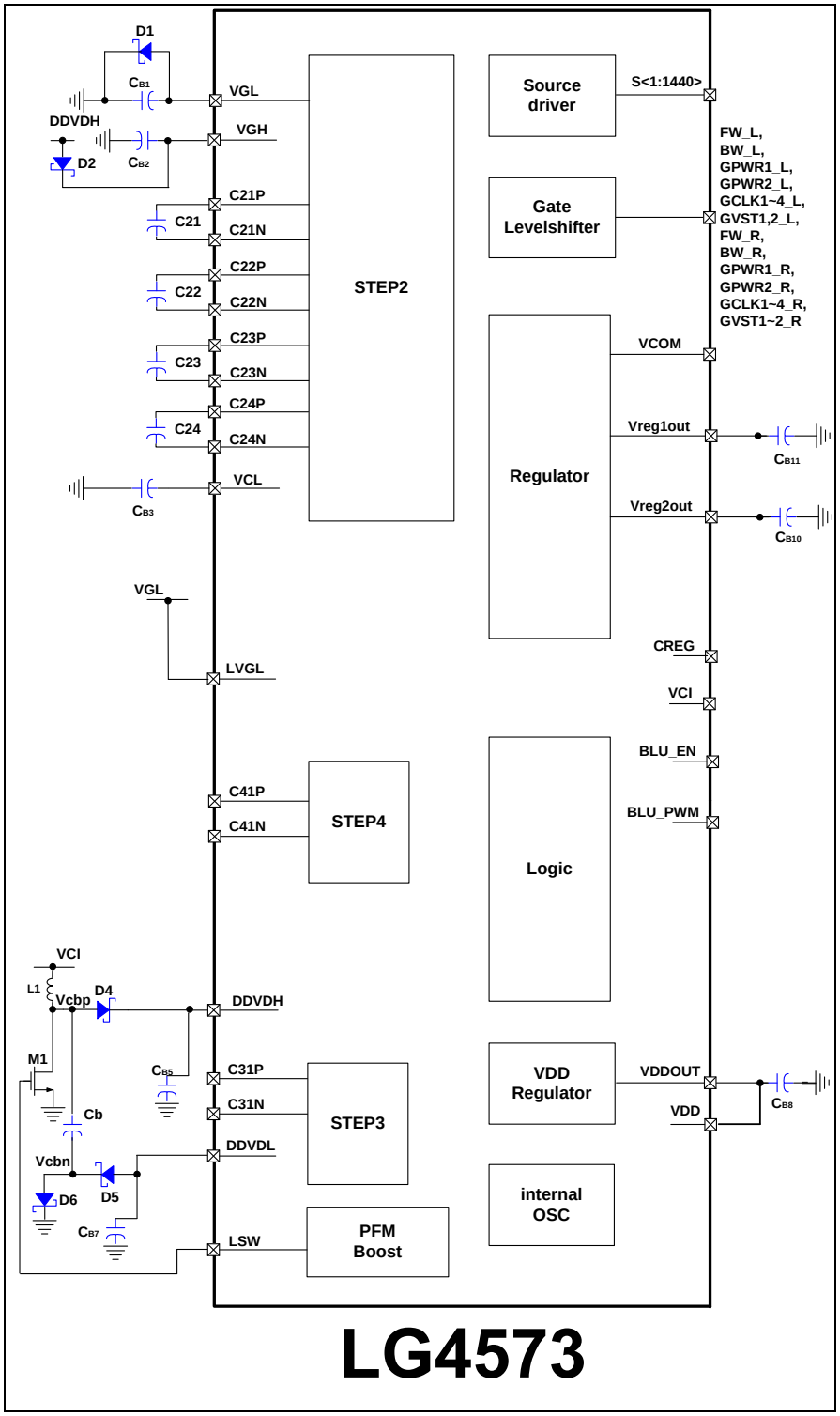
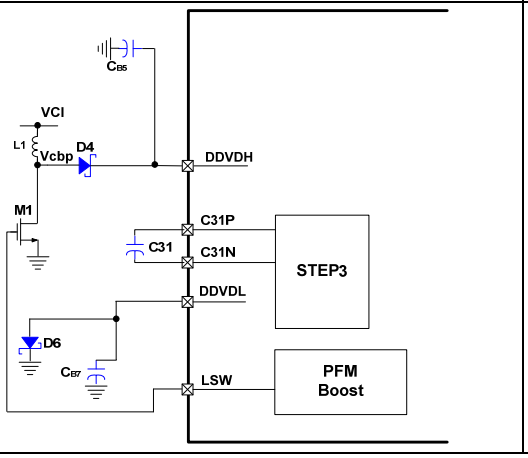
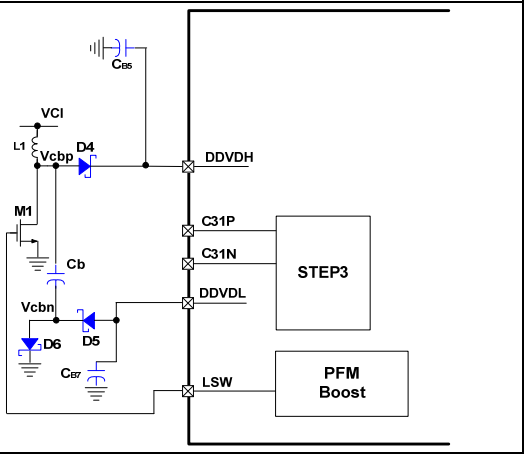


Figure 39. One example of application circuits for the STMODE=7 case.

Some application circuitries in the above power supply circuit configuration should be changed according to the below setting modes. Please see the followings.

STMODE[2:0] = 6 (PFM – Step-up 3)	STMODE[2:0] = 7 (PFM – Diode Inverting)
	

Under some abnormal situations, such as no power-on reset in the system or as un-kept power on/off sequences or as something else, external MOS switch should be protected by inserting high pass filter between LSW and MOS gate node of n1 in the following figure. The HPF circuits in the following figure is a recommended one. The connection of 1uF capacitance near to inductor and/or MOS switch could help to reduce the noises from VCI power node. But they are all optionals for special cases.

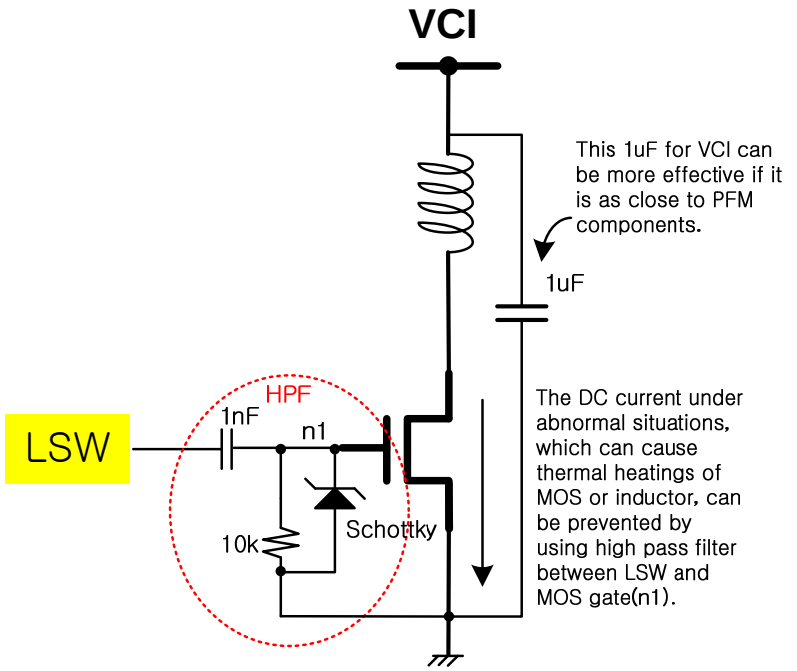


Figure 40. HPF (High Pass Filter) application circuits for protecting external MOS Tr.

Specification of External Elements Connected to LG4573 Power Supply

The following tables show specifications of external element connected to the LG4573's power supply circuit.

Table 18. Capacitor

Capacity	Recommended voltage	Pin connection
1uF (B characteristics)	6V	C24, CB3, CB10**, CB11**
	10V	C21, C22, C23, C31*
	25V	CB1, CB2
1.0uF	10V	CB5, CB7
1.0uF	6V	CB8
0.47uF	10V	Cb*

Note: Some components* are optional according to the specific usages and some components** would be eliminated after reliability test.

Table 19. Schottky diode

Feature	Pin connection
VF < 0.4V/20mA at 25°C , VR>30V	D1**, D2, D4, D5*, D6**

Note: Some components* are optional according to the specific usages and some components** would be eliminated after reliability test.

Table 20. N-ch MOSFET

Feature	Specification
M1	IDSS<1μA at VDS>16V, VGS=0V, and 25°C Ron<1.25Ω at VGS=2.5V and ID=300mA ton<30ns(Typ.) toff<30ns(Typ.)

Note: Recommended N-ch MOSFETs:

1. Si1012R/X (Vishay Siliconix)
2. RUM003N02 (ROHM)

Table 21. Inductor for Booster

Feature	Inductance Specification
L1	Inductance value = 4.7uH Inductance tolerance < ± 20% DC resistance (± 30%) < 0.24ohm Max. rated current > 145mA at saturation Max. rated current > 470mA at temperature rise

Note: Recommended inductor components:

1. CBMF1608T4R7M (TAIYO YUDEN)
2. VLF3010AT-4R7MR70 (TDK)

9 History of Revision

Ver.	Date	Note
1.1.5	2010.09.03	- The chip thickness is changed from 300um to 250um. The others are same with LG4573 V1.1.5.