Kria SOM Carrier Card

Design Guide

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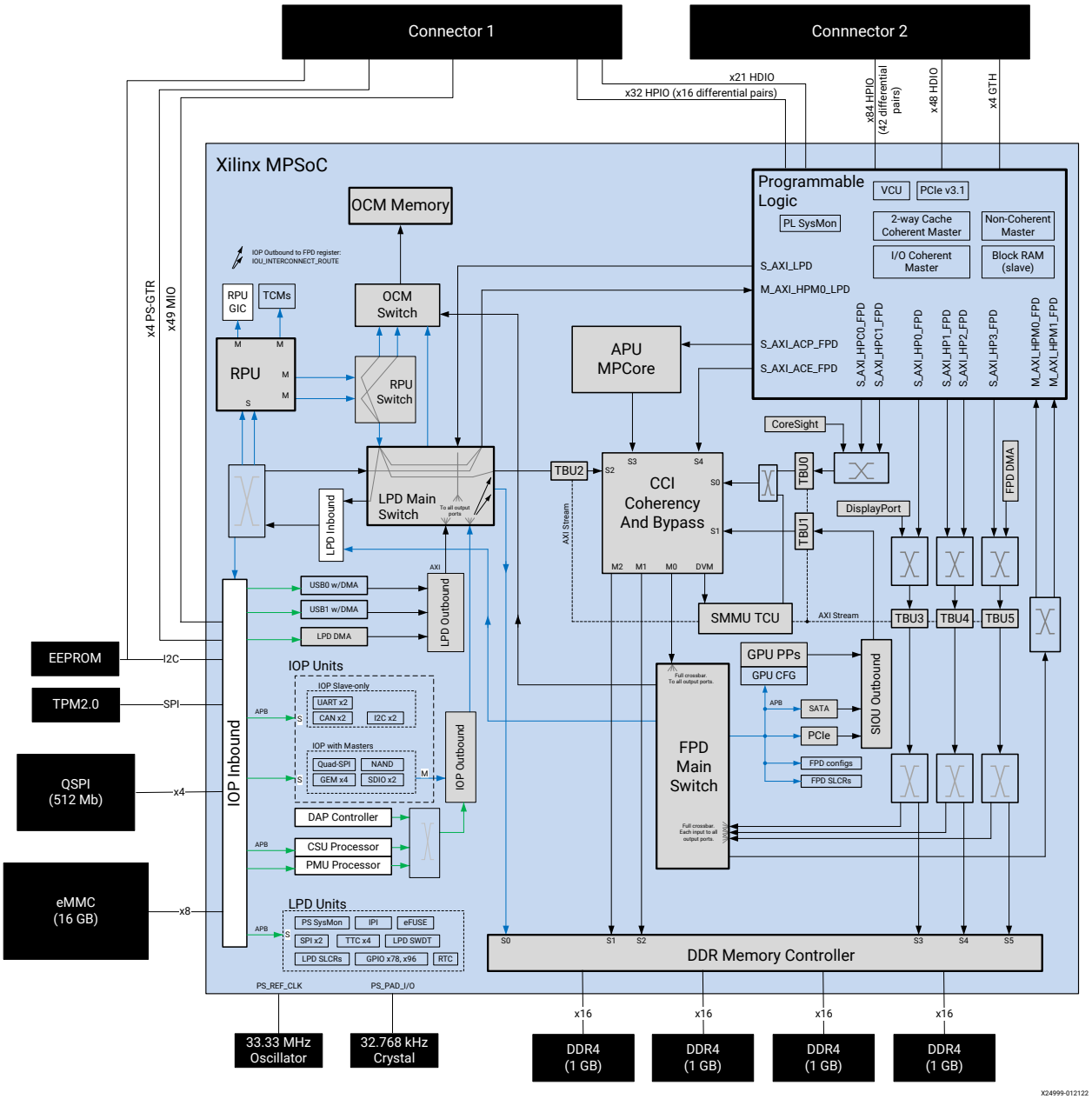
Chapter 1

Introduction

The purpose of this design guide is to support hardware, system, and firmware engineers implementing a product using a Xilinx® Kria™ SOM. The guide outlines electrical, mechanical, firmware, and power-on configuration design considerations that must be addressed as part of designing a Xilinx SOM compatible carrier card. The document is not intended to be self-contained, meaning that there are references to other Xilinx product documentation to help the reader find more detailed technical information available in corresponding technical reference manuals, software design guides, and thermal design guides. The Kria K26 SOM is used as an example throughout the guide and is shown in the following block diagram.

Figure 1: **K26 SOM Block Diagram**



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Chapter 2

Electrical Design Considerations

This chapter describes the electrical interface details needed to design your carrier card to mate with the Kria™ K26 SOM. The electrical interface design guidelines include the SOM connector details and signal names, signal routing guidelines, and power supply design.

SOM Connector Overview

The K26 SOM uses two 240-pin connectors to provide electrical connectivity between the SOM and the carrier card. These two connectors are referred to as SOM240_1 and SOM240_2.

The SOM240_1 and SOM240_2 connectors use the Samtec 0.635 mm AcceleRate HD high-density 4-row, 60 position connector set. The part number for the socket (ADF6-60-03.5-L-4-2-A) is used on the bottom side of the SOM. The part number for the terminal (ADM6-60-01.5-L-4-2-A) is for use on the carrier card. The SOM240_1 and SOM240_2 connectors provide support for following interfaces.

- Control and status signals
- Multiplexed I/O (MIO) bank
- PS-GTR high-speed serial transceiver signals
- High-performance I/O (HPIO) bank signals
- High-density I/O (HDIO) bank signals
- GTH high-speed serial transceiver signals
- Power system

Signal Naming Conventions

For signal to connector mapping in text format, see the relevant XDC and trace delay files. These files provide the Zynq® UltraScale+™ MPSoC constraints and package pin name to SOM240_x mapping. The SOM240 connectors adopt the naming conventions outlined in the following table.

Table 1: **SOM240 Signal Naming Conventions**

Signal	Description
Module (M)	The SOM, in this case the K26 SOM.
Carrier card (C)	The board that the SOM is plugged into is called the carrier card.
C2M	Signal names with `C2M` indicate that the signal is driven by the carrier card and received by the SOM.
M2C	Signal names with `M2C` indicate that the signal is driven by the SOM and received by the carrier card.
_P	The postfix `_P` on differential signal pairs indicates the positive component of a differential signal.
_N	The postfix `_N` on differential signal pairs indicates the negative component of a differential signal.
_L	The postfix `_L` on a single-ended signal indicates an active-Low signal. This is used for the connector pinouts only. The postfix _B is also used to indicate an active-Low signal.

Table 2: **Legend for Connector Pinouts**

Example	SOM240 Connector	Function
GND	Both SOM240_1 and SOM240_2	Ground pins
VCC_SOM	Both SOM240_1 and SOM240_2	Power connection pins
MIO35	SOM240_1	MIO 501 bank pins
MIO58	SOM240_1	MIO 502 bank pins
JTAG_TMS_C2M	SOM240_1	Configuration and control pins
GTR_DP1_M2C_P	SOM240_1	PS-GTR transceiver pins
HPA04_P	SOM240_1	HPA pins
HDA00_CC	SOM240_1	HDA pins
HPB15_CC_P	SOM240_2	HPB pins
HPC07_P	SOM240_2	HPC pins
HDB12	SOM240_2	HDB pins
HDC00_CC	SOM240_2	HDC pins
GTH_DP2_C2M_P	SOM240_2	GTH transceiver pins

Refer to the *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide* (UG1075) for more information on pin types.

Table 3: **Legend for Pin Types**

Example	Definition
GC	Global clock
HDGC	Global clock
VRP	DCI voltage reference resistor
QBC	Byte lane clock
DBC	Byte lane clock
PERSTN	Default reset pin locations for integrated block for PCI Express®
PU18_10	10.0 KΩ pull-up resistor to VCC_PS_1V80
PU18_2p2	2.21 KΩ pull-up resistor to VCC_PS_1V80
PU18_4p7	4.7 KΩ pull-up resistor to VCC_PS_1V80
PU50	10.0 KΩ pull-up resistor to VCC_5V0
PD50	49.9 KΩ pull-down resistor to VCC_5V0
AC01UF	AC coupled with 0.01 µF capacitor on the SOM

SOM240_1 Connector Pinout

The SOM240_1 connector provides access to two MIO banks (MIO501, MIO502), HPIO bank 66 (HPA), HDIO bank 45 (HDA), and the PS-GTR transceivers (MIO505). It also provides sideband signals for configuration and operation of the board. For additional pin definitions see the K26 SOM XDC file.

Table 4: **SOM240_1 Connector Pinout**

Connector Row/Pin Number	A	B	C	D
1	VCC_BATT	HPA05_CC_P	GND	VCCO_HPA
2	GND	HPA05_CC_N	GND	VCCO_HPA
3	HPA06_P	GND	HPA00_CC_P	GND
4	HPA06_N	HPA04_P	HPA00_CC_N	HPA02_P
5	GND	HPA04_N	GND	HPA02_N
6	HPA_CLK0_P	GND	HPA03_P	GND
7	HPA_CLK0_N	HPA07_P	HPA03_N	HPA01_P
8	GND	HPA07_N	GND	HPA01_N
9	HPA12_P	GND	HPA08_P	GND
10	HPA12_N	HPA11_P	HPA08_N	HPA09_P
11	GND	HPA11_N	GND	HPA09_N
12	HPA13_P	GND	HPA10_CC_P	GND
13	HPA13_N	VCCO_HDA	HPA10_CC_N	HPA14_P

Table 4: **SOM240_1 Connector Pinout** *(cont'd)*

Connector Row/Pin Number	A	B	C	D
14	GND	VCCO_HDA	GND	HPA14_N
15	HDA09	GND	PS_POR_L	GND
16	HDA10	HDA03	PS_SRST_C2M_L	HDA00_CC
17	HDA11	HDA04	GND	HDA01
18	GND	HDA05	HDA06	HDA02
19	VCCOEN_PS_M2C	GND	HDA07	GND
20	VCCOEN_PL_M2C	HDA15	HDA08_CC	HDA12
21	GND	HDA16_CC	GND	HDA13
22	JTAG_TMS_C2M	HDA17	HDA18	HDA14
23	JTAG_TDO_M2C	GND	HDA19	GND
24	JTAG_TDI_C2M	PS_ERROR_OUT_M2C	HDA20	PWRGD_FPD_M2C
25	JTAG_TCK_C2M	PS_ERROR_STATUS_M2C	GND	PWRGD_LPD_M2C
26	GND	PWROFF_C2M_L	MIO24_I2C_SCK	PWRGD_PL_M2C
27	MODE0_C2M	GND	MIO25_I2C_SDA	GND
28	MODE1_C2M	MIO35_WD_OUT	MIO12_FWUEN_C2M_L	MIO26
29	MODE2_C2M	MIO36	GND	MIO27
30	MODE3_C2M	MIO37	MIO29	MIO28
31	Reserved	GND	MIO30	GND
32	Reserved	MIO38	MIO31_SHUTDOWN	MIO44
33	GND	MIO39	GND	MIO45
34	MIO41	MIO40	MIO47	MIO46
35	MIO42	GND	MIO48	GND
36	MIO43	MIO50	MIO49	MIO52
37	GND	MIO51	GND	MIO53
38	MIO61	Reserved	MIO55	MIO54
39	MIO62	GND	MIO56	GND
40	MIO63	MIO58	MIO57	MIO64
41	GND	MIO59	GND	MIO65
42	MIO73	MIO60	MIO67	MIO66
43	MIO74	GND	MIO68	GND
44	MIO75	MIO70	MIO69	MIO76
45	GND	MIO71	Reserved	MIO77
46	GND	MIO72	GND	Reserved
47	GTR_DP1_M2C_P	GND	GTR_REFCLK0_C2M_P	GND
48	GTR_DP1_M2C_N	GND	GTR_REFCLK0_C2M_N	GND
49	GND	GTR_REFCLK1_C2M_P	GND	GTR_DP3_C2M_P
50	GND	GTR_REFCLK1_C2M_N	GND	GTR_DP3_C2M_N

Table 4: **SOM240_1 Connector Pinout** *(cont'd)*

Connector Row/Pin Number	A	B	C	D
51	GTR_REFCLK3_C2M_P	GND	GTR_DP3_M2C_P	GND
52	GTR_REFCLK3_C2M_N	GND	GTR_DP3_M2C_N	GND
53	GND	GTR_DP2_C2M_P	GND	GTR_REFCLK2_C2M_P
54	GND	GTR_DP2_C2M_N	GND	GTR_REFCLK2_C2M_N
55	GTR_DP0_C2M_P	GND	GTR_DP1_C2M_P	GND
56	GTR_DP0_C2M_N	GND	GTR_DP1_C2M_N	GND
57	GND	GTR_DP0_M2C_P	GND	GTR_DP2_M2C_P
58	GND	GTR_DP0_M2C_N	GND	GTR_DP2_M2C_N
59	VCC_SOM	GND	VCC_SOM	GND
60	VCC_SOM	VCC_SOM	VCC_SOM	VCC_SOM

SOM240_1 Signal Names and Descriptions

See the *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide* (UG1075) for further pin descriptions.

Table 5: **SOM240_1 Signal Pins**

Pin Number	Pin Type	Signal Name	Signal Description
Connector Row A			
A1		VCC_BATT	PS BBRAM and real-time clock (RTC) supply voltage, requires external battery. Connect to GND when battery is not used.
A2		GND	Ground, connect to carrier card ground plane
A3		HPA06_P	HPIO on bank 66
A4		HPA06_N	HPIO on bank 66
A5		GND	Ground, connect to carrier card ground plane
A6	GC	HPA_CLK0_P	HPIO global clock pin on bank 66
A7	GC	HPA_CLK0_N	HPIO global clock pin on bank 66
A8		GND	Ground, connect to carrier card ground plane
A9		HPA12_P	HPIO on bank 66
A10		HPA12_N	HPIO on bank 66
A11		GND	Ground, connect to carrier card ground plane
A12	QBC	HPA13_P	HPIO on bank 66
A13	QBC	HPA13_N	HPIO on bank 66
A14		GND	Ground, connect to carrier card ground plane
A15	HDGC	HDA09	HDIO on bank 45
A16		HDA10	HDIO on bank 45

Table 5: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
A17		HDA11	HDIO on bank 45
A18		GND	Ground, connect to carrier card ground plane
A19	PD50	VCCOEN_PS_M2C	Indication to turn on power for PS I/O peripherals on the carrier card
A20	PD50	VCCOEN_PL_M2C	Indication to turn on power for PL /IO peripherals on the carrier card
A21		GND	Ground, connect to carrier card ground plane
A22	PU18_4p7	JTAG_TMS_C2M	JTAG mode select
A23	PU18_4p7	JTAG_TDO_M2C	JTAG data out
A24	PU18_4p7	JTAG_TDI_C2M	JTAG data in
A25	PU18_4p7	JTAG_TCK_C2M	JTAG clock
A26		GND	Ground, connect to carrier card ground plane
A27	PU18_4p7	MODE0_C2M	PS mode bit 0
A28	PU18_4p7	MODE1_C2M	PS mode bit 1
A29	PU18_4p7	MODE2_C2M	PS mode bit 2
A30	PU18_4p7	MODE3_C2M	PS mode bit 3
A31		Reserved	No connect on the SOM
A32		Reserved	No connect on the SOM
A33		GND	Ground, connect to carrier card ground plane
A34		MIO41	PS MIO signal on bank 501
A35		MIO42	PS MIO signal on bank 501
A36		MIO43	PS MIO signal on bank 501
A37		GND	Ground, connect to carrier card ground plane
A38		MIO61	PS MIO signal on bank 502
A39		MIO62	PS MIO signal on bank 502
A40		MIO63	PS MIO signal on bank 502
A41		GND	Ground, connect to carrier card ground plane
A42		MIO73	PS MIO signal on bank 502
A43		MIO74	PS MIO signal on bank 502
A44		MIO75	PS MIO signal on bank 502
A45		GND	Ground, connect to carrier card ground plane
A46		GND	Ground, connect to carrier card ground plane
A47		GTR_DP1_M2C_P	PS-GTR lane 1 TX, bank 505
A48		GTR_DP1_M2C_N	PS-GTR lane 1 TX, bank 505
A49		GND	Ground, connect to carrier card ground plane
A50		GND	Ground, connect to carrier card ground plane
A51	AC01UF	GTR_REFCLK3_C2M_P	PS-GTR REFCLK3 input, bank 505
A52	AC01UF	GTR_REFCLK3_C2M_N	PS-GTR REFCLK3 input, bank 505
A53		GND	Ground, connect to carrier card ground plane

Table 5: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
A54		GND	Ground, connect to carrier card ground plane
A55		GTR_DP0_C2M_P	PS-GTR lane 0 RX, bank 505
A56		GTR_DP0_C2M_N	PS-GTR lane 0 RX, bank 505
A57		GND	Ground, connect to carrier card ground plane
A58		GND	Ground, connect to carrier card ground plane
A59		VCC_SOM	SOM main supply voltage, +5V
A60		VCC_SOM	SOM main supply voltage, +5V
Connector Row B			
B1	QBC	HPA05_CC_P	HPIO clock-capable pin on bank 66
B2	QBC	HPA05_CC_N	HPIO clock-capable pin on bank 66
B3		GND	Ground, connect to carrier card ground plane
B4		HPA04_P	HPIO on bank 66
B5		HPA04_N	HPIO on bank 66
B6		GND	Ground, connect to carrier card ground plane
B7		HPA07_P	HPIO on bank 66
B8		HPA07_N	HPIO on bank 66
B9		GND	Ground, connect to carrier card ground plane
B10	GC	HPA11_P	HPIO on bank 66
B11	GC	HPA11_N	HPIO on bank 66
B12		GND	Ground, connect to carrier card ground plane
B13		VCCO_HDA	HDA I/O voltage rail, 1.2V to 3.3V
B14		VCCO_HDA	HDA I/O voltage rail, 1.2V to 3.3V
B15		GND	Ground, connect to carrier card ground plane
B16		HDA03	HDIO on bank 45
B17		HDA04	HDIO on bank 45
B18		HDA05	HDIO on bank 45
B19		GND	Ground, connect to carrier card ground plane
B20		HDA15	HDIO on bank 45
B21	HDGC	HDA16_CC	HDIO clock-capable pin on bank 45
B22	HDGC	HDA17	HDIO on bank 45
B23		GND	Ground, connect to carrier card ground plane
B24		PS_ERROR_OUT_M2C	PS error indication from SOM
B25		PS_ERROR_STATUS_M2C	PS error status from SOM
B26	PU50	PWROFF_C2M_L	Control signal to turn off all power rails on the SOM
B27		GND	Ground, connect to carrier card ground plane
B28		MIO35_WD_OUT	PS MIO signal on bank 501. Optional use as PMU output. Default use as PMU watchdog output in the released Kria PetaLinux BSPs.

Table 5: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
B29		MIO36	PS MIO signal on bank 501. Optional use as PMU output. Default use as UART txd in the released Kria PetaLinux BSPs.
B30		MIO37	PS MIO signal on bank 501. Optional use as PMU output. Default use as UART rxd in the released Kria PetaLinux BSPs.
B31		GND	Ground, connect to carrier card ground plane
B32		MIO38	PS MIO signal on bank 501
B33		MIO39	PS MIO signal on bank 501
B34		MIO40	PS MIO signal on bank 501
B35		GND	Ground, connect to carrier card ground plane
B36		MIO50	PS MIO signal on bank 501
B37		MIO51	PS MIO signal on bank 501
B38		Reserved	Not connected to SOM connector
B39		GND	Ground, connect to carrier card ground plane
B40		MIO58	PS MIO signal on bank 502
B41		MIO59	PS MIO signal on bank 502
B42		MIO60	PS MIO signal on bank 502
B43		GND	Ground, connect to carrier card ground plane
B44		MIO70	PS MIO signal on bank 502
B45		MIO71	PS MIO signal on bank 502
B46		MIO72	PS MIO signal on bank 502
B47		GND	Ground, connect to carrier card ground plane
B48		GND	Ground, connect to carrier card ground plane
B49	AC01UF	GTR_REFCLK1_C2M_P	PS-GTR REFCLK1 input, bank 505
B50	AC01UF	GTR_REFCLK1_C2M_N	PS-GTR REFCLK1 input, bank 505
B51		GND	Ground, connect to carrier card ground plane
B52		GND	Ground, connect to carrier card ground plane
B53		GTR_DP2_C2M_P	PS-GTR lane 2 RX, bank 505
B54		GTR_DP2_C2M_N	PS-GTR lane 2 RX, bank 505
B55		GND	Ground, connect to carrier card ground plane
B56		GND	Ground, connect to carrier card ground plane
B57		GTR_DP0_M2C_P	PS-GTR lane 0 TX, bank 505
B58		GTR_DP0_M2C_N	PS-GTR lane 0 TX, bank 505
B59		GND	Ground, connect to carrier card ground plane
B60		VCC_SOM	SOM main supply voltage, +5V
Connector Row C			
C1		GND	Ground, connect to carrier card ground plane
C2		GND	Ground, connect to carrier card ground plane
C3	DBC	HPA00_CC_P	HPIO clock-capable pin on bank 66
C4	DBC	HPA00_CC_N	HPIO clock-capable pin on bank 66

Table 5: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
C5		GND	Ground, connect to carrier card ground plane
C6	DBC	HPA03_P	HPIO on bank 66
C7	DBC	HPA03_N	HPIO on bank 66
C8		GND	Ground, connect to carrier card ground plane
C9	QBC	HPA08_P	HPIO on bank 66
C10	QBC	HPA08_N	HPIO on bank 66
C11		GND	Ground, connect to carrier card ground plane
C12	GC, QBC	HPA10_CC_P	HPIO clock-capable pin on bank 66
C13	GC, QBC	HPA10_CC_N	HPIO clock-capable pin on bank 66
C14		GND	Ground, connect to carrier card ground plane
C15	PU18_4p7	PS_POR_L	PS power-on reset driven by the carrier card. When deasserted, the PS begins the boot process.
C16	PU18_4p7	PS_SRST_C2M_L	PS system reset driven by the carrier card. When asserted, forces the PS to enter the system reset sequence.
C17		GND	Ground, connect to carrier card ground plane
C18		HDA06	HDIO on bank 45
C19		HDA07	HDIO on bank 45
C20	HDGC	HDA08_CC	HDIO clock-capable pin on bank 45
C21		GND	Ground
C22		HDA18	HDIO on bank 45
C23		HDA19	HDIO on bank 45
C24		HDA20	HDIO on bank 45
C25		GND	Ground, connect to carrier card ground plane
C26	PU18_2p2	MIO24_I2C_SCK	PS I2C clock output, bank 500
C27	PU18_2p2	MIO25_I2C_SDA	PS I2C serial data, bank 500
C28	PU18_10	MIO12_FWUEN_C2M_L	PS MIO signal on bank 500. Optional default use as firmware update enable indication in the released Kria PetaLinux BSPs.
C29		GND	Ground, connect to carrier card ground plane
C30		MIO29	PS MIO signal on bank 501. Optional use as PMU input.
C31		MIO30	PS MIO signal on bank 501. Optional use as PMU input.
C32		MIO31_SHUTDOWN	PS MIO signal on bank 501. Optional use as PMU input. In default Kria PetaLinux BSPs, this is a PMU library enabled input for hardware-initiated shutdown by the PMU.
C33		GND	Ground, connect to carrier card ground plane
C34		MIO47	PS MIO signal on bank 501
C35		MIO48	PS MIO signal on bank 501
C36		MIO49	PS MIO signal on bank 501
C37		GND	Ground, connect to carrier card ground plane
C38		MIO55	PS MIO signal on bank 502
C39		MIO56	PS MIO signal on bank 502

Table 5: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
C40		MIO57	PS MIO signal on bank 502
C41		GND	Ground, connect to carrier card ground plane
C42		MIO67	PS MIO signal on bank 502
C43		MIO68	PS MIO signal on bank 502
C44		MIO69	PS MIO signal on bank 502
C45		Reserved	No connect on the SOM
C46		GND	Ground, connect to carrier card ground plane
C47	AC01UF	GTR_REFCLK0_C2M_P	PS-GTR REFCLK0 input, bank 505
C48	AC01UF	GTR_REFCLK0_C2M_N	PS-GTR REFCLK0 input, bank 505
C49		GND	Ground, connect to carrier card ground plane
C50		GND	Ground, connect to carrier card ground plane
C51		GTR_DP3_M2C_P	PS-GTR lane 3 TX, bank 505
C52		GTR_DP3_M2C_N	PS-GTR lane 3 TX, bank 505
C53		GND	Ground, connect to carrier card ground plane
C54		GND	Ground, connect to carrier card ground plane
C55		GTR_DP1_C2M_P	PS-GTR lane 1 RX, bank 505
C56		GTR_DP1_C2M_N	PS-GTR lane 1 RX, bank 505
C57		GND	Ground, connect to carrier card ground plane
C58		GND	Ground, connect to carrier card ground plane
C59		VCC_SOM	SOM main supply voltage, +5V
C60		VCC_SOM	SOM main supply voltage, +5V
Connector Row D			
D1		VCCO_HPA	HPA I/O voltage rail, 1.0V to 1.8V
D2		VCCO_HPA	HPA I/O voltage rail, 1.0V to 1.8V
D3		GND	Ground, connect to carrier card ground plane
D4		HPA02_P	HPIO on bank 66
D5		HPA02_N	HPIO on bank 66
D6		GND	Ground, connect to carrier card ground plane
D7		HPA01_P	HPIO on bank 66
D8		HPA01_N	HPIO on bank 66
D9		GND	Ground, connect to carrier card ground plane
D10	GC	HPA09_P	HPIO on bank 66
D11	GC	HPA09_N	HPIO on bank 66
D12		GND	Ground, connect to carrier card ground plane
D13		HPA14_P	HPIO on bank 66
D14		HPA14_N	HPIO on bank 66
D15		GND	Ground, connect to carrier card ground plane
D16	HDGC	HDA00_CC	HDIO clock-capable pin on bank 45

Table 5: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
D17	HDGC	HDA01	HDIO on bank 45
D18		HDA02	HDIO on bank 45
D19		GND	Ground, connect to carrier card ground plane
D20	HDGC	HDA12	HDIO on bank 45
D21	HDGC	HDA13	HDIO on bank 45
D22		HDA14	HDIO on bank 45
D23		GND	Ground, connect to carrier card ground plane
D24	PD50	PWRGD_FPD_M2C	Power good indication for PS FPD power rails
D25	PD50	PWRGD_LPD_M2C	Power good indication for PS LPD power rails
D26	PD50	PWRGD_PL_M2C	Power good indication for all PL power rails
D27		GND	Ground, connect to carrier card ground plane
D28		MIO26	PS MIO signal on bank 501. Optional use as PMU input.
D29		MIO27	PS MIO signal on bank 501. Optional use as PMU input.
D30		MIO28	PS MIO signal on bank 501. Optional use as PMU input.
D31		GND	Ground, connect to carrier card ground plane
D32		MIO44	PS MIO signal on bank 501
D33		MIO45	PS MIO signal on bank 501
D34		MIO46	PS MIO signal on bank 501
D35		GND	Ground, connect to carrier card ground plane
D36		MIO52	PS MIO signal on bank 502
D37		MIO53	PS MIO signal on bank 502
D38		MIO54	PS MIO signal on bank 502
D39		GND	Ground, connect to carrier card ground plane
D40		MIO64	PS MIO signal on bank 502
D41		MIO65	PS MIO signal on bank 502
D42		MIO66	PS MIO signal on bank 502
D43		GND	Ground, connect to carrier card ground plane
D44		MIO76	PS MIO signal on bank 502
D45		MIO77	PS MIO signal on bank 502
D46		Reserved	No connect on the SOM
D47		GND	Ground, connect to carrier card ground plane
D48		GND	Ground, connect to carrier card ground plane
D49		GTR_DP3_C2M_P	PS-GTR lane 3 RX, bank 505
D50		GTR_DP3_C2M_N	PS-GTR lane 3 RX, bank 505
D51		GND	Ground, connect to carrier card ground plane
D52		GND	Ground, connect to carrier card ground plane
D53	AC01UF	GTR_REFCLK2_C2M_P	PS-GTR REFCLK2 input, bank 505
D54	AC01UF	GTR_REFCLK2_C2M_N	PS-GTR REFCLK2 input, bank 505

Table 5: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
D55		GND	Ground, connect to carrier card ground plane
D56		GND	Ground, connect to carrier card ground plane
D57		GTR_DP2_M2C_P	PS-GTR lane 2 TX, bank 505
D58		GTR_DP2_M2C_N	PS-GTR lane 2 TX, bank 505
D59		GND	Ground, connect to carrier card ground plane
D60		VCC_SOM	SOM main supply voltage, +5V

SOM240_2 Connector Pinout

The SOM240_2 connector provides access to two HPIO bank 65 (HPB), HPIO bank 64 (HPC), HDIO bank43 (HDB, HDIO bank 44 (HDC), and the PL GTH Quad. For additional pin definitions see the K26 SOM XDC file.

Table 6: **SOM240_2 Connector Pinout**

Connector Row/Pin Number	A	B	C	D
1	GND	GTH_DP2_C2M_P	GND	GTH_DP1_C2M_P
2	GND	GTH_DP2_C2M_N	GND	GTH_DP1_C2M_N
3	GTH_DP3_M2C_P	GND	GTH_REFCLK0_C2M_P	GND
4	GTH_DP3_M2C_N	GND	GTH_REFCLK0_C2M_N	GND
5	GND	GTH_DP2_M2C_P	GND	GTH_DP3_C2M_P
6	GND	GTH_DP2_M2C_N	GND	GTH_DP3_C2M_N
7	GTH_REFCLK1_C2M_P	GND	GTH_DP1_M2C_P	GND
8	GTH_REFCLK1_C2M_N	GND	GTH_DP1_M2C_N	GND
9	GND	GTH_DP0_C2M_P	GND	GTH_DP0_M2C_P
10	GND	GTH_DP0_C2M_N	GND	GTH_DP0_M2C_N
11	HPB15_CC_P	GND	HPB09_P	GND
12	HPB15_CC_N	HPB10_CC_P	HPB09_N	HPB01_P
13	GND	HPB10_CC_N	GND	HPB01_N
14	HPB08_P	GND	HPB14_P	GND
15	HPB08_N	HPB07_P	HPB14_N	HPB00_CC_P
16	GND	HPB07_N	GND	HPB00_CC_N
17	HPB12_P	GND	HPB02_P	GND
18	HPB12_N	HPB05_CC_P	HPB02_N	HPB_CLK0_P
19	GND	HPB05_CC_N	GND	HPB_CLK0_N

Table 6: **SOM240_2 Connector Pinout** *(cont'd)*

Connector Row/Pin Number	A	B	C	D
20	HPB06_P	GND	HPB13_P	GND
21	HPB06_N	HPB11_P	HPB13_N	HPB04_P
22	GND	HPB11_N	GND	HPB04_N
23	HPB16_P	GND	HPB_18_P	GND
24	HPB16_N	HPB03_P	HPB_18_N	HPB17_P
25	GND	HPB03_N	GND	HPB17_N
26	HPB_19_P	GND	HPC17_P	GND
27	HPB_19_N	HPC06_P	HPC17_N	HPC09_P
28	GND	HPC06_N	GND	HPC09_N
29	HPC08_P	GND	HPC10_CC_P	GND
30	HPC08_N	HPC13_P	HPC10_CC_N	HPC01_P
31	GND	HPC13_N	GND	HPC01_N
32	HPC19_P	GND	HPC11_P	GND
33	HPC19_N	HPC16_P	HPC11_N	HPC00_CC_P
34	GND	HPC16_N	GND	HPC00_CC_N
35	HPC14_P	GND	HPC12_P	GND
36	HPC14_N	HPC07_P	HPC12_N	HPC02_P
37	GND	HPC07_N	GND	HPC02_N
38	HPC15_CC_P	GND	HPC05_CC_P	GND
39	HPC15_CC_N	HPC18_P	HPC05_CC_N	HPC04_P
40	GND	HPC18_N	GND	HPC04_N
41	HPC03_P	GND	HPC_CLK0_P	GND
42	HPC03_N	VCCO_HPB	HPC_CLK0_N	VCCO_HPC
43	GND	GND	GND	GND
44	VCCO_HPB	HDB12	VCCO_HPC	HDB00_CC
45	GND	HDB13	GND	HDB01
46	HDB18	HDB14	HDB06	HDB02
47	HDB19	GND	HDB07	GND
48	HDB20	HDB15	HDB08_CC	HDB03
49	GND	HDB16_CC	GND	HDB04
50	HDB21	HDB17	HDB09	HDB05
51	HDB22	GND	HDB10	GND
52	HDB23	HDC12	HDB11	HDC00_CC
53	GND	HDC13	GND	HDC01
54	HDC18	HDC14	HDC06	HDC02
55	HDC19	GND	HDC07	GND
56	HDC20	HDC15	HDC08_CC	HDC03

Table 6: **SOM240_2 Connector Pinout** *(cont'd)*

Connector Row/Pin Number	A	B	C	D
57	GND	HDC16_CC	GND	HDC04
58	HDC21	HDC17	HDC09	HDC05
59	HDC22	VCCO_HDB	HDC10	VCCO_HDC
60	HDC23	VCCO_HDB	HDC11	VCCO_HDC

SOM240_2 Signal Names and Descriptions

See the *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide* (UG1075) for further pin descriptions.

Table 7: **SOM240_2 Signal Pins**

Pin Number	Pin Type	Signal Name	Signal Description
Connector Row A			
A1		GND	Ground, connect to carrier card ground plane
A2		GND	Ground, connect to carrier card ground plane
A3		GTH_DP3_M2C_P	GTH lane 3 TX, bank 224
A4		GTH_DP3_M2C_N	GTH lane 3 TX, bank 224
A5		GND	Ground, connect to carrier card ground plane
A6		GND	Ground, connect to carrier card ground plane
A7	AC01UF	GTH_REFCLK1_C2M_P	GTH REFCLK1 input, bank 224
A8	AC01UF	GTH_REFCLK1_C2M_N	GTH REFCLK1 input, bank 224
A9		GND	Ground, connect to carrier card ground plane
A10		GND	Ground, connect to carrier card ground plane
A11	DBC	HPB15_CC_P	HPIO clock-capable pin on bank 65
A12	DBC	HPB15_CC_N	HPIO clock-capable pin on bank 65
A13		GND	Ground, connect to carrier card ground plane
A14	QBC	HPB08_P	HPIO on bank 65
A15	QBC	HPB08_N	HPIO on bank 65
A16		GND	Ground, connect to carrier card ground plane
A17		HPB12_P	HPIO on bank 65
A18		HPB12_N	HPIO on bank 65
A19		GND	Ground, connect to carrier card ground plane
A20		HPB06_P	HPIO on bank 65
A21		HPB06_N	HPIO on bank 65
A22		GND	Ground, connect to carrier card ground plane

Table 7: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
A23		HPB16_P	HPIO on bank 65
A24		HPB16_N	HPIO on bank 65
A25		GND	Ground, connect to carrier card ground plane
A26	PERSTN1	HPB_19_P	HPIO on bank 65
A27	PERSTN0	HPB_19_N	HPIO on bank 65
A28		GND	Ground, connect to carrier card ground plane
A29	QBC	HPC08_P	HPIO on bank 64
A30	QBC	HPC08_N	HPIO on bank 64
A31		GND	Ground, connect to carrier card ground plane
A32		HPC19_P	HPIO on bank 64
A33		HPC19_N	HPIO on bank 64
A34		GND	Ground, connect to carrier card ground plane
A35		HPC14_P	HPIO on bank 64
A36		HPC14_N	HPIO on bank 64
A37		GND	Ground, connect to carrier card ground plane
A38	DBC	HPC15_CC_P	HPIO clock-capable pin on bank 64
A39	DBC	HPC15_CC_N	HPIO clock-capable pin on bank 64
A40		GND	Ground, connect to carrier card ground plane
A41	DBC	HPC03_P	HPIO on bank 64
A42	DBC	HPC03_N	HPIO on bank 64
A43		GND	Ground, connect to carrier card ground plane
A44		VCCO_HPB	HPB I/O voltage rail, 1.0V to 1.8V
A45		GND	Ground, connect to carrier card ground plane
A46		HDB18	HDIO on bank 43
A47		HDB19	HDIO on bank 43
A48		HDB20	HDIO on bank 43
A49		GND	Ground, connect to carrier card ground plane
A50		HDB21	HDIO on bank 43
A51		HDB22	HDIO on bank 43
A52		HDB23	HDIO on bank 43
A53		GND	Ground, connect to carrier card ground plane
A54		HDC18	HDIO on bank 44
A55		HDC19	HDIO on bank 44
A56		HDC20	HDIO on bank 44
A57		GND	Ground, connect to carrier card ground plane
A58		HDC21	HDIO on bank 44
A59		HDC22	HDIO on bank 44
A60		HDC23	HDIO on bank 44

Table 7: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
Connector Row B			
B1		GTH_DP2_C2M_P	GTH lane 2 RX, bank 224
B2		GTH_DP2_C2M_N	GTH lane 2 RX, bank 224
B3		GND	Ground, connect to carrier card ground plane
B4		GND	Ground, connect to carrier card ground plane
B5		GTH_DP2_M2C_P	GTH lane 2 TX, bank 224
B6		GTH_DP2_M2C_N	GTH lane 2 TX, bank 224
B7		GND	Ground, connect to carrier card ground plane
B8		GND	Ground, connect to carrier card ground plane
B9		GTH_DP0_C2M_P	GTH lane 0 RX, bank 224
B10		GTH_DP0_C2M_N	GTH lane 0 RX, bank 224
B11		GND	Ground, connect to carrier card ground plane
B12	GC, QBC	HPB10_CC_P	HPIO clock-capable pin on bank 65
B13	GC, QBC	HPB10_CC_N	HPIO clock-capable pin on bank 65
B14		GND	Ground, connect to carrier card ground plane
B15		HPB07_P	HPIO on bank 65
B16		HPB07_N	HPIO on bank 65
B17		GND	Ground, connect to carrier card ground plane
B18	QBC	HPB05_CC_P	HPIO clock-capable pin on bank 65
B19	QBC	HPB05_CC_N	HPIO clock-capable pin on bank 65
B20		GND	Ground, connect to carrier card ground plane
B21	GC	HPB11_P	HPIO on bank 65
B22	GC	HPB11_N	HPIO on bank 65
B23		GND	Ground, connect to carrier card ground plane
B24	DBC	HPB03_P	HPIO on bank 65
B25	DBC	HPB03_N	HPIO on bank 65
B26		GND	Ground, connect to carrier card ground plane
B27		HPC06_P	HPIO on bank 64
B28		HPC06_N	HPIO on bank 64
B29		GND	Ground, connect to carrier card ground plane
B30	QBC	HPC13_P	HPIO on bank 64
B31	QBC	HPC13_N	HPIO on bank 64
B32		GND	Ground, connect to carrier card ground plane
B33		HPC16_P	HPIO on bank 64
B34		HPC16_N	HPIO on bank 64
B35		GND	Ground, connect to carrier card ground plane
B36		HPC07_P	HPIO on bank 64
B37		HPC07_N	HPIO on bank 64

Table 7: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
B38		GND	Ground, connect to carrier card ground plane
B39	DBC	HPC18_P	HPIO on bank 64
B40	DBC	HPC18_N	HPIO on bank 64
B41		GND	Ground, connect to carrier card ground plane
B42		VCCO_HPB	HPB I/O voltage rail, 1.0V to 1.8V
B43		GND	Ground, connect to carrier card ground plane
B44	HDGC	HDB12	HDIO on bank 43
B45	HDGC	HDB13	HDIO on bank 43
B46		HDB14	HDIO on bank 43
B47		GND	Ground, connect to carrier card ground plane
B48		HDB15	HDIO on bank 43
B49	HDGC	HDB16_CC	HDIO clock-capable pin on bank 43
B50	HDGC	HDB17	HDIO on bank 43
B51		GND	Ground, connect to carrier card ground plane
B52	HDGC	HDC12	HDIO on bank 44
B53	HDGC	HDC13	HDIO on bank 44
B54		HDC14	HDIO on bank 44
B55		GND	Ground, connect to carrier card ground plane
B56		HDC15	HDIO on bank 44
B57	HDGC	HDC16_CC	HDIO clock-capable pin on bank 44
B58	HDGC	HDC17	HDIO on bank 44
B59		VCCO_HDB	HDB I/O voltage rail, 1.2V to 3.3V
B60		VCCO_HDB	HDB I/O voltage rail, 1.2V to 3.3V
Connector Row C			
C1		GND	Ground, connect to carrier card ground plane
C2		GND	Ground, connect to carrier card ground plane
C3	AC01UF	GTH_REFCLK0_C2M_P	GTH REFCLK0 input, bank 224
C4	AC01UF	GTH_REFCLK0_C2M_N	GTH REFCLK0 input, bank 224
C5		GND	Ground, connect to carrier card ground plane
C6		GND	Ground, connect to carrier card ground plane
C7		GTH_DP1_M2C_P	GTH lane 1 TX, bank 224
C8		GTH_DP1_M2C_N	GTH lane 1 TX, bank 224
C9		GND	Ground, connect to carrier card ground plane
C10		GND	Ground, connect to carrier card ground plane
C11	GC	HPB09_P	HPIO on bank 65
C12	GC	HPB09_N	HPIO on bank 65
C13		GND	Ground, connect to carrier card ground plane

Table 7: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
C14		HPB14_P	HPIO on bank 65
C15		HPB14_N	HPIO on bank 65
C16		GND	Ground, connect to carrier card ground plane
C17		HPB02_P	HPIO on bank 65
C18		HPB02_N	HPIO on bank 65
C19		GND	Ground, connect to carrier card ground plane
C20	QBC	HPB13_P	HPIO on bank 65
C21	QBC	HPB13_N	HPIO on bank 65
C22		GND	Ground, connect to carrier card ground plane
C23		HPB_18_P	HPIO on bank 65
C24		HPB_18_N	HPIO on bank 65
C25		GND	Ground, connect to carrier card ground plane
C26		HPC17_P	HPIO on bank 64
C27		HPC17_N	HPIO on bank 64
C28		GND	Ground, connect to carrier card ground plane
C29	GC, QBC	HPC10_CC_P	HPIO clock-capable pin on bank 64
C30	GC, QBC	HPC10_CC_N	HPIO clock-capable pin on bank 64
C31		GND	Ground, connect to carrier card ground plane
C32	GC	HPC11_P	HPIO on bank 64
C33	GC	HPC11_N	HPIO on bank 64
C34		GND	Ground, connect to carrier card ground plane
C35		HPC12_P	HPIO on bank 64
C36		HPC12_N	HPIO on bank 64
C37		GND	Ground, connect to carrier card ground plane
C38	QBC	HPC05_CC_P	HPIO clock-capable pin on bank 64
C39	QBC	HPC05_CC_N	HPIO clock-capable pin on bank 64
C40		GND	Ground, connect to carrier card ground plane
C41	GC	HPC_CLK0_P	HPIO global clock pin on bank 64
C42	GC	HPC_CLK0_N	HPIO global clock pin on bank 64
C43		GND	Ground, connect to carrier card ground plane
C44		VCCO_HPC	HPC I/O voltage rail, 1.0V to 1.8V
C45		GND	Ground, connect to carrier card ground plane
C46		HDB06	HDIO on bank 43
C47		HDB07	HDIO on bank 43
C48	HDGC	HDB08_CC	HDIO clock-capable pin on bank 43
C49		GND	Ground, connect to carrier card ground plane
C50	HDGC	HDB09	HDIO on bank 43
C51		HDB10	HDIO on bank 43

Table 7: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
C52		HDB11	HDIO on bank 43
C53		GND	Ground, connect to carrier card ground plane
C54		HDC06	HDIO on bank 44
C55		HDC07	HDIO on bank 44
C56	HDGC	HDC08_CC	HDIO clock-capable pin on bank 44
C57		GND	Ground, connect to carrier card ground plane
C58	HDGC	HDC09	HDIO on bank 44
C59		HDC10	HDIO on bank 44
C60		HDC11	HDIO on bank 44
Connector Row D			
D1		GTH_DP1_C2M_P	GTH lane 1 RX, bank 224
D2		GTH_DP1_C2M_N	GTH lane 1 RX, bank 224
D3		GND	Ground, connect to carrier card ground plane
D4		GND	Ground, connect to carrier card ground plane
D5		GTH_DP3_C2M_P	GTH lane 3 RX, bank 224
D6		GTH_DP3_C2M_N	GTH lane 3 RX, bank 224
D7		GND	Ground, connect to carrier card ground plane
D8		GND	Ground, connect to carrier card ground plane
D9		GTH_DP0_M2C_P	GTH lane 0 TX, bank 224
D10		GTH_DP0_M2C_N	GTH lane 0 TX, bank 224
D11		GND	Ground, connect to carrier card ground plane
D12		HPB01_P	HPIO on bank 65
D13		HPB01_N	HPIO on bank 65
D14		GND	Ground, connect to carrier card ground plane
D15	DBC	HPB00_CC_P	HPIO clock-capable pin on bank 65
D16	DBC	HPB00_CC_N	HPIO clock-capable pin on bank 65
D17		GND	Ground, connect to carrier card ground plane
D18	GC	HPB_CLK0_P	HPIO global clock pin on bank 65
D19	GC	HPB_CLK0_N	HPIO global clock pin on bank 65
D20		GND	Ground, connect to carrier card ground plane
D21		HPB04_P	HPIO on bank 65
D22		HPB04_N	HPIO on bank 65
D23		GND	Ground, connect to carrier card ground plane
D24	DBC	HPB17_P	HPIO on bank 65
D25	DBC	HPB17_N	HPIO on bank 65
D26		GND	Ground, connect to carrier card ground plane
D27	GC	HPC09_P	HPIO on bank 64
D28	GC	HPC09_N	HPIO on bank 64

Table 7: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
D29		GND	Ground, connect to carrier card ground plane
D30		HPC01_P	HPIO on bank 64
D31		HPC01_N	HPIO on bank 64
D32		GND	Ground, connect to carrier card ground plane
D33	DBC	HPC00_CC_P	HPIO clock-capable pin on bank 64
D34	DBC	HPC00_CC_N	HPIO clock-capable pin on bank 64
D35		GND	Ground, connect to carrier card ground plane
D36		HPC02_P	HPIO on bank 64
D37		HPC02_N	HPIO on bank 64
D38		GND	Ground, connect to carrier card ground plane
D39		HPC04_P	HPIO on bank 64
D40		HPC04_N	HPIO on bank 64
D41		GND	Ground, connect to carrier card ground plane
D42		VCCO_HPC	HPC I/O voltage rail, 1.0V to 1.8V
D43		GND	Ground, connect to carrier card ground plane
D44	HDGC	HDB00_CC	HDIO clock-capable pin on bank 43
D45	HDGC	HDB01	HDIO on bank 43
D46		HDB02	HDIO on bank 43
D47		GND	Ground, connect to carrier card ground plane
D48		HDB03	HDIO on bank 43
D49		HDB04	HDIO on bank 43
D50		HDB05	HDIO on bank 43
D51		GND	Ground, connect to carrier card ground plane
D52	HDGC	HDC00_CC	HDIO clock-capable pin on bank 44
D53	HDGC	HDC01	HDIO on bank 44
D54		HDC02	HDIO on bank 44
D55		GND	Ground, connect to carrier card ground plane
D56		HDC03	HDIO on bank 44
D57		HDC04	HDIO on bank 44
D58		HDC05	HDIO on bank 44
D59		VCCO_HDC	HDC I/O voltage rail, 1.2V to 3.3V
D60		VCCO_HDC	HDC I/O voltage rail, 1.2V to 3.3V

Supported I/O Standards

The K26 SOM supports all I/O standards supported by the respective bank that a signal is connected to with the exception of I/O standards that require a reference voltage (V_{REF}). For more information, refer to the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

During power-up and configuration, internal pull-up resistors are disabled and each SelectIO™ pin is set to 3-state.

The K26 SOM is built with the XCK26-SFVC784-2LV device; which has a -2 speed grade and is an LV device (operates at V_{CCINT} = 0.72V). Consult the corresponding I/O speed tables in *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925) for the definition of maximum data rates.

Signal Routing Guidelines

This section provides signal routing guidelines and required PCB layout constraints for all interfaces provided on the SOM.

Note: Consult the *UltraScale Architecture PCB Design User Guide* (UG583) for detailed information.

MIO Signals

- Route all MIO signals MIO[77:26] as single-ended 50Ω traces.
- The maximum data rate supported on MIO signals is 250 Mb/s.
- Implement length matching as required by the interface used on individual MIO signal groups defined by the application MIO configuration.
- All MIO signals must be 1.8V compatible.

HDIO Signals

- Route all HDIO signals as single-ended 50Ω traces.
- The maximum data rate supported on HDIO signals is 250 Mb/s. See *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925) for more information on HDIO signals.
- Implement length matching as required by the application PL-based interface mapped to the HDIO signal groups.

HPIO Signals

HPIO signals can be implemented as high-speed differential signaling such as MIPI interfaces or other application specific interfaces.

- HPIO P/N pairs should be routed as standard 50Ω single-ended traces.
- The maximum data rate supported on HPIO signals is 2.5 Gb/s. See *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925) for more information on HPIO signals.
- Implement length matching as required by the interface used on individual HPIO signal groups.
- Match P and N signals within an HPIO differential pair to within ±0.5 mils of each other.
- If using MIPI differential signals, length match the MIPI interface HPIO signal groups (pair to pair) within ±50 mils.
- MIPI differential signals to all other signal spacing should be 2.5 times the distance between signal to nearest GND plane.
- Match other application-specific HPIO use cases per the HPIO signal group interface requirement.

PS-GTR Transceivers

PS-GTR transceivers support a maximum transfer rate of 6 Gb/s over each lane.

- To minimize the impedance discontinuity at the SOM connector interface, route the PS-GTR signals using a 90Ω differential impedance.
- Match P and N differential signals to within ±0.5 mils of each other.
- Route PS-GTR signals in internal routing layers as a stripline structure.
- Route PS-GTR signals with a maximum of two via transitions. Ensure adequate ground return vias are placed next to the signal vias to minimize crosstalk.
- Route PS-GTR signals to have a maximum via stub length of less than 50 mils. It is a good design practice to minimize the stub length to avoid reflections.
- PS-GTR differential signals to all other signal spacing should be four times the distance between the signal to the nearest GND plane.
- For design flexibility, no transceiver capacitors are added to the data lanes on the PS-GTR transceivers.
- For more information on proper decoupling and interface standards, see the *PCB Guidelines for the PS Interface in the Zynq UltraScale+ MPSoC* chapter in the *UltraScale Architecture PCB Design User Guide* (UG583).

GTH Transceivers

GTH transceivers support a maximum transfer rate of 12.5 Gb/s over each lane.

- To minimize the impedance discontinuity at the SOM connector interface, route the GTH signals using a 90Ω differential impedance.
- Match P and N differential signals to within ±0.5 mils of each other.
- Route GTH signals in internal routing layers as a stripline structure.
- Route GTH signals with a maximum of two via transitions. Ensure adequate ground return vias are placed next to the signal vias to minimize crosstalk.
- Route GTH signals to have a maximum via stub length of less than 24 mils. It is a good design practice to minimize the stub length to avoid reflections.
- GTH differential signals to all other signal spacing should be five times the distance between the signal to the nearest GND plane.
- For design flexibility, no transceiver capacitors are added to the data lanes on the GTH transceivers.
- For more information on proper decoupling and interface standards, see the *PCB Design Checklist* chapter in the *UltraScale Architecture GTH Transceivers User Guide* (UG576).

Transceiver Reference Clocks

Both the PS-GTR and PL-GTH transceivers differential clock signals (REFCLKs) must meet following signal integrity requirements.

- The target differential impedance of 100Ω.
- Match P and N differential signals to within ±0.5 mils of each other.
- REFCLK to all other signal spacing should be five times the distance between the signal to the nearest GND plane.

The Kria K26 SOM includes 0.01 µF capacitors on the MGTREFCLKs to aid clock quality.

I/O Constraints Definition

SOM I/O Timing Model

When creating an I/O timing model, you should include the Zynq® UltraScale+™ MPSoC package and K26 SOM PCB signal delays for all MIO, HDIO, and HPIO related interfaces. As the carrier card designer, you must include the trace length definitions associated with your implementation.

The Vivado device model captures the MPSoC-related timing model information. When designing a carrier card, you need to include the physical trace length of the MPSoC to board-to-board connector on the SOM as well as the board-to-board connector to peripheral device on your carrier card. The MPSoC package delay and SOM trace length information provided in the *Kria K26 SOM Trace Delay File* (XTP688) is defined by the board-to-board connector pin name and associated MPSoC pin function net name.

TIP: *The K26 SOM device and package delay file is available in the Vivado® tools.*

SOM I/O Drive Strength Definition

For up to eight inches of trace length on the carrier card, the recommendation is to use a 4 mA drive strength and a slow slew rate for all MIO and HDIO signals. When trace lengths on the carrier card are longer than eight inches, signal integrity simulations might be necessary to select the correct drive strength and proper termination.

RECOMMENDED: *For MIO signals that are local to the SOM on MIO bank 500 and part of MIO bank 501, the recommendation is to use a 4 mA drive strength and slow slew rate.*

For I/O modeling, including drive strength settings, the Zynq UltraScale+ MPSoC IBIS models can be downloaded from the Xilinx website.

SOM Configuration and Control Signals

This section outlines the configuration and control signals associated with the Zynq UltraScale+ MPSoC on the SOM.

Power-on Reset (PS_POR_B) Signal

This is the Zynq UltraScale+ MPSoC power-on reset signal. In Xilinx documentation this signal is also described as PS_POR_B. The POR_B signal is an active-Low signal that must be asserted during the SOM power-up sequence.

System Reset (PS_SRST_B) Signal

This system reset is primarily used for debug activities and is functionally equivalent to POR_B except for clearing a subset of PS power-on and error registers. See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) for more information.

BOOT_MODE Signals

The BOOT_MODE pins define the physical device that the Zynq UltraScale+ MPSoC will read boot firmware from. The boot firmware is prepackaged as a `boot.bin`, which is a consolidated boot firmware binary constructed using the Xilinx Bootgen tool outlined in the *Bootgen User Guide* (UG1283).

Note: Xilinx documentation uses PS_MODE and BOOT_MODE interchangeably.

The SOM includes two non-volatile storage devices: QSPI and eMMC. The BOOT_MODE strapping defines the primary boot device. Alternative boot devices can be designed on your carrier card via MIO banks 501 and 502. The BOOT_MODE memory device selection resistor strapping is defined in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

JTAG Port Interfaces

The JTAG interface uses a serial configuration mode, popular for prototyping and board test. The four-pin JTAG interface consisting of pins TMS, TDO, TDI, and TCK is included for debug purposes and recommended to be accessible through the carrier card, regardless of boot mode selected. For more information, see the JTAG Interface section in *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

PS_ERROR_OUT Signal, PS_ERROR_STATUS Commands

PS_ERROR_OUT is asserted when there is an accidental loss of power, a hardware error, or an exception in the PMU. For secure scenarios where device status is disabled from external visibility, there are PMU control registers to mask PS_ERROR_OUT. PS_ERROR_OUT is sourced from a 1.8V power domain. For more information, see the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

PS_ERROR_STATUS indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status. For secure scenarios where device status is disabled from external visibility, there are PMU control registers to mask PS_ERROR_STATUS. PS_ERROR_STATUS is sourced from a 1.8V power domain. For more information, see the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

Power Management Unit (PMU)

The PMU processor of the Zynq UltraScale+ MPSoC has access to a subset of the I/O in bank 501 that should be given special consideration during the implementation of power-down and power control functionality in the SOM and carrier card design. The PMU application can be customized by the carrier card designer. However, the Xilinx PMU reference implementation uses the following pin mappings:

- **HW Requested Shutdown:** MIO31 is the SOM input signal
- **External Watchdog Trigger:** MIO35 is the SOM output signal

Sideband Signals

The sideband signals consist of power, processor, and configuration signals. V_{CCO} for sideband signals is 1.80V.

- **JTAG:** The JTAG signals JTAG_TCK_C2M, JTAG_TMS_C2M, JTAG_TDI_C2M, and JTAG_TDO_M2C connect to the SOM Zynq UltraScale+ MPSoC JTAG port.
- **PS_REF_CLK:** The PS_REF_CLK input is connected to a 33.33 MHz oscillator.
- **PS_PAD_I/O:** The PS RTC inputs are connected to a 32.768 kHz crystal.
- **I2C:** The I2C signals I2C_SCK and I2C_SDA connect to an I2C master on MIO bank 500 of the SOM Zynq UltraScale+ MPSoC. The I2C I/O standard is 1.8V.
- **PS_MODE[3:0]:** The connector PS_MODE[3:0] pins connect to the SOM Zynq UltraScale+ MPSoC PS_MODE pins. All mode pins are pulled High to 1.8V through a resistor on the SOM.The carrier card boot mode is required to set the PS_MODE pins to a valid boot mode as defined in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085). To configure a PS_MODE pin to a logic 1, the pin must be left floating, to configure a logic 0, the PS_MODE pin must be connected to GND with a 0Ω resistor.
- **PS_POR_L:** During power up, a voltage monitor keeps PS_POR_L asserted (Low) until all SOM power rails are stabilized. Afterward, PS_POR_L is released and the boot process starts. A carrier card can use PS_POR_L to reset any on-board devices. The carrier card can also force PS_POR_L Low to extend the reset during power on to reset the system at any time.
- **PS_SRST_C2M_L:** The PS_SRST_C2M_L pin connects to PS_SRST_B signal on the SOM Zynq UltraScale+ MPSoC. PS_SRST_B input signal to the Zynq UltraScale+ MPSoC is the system reset signal, and it is commonly used during debug. PS_SRST_C2M_L is pulled High to 1.8V on the SOM.

Power Management Signals

- **PWROFF_ C2M_L:**
  - PWROFF_C2M_L is an active-Low signal to power down the SOM and pulled High to the +5V SOM input power rail.
  - When PWROFF_C2M_L is asserted, the SOM power regulators perform a full-power shutdown of the device following the correct regulator power-down sequence. This signal does not alert application software to the power shutdown.
  - Upon deassertion of PWROFF_C2M_L, the SOM power regulators initiate a power-on sequence.

  ***Note*:** Asserting PWROFF_C2M_L does not perform a software shutdown or notify the system of the shutdown. The power regulators will start to power down instantly. Use the MIO31_SHUTDOWN pin and PMU functionality to initiate a software shutdown.

- **PWRGD_LPD_M2C:** PWRGD_LPD_M2C is an active-High push-pull output signal from the SOM power system that indicates the power status of all SOM PS low-power domain (LPD) rails. PWRGD_PL_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal to monitor LPD status.
- **PWRGD_FPD_M2C:** PWRGD_FPD_M2C is an active-High push-pull output signal from the SOM power system that indicates the power status of all SOM PS full-power domain (FPD) rails. PWRGD_FPD_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal to monitor FPD status.

  ***Note*:** The K26 SOM does not have split rails for LPD and FPD. PWRGD_LPD_M2C and PWRGD_FPD_M2C are tied together on the SOM.
- **PWRGD_PL_M2C:** PWRGD_PL_M2C is an active-High push-pull output signal from the SOM power system that indicates the power status of all SOM PL power rails. PWRGD_PL_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal to monitor PL power status.
- **VCCOEN_PS_M2C:** VCCOEN_PS_M2C is an active-High push-pull output signal from the SOM power system to enable the PS V_{CCO} rails that are supplied by the carrier card. VCCOEV_PS_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal as an indication to turn power on for all PS peripherals.
- **VCCOEN_PL_M2C:** VCCOEN_PL_M2C is an active-High push-pull output signal from the SOM power system to enable the PL V_{CCO} rails that are supplied by the carrier card. VCCOEN_PL_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal as an indication to turn power on for all PL peripherals.

SOM MIO Design Considerations

The Zynq UltraScale+ MPSoC on the SOM has a set of integrated, built-in interface IPs. These interface IPs are made available to external pins through multiplexed I/O (MIO) selection, which can be selected and customized for a carrier card design. The MIO interface configuration is set as part of the Vivado design project through the Vivado processor configuration wizard (PCW).

The design of the SOM carrier card must give special consideration to the MIO pins to ensure that the desired MIO peripherals are mappable to the physical pins defined by the electrical design of the carrier card. The SOM fixes the mapping of MIO bank 500 for SOM based peripherals and a subset of bank 501 for SOM power management signals. The remaining MIO pins are configurable for flexibility in the carrier card design. The full MIO peripheral IP mapping to physical pin mapping is defined in the *MIO Interfaces* table in *Zynq UltraScale+ Device Technical Reference Manual* (UG1085). MIO mapping must comply with the Zynq UltraScale+ MPSoC design constraints and requirements.

MIO Bank 500

The SOM fixed MIO configurations for bank 500 are outlined in the following table. This MIO configuration is defined by the physical SOM design and cannot be modified by carrier-card designers. It defines the MIO configuration for the SOM peripherals: QSPI, TPM SPI, LEDs, eMCC, and I2C configuration bus.

MIO #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Peripheral	QSPI						SPI1	GPIO0		SPI1			GPIO0	eMMC (SD0)										GPIO0	I2C1	
Pin Fct	sclk_out	miso_mo1	mo2	mo3	mosi_mi0	n_ss_out	sclk_out	LED_ DS35	LED_ DS36	n_ss_out	miso	mosi	FW_Upd	data[0]	data[1]	data[2]	data[3]	data[4]	data[5]	data[6]	data[7]	cmd_out	clk_out	eMMC_Rst	scl	sda

MIO Bank 500 – Extensible I2C Bus

This MIO configuration must be considered fixed and will be pre-populated in the corresponding SOM Vivado board files. In SOM bank 500, predefined configuration of the PS I2C interface is made available to the carrier card via the I2C_SCK and I2C_SDA signals on the som_240_1 connector. If the carrier card does not need to extend this I2C bus, the carrier card should leave them as no connects. If the carrier card design extends this bus, they need to ensure they do not introduce an address conflict with the I2C devices on the SOM. The I2C devices are defined in the corresponding table of the *Kria K26 SOM Data Sheet* (DS987).

MIO Bank 501 – PMU MIO Considerations

The Zynq UltraScale+ MPSoC platform management unit (PMU) processor has access to a subset of the MIO in bank 501 that are also available to the clock-capable I/O and should be given special consideration for the implementation of power-down and power control functionality of the SOM and carrier card design. The SOM power management reserved pins MIO32–34 and are identified in green.

There are also two pins related to optional PMU features made available in the SOM PMU reference implementation. They implement an external shutdown request and can control an external platform watchdog function. These MIO501 optional feature pins are shown in orange.

- External shutdown request: MIO31 – PMU input pin
- External watchdog toggle: MIO35 – PMU output pin

MIO Bank 501 – UART

RECOMMENDED: *The carrier card design should include a UART for board bring-up and initial debug. The Xilinx K26 boot firmware and PetaLinux BSP default the UART interface to MIO36 and MIO37. It is recommended that carrier card designs use this same mapping to be able to use the Xilinx provided software references.*

MIO #	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
Peripheral						PMU_GPI	PMU_GPO	PMU_GPO	PMU_GPO	PMU_GPO	UART1															
Pin Fct						SHUTDOWN	FPD_Pwr_En	PL_Pwr_EN	PS_Pwr_En	WD_OUT	txd	rxd														

MIO Bank 502

MIO bank 502 has no pin reservations relative to the carrier card design, beyond those defined in *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

SOM Power

Your carrier card should provide:

- The SOM main power supply (+5V power rail).
- The V_{CCO} power rails for the programmable logic (PL) HPIO and HDIO banks on the K26 SOM.
- Optionally, the carrier card can supply an external battery power to the V_{CC_BATT} pin for real-time clock (RTC) battery backup power.

SOM Connector Power Pins

The following table lists all power rails required for the proper operation of the K26 SOM. The carrier card designed for your application should provide these power rails based on the required peripheral I/O voltage. These supplies must be intentionally sequenced as outlined in the Power Sequencing section. Connect the VCCO pins of unused banks together and to the same potential (GND or a valid V_{CCO} voltage).

Table 10: **SOM Power Rails**

Power Rail Name	Supported Voltage Range	Maximum Current	Description
V_{CC_SOM}	5V (4.75V – 5.25V) 50 mV p-p maximum noise	4A	Main power input to the SOM. Supplies power to on-board power regulators.
V_{CC_BATT}[1]	1.20 – 1.50V	150 nA – 3650 nA	External battery input for the RTC
V_{CCO_HPA}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 66
V_{CCO_HPB}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 65
V_{CCO_HPC}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 64
V_{CCO_HDA}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 45
V_{CCO_HDB}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 43
V_{CCO_HDC}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 44

Notes:

1. See *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925) for recommended device conditions when RTC is enabled or disabled.

For the selected I/O type, the supply voltage tolerance at the SOM connector must be within +3%/–2%. For example:

- If an HPIO bank is configured for the LVDS (1.8V) standard, the V_{CCO} at the SOM connector pin must be within 1.764V–1.854V.

- If an HDIO bank is configured for the LVDS_25 standard, the V_{CCO} at the SOM connector pin must be within 2.450V–2.575V.

Power Management

The SOM is based on a custom MPSoC. Designing power should then follow the same design practices. Signaling is provided to help with this, and it is recommended that you split the power system on your carrier card into three power domains:

- **Always On Power Domain:** The +5V main power and auxiliary power support infrastructure components such as the power management and telemetry circuits, reset circuits, and clocking circuits.
- **PS Power Domain:** The power rails that support the peripherals connected to the PS MIO and PS-GTR signals.
- **PL Power Domain:** The power rails that support the peripherals connected to the PL HDIO and HPIO signals and the V_{CCO} rails.

Power Sequencing

The carrier card power management circuit for your application must use the following sequence to power on the K26 SOM. Your carrier card supplies the +5V SOM power rail (V_{CC_SOM}).

1. When the V_{CC_SOM} voltage level is within the specified range, the carrier card deasserts the POWER_OFF_C2M_L signal.
2. The K26 SOM initiates onboard power sequencing.
3. The K26 SOM asserts the VCCOEN_PS_M2C signal, indicating to the carrier card to turn on the supply rails for the PS peripheral devices.
4. The K26 SOM asserts the VCCOEN_PL_M2C signal, indicating to the carrier card to turn on the supply rails for the PL peripheral devices as well as all V_{CCO} rails for the HPIO and HDIO banks.

Power Telemetry

RECOMMENDED: *Your carrier card should employ a current sensing device to monitor the input current on the V_{CC_SOM} supply rail that is powering the SOM. Xilinx carrier cards add this current sensing device to the PS I2C bus to minimize I/O.*

Voltage Rail Monitoring

A subset of the SOM rails can be monitored using the system monitor (SYSMON) available on the Zynq UltraScale+ MPSoC. For more information on the SYSMON, see *UltraScale Architecture System Monitor User Guide* (UG580).

Table 11: **Voltage Rail Domains**

Domain	SYSMON on Zynq UltraScale+ MPSoC	Power Rail on SOM
+5V Input	V_P/V_N	V_{IN_5V0}
PS	$V_{CC\_PSINTLP}$ $V_{CC\_PSINTFP}$	$V_{CC\_PS\_0V85}$ (0.85V)
PS	V_{CC_PSAUX}	$V_{CC\_PS\_1V80}$ (1.8V)
PL	V_{CCINT}	$V_{CC\_PL\_0V72}$ (0.72V)
PL	V_{CCAUX}	$V_{CC\_PL\_1V80}$ (1.8V)
PL	V_{CCBRAM}	$V_{CC\_PL\_0V85}$ (0.85V)

The Zynq UltraScale+ MPSoC SYSMON is supported for Linux applications by the Xilinx analog mixed signal (AMS) driver, available in the Xilinx ADC GitHub. The SYSMON is supported for bare-metal applications by the SYSMONPSU driver.

SOM Power Integrity

The K26 SOM is equipped with adequate decoupling capacitors on all PS and PL voltage rails to support a defined set of transient step loads. The programmable logic (PL) and processing system (PS) designs must not exceed the specified maximum current limit and the corresponding step loads as listed in the following tables.

Table 12: **PL Design Limits**

Voltage Rail	Voltage (V)	Maximum Current (A)	Step Load (% of Maximum Current)
V_{CCINT}	0.72	6.5	50
V_{CCINT_VCU}	0.9	3.5	50

Table 13: **PS Design Limits**

Voltage Rail	Voltage (V)	Maximum Current (A)	Step Load (% of Maximum Current)
$V_{CC\_PSINTLP}$ and $V_{CC\_PSINTFP}$	0.85	3.5	25
V_{CCO_PSIO}	1.8	0.300	100

SOM Power Estimation

Xilinx has created the Power Design Manager (PDM) tool (download at www.xilinx.com/power) for power estimation. The PDM tool supports SOM developers to get power estimation based on their applications. The *Kria K26 SOM Thermal Design Guide* (UG1090), provides documentation to support the integration of the SOM into your application system thermal and mechanical solutions including thermal modeling and detailed design specifications.

Mechanical Design Considerations

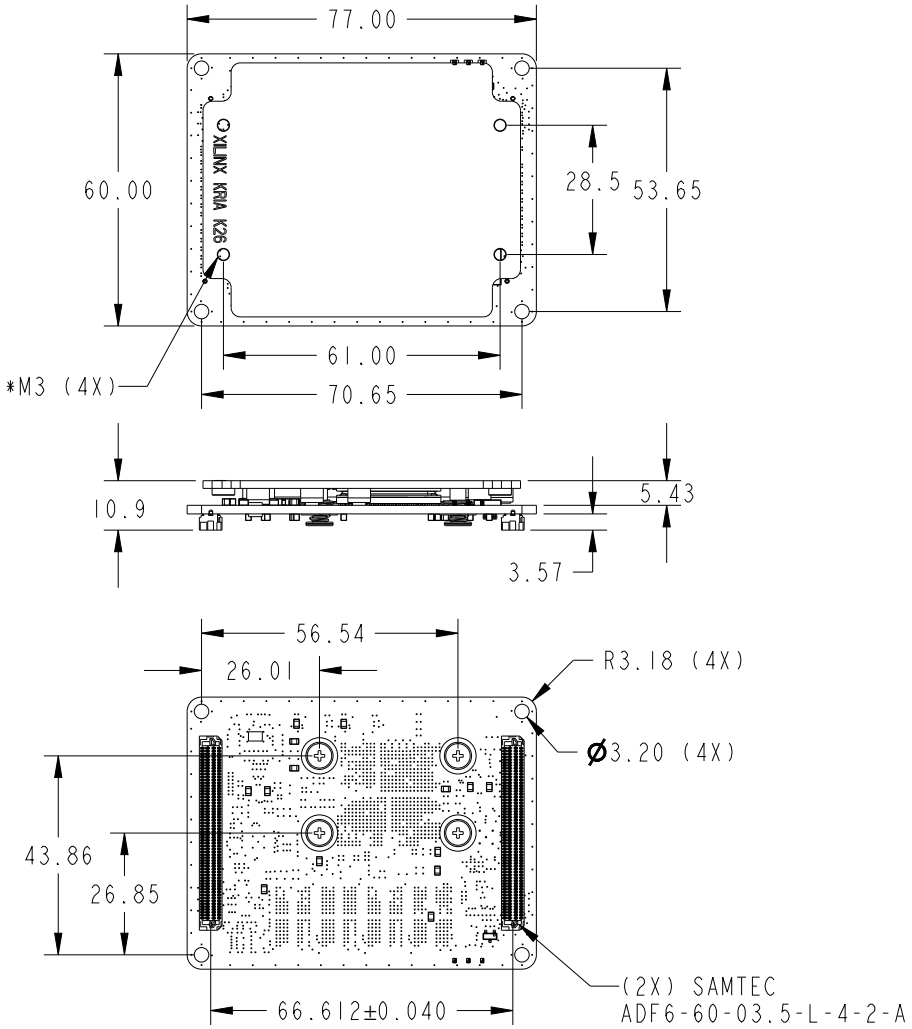
Mechanical Dimensions

The following table and figures define the mechanical specifications of the K26 SOM. The following mechanical drawing provides the detailed dimensions of the SOM.

Table 14: **K26 SOM Mechanical Specifications**

Parameter	Specification
SOM length	77 mm
SOM width	60 mm
SOM height (without a thermal solution)	10.9 mm
Mass	58 grams

Figure 2: **K26 SOM Dimensions**



Notes:

1. All dimensions in mm.
2. Mass: 58G.
3. Mounting holes (*) are reserved for customer's cooling installation.
4. Tolerance unless otherwise specified: ±0.13.

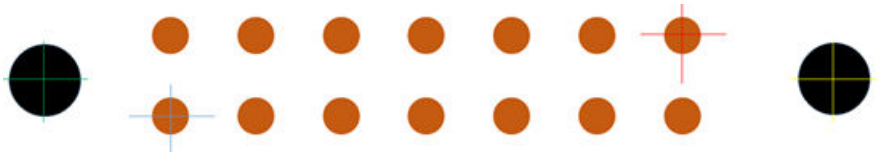
X26219-031522

The K26 SOM 3D CAD files are available for your platform or carrier design reference. These files are design aides in your cooling mechanical design, system assembly interference and clearance reviews, and board-to-board (B2B) connector placement alignment checks.

PCB Fabrication and Assembly House Requirements

The following are requirements for the fabrication of the PC board assembly.

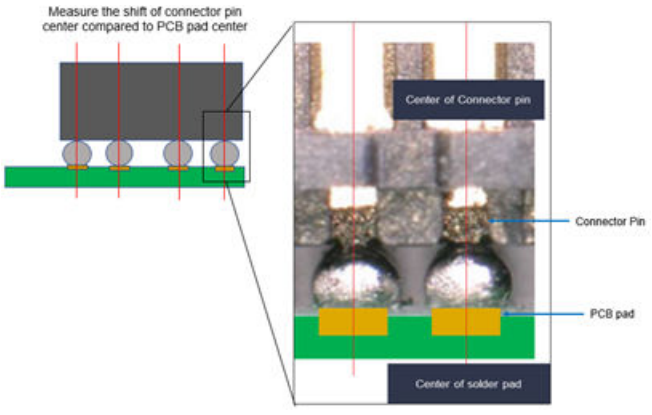
- Carrier card PCB pad-to-pad tolerance should be < ±25 µm.



  The blue to red cross (surface pad to surface pad) tolerance with respect to the Gerber pad location should be less than ±1mil (25 µm).
- Carrier card assembly house placement capability should be < ±26 µm.
- RMS value of the PCB pad-to-pad and component placement tolerance, based on the capabilities listed above should be < ±36 µm.
- Samtec recommends a tolerance of ±0.04 mm in the distance between the connectors.
- The combination of all these requirements must be controlled to less than ±40 µm.

The evaluation of Samtec connector placement is conducted by shifting the placement of the connector from 0% (PCB pad center aligned with connector pin center) to 15% (pin center offset by 15% of PCB pad width). The shifted connectors are capable of self-aligning after a reflow soldering process. The following image shows that even though placement of the connector shifted by 15% of the pad width, the connector solder ball was still able to self-align to the center of pad.

Figure 3: **Connector Pin/Pad Placement**



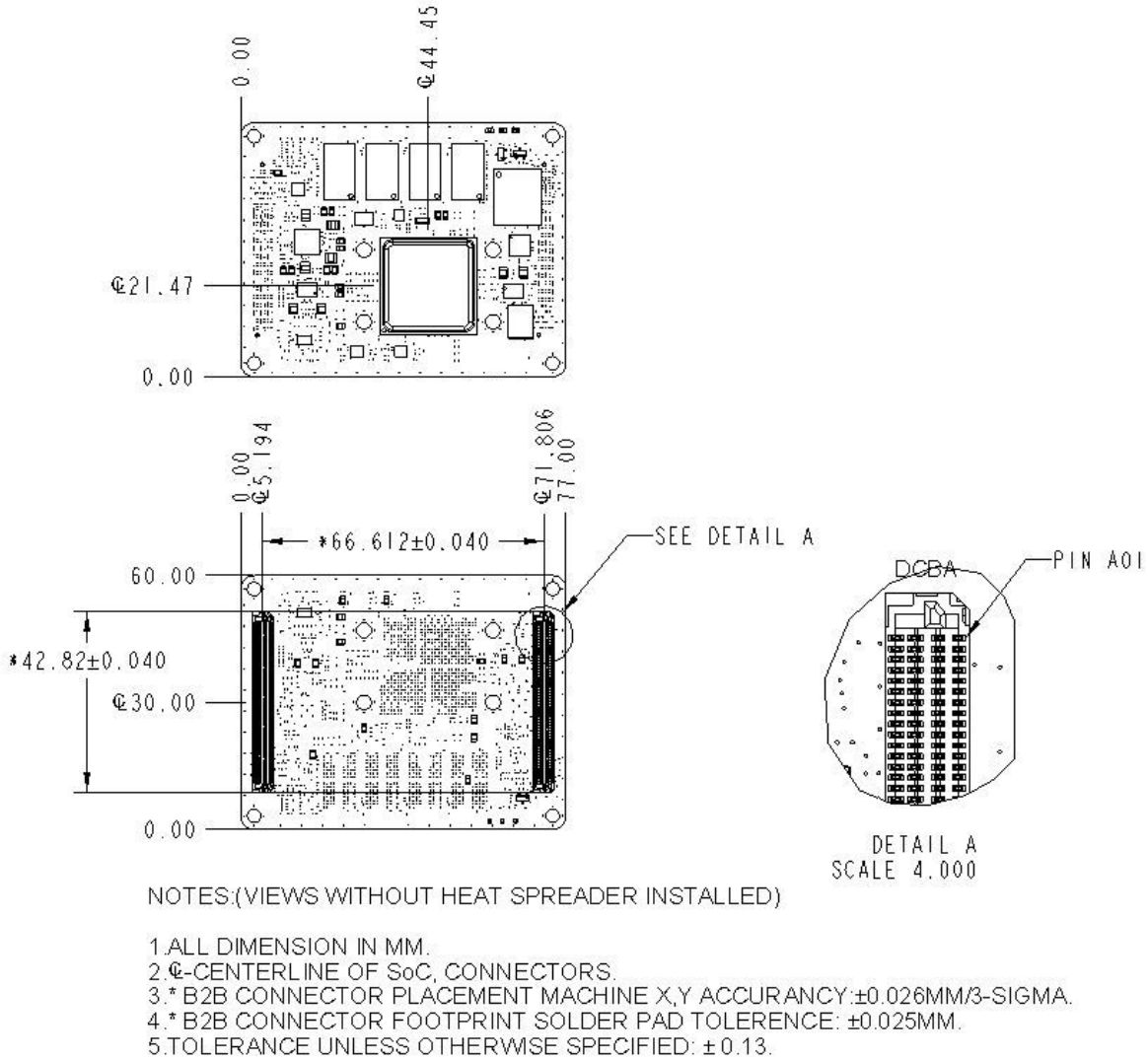
Note: PCB fab and assembly contractors must be able to produce carrier cards to the specifications listed in the PCB Fabrication and Assembly House Requirements section. In addition, the connectors that are shifted by 15% of the pad width must be capable of self-aligning after a reflow soldering process.

SOM to Carrier Card Samtec Connector Placement Guidelines

Both the commercial (C) grade and industrial (I) grade SOMs have two Samtec 0.635 mm AcceleRate® HD high-density, 4-row, 60-position connectors. The Samtec part number is ADF6-60-03.5-L-4-2-A. The connectors are placed on the bottom side of the carrier card centered between the mounting holes shown in Figure 2: K26 SOM Dimensions.

Board-to-board (B2B) mating connectors must be precisely placed on the PCB, particularly for multi-pair connector applications. Tight control is required during the board layout design and the manufacturing process for product reliability and a decent yield rate. To avoid over-stressing the mechanical design of the connectors and creating functional damage during system assembly, the next figure includes the recommended maximum position tolerance of the connector. Auto-placement machine accuracy and the tolerance of the connector pin solder pad position contributes to this recommendation.

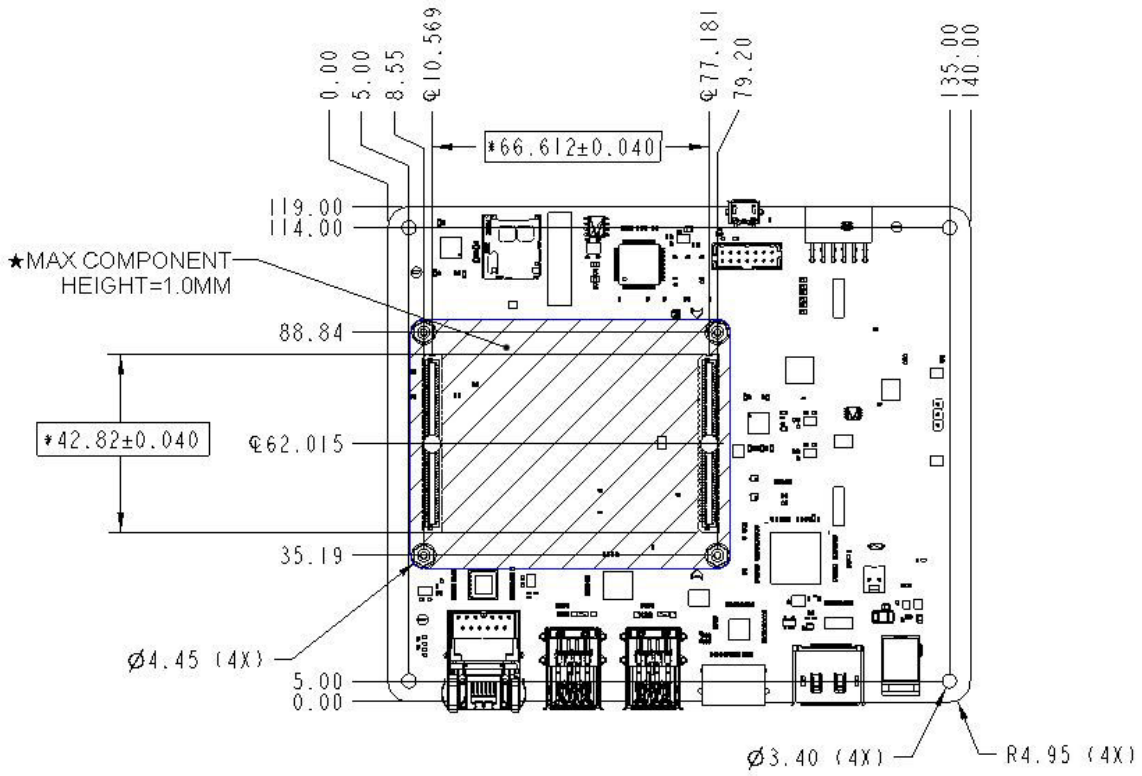
Figure 4: **K26 SOM Samtec Connector Position Tolerance**



Carrier Card Board to Board Connector Placement Guideline

Corresponding to the Samtec 0.635 mm AcceleRate HD connectors (ADF6-60-03.5-L-4-2-A) on the SOM, the mating connectors (ADM6-60-01.5-L-4-2-A) are placed on your carrier card. The two SOM mating connectors must be placed and positioned using a tightly controlled design and manufacture processing. The following figure shows the keep-out area and connector position tolerance information used on an example carrier card design. The keep out area defined maximum component height is 1.0 mm.

Figure 5: **Carrier Card Board to Board Connector Placement Tolerances**

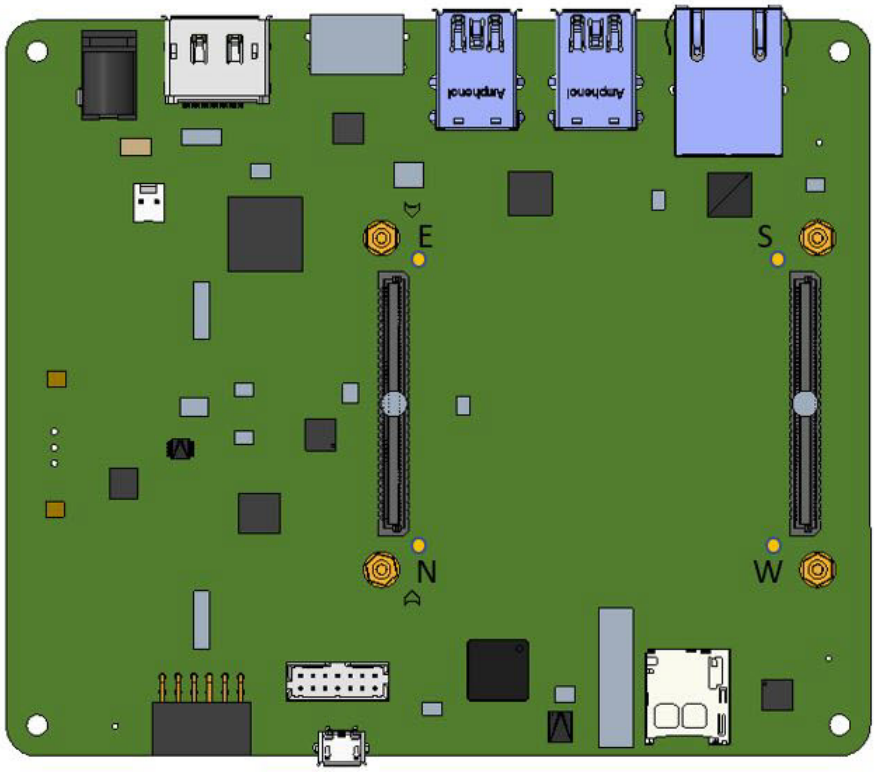


NOTES:

1.ALL DIMENSION IN MM.
2.℄-CENTERLINE OF CONNECTOR.
3.* B2B CONNECTOR PLACEMENT MACHINE X,Y ACCURANCY:±0.026MM/3-SIGMA.
4.* B2B CONNECTOR FOOTPRINT SOLDER PAD TOLERENCE: ±0.025MM.
5.★DETAIL COMPONENT KEEPOUT INFO REFER TO PCB LAYOUT DESIGN GUIDELINE.
6.TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.13.

During board-to-board insertion and removal, the installation process should work within the following recommended strain limits. The following figure shows the recommended locations (E–W, N–S) for a strain measurement on a carrier card. Diagonal strain should not exceed 500 micro-strain during mating. Strain rate duration taken to reach maximum 500 micro-strain should not be less than four seconds. Based on experimental data, the maximum strain of 428 micro-strain reached in 3.63 seconds duration and was validated through dye and pry, where the sample passed.

Figure 6: **Recommended Locations for Strain Measurement on a Carrier Card**



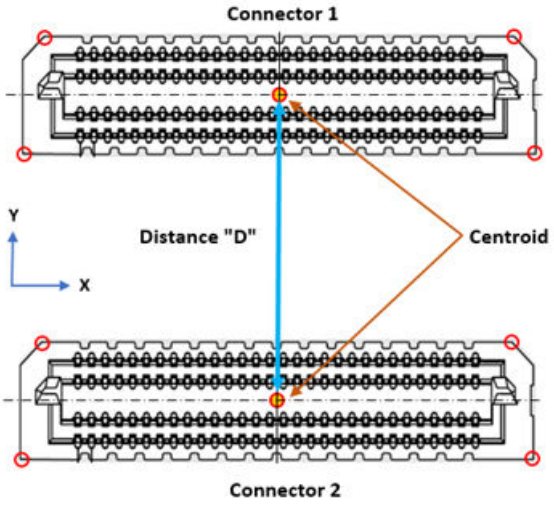
Board to Board Connector Distance Tolerance Control

The distance between the mating ADM6 connectors on the carrier card must match the distance between the ADF6 connectors on the SOM. The final connector position is dictated by auto-placement machine accuracy and PCB pad position tolerance. The way the distance is measured between connectors is crucial to ensure seamless board-to-board mating, without applying mechanical stress.

To determine the centroid of the connector, use the four corners of the connector edges marked with red circles as shown in the following figure. By using a high-accuracy optical measurement instrument, measure the distance *D*. Distance *D* should be 66.612 mm (nominal). The allowable distance *D* and tolerance is 66.612 ±0.04 mm center to center. The following table shows the recommended optical measurement instrument specifications.

Name	OGP Smartscope
Model	CNC670
Accuracy	±5 µm

Figure 7: **Connector Distance Measurement**

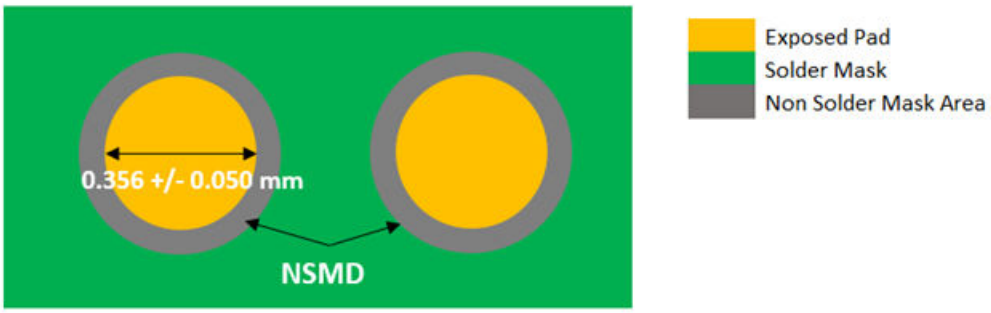


Board to Board Connector PCB Layout

Footprint Details

PCB pad design should be in a circular shape with diameter of 0.356 ±0.050 mm (14.0 ±2.0 mils). Non-solder mask defined (NSMD) pad design as shown in the following figure is recommended for better reliability performance.

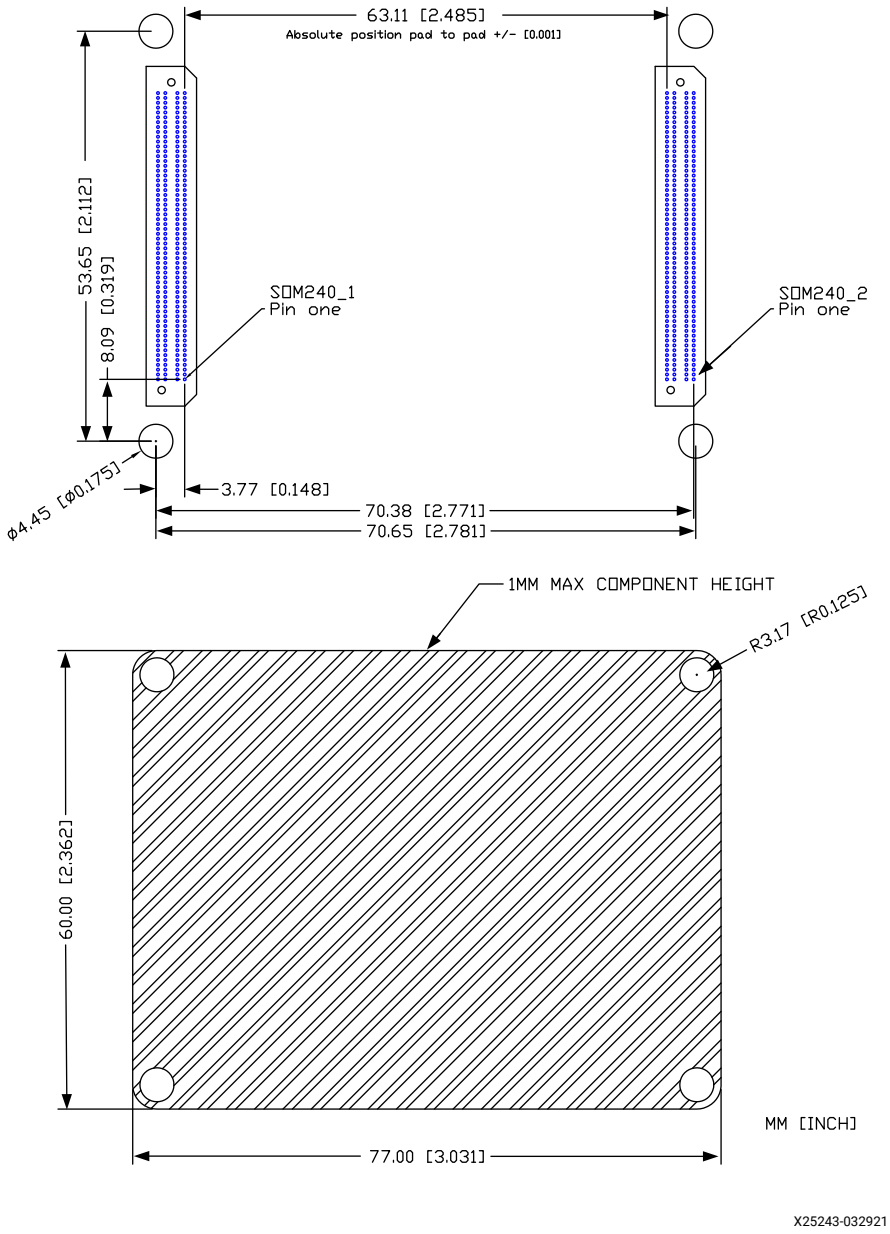
Figure 8: **Recommended PCB Layout for Board to Board Connector**



Board to Board Connector Pad Placement

The following figure outlines the carrier card connector pads and mechanical standoff relative placement.

Figure 9: **SOM240 Connector Pad and Standoff Placement**



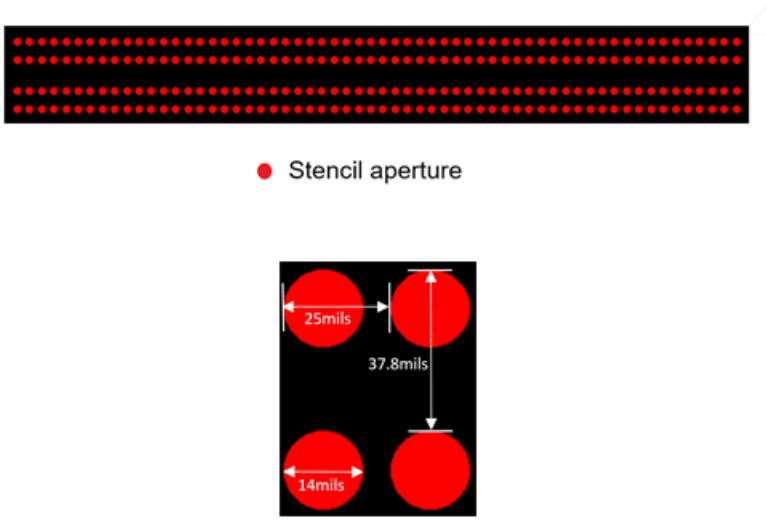
Board to Board Connector Stencil Design

To ensure that at time zero no crack has occurred, solder paste is applied to PCB metal pads using screen printing. The volume of the printed solder paste is determined by the stencil aperture and its thickness. In most cases, the thickness of a stencil must be matched to the needs of all components on the PCB. Stencil apertures should be a circular shape. A laser cutting (mostly made from stainless steel) with nickel blanking is preferred to ensure that both uniform and high-solder paste is transferred to the PCB. The recommended stencil design dimensions are listed in the following table and shown in the image.

Table 16: **Board to Board Connector Recommended Stencil Design**

Aperture Shape	Pitch	Diameter	Stencil Thickness
Round	25 mils and 37.8 mils	14 mils	5 mils

Figure 10: **Board to Board Connector Recommended Stencil Design**



Recommended Pb-free Reflow Soldering Profile

Xilinx does not support soldering SnAgCu BGA connectors with Sn/Pb solder paste during the soldering process. Traditional Sn/Pb soldering processes have a peak reflow temperature of 220°C. At this temperature range, the SnAgCu BGA solder balls cannot properly melt and wet to the soldering surfaces. As a result, reliability and assembly yields can be compromised.

The optimal profile must take a few factors into account:

- Solder paste flux used
- Size of the board
- Density of the components on the board
- Ratio of large and small, lighter components (the mixture)

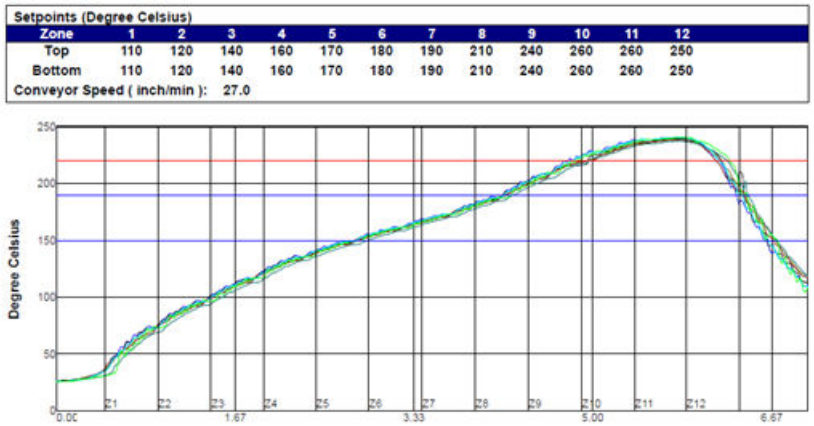
Profiles should be established for all new board designs using thermocouples placed at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various board locations to ensure that the minimum reflow temperature is reached on the larger components, and at the same time the temperature does not exceed the threshold that might damage the smaller, heat sensitive components.

The following tables and figures provide the recommended guidelines for Pb-free solder PCB assembly reflow. In general, a gradual-linear ramp into a spike is proven, by various sources, to be the optimal reflow profile for Pb-free solder. This profile results in a better wetting yield and less thermal shock than the conventional ramp-soak-spike profile. It is a known fact that SnAgCu (SAC) alloy reaches its full liquidus at a temperature of 235°C. In the reflow profiling, the coldest solder joints need to be identified and to ensure that they reach a minimum peak temperature of 235°C for at least 10 seconds. Reflowing at high-peak temperatures of 260°C or above can damage the heat sensitive components and cause board warpage. Refer to the latest IPC/JEDEC J-STD-020 standard for allowable peak temperature on the components. The allowable component peak temperature is determined by the component size. The following table lists the reflow soldering temperature profile information. In any case, use as low of a peak temperature reflow profile as possible. The following image shows an example of the reflow temperature profile.

Table 17: **Recommended Reflow Soldering Temperature Profile**

Profile Feature	Convection, IR/Convection
Preheat ramp-up rate 30°–150°C	3°C/s maximum
Preheat temperature soak time 150°–200°C	60–120 seconds
Temperature maintained above 217°C	60–120 seconds (60–90 seconds typical)
Time within 5°C of actual peak temperature	30 seconds maximum
Peak temperature (lead/ball)	235°C–245°C typical (depends on solder paste, board size, component mixture)
Ramp-down rate	4°C/s maximum

Figure 11: **Recommended Reflow Soldering Temperature Profile**



Carrier Card to SOM Standoff Press-fit Process

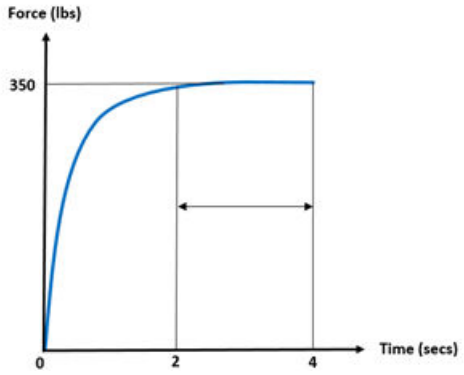
The carrier card to SOM interface requires a 5 mm (height) mechanical stand-off.

In cases where there is an expectation that the SOM will be removed from the carrier card, the recommended solution is to use the following Samtec JSOM. The Samtec JSOM-0515-01 standoffs require a press-fit process to install them onto the PCB. The JSOM standoff press-fit recommended parameters are shown the following table and the press profile is shown in the following diagram.

Table 18: **JSOM Standoff Press-fit Parameters**

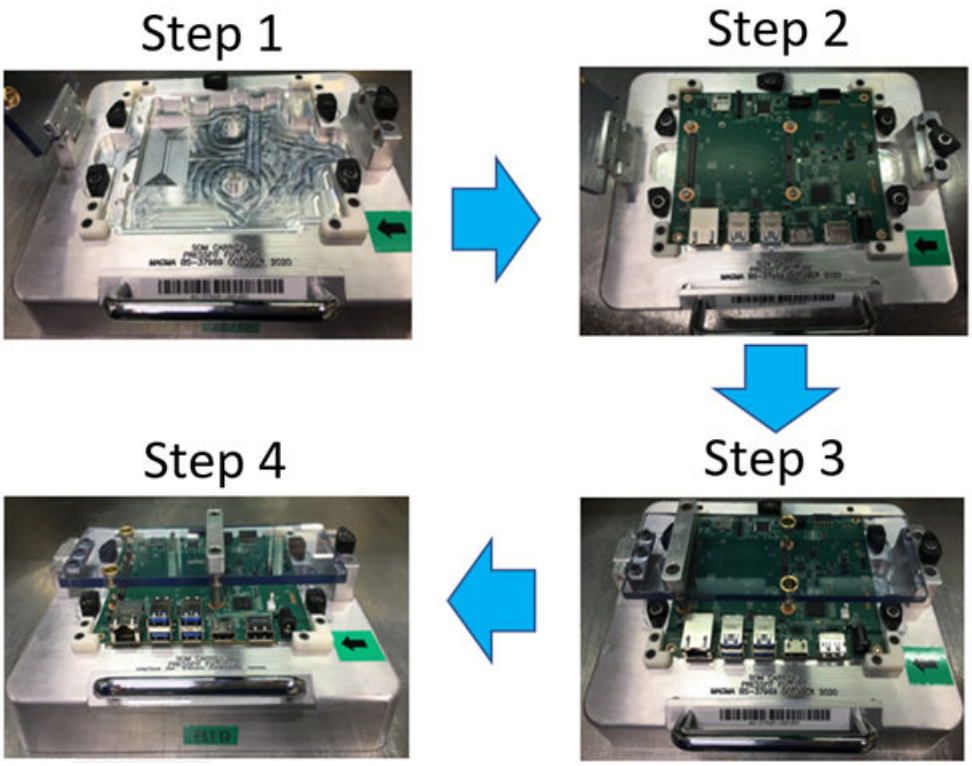
Press Parameter	Setting	Unit	Press Time
Force	350 ±10	lbs	2 secs

Figure 12: **Press Profile (Force Over Time)**



The following images detail the installation process by using a press-fit jig.

Figure 13: **JSOM Standoff Installation Steps**

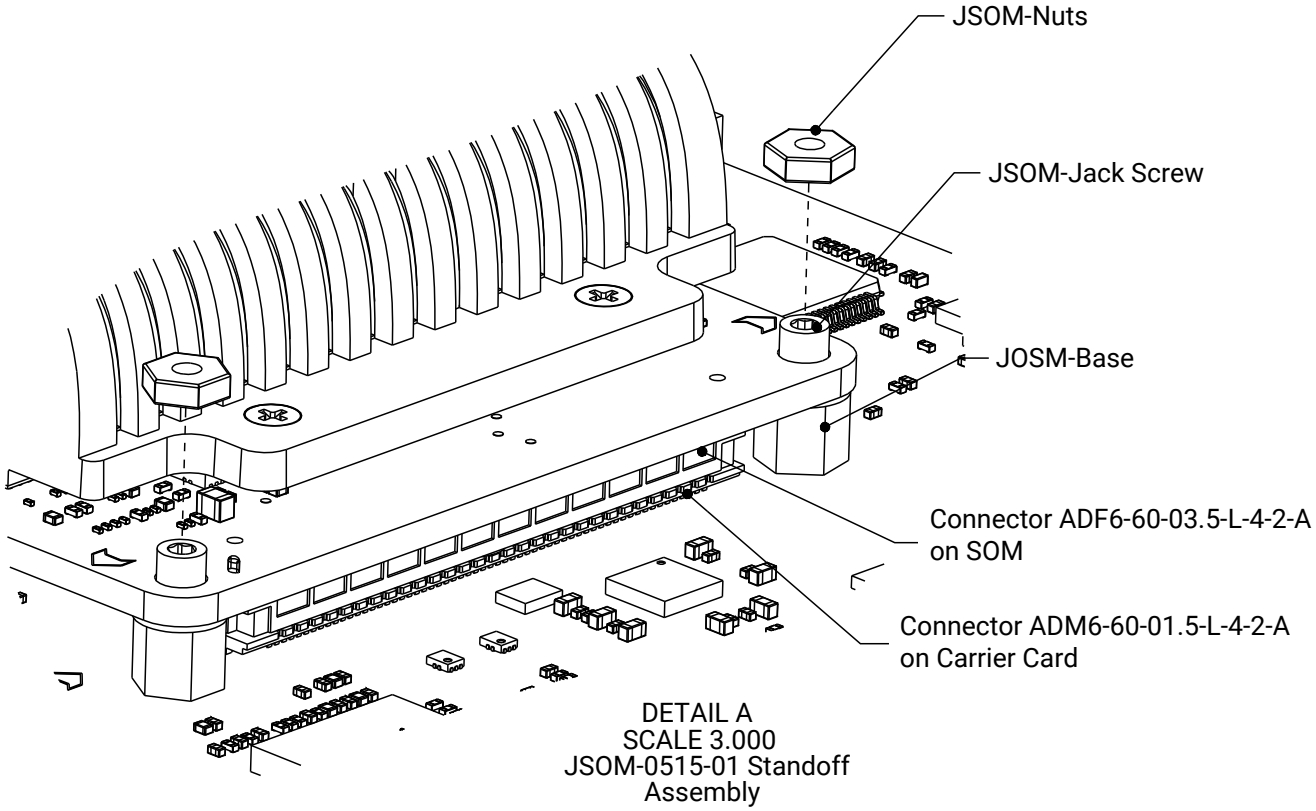


1. Open the top cover of the press-fit jig
2. Place the carrier card on the press-fit jig and insert the JSOM standoff. Close the press-fit jig cover.
3. Insert the connector top tool in the press-fit cover and place it on top of the two JSOMs located beside connector JA2. Press the JSOM standoff into the card following the parameters listed in Table 18: JSOM Standoff Press-fit Parameters. Remove the top tool once the press-fit is completed.
4. Repeat step 3 to install the JSOM standoff located beside connector JA1. Remove the board from the jig and inspect whether the JSOM standoff is fully flush.

Board to Board Assembly Guidelines

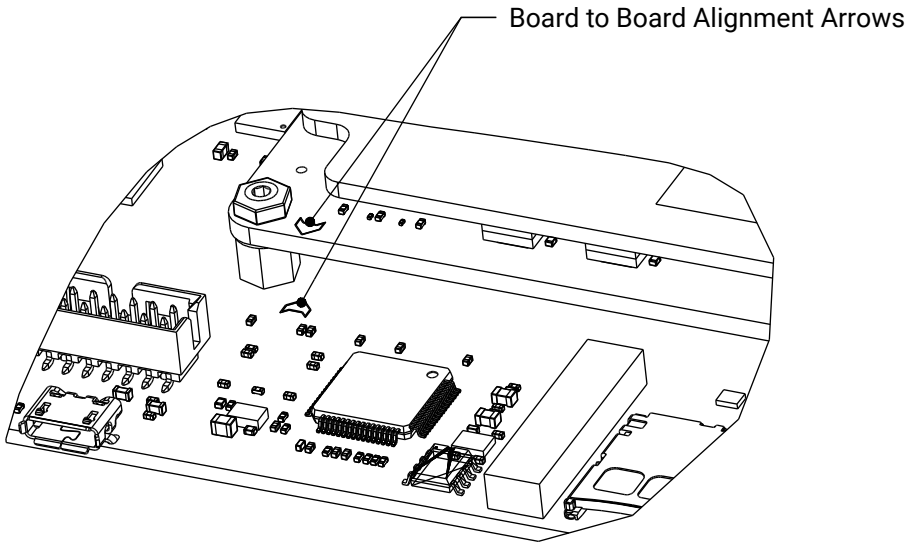
Samtec jack screw standoff, part number JSOM-0515-01, is recommended by Samtec to be used as mechanical support in its board-to-board (B2B) connector assembly. This JSOM type standoff protects connectors from over mechanical stresses during mating and de-mating assembly.

Figure 14: **B2B Assembly with Samtec JSOM Standoffs**



A recommended best practice is to put board-to-board alignment arrows on your carrier card silkscreen to aid in the orientation of the SOM to carrier card. It is important to check the connector alignment key positions before gently pressing down to fully engage the B2B connectors.

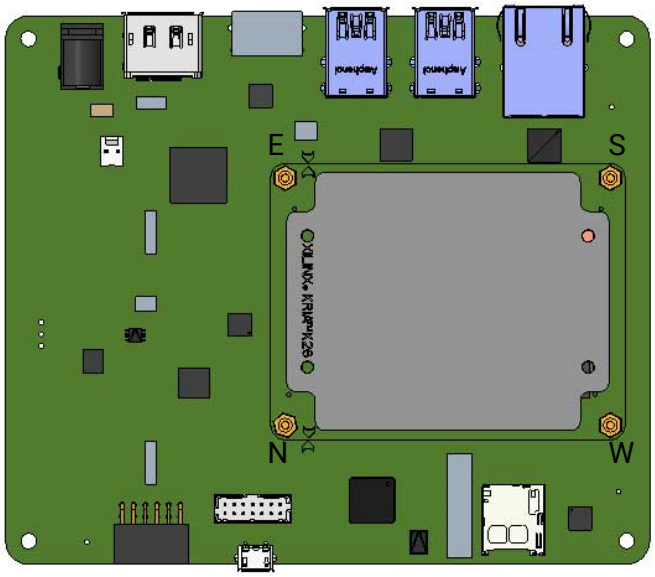
Figure 15: **B2B Connector Orientation and Alignment**



Mating: JSOM Standoff-nut Tighten Sequence and Torque Setup

To protect the mating connector from over mechanical stress and to minimize strain during board-to-board assembly, it is important to tighten the standoff nut in a specific sequence. The recommended mechanical standoff tightening sequence (S > W > N > E) is shown in the following figure. Once the S and W nuts are tightened, the SOM board will be almost flat to the carrier card. The subsequent tightening of nuts N and E ensure the SOM and carrier connectors are completely engaged.

Figure 16: **Connector Mating Sequence**



The recommended torque driver setting and operation parameters are specified in the following table.

Table 19: **Torque Driver Information**

Torque Driver	Controller Module	Torque Driver	Torque Setting	Assembly Duration	RPM Setting for Each Step
Smart Torque Electrical Driver	Atlas Copco MTF600	ETD M 50 ABL V2	3.0 in.lbs (±0.5 in.lbs)	10 secs	Step 1: 300 RPM
					Step 2: 600 RPM
					Step 3: 150 RPM

De-mating: JSOM Standoff-nut and Jack Screw Untighten Sequence

There is no special sequence required to untighten the four standoff nuts. However, they must be removed before proceeding to untighten the four jack screws. The order to untighten the four jack screws is not critical. Once all four of the jack screws are completely untightened, the SOM board will pop up and the SOM connectors (male) automatically uncouple from the connectors (female) on the carrier card. Remove the SOM by carefully holding the card on the two edges.

SOM System B2B Connector Assembly Validation-DOE (To Ensure Time 0 No Crack)

The Samtec ADF and ADM connectors placement were shifted 0% and 15% (based on connector pad diameter) on the X and Y-axis for both the SOM and carrier cards. The shifted connectors were reflowed and were able to mate without any issue.

The mated connector boards were submitted for cross section testing to validate their mating conditions. Based on the cross-section images, the connectors which shifted by 15% were able to self-align during reflow soldering. The following photos are a cross section image of the mated connectors. The proper contact of the female and male connector pins is achieved.

Figure 17: **Cross-section Image of Mated Connectors for 0% Shift**

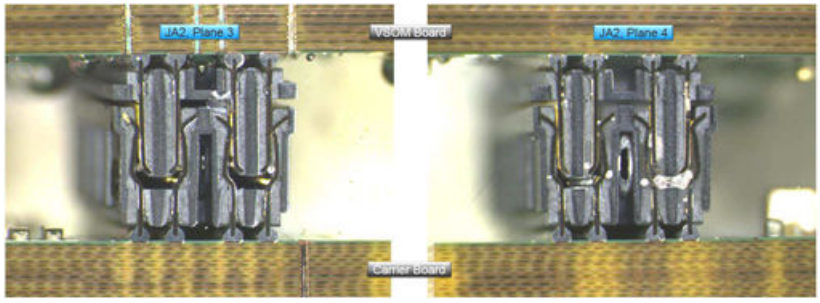
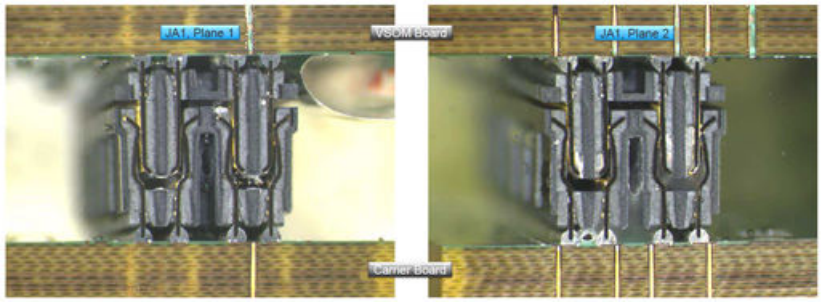


Figure 18: **Cross-section Image of Mated Connectors for 15% Shift**



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Chapter 4

Hardware Configuration Using Vivado Tools

The following section provides an overview of the Vivado® Design Suite carrier card hardware design support.

Vivado Tools Board File

The Vivado tools board file provides a design abstraction to capture aspects of the hardware configuration that are fixed by the SOM physical hardware design. The board file, when combined with the Vivado tools board automation, can pre-populate the MIO configuration associated with these SOM fixed peripherals:

- DDR4 memory interface and associated timing configuration
- QSPI non-volatile memory and associated clocking
- eMMC non-volatile memory and associated clocking
- SPI interface for a trusted platform module (TPM)
- I2C peripheral bus for SOM peripherals and extensible via carrier card design
- UART for board bring-up and software debug (assumes the carrier card pins out MIO36 and MIO37 for proper UART function)
- PMU input/output (need to check default board file configuration)

The SOM is available in a Vivado tools board file on the Xilinx® GitHub Board Store.

Documentation on installing and using the Vivado tools board files is available in the Wiki referenced on the Xilinx GitHub.

Vivado Software SOM Connector Abstraction

The SOM board files introduce a SOM connector abstraction that allows the hardware configuration to focus on SOM connector level physical mapping. This is intended to help eliminate the need for the carrier card designer to have to create a physical pin translation table.

The SOM connector infrastructure uses the convention of: `<connector name> + <_> + <connector_pin_number>`. For example, a SOM connector pin name of `som240_1_c18` refers to the pin C18 of the SOM240_1 connector. Using this convention and the XDC *get ports* functionality, a carrier card constraints file can be described in terms of a SOM physical interface when combined with a SOM constraint file that captures the Zynq® UltraScale+™ MPSoC to SOM connector pin definition.

SOM Vivado Tools XDC Files

The SOM Vivado board file includes an XDC file that captures the Zynq UltraScale+ MPSoC package mapping to SOM connector pin definitions. This file can be used by the carrier card designer to identify the full SOM plus carrier card design constraints.

A carrier card designer can also refer to the KV260 Starter Kit carrier card XDC files for an example implementation of a decoupled SOM and carrier card constraint definition.

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Appendix A

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

***Note*:** For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

1. *Kria K26 SOM Data Sheet* (DS987)
2. *Kria K26 SOM Thermal Design Guide* (UG1090)
3. *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925)
4. *Kria KV260 Vision AI Starter Kit User Guide* (UG1089)
5. *Kria KV260 Vision AI Starter Kit Data Sheet* (DS986)
6. *UltraScale Architecture SelectIO Resources User Guide* (UG571)
7. *UltraScale Architecture PCB Design User Guide* (UG583)
8. *Zynq UltraScale+ Device Technical Reference Manual* (UG1085)
9. *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide* (UG1075)
10. *Bootgen User Guide* (UG1283)
11. *UltraScale Architecture System Monitor User Guide* (UG580)
12. Associated files:
    a. Kria K26 SOM XDC file (XTP685)
    b. Kria K26 carrier card XDC file (XTP686)
    c. Kria K26 trace delay values (XTP688)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
3/16/2022 Version 1.2	
Chapter 1: Introduction	Updated Figure 1: K26 SOM Block Diagram
Signal Naming Conventions	Added Table 3: Legend for Pin Types. Added signal to connector mapping using XDC file discussion.
SOM240_1 Signal Names and Descriptions	Added the pin type column and updated the descriptions for B28 (MIO35), B29 (MIO36), B30 (MIO37), C30 (MIO29), and C31 (MIO30), and C32 (MIO31).
SOM240_2 Connector Pinout	Updated A4 description.
SOM240_2 Signal Names and Descriptions	Added the pin type column.
Supported I/O Standards	Added power-up and configuration information.
PS-GTR Transceivers	Added additional transceiver details.
GTH Transceivers	Added additional transceiver details.
Transceiver Reference Clocks	Added additional transceiver details.
SOM Configuration and Control Signals	Clarifying edits to PS_ERROR_OUT Signal, PS_ERROR_STATUS Commands section.
Power Management Signals	Updated descriptions on the signals in this section.

Section	Revision Summary
SOM MIO Design Considerations	Updated mapping instructions and bank diagrams.
Mechanical Dimensions	Added clarifying edits to the Figure 2: K26 SOM Dimensions mechanical drawing.
7/23/2021 Version 1.1	
Chapter 1: Introduction	Updated Figure 1: K26 SOM Block Diagram.
SOM240_1 Connector Pinout	Updated MIO35_WD_OUT and MIO26.
SOM240_1 Signal Names and Descriptions	Updated descriptions in table.
SOM240_2 Connector Pinout	Corrected errors in table.
SOM240_2 Signal Names and Descriptions	Updated descriptions in table.
Supported I/O Standards	Added description of XCK26 device.
SOM I/O Timing Model	Added information on designing with trace length and signal delays, and removed Table 7: K26 SOM PCB Signal Delays by I/O Bank
Sideband Signals	Added PS_REF_CLK and PS_PAD_I/O.
SOM Connector Power Pins	Updated the V_{BATT} recommended conditions Table 10: SOM Power Rails. Added discussion on connecting unused I/O bank VCCO pins.
Power Management	Added further details on power management and PWRGD signals.
SOM Power Estimation	Added link to *Kria K26 SOM Thermal Design Guide* (UG1090).
Carrier Card Board to Board Connector Placement Guideline	Corrected Samtec mating connector model (ADM6–60–01.5–L–4–2–A).
References	Added link to *Kria K26 SOM Thermal Design Guide* (UG1090).
4/20/2021 Version 1.0	
Initial release.	N/A

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