FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27204-6E

ASSP
BIPOLAR

SWITCHING REGULATOR CONTROLLER

MB3775

■ LOW VOLTAGE DUAL PWM SWITCHING REGULATOR CONTROLLER

The MB3775 is a dual pulse-width-modulation control circuit. It contains the basic circuits required for two PWM control circuits. Complete synchronization is obtained by using the same oscillator output waveform.
This IC can provide following types of output voltage: step down, step up, and inverter. Power consumption is low, thus the MB3775 is ideal for use in high-efficiency portable equipment.

■ FEATURES

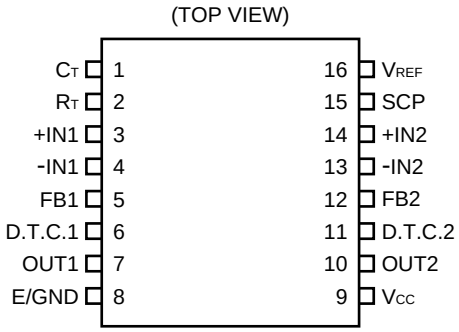
- Wide supply voltage range: 3.6 V to 18 V
- Low current consumption: 1.3 mA typical
- Wide oscillation frequency range: 1 kHz to 500 kHz
- On-chip timer latch short protection circuit
- On-chip under voltage lockout protection
- On-chip reference voltage: 1.28 V
- Variable dead time provides control over total operating range.
- Two types of packages (SOP-16pin : 1 type, SSOP-16pin : 1 type)

■ APPLICATIONS

- LCD monitor/panel
- Surveillance camera etc.

2010.9

■ PIN ASSIGNMENT

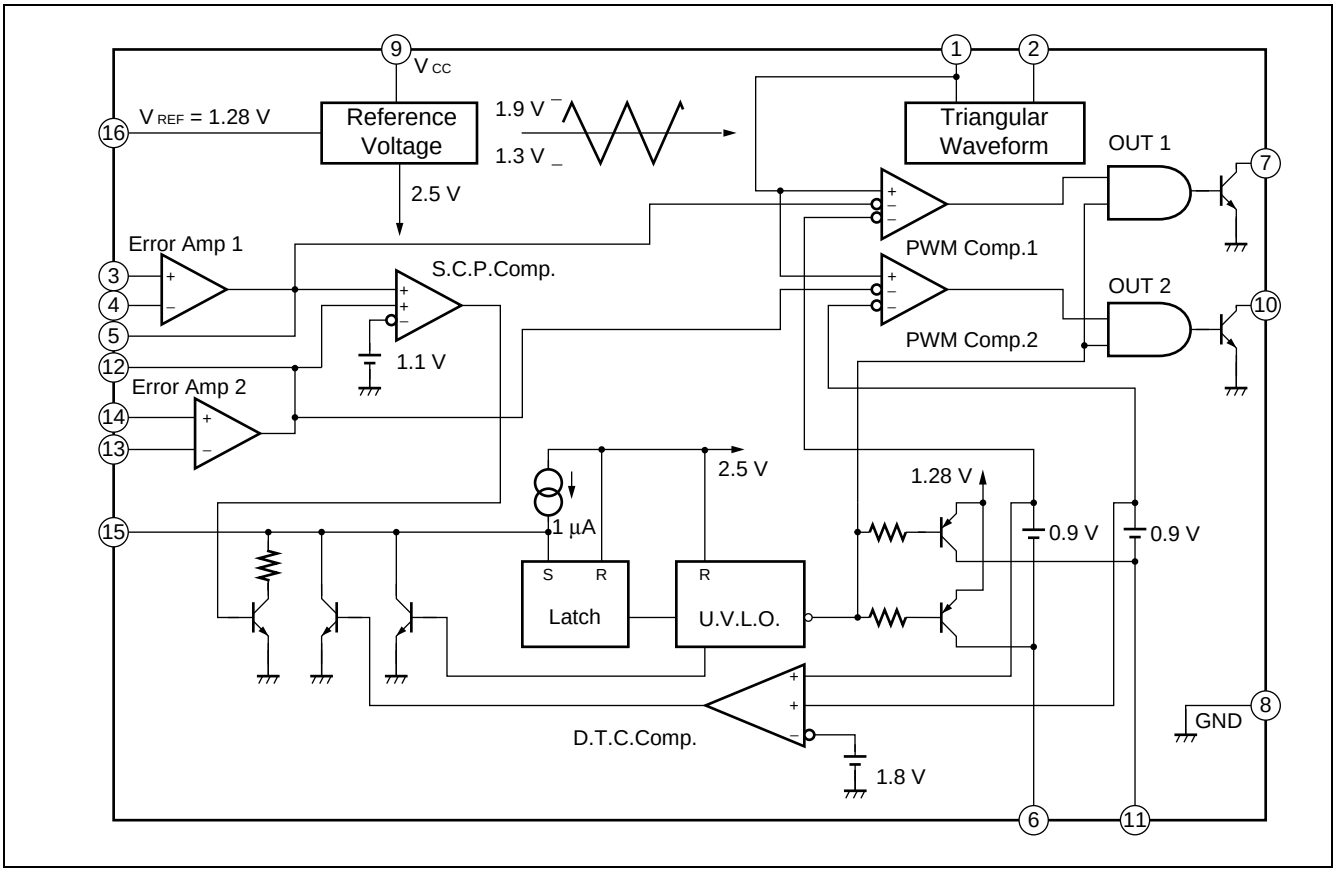


(FPT-16P-M06)
(FPT-16P-M05)

■ PIN DESCRIPTION

No.	Pin	Function
1	C_T	Oscillator timing capacitor pin (150 pF to 15,000 pF) .
2	R_T	Oscillator timing resistor pin (5.1 kΩ to 100 kΩ) .
3	+IN1	Error amplifier 1 non-inverted input pin.
4	–IN1	Error amplifier 1 inverted input pin.
5	FB1	Error amplifier 1 output pin. A resistor and a capacitor are connected between this pin and the –IN1 pin to adjust gain and frequency.
6	DTC1	OUT1 dead-time control pin. Dead-time control is adjusted by an external resistive divider connected to the V_{REF} pin. A capacitor connected between this pin and GND enables soft-start operation.
7	OUT1	Open collector output pin. Output transistor has common ground independent of signal ground. This output can source or sink up to 50 mA.
8	E/GND	Ground pin.
9	V_{CC}	Power supply pin (3.6 V to 18 V)
10	OUT2	Open collector output pin. Output transistor has common ground independent of signal ground. This output can source or sink up to 50 mA.
11	DTC2	Sets the dead-time of OUT2. The use of this pin is the same as that of DTC1.
12	FB2	Error amplifier 2 output pin. A resistor and a capacitor are connected between this pin and the -IN2 pin to adjust gain and frequency.
13	–IN2	Error amplifier 2 inverted input pin.
14	+ IN2	Error amplifier 2 non-inverted input pin.
15	SCP	The time constant setting capacitor connection pin of the timer latch short-circuit protection circuit. Connects a capacitor between this pin and GND. For details, see “■ HOW TO SET TIME CONSTANT FOR TIMER LATCH SHORT-CIRCUIT PROTECTION CIRCUIT”.
16	V_{REF}	1.28 V reference voltage output pin which can be obtained up to 1 mA. This pin is used to set the reference input and idle period of the error amplifiers.

■ BLOCK DIAGRAM



■ OPERATION DESCRIPTION

1. Reference voltage

The reference voltage circuit generates a stable, temperature-compensated 2.5 V reference from Vcc pin (pin 9) for use by internal circuits.
A reference voltage of temperature compensated 1/2 V_{REF} can be obtained to external circuit by V_{REF} pin (pin 16).

2. Oscillator

A triangular waveform of any frequency is obtained by connecting an external capacitor and resistor to the C_T pin (pin 1) and R_T pin (pin 2).
The amplitude of this waveform is from 1.3 V to 1.9 V. The oscillator is internally connected to the non-inverting inputs of the PWM comparators. The oscillator waveform is available at the C_T pin (pin 1).

3. Error amplifiers

The error amplifier detects the output voltage of the switching regulator.
The common-mode input voltage range is –0.2 V to 1.45 V, so the input reference voltage can be set the V_{REF} pin (pin 16) and GND pin levels. Error amplifiers can be used as either inverting and non-inverting amplifiers.
The voltage gain is fixed. Phase compensation is possible by connecting a capacitor to the FB pins (pins 5 and 12) of the error amplifiers.
The error amplifier output are internally connected to the inverting inputs of the PWM comparators and also to the short protection circuit.

4. Timer latch short protection circuit

The timer latch short protection circuit detects the output levels of the error amplifiers. If one or both error amplifier outputs are 1.1 V or lower, the timer circuit begins charging the externally connected protection enable capacitor. If the output level of the error amplifier does not drop below the normal voltage range before the capacitor voltage reaches the transistor base-emitter voltage V_{BE} (≒ 0.65 V), the latch circuit turns the output drive transistor off and sets the dead time to 100 %.

5. Under voltage lockout protection circuit

An ambiguous transition state at power-on or a momentary fluctuation in the supply line may result in loss of control and may adversely affect or even destroy the system. The under voltage lockout protection circuit compares the internal reference voltage level with the supply voltage level. If the supply voltage level falls below the reference level the latch circuit is reset the output drive transistor is turned off and the dead time is set to 100%. The protection enable pin (pin 15) is pulled “Low”.

6. PWM comparator

Each PWM comparator has two inverting inputs and one non-inverting input. This voltage-to-pulse-width converter controls the output pulse width according to the input voltage.
The PWM comparator turns the output drive transistor on when the oscillator triangular waveform is higher than the error amplifier output and the dead time control pin voltage.

7. Output drive transistor

The open-collector output-drive transistors provide common-emitter output of 18 V dielectric capability. The output drive transistors can source up to 50 mA of drive current to the switching power transistor.

■ ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power Supply Voltage	V_{CC}	—	—	20	V
Error Amp Input Voltage	V_I	—	–0.3	+10	V
Collector Output Voltage	V_O	—	—	20	V
Collector Output Current	I_O	—	—	75	mA
Power Dissipation	P_D	Ta ≤ +25 °C(SOP)	—	*620	mW
		Ta ≤ +25 °C(SSOP)	—	*430	mW
Operating Ambient Temperature	Ta	—	–30	+85	°C
Storage temperature	T_{stg}	—	–55	+125	°C

*: The packages are mounted on the epoxy board (4 cm x 4 cm x 1.5 mm).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	3.6	6.0	18	V
Error Amp Input Voltage	V_I	–0.2	—	+1.45	V
Collector Output Voltage	V_O	—	—	18	V
Collector Output Current	I_O	0.3	—	50	mA
Phase Compensation Capacitor	C_P	—	0.1	—	µF
Timing Capacitor	C_T	150	—	15000	pF
Timing Resistor	R_T	5.1	—	100	kΩ
Oscillator Frequency	f_{OSC}	1	—	500	kHz
Reference Voltage Output Current	I_{REF}	–3	–1	—	mA
Operating Ambient Temperature	Ta	–30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = +25 °C, V_{CC} = 6 V)

Parameter		Condition	Symbol	Value			Unit
				Min	Typ	Max	
Reference Section	Output Voltage	I_{OR} = –1 mA	V_{REF}	1.26	1.28	1.30	V
	Output Temp. Stability	Ta = –30 °C to +85 °C	V_{RTC}	–2	±0.2	+2	%
	Input Stability	V_{CC} = 3.6 V to 18 V	Line	—	2	10	mV
	Load Stability	I_{OR} = –0.1 mA to –1 mA	Load	—	1	7.5	mV
	Short Circuit Output Current	V_{REF} = 0 V	I_{OS}	—	–30	–10	mA
Under Voltage Lockout Protection Section	Threshold Voltage	I_{OR} = –0.1 mA	V_{tH}	—	2.72	—	V
		I_{OR} = –0.1 mA	V_{tL}	—	2.60	—	V
	Hysteresis Width	I_{OR} = –0.1 mA	V_{HYS}	80	120	—	mV
	Reset Voltage (V_{CC})	—	V_R	1.5	1.9	—	V
Protection Circuit Section	Input Threshold Voltage	—	V_{tPC}	0.60	0.65	0.7	V
	Input Stand by Voltage	No pull up	V_{STB}	—	50	100	mV
	Input Latch Voltage	No pull up	V_I	—	50	100	mV
	Input Source Current	—	I_{bpc}	–1.4	–1.0	–0.6	µA
	Comparator Threshold Voltage	Pin 5, Pin 12	V_{tC}	—	1.1	—	V
Triangular Waveform Oscillator Section	Oscillator Frequency	C_T = 330 pF, R_T = 15 kΩ	f_{OSC}	—	200	—	kHz
	Frequency Deviation	C_T = 330 pF, R_T = 15 kΩ	f_{dev}	—	10	—	%
	Frequency Stability (V_{CC})	V_{CC} = 3.6 V to 18 V	f_{dV}	—	1	—	%
	Frequency Stability (Ta)	Ta = –30 °C to +85 °C	f_{dT}	–4	–	+4	%
Dead-Time Control Section	Input Threshold Voltage (f_{OSC} = 10 kHz)	Duty Cycle = 0 %	V_{t0}	—	1.0	V_{REF} –0.15	V
		Duty Cycle = 100 %	V_{t100}	0.2	0.4	—	V
	Input Bias Current	—	I_{bdt}	—	–0.2	–1	µA
	Latch Mode Source Current	V_{dt} = 0.7 V	I_{dt}	—	–150	–80	µA
	Latch Input Voltage	Idt = –40 µA	Vdt	V_{REF} –0.1	—	—	V

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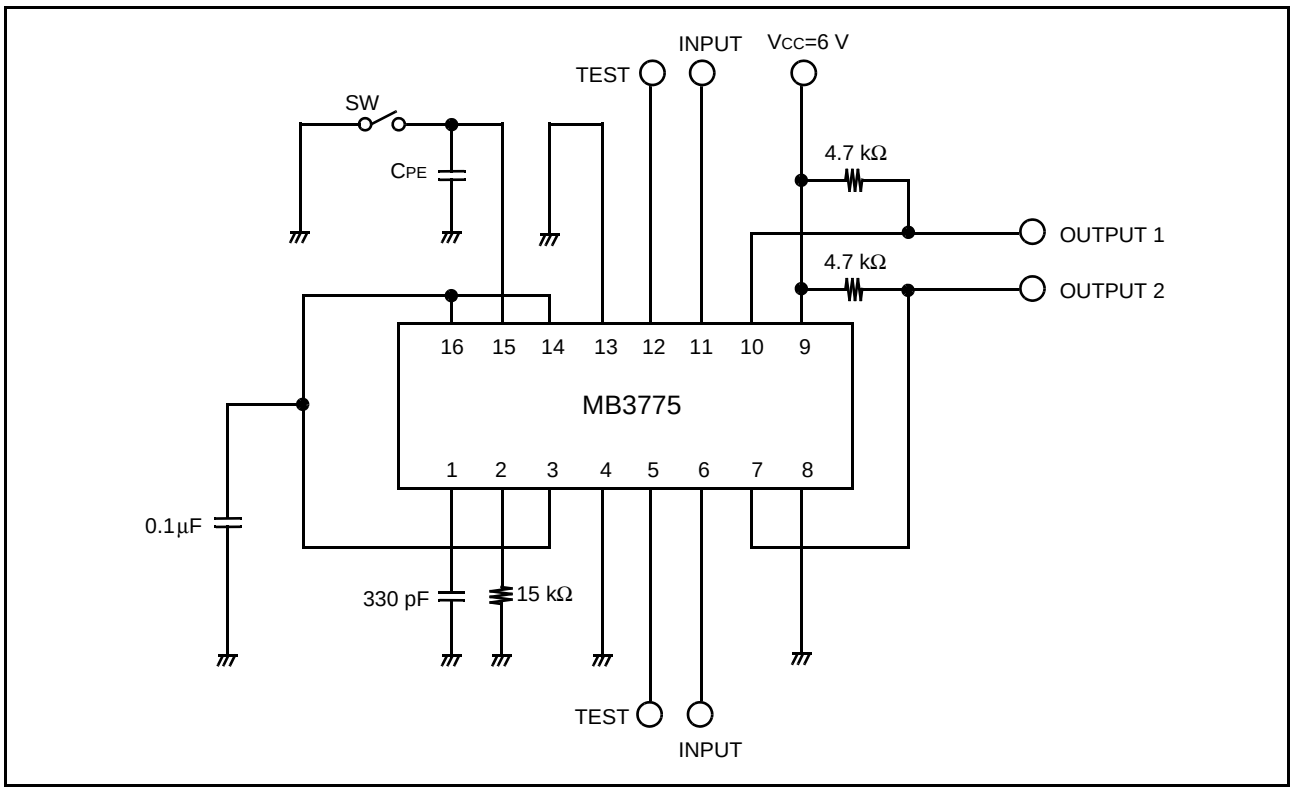
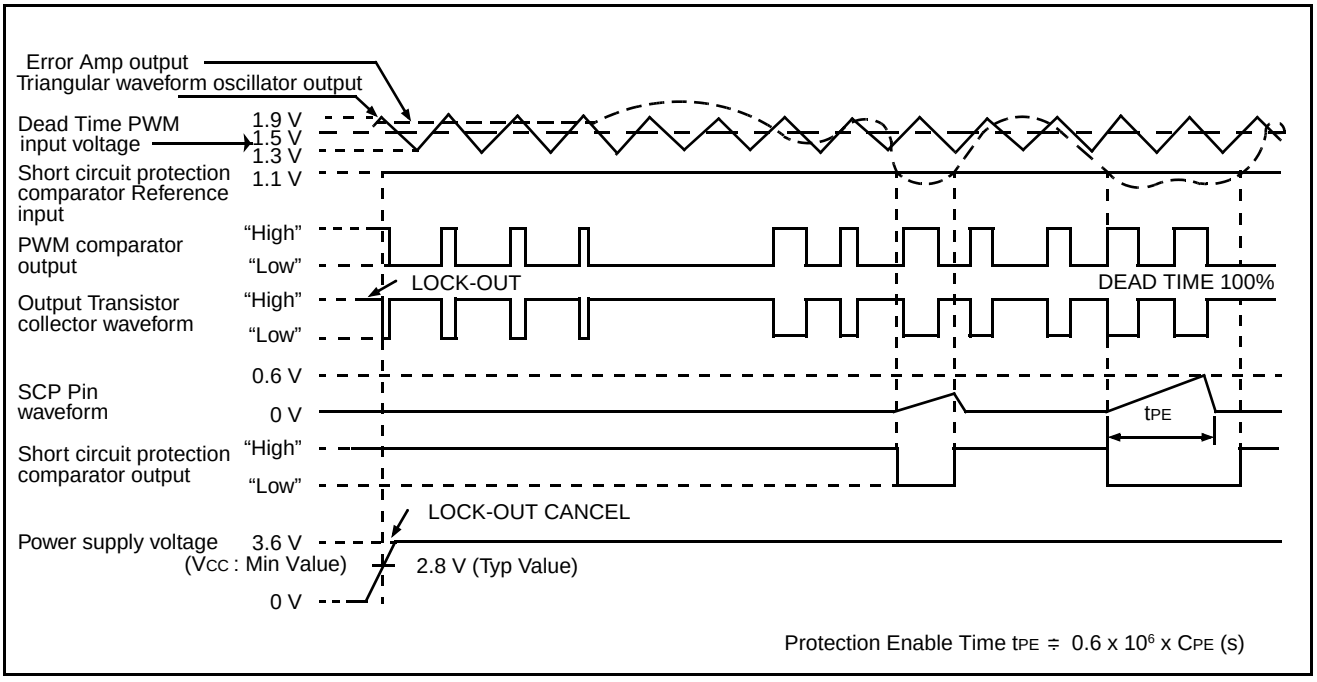
(Ta = +25 °C, V_{CC} = 6 V)

Parameter		Condition	Symbol	Value			Unit
				Min	Typ	Max	
Error Amp Section	Input Offset Voltage	V_O = 1.6 V	V_{IO}	–10	—	+10	mV
	Input Offset Current	V_O = 1.6 V	I_{IO}	–100	—	+100	nA
	Input Bias Current	V_O = 1.6 V	I_B	–500	–100	—	nA
	Common Mode Input Voltage Range	V_{CC} = 3.6 V to 18 V	V_{ICR}	–0.2	—	+1.45	V
	Voltage Gain		A_V	84	120	—	V/V
	Frequency Band Width	A_V = –3 dB	BW	—	3	—	MHz
	Common Mode Rejection Ratio		CMRR	60	80	—	dB
	Max Output Voltage Width		V_{OM+}	2.2	2.4	—	V
			V_{OM-}	–	0.7	0.9	V
	Output Sink Current	V_O = 1.6 V	I_{OM+}	24	50	—	µA
	Output Source Current	V_O = 1.6 V	I_{OM-}	—	–1.2	–0.7	mA
PWM Comparator Section	Input Threshold Voltage (f_{OSC}=10 kHz)	Duty Cycle = 0 %	V_{t0}	—	1.9	2.1	V
		Duty Cycle = 100 %	V_{t100}	1.05	1.3	—	V
	Input Sink Current	Pin 5, Pin 12 = 1.6 V	I_{IN+}	24	50	—	µA
	Input Source Current	Pin 5, Pin 12 = 1.6 V	I_{IN-}	—	–1.2	–0.7	mA
Output Section	Output Leak Current	V_O = 18 V	Leak	—	—	10	µA
	Output Saturation Voltage	I_O = 50 mA	V_{SAT}	—	1.1	1.4	V
Stand by Current		Output “OFF”	I_{CCS}	—	1.3	1.8	mA
Average Supply Current		R_T = 15 kΩ	I_{CCa}	—	1.7	2.4	mA

■ TEST CIRCUIT



■ TIMING CHART (Internal Waveform)



■ APPLICATION CIRCUIT

Fig. 1 - Chopper Type Step Down/Inverting

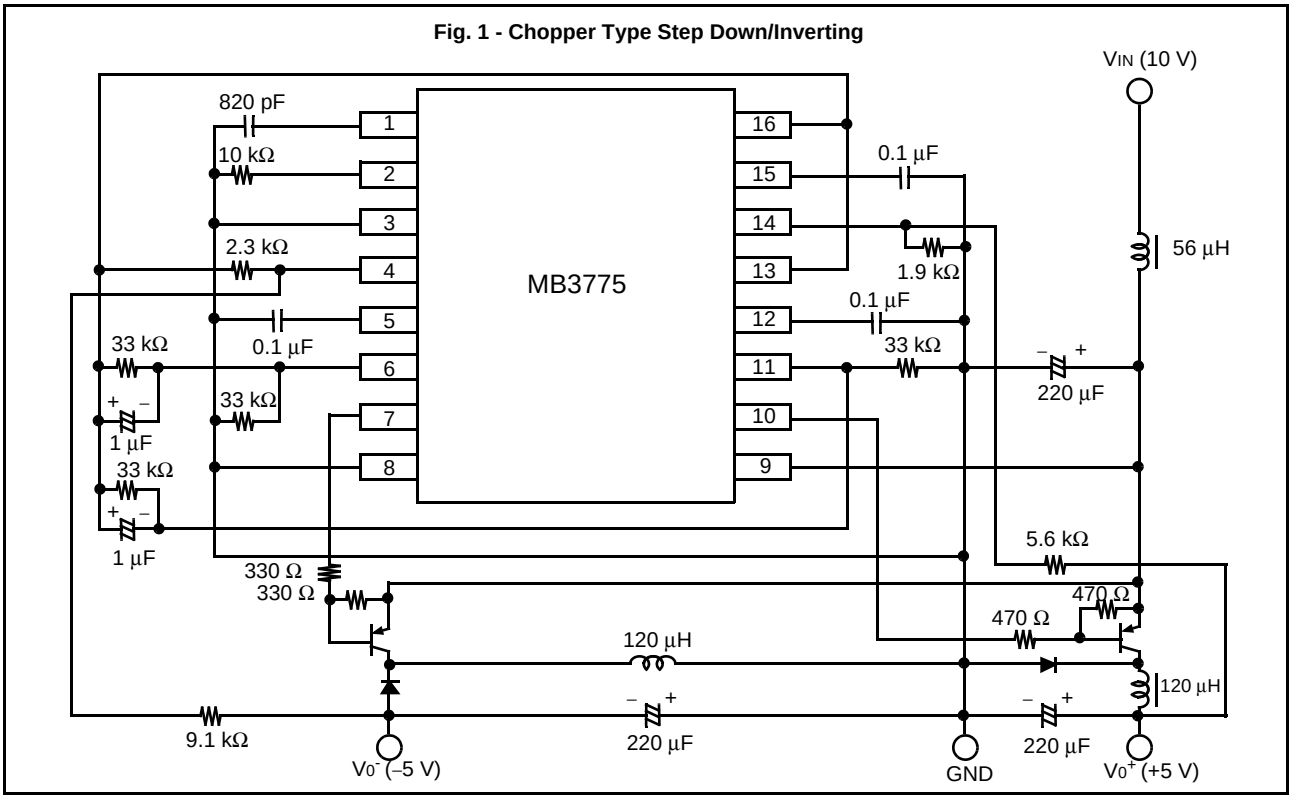


Fig. 2 - Chopper Type Step Up/Inverting

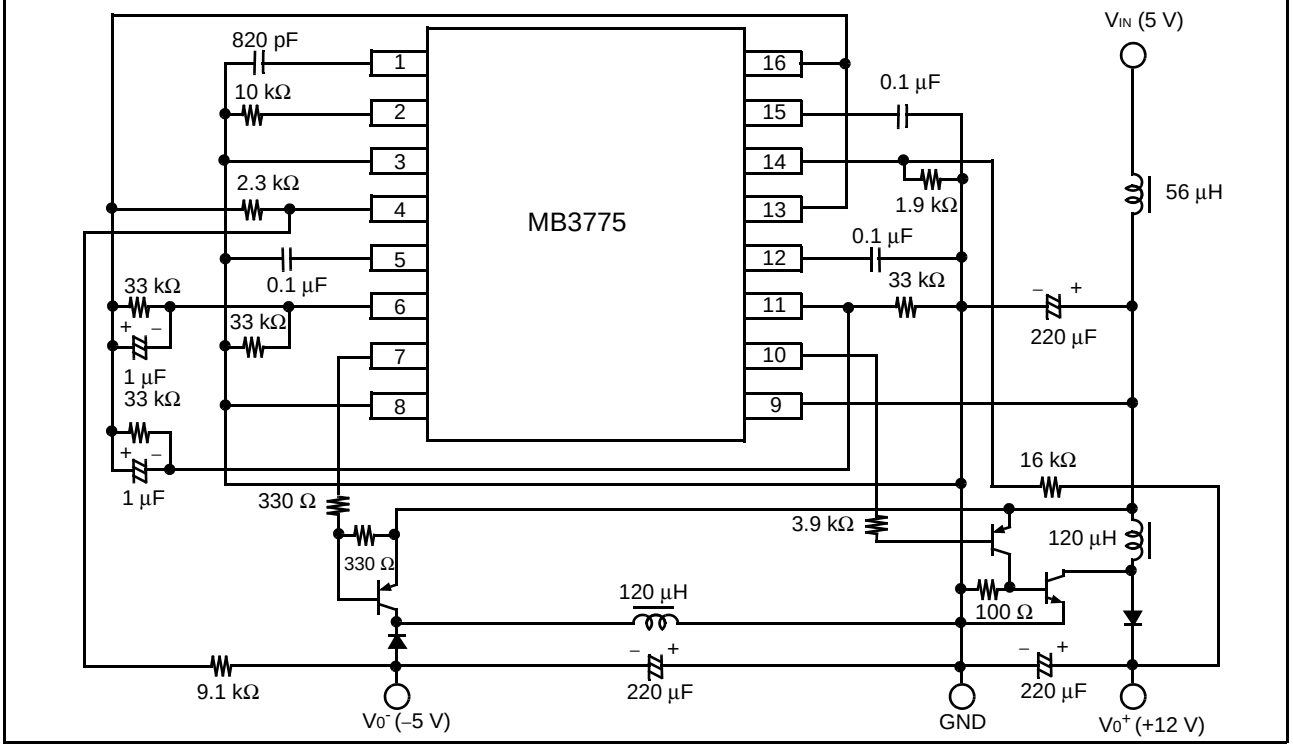


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Fig. 3 - Chopper Type Step Up/Inverting (For High Speed)

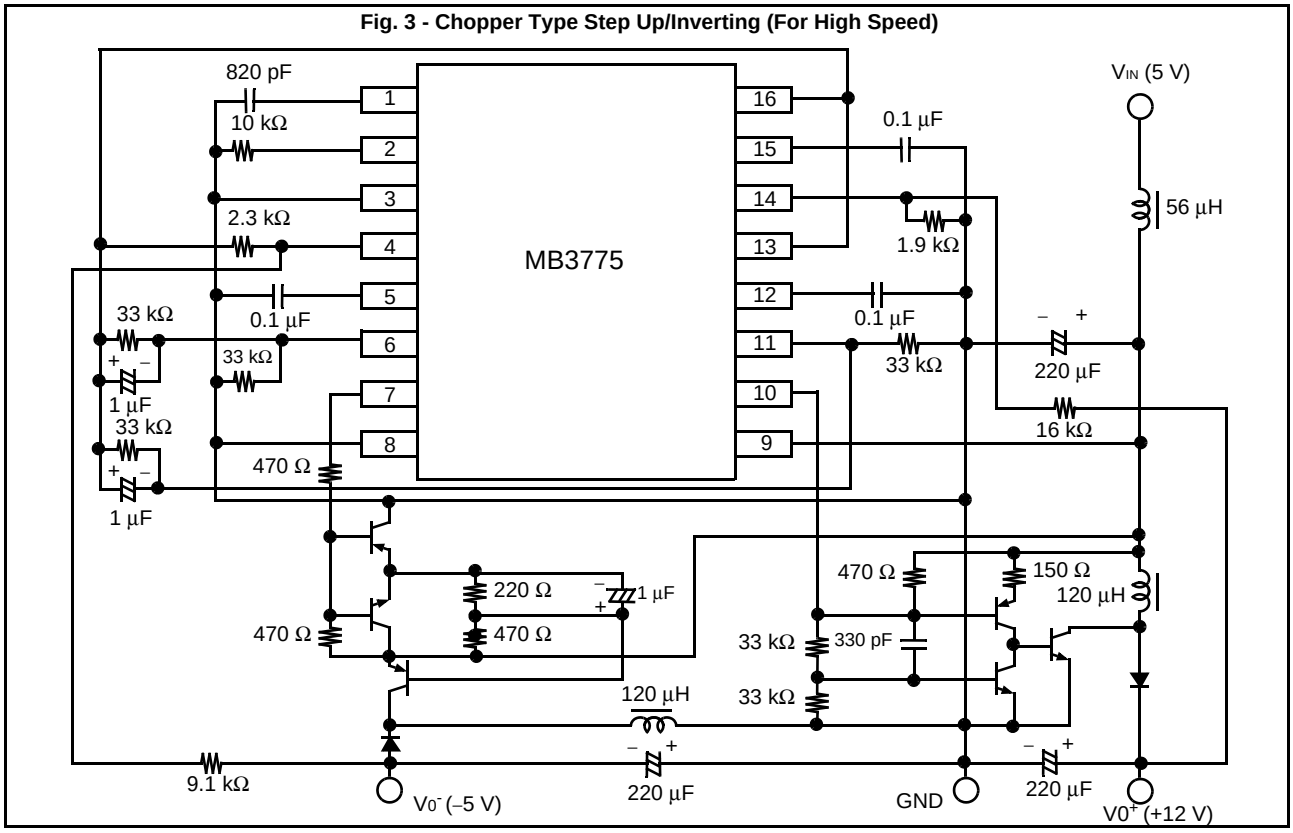
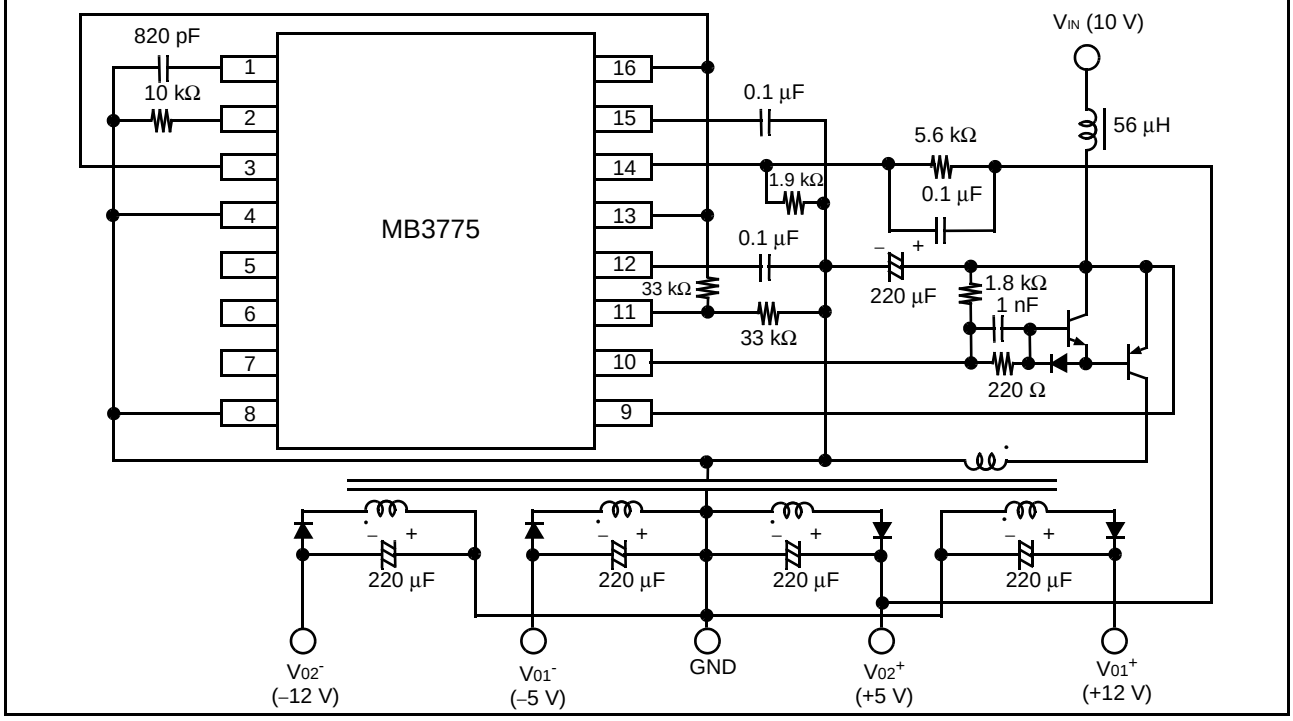


Fig. 4 - Multi Output Type (Apply Transformer)



■ HOW TO SET OUTPUT VOLTAGE

The output voltage is set using the connection shown in Fig. 5 and 6.
The error amplifiers are supplied to the internal reference voltage circuit as are the other internal circuits. The common-mode input voltage range is from –0.2 V to +1.45 V.
When the amplifiers are operated non-inverting, tie the inverting pin to V_{REF} (≒ 1.28 V). When the amplifiers are operated inverting, tie the non-inverting pin to ground.

Fig. 5 -Connection of Error Amp
Output Voltage V_0 is plus

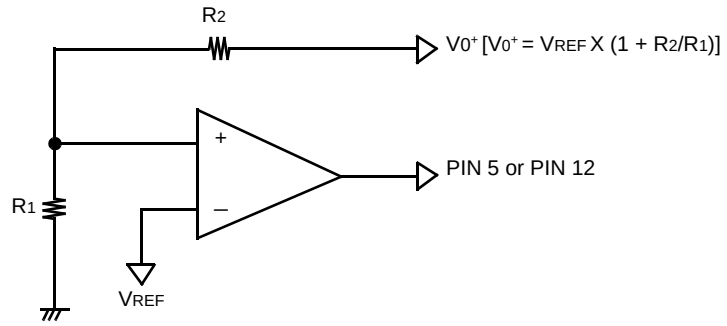
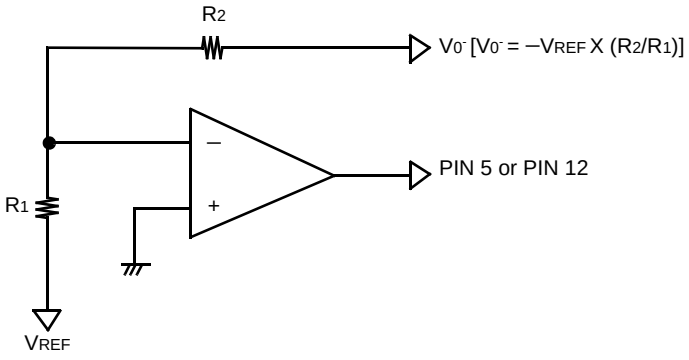


Fig. 6 -Connection of Error Amp
Output Voltage V_0 is minus



■ HOW TO SET TIME CONSTANT FOR TIMER LATCH SHORT PROTECTION CIRCUIT

TIMING CHART shows the configuration of the protection latch circuit.
Error amplifier outputs, are internally connected to the non-inverting inputs of the short-circuit protection comparator and are compared with the reference voltage (1.1 V) connected to the inverting input.
When the load condition of the switching regulator is stable, the error amplifier has no output fluctuation. Thus, short-circuit protection control is also kept in balance, and the protection enable pin (pin 15) voltage is kept at about 50 mV.
If the load condition drastically changes due to a load short-circuit and if low-level signals (1.1 V or lower) are input to the non-inverting inputs of the short-circuit protection comparator from the error amplifiers, the short-circuit protection comparator outputs a “Low” level to turn transistor Q_1 off. The protection enable pin voltage is discharged, and then the short-circuit protection comparator charges the externally connected protection enable capacitor C_{PE} according to the following formula:

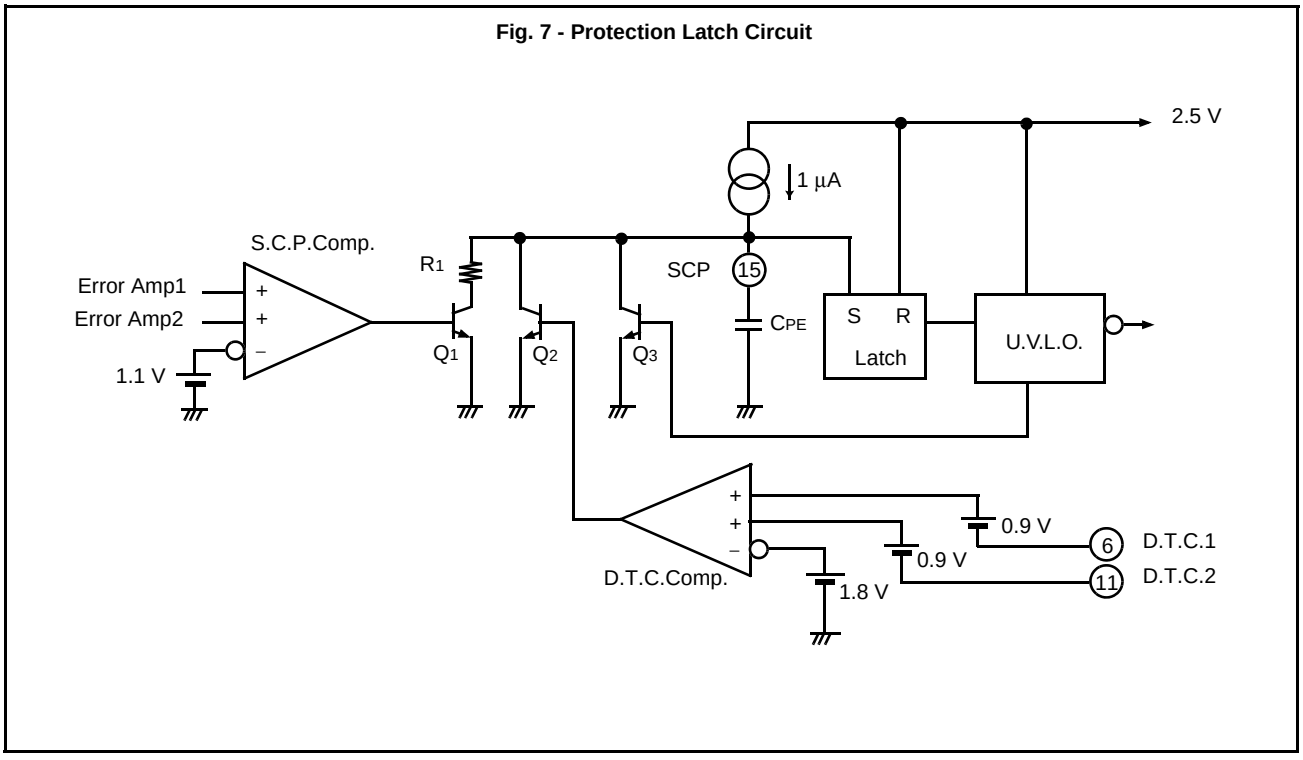
$$V_{PE} = 50\ mV + t_{PE} \times 10^{-6}/C_{PE}$$

$$0.65 = 50\ mV + t_{PE} \times 10^{-6}/C_{PE}$$

$$C_{PE} = t_{PE}/0.6\ (\mu F)$$

When the protection enable capacitor charges to about 0.65 V, the protection latch is set to enable the under voltage lockout protection circuit and to turn the output drive transistor off. The dead time is set to 100 %.
Once the under voltage lockout protection circuit is enabled, the protection enable is released; however, the protection latch is not reset if the power is not turned off.
The non-inverting inputs of the D.T.C. comparator are connected to the D.T.C. pins (pins 6 and 11) through the power supply (about 0.9 V) and are compared with a reference voltage (about 1.8 V) connected to the inverting input.
To prevent malfunction of the short protection circuit in soft-start mode (using D.T.C. pins), the D.T.C. comparator outputs a “High” level to turn Q_2 on until the D.T.C. pins (pins 6 and 11) voltage drops to about 0.9 V.

Fig. 7 - Protection Latch Circuit



■ SETTING THE IDLE PERIOD

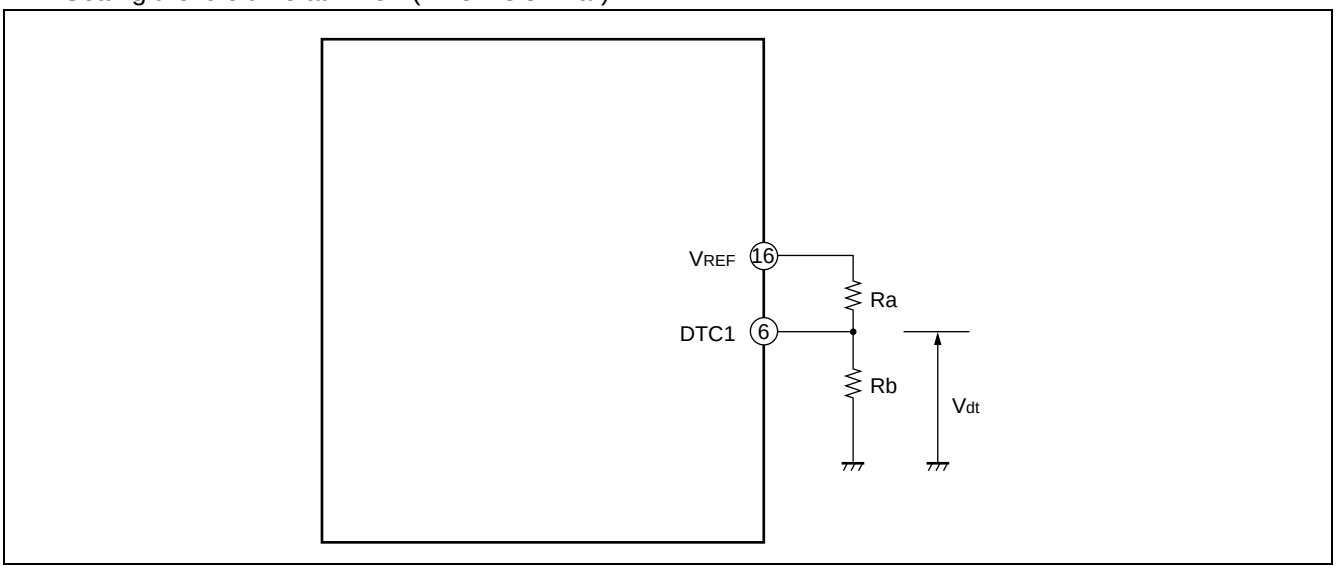
When voltage step-up, fly-back step-up or inverted output are set, the voltage at the FB pin may go lower than the triangular wave voltage due to load fluctuation, etc. In this case the output transistor will be in full-on state (ON duty 100%). This can be prevented by setting the maximum duty for the output transistor. This is done by setting the DTC1 pin (pin 6) voltage using resistance division of the V_{REF} voltage as illustrated below.

When the DTC1 pin voltage is lower than the triangular waveform voltage, the output transistor is turned on. If the triangular waveform amplitude ≒ 0.6 V, the lower limit voltage of the triangular waveform ≒ 1.3 V and the offset voltage is 0.9 V, the formula for the maximum duty would be as follows (Other channels are this conditions) :

$$\text{Duty (ON) Max (\%)} \fallingdotseq \frac{1.9\ \text{V} - (\text{Vdt} + 0.9\ \text{V})}{0.6\ \text{V}} \times 100 \fallingdotseq \frac{1.0\ \text{V} - \text{Vdt}}{0.6\ \text{V}} \times 100,\ V_{dt}\,(\text{V}) = \frac{\text{Rb}}{(\text{Ra} + \text{Rb})} \times V_{REF}$$

Also, if no output duty setting is required, the voltage should be set greater than the lower limit voltage of the triangular waveform, which is 1.3 V (Vdt = 0.4 V).

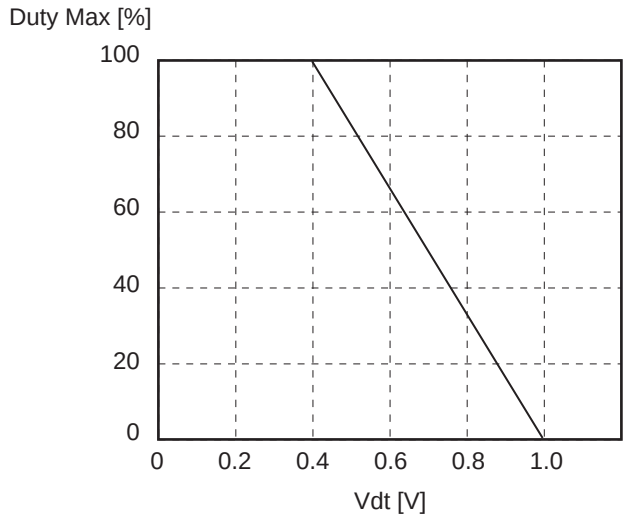
- Setting the idle time at DTC1 (DTC2 is similar)



• V_{CC} and V_O

- Step down DUTY[%] $= \frac{V_O}{V_{CC}} \times 100$
- Step up DUTY[%] $= \frac{V_O - V_{CC}}{V_O} \times 100$
- Inverter DUTY[%] $= \frac{V_O}{V_O - V_{CC}} \times 100$

Set the DTC voltage using the following Duty Max vs. Vdt characteristics so that this duty is set to the maximum duty or less.



Duty Max vs. Vdt characteristics (applies to Vdt 1 and Vdt 2)

■ SETTING THE SOFT START TIME

When power is switched on, the current begins charging the capacitor (C_{DTC1}) connected the DTC1 pin (pin 6). The soft start process operates by comparing the soft start setting voltage, which is proportional to the DTC1 pin voltage, with the triangular waveform, and varying the ON-duty of the OUT pin (pin 7).

The soft start time until the ON duty reaches 50% is determined by the following equation:

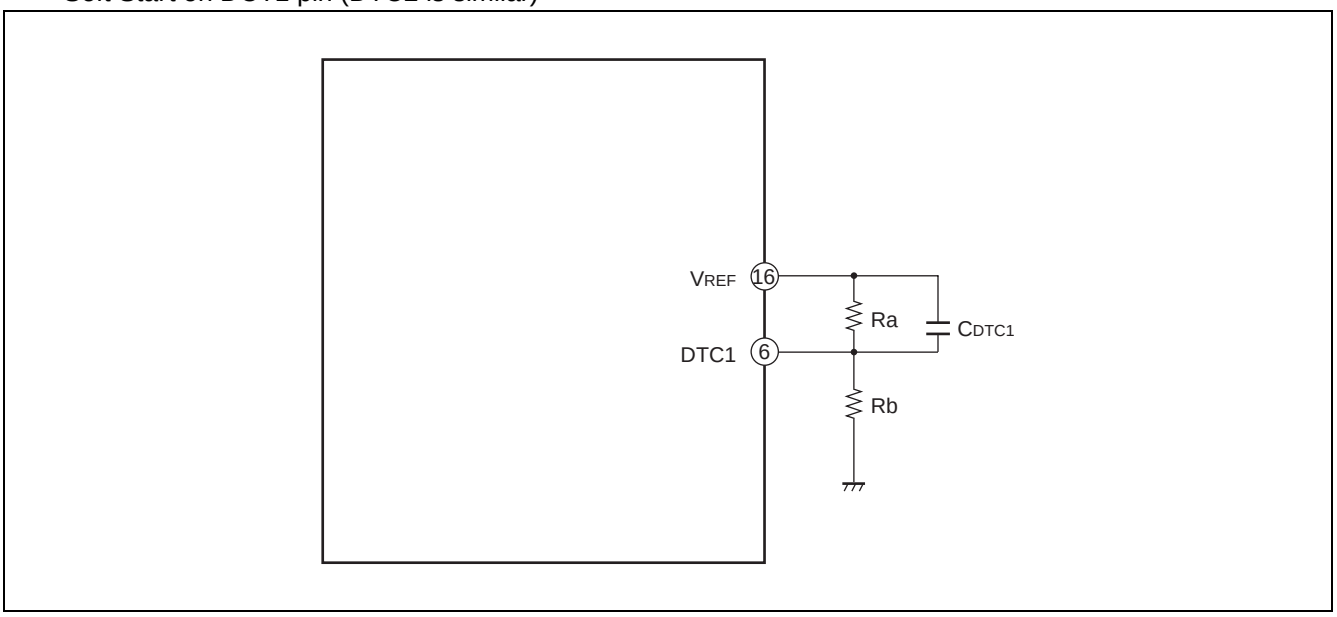
Soft start time (time until output ON duty = 50%) .

$ts\ (s) \fallingdotseq -C_{DTC1} \times Ra \times Rb\ /\ (Ra + Rb) \times \ln (1 - 0.7\ (Ra + Rb)\ /\ (1.28\ Ra))$

For example, if Ra = 10 kΩ and Rb = 4.7 kΩ, the result is:

$ts\ (s) \fallingdotseq 0.005 \times C_{DTC1}\ (\mu F)$

- Soft Start on DCT1 pin (DTC2 is similar)



■ SYNCHRONIZATION OF ICs

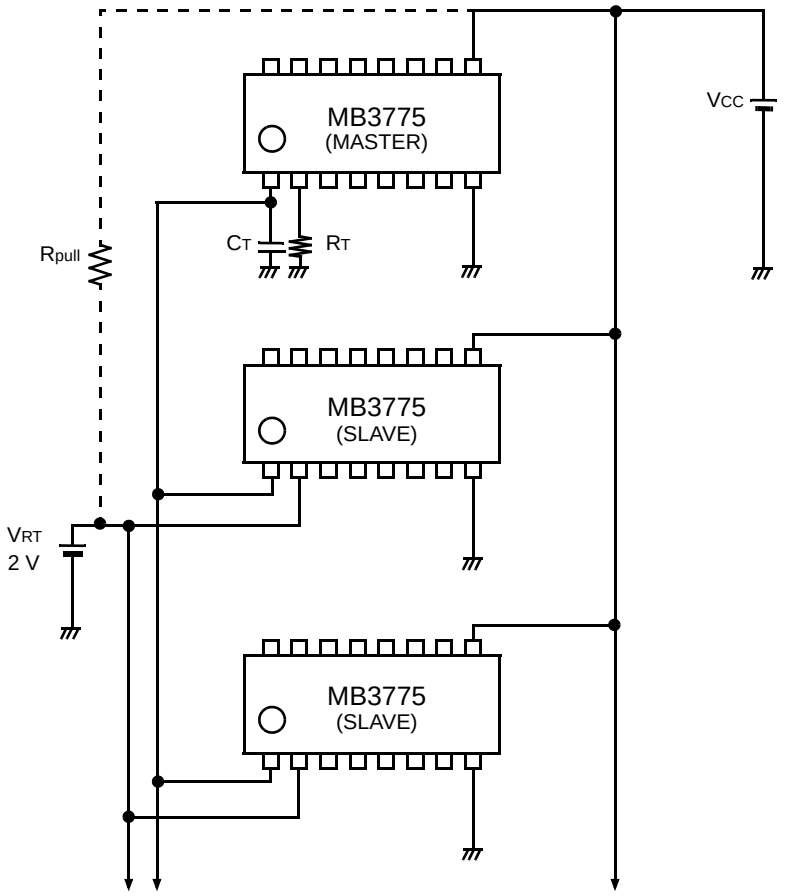
To synchronize MB3775 ICs, first, the specified capacitor and resistor are connected to the C_T and R_T pins (pins 1 and 2) of the master IC to start self oscillation. Next, 2 V is applied to the R_T pin (pin 2) of the slave ICs to disable the charge/discharge circuit for triangular wave oscillation. Finally, the C_T pin (pin 1) of the master and slave ICs are connected.

Instead of applying V_{RT} to the R_T pin (pin 2), these pins can be pulled up by a resistor (see resistance indicated by the dashed line in Fig. 8). Select the pull-up resistance R_{pull} from the formula given below.

$$\frac{V_{CC}}{0.5 \times N} \geq R_{pull}$$

R_{pull}: Pull up Resistor (kΩ)
V_{CC}: Power Supply Voltage (V)
N: Number of Slave ICs

Fig. 8 - Connection of Master, Slave



■ TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 9 - Reference voltage vs. Power supply voltage

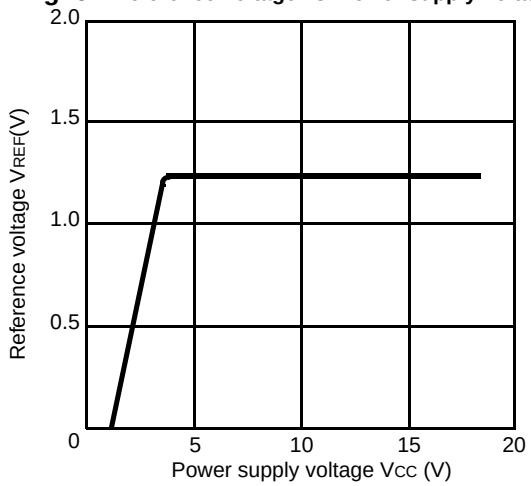


Fig. 10 - Average supply current vs. Power supply voltage

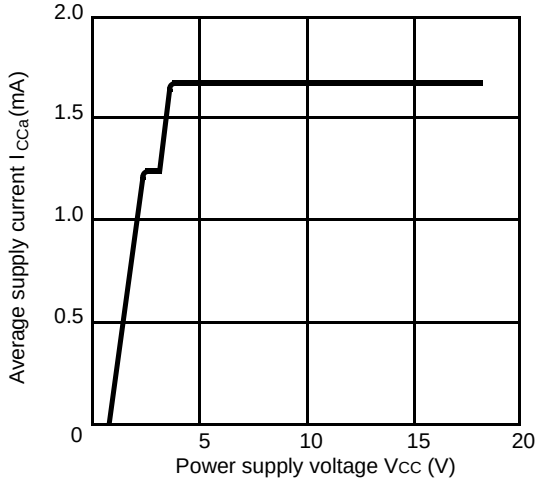


Fig. 11 - Stand by current vs. Power supply voltage

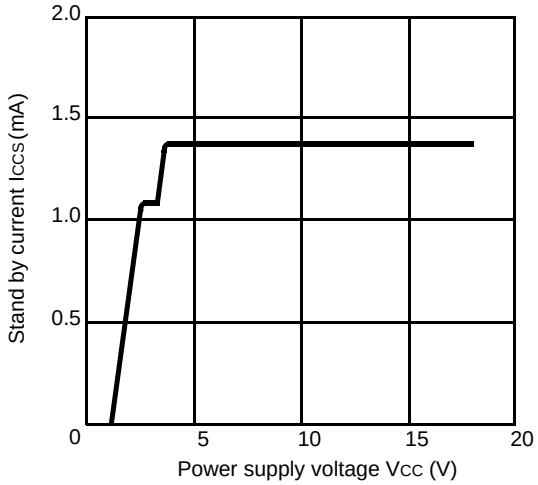


Fig. 12 - Reference voltage vs. Operating ambient temperature

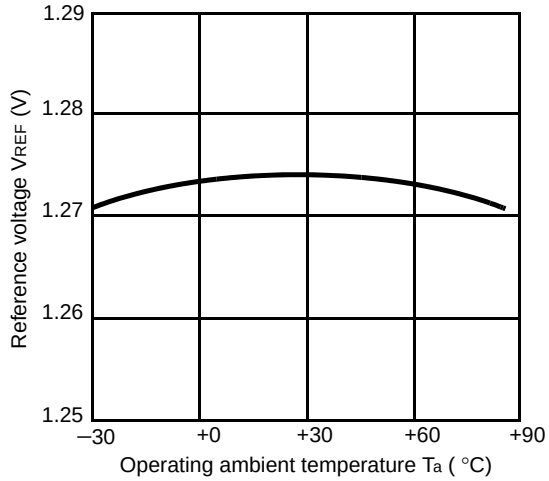


Fig. 13 - Collector saturation voltage vs. Sink current

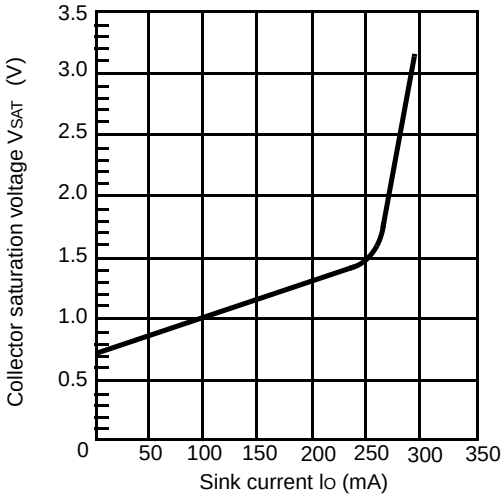
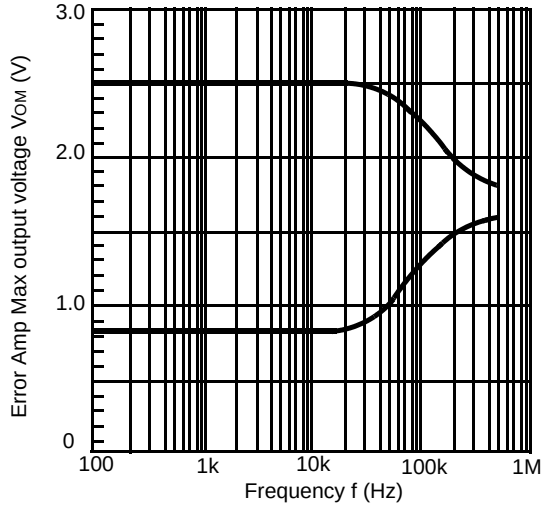


Fig. 14 - Error Amp Max output voltage vs. Frequency



(Continued)

Fig. 15 - Oscillation Frequency vs. Timing resistor

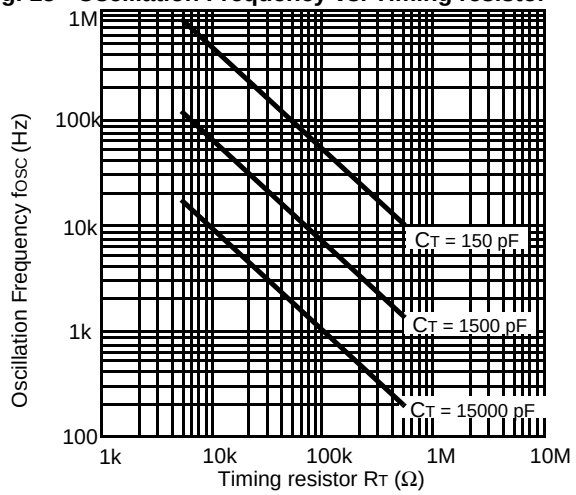


Fig. 16 - Triangular waveform cycle vs. Timing capacitor

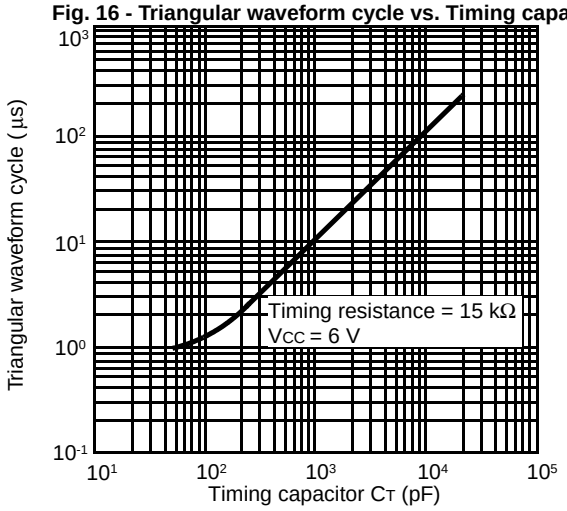


Fig. 17 - Triangular waveform Max Amplitude voltage vs. Timing capacitor

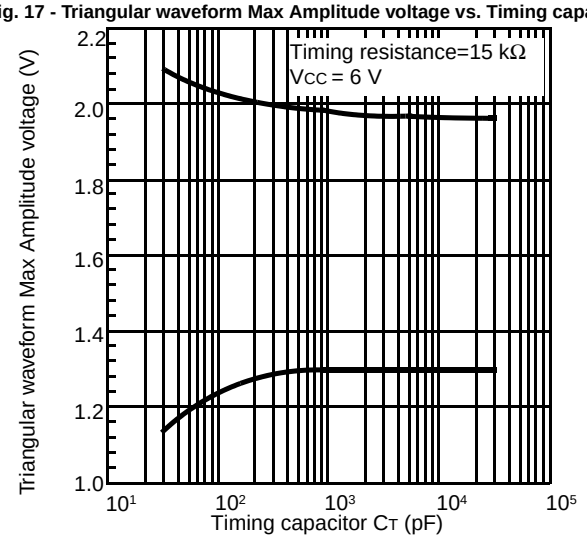


Fig. 18 - Gain/Phase vs. Frequency

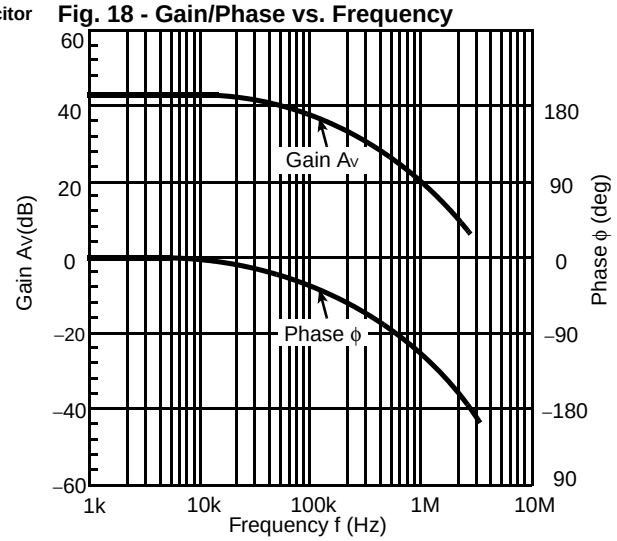


Fig. 19 - Gain/Phase vs. Frequency (Actual Data)

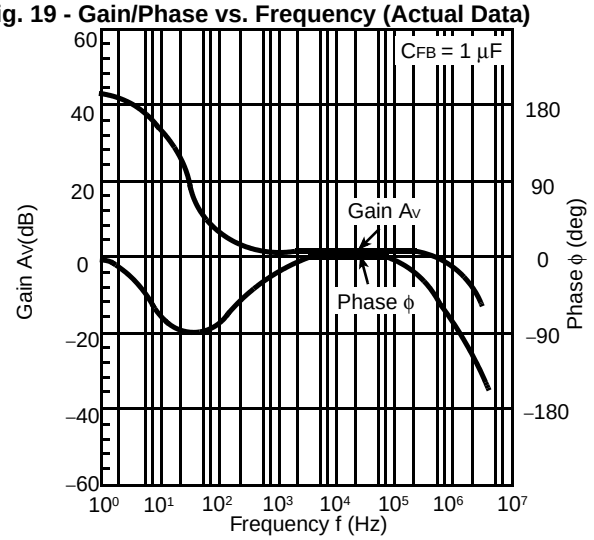
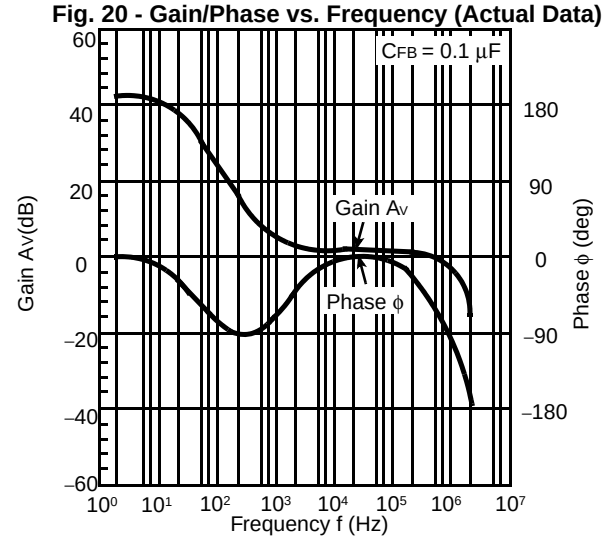


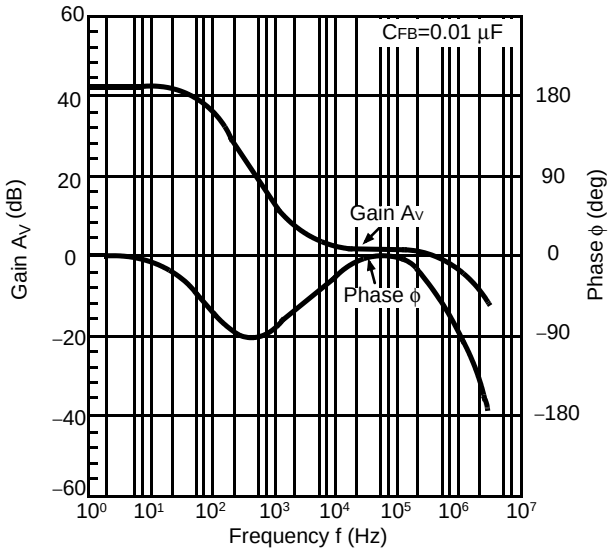
Fig. 20 - Gain/Phase vs. Frequency (Actual Data)



(Continued)

(Continued)

Fig. 21 - Gain/Phase vs. Frequency (Actual Data)



■ HOW TO SET THE ERROR AMPLIFIER FREQUENCY CHARACTERISTIC

Figure 22 shows the equivalent circuit of the error amplifier.
The frequency characteristic of the error amplifier is set by R_1, R_2, and C_P. The high-frequency gain is set by the ratio of resistors R_1 and R_2 in the IC (set value ≒ 0 dB).
When C_P = 0.1 µF, the gain at 20 kHz ≤ f ≤ 5 MHz is about 0 dB. The roll-off frequency is adjusted by changing external phase compensating capacitor C_P (see Fig. 24).
When high frequency gain is needed or the phase must be advanced at a low frequency, connect a resistor R_P between the FB pins (pins 5 and 12) and C_P as shown in Figure 23 (see Fig. 25).

Fig. 22 - Error Amp Equivalent Circuit

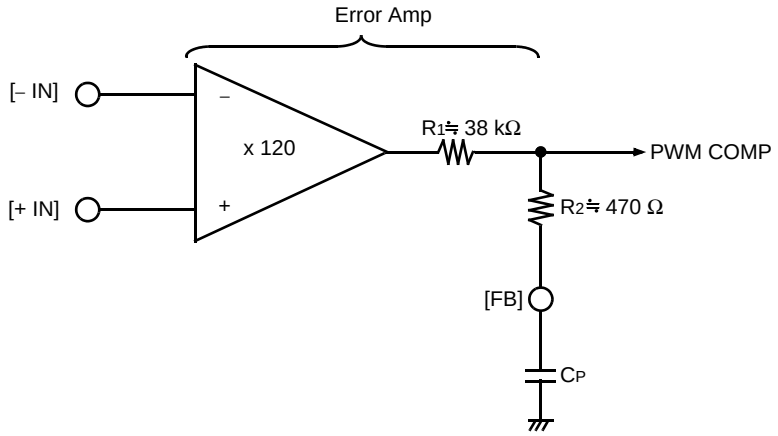
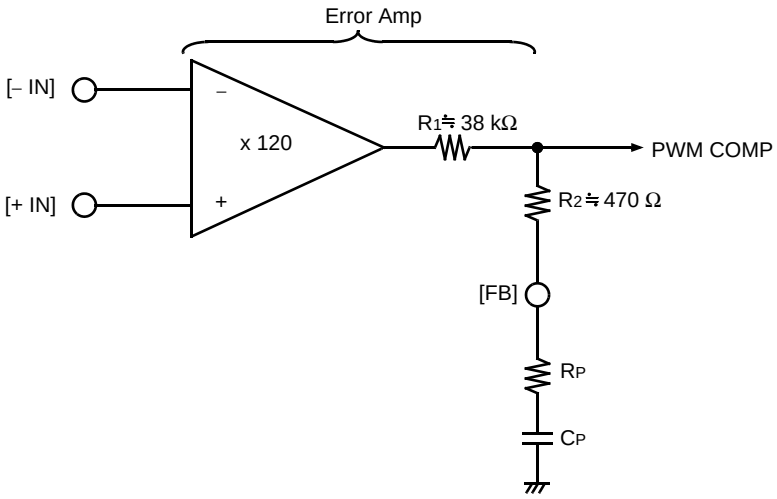


Fig. 23 - Error Amp Equivalent Circuit (Insert R_P)



Note: As shown above, the frequency characteristic of the error amplifier is set by the external phase compensating capacitor CP.
When a ceramic chip capacitor must be used to meet the requirements of a small system, be careful of its temperature characteristic. (–30 °C≒1/5 and +80 °C≒1/3 for the frequency characteristic, so a sufficient phase margin must be allowed for at room temperature.) Ceramic chip capacitors with a low temperature characteristic (B characteristic) or film capacitors are recommended (see Fig. 26 to 28).

Fig. 24 - Error Amp Frequency characteristics

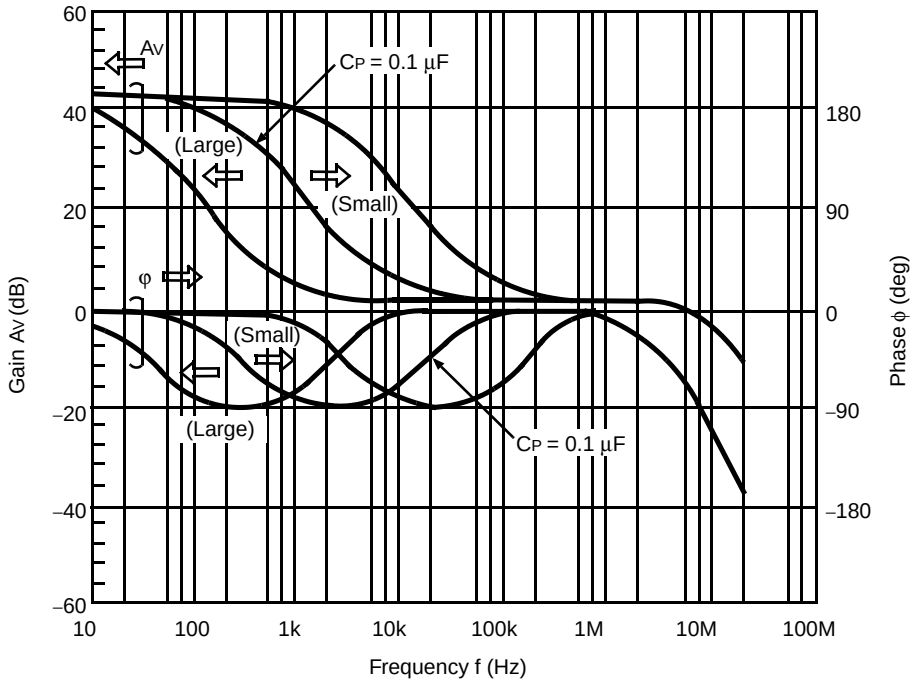


Fig. 25 - Error Amp Frequency characteristics

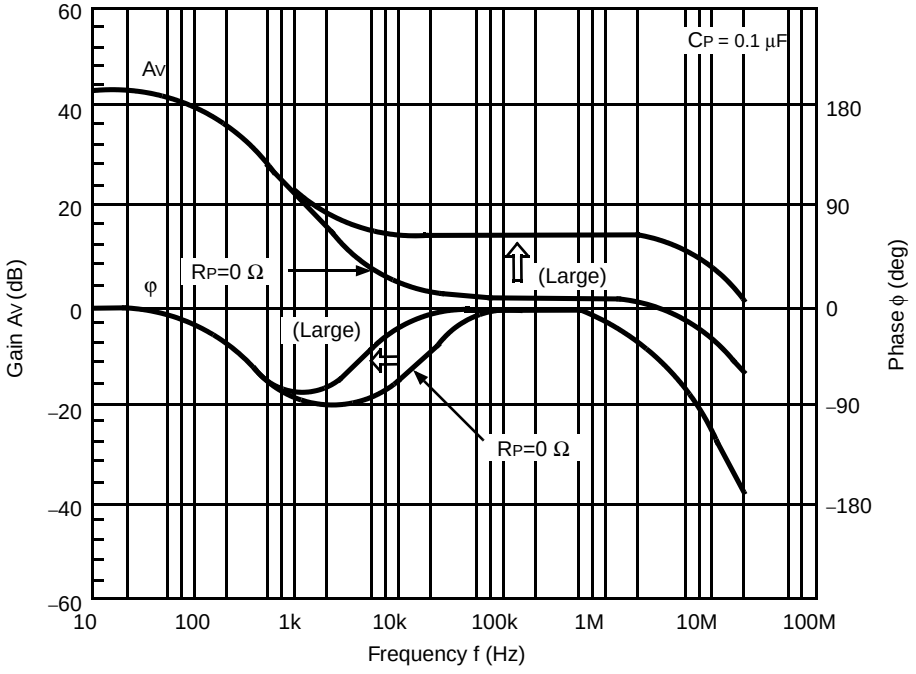


Fig. 26 - Ceramic Chip Capacitor (0.1 μF)

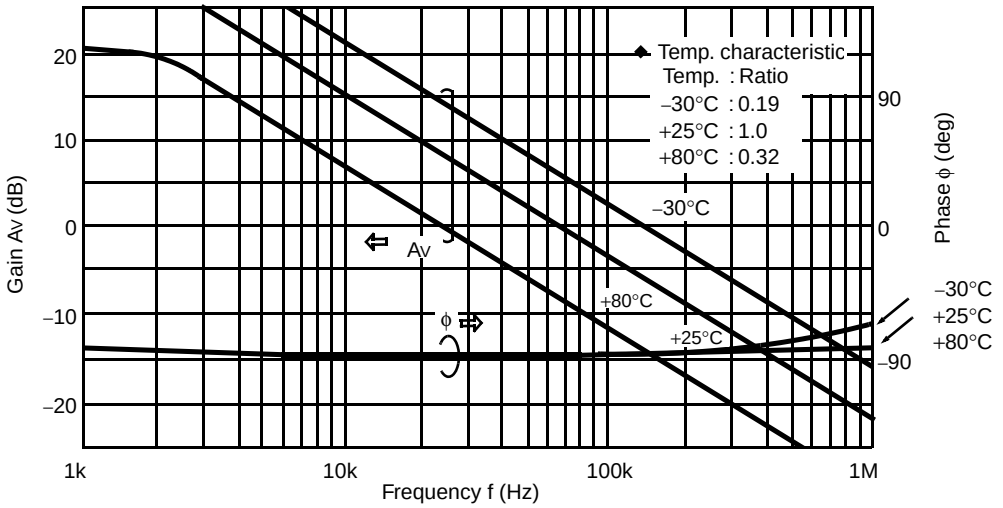


Fig. 27 - Tantal Capacitor (0.33 μF)

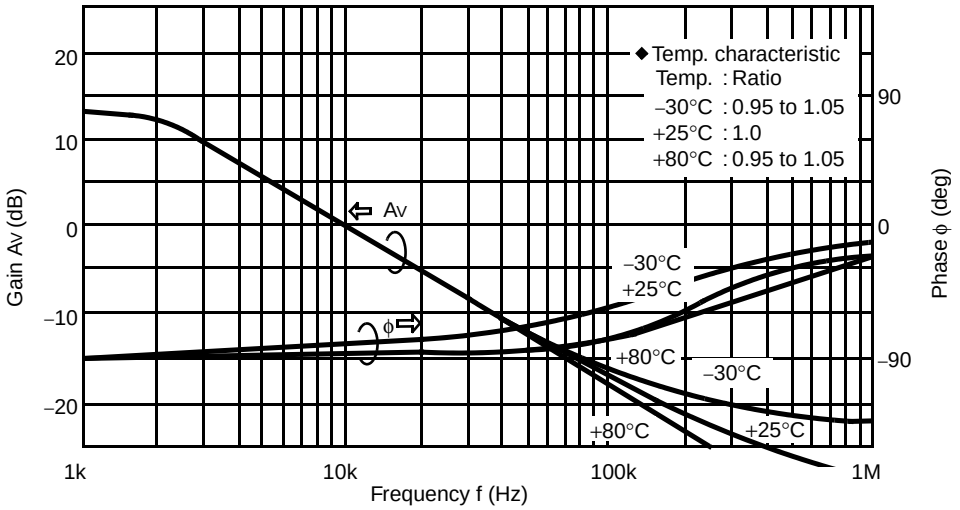
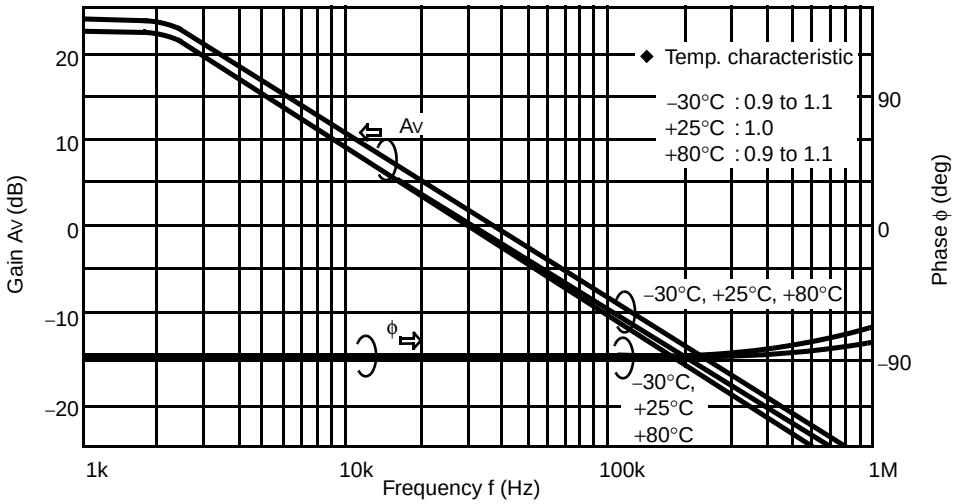


Fig. 28 - Film Capacitor (0.1 μF)



■ EFFECT OF EQUIVALENT SERIES RESISTANCE OF SMOOTHING CAPACITOR

The equivalent series resistance (ESR) of the smoothing capacitor in the DC/DC converter greatly affects the loop phase characteristic.

A smoothing capacitor with a low ESR reduces system stability by increasing the phase shift in the high-frequency region (see Fig. 30). Therefore, a smoothing capacitor with a high ESR will improve system stability. Be careful when using low ESR semiconductor electrolytic capacitors (OS-CON™) and tantalum capacitors.

Note: OS-CON is the trademark of Sanyo Electric Co., Ltd.

Fig. 29 - Step Down DC/DC Converter Basic Circuit

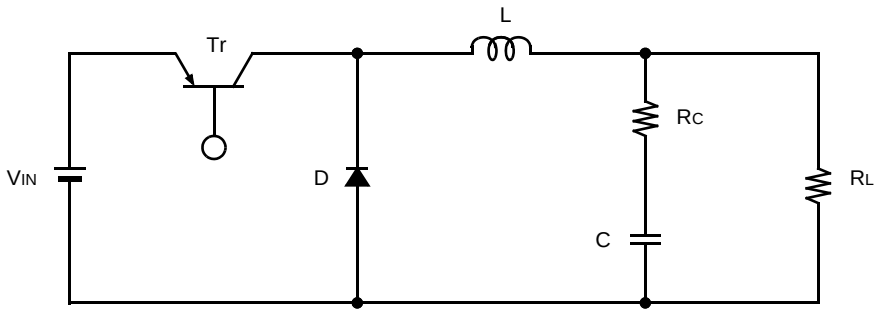


Fig. 30 - Gain vs. Frequency

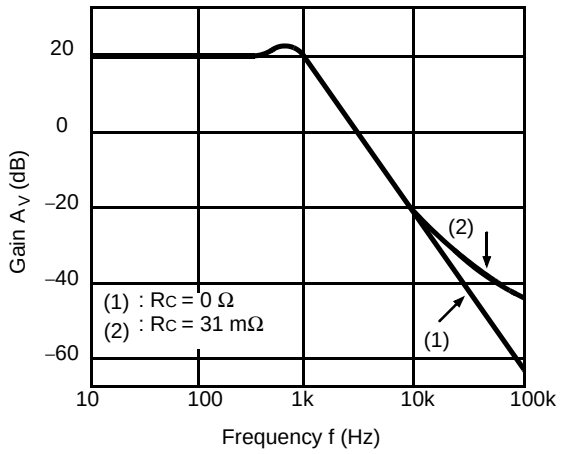
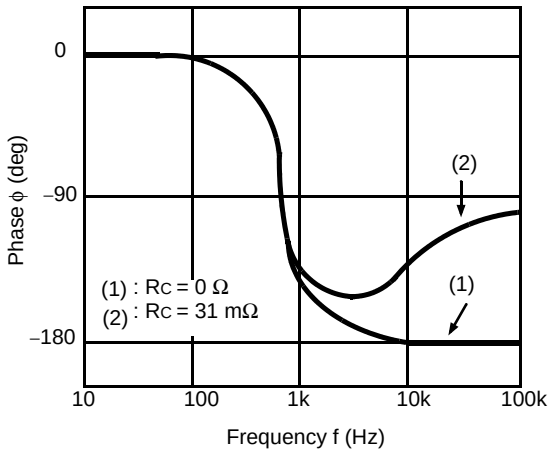


Fig. 31 - Phase vs. Frequency



Reference data

If an aluminum electrolytic smoothing capacitor ($R_C \fallingdotseq 1.0\ \Omega$) is replaced with a low ESR semiconductor electrolytic capacitor (OS-CON™: $R_C \fallingdotseq 0.2\ \Omega$), the phase shift is reduced by half (see Fig. 33 and 34).

Fig. 32 - DC/DC Converter A_V vs. ϕ characteristic Test Circuit

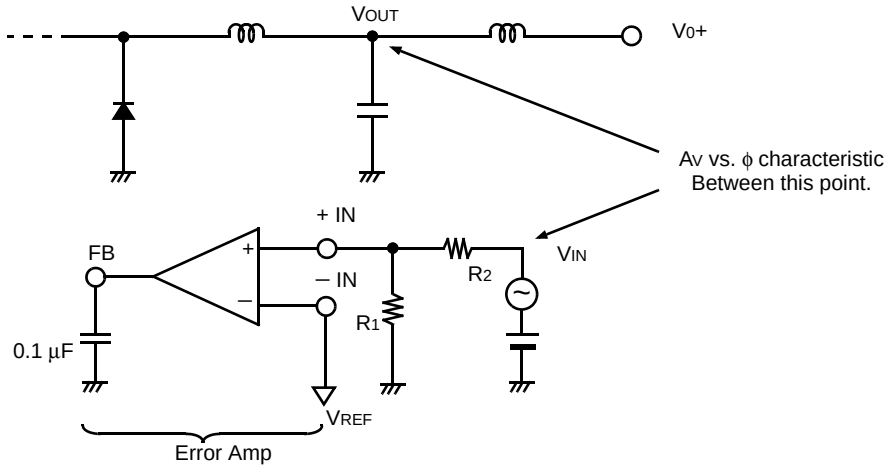


Fig. 33 - DC/DC Converter +5 V Gain/Phase vs. Frequency

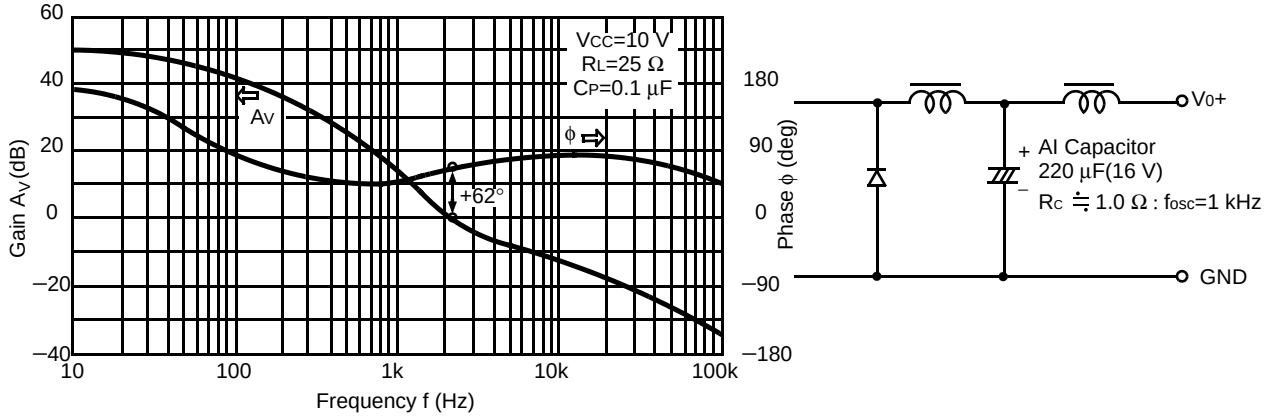
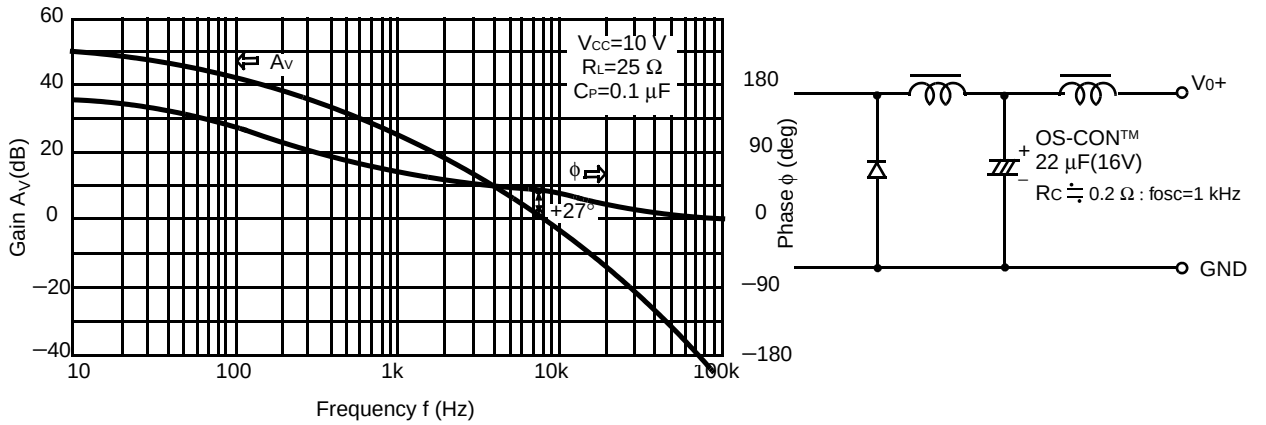


Fig. 34 - DC/DC Converter +5 V Gain/Phase vs. Frequency



■ MEASURES FOR ENSURING SYSTEM STABILITY WHEN A LOW ESR SMOOTHING CAPACITOR IS USED

When a low ESR smoothing capacitor is used in the DC/DC converter, only the L and C are apparent even in the high-frequency region, and the phase is delayed by almost 180°. Consequently, the system phase margin and stability are reduced. On the other hand, a low ESR capacitor is needed to reduce the amount of output ripple. This is contrary to the system stability explained above.
To solve this problem, phase compensation can be used. This method increases the phase margin by advancing the phase when the phase margin is reduced by a low ESR capacitor.
The three suggestions listed below are recommended for DC/DC converters using the MB3775.

(1) As shown in Fig. 35, a capacitor is connected in parallel with the output feedback resistor to advance the phase. Use the formula below as a guideline for the capacitance.

$$C_1 \fallingdotseq \frac{1}{2\pi f R_2}$$

f: Unstable Frequency (See Fig. 32)

Fig. 35 - External circuit example1 to advance the phase

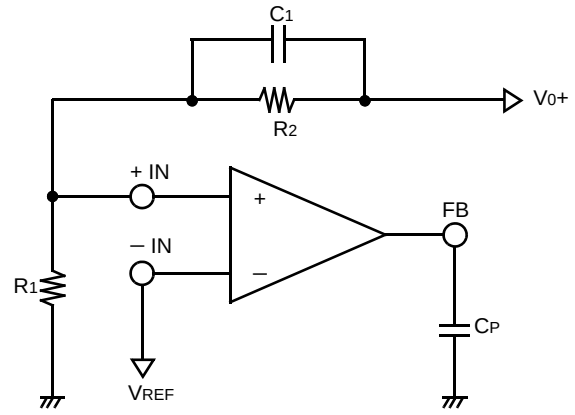
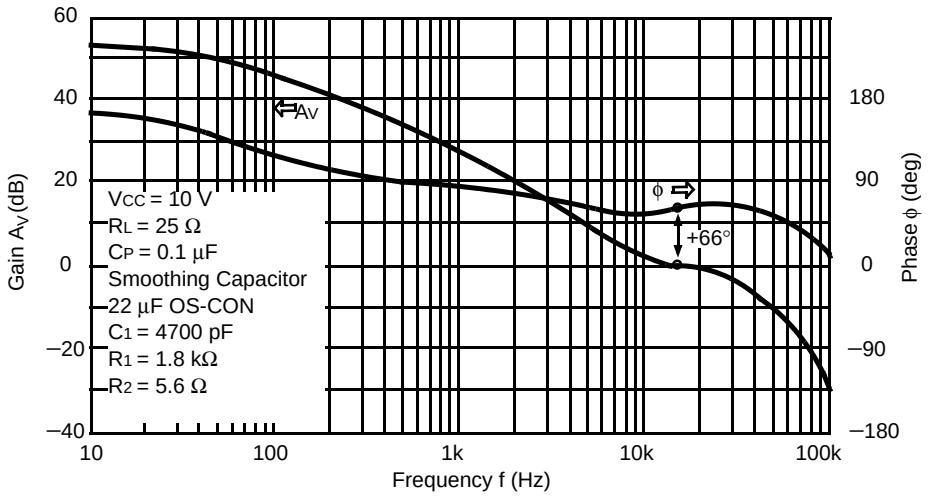


Fig. 36 - DC/DC Converter +5 V Gain/Phase vs. Frequency



(2) As shown in Figure 37, a resistor (R_P) is connected between the FB pins (pins 5 and 12) and C_P of the error amplifier to advance the phase. The more R_P is increased, the more the phase is advanced. However, the gain in the high-frequency range is also increased, which causes instability. Therefore, select the optimum resistance (see Fig. 38).

Fig. 37 - External circuit example 2 to advance the phase

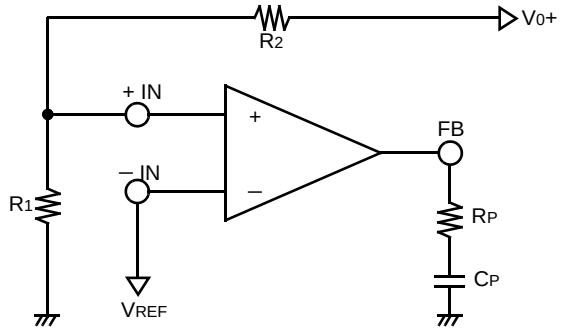
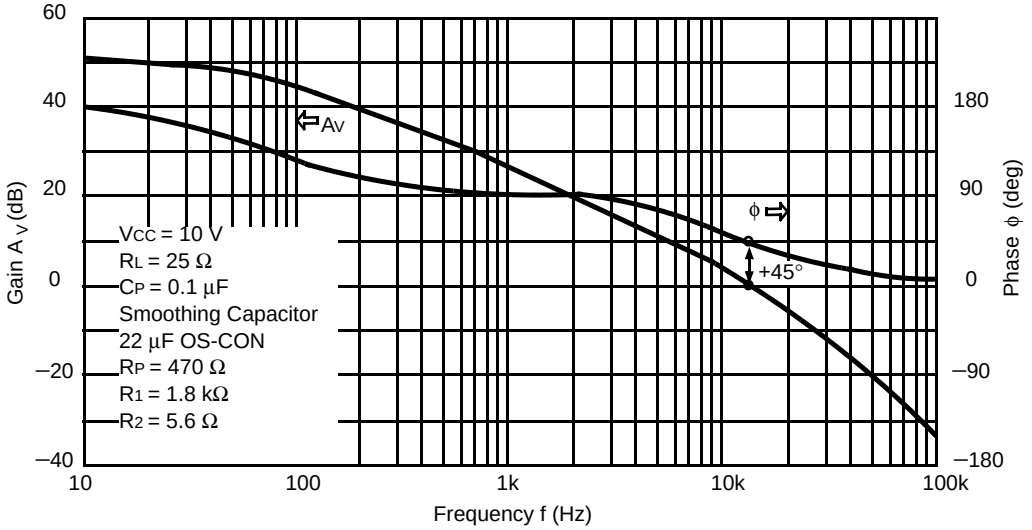
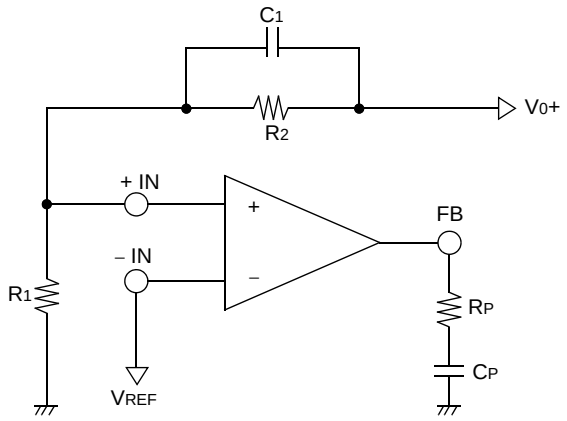


Fig. 38 - DC/DC Converter +5 V Gain/Phase vs. Frequency



(3) As shown in Fig. 39, the phase is advanced by using both example 1 and 2 (Fig. 35 and 37).

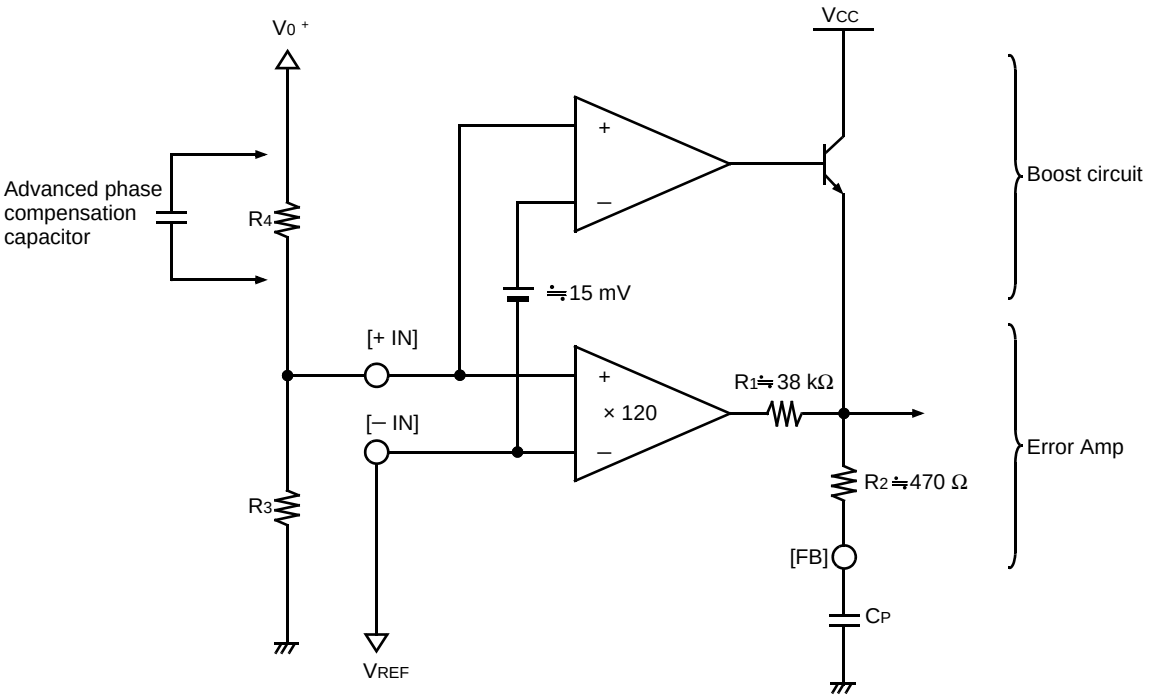
Fig. 39 - External circuit example 3 to advance the phase



■ ERROR AMPLIFIER INPUT RIPPLE VOLTAGE

The boost circuit for charging the phase compensating capacitor C_P is connected to the error amplifier as shown in Figure 40 to protect against output voltage overload at power-on.
A ≒15 mV offset voltage is provided for the negative input side so that the boost circuit only operates at power-on. When a capacitor is connected in parallel with the output feedback resistor, because the output ripple is too large or for advanced phase compensation, the boost circuit starts operating, which may degrade regulation if the differential input voltage of the error amplifier exceeds =15 mV. Be careful with the differential input voltage of the error amplifier.

Fig. 40 - Error Amp /Boost Equivalent circuit



■ NOTES ON USE

- Take account of common impedance when designing the earth line on a printed wiring board.

- Take measures against static electricity.
  - For semiconductors, use antistatic or conductive containers.
  - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  - The work table, tools and measuring instruments must be grounded.
  - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.

- Do not apply a negative voltage
  - Applying a negative voltage of –0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

■ ORDERING INFORMATION

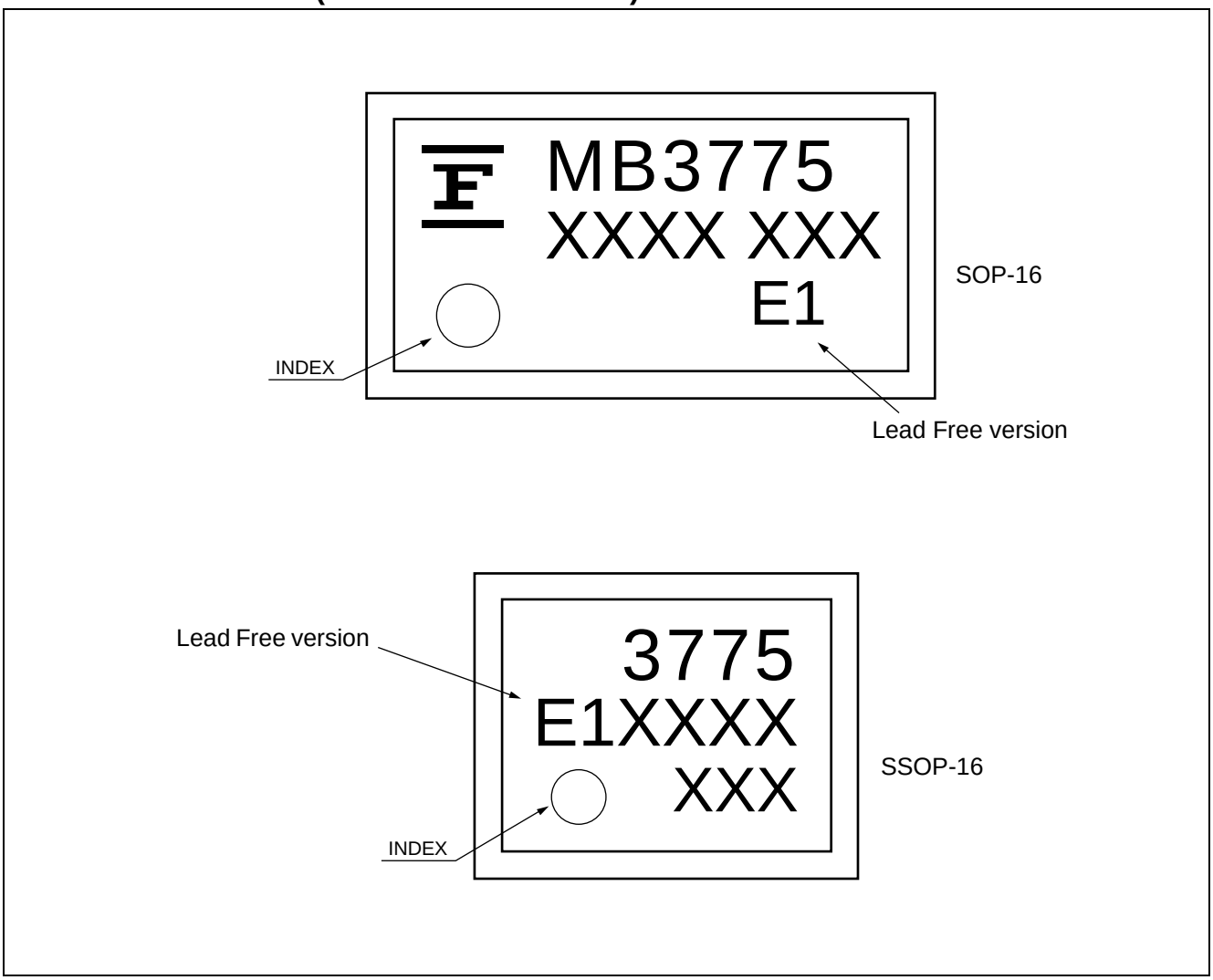
Part number	Package	Remarks
MB3775PF	16-pin plastic SOP (FPT-16P-M06)	
MB3775PFV	16-pin plastic SSOP (FPT-16P-M05)	

■ RoHS COMPLIANCE INFORMATION OF LEAD (PB) FREE VERSION

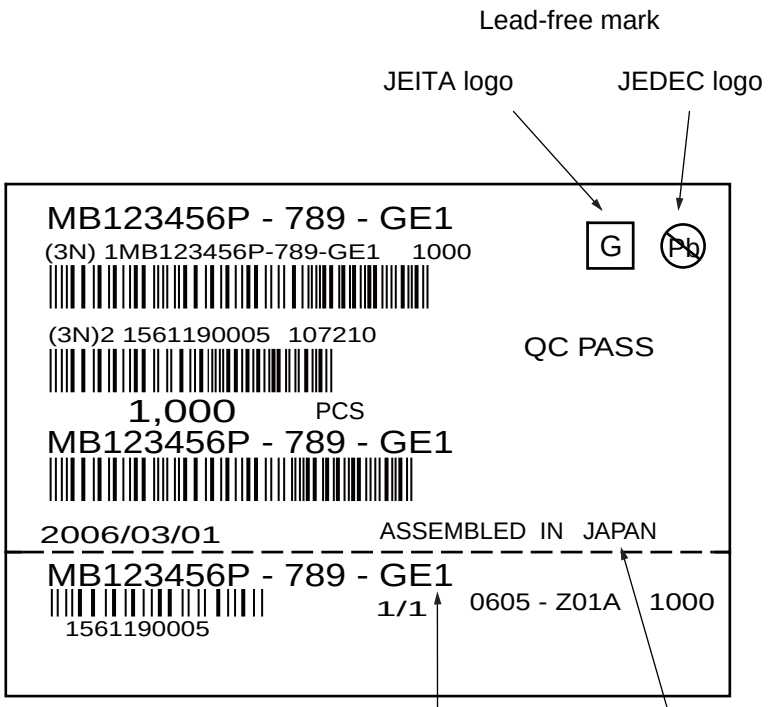
The LSI products of FUJITSU SEMICONDUCTOR with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) .

The product that conforms to this standard is added “E1” at the end of the part number.

■ MARKING FORMAT (LEAD FREE VERSION)



■ LABELING SAMPLE (LEAD FREE VERSION)



The part number of a lead-free product has the trailing characters “E1”.

“ASSEMBLED IN CHINA” is printed on the label of a product assembled in China.

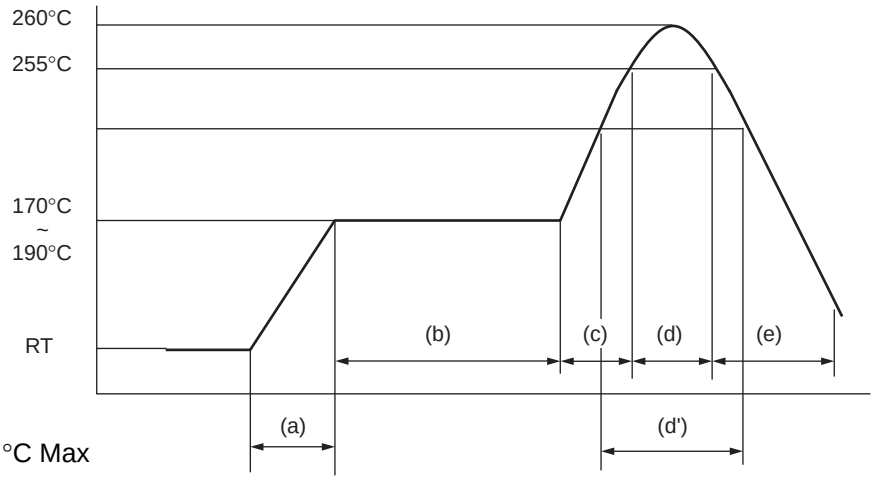
■ MB3775PF, MB3775PFV RECOMMENDED CONDITIONS of MOISTURE SENSITIVITY LEVEL

[FUJITSU SEMICONDUCTOR Recommended Mounting Conditions]

Item	Condition	
Mounting Method	IR (infrared reflow), warm air reflow	
Mounting times	2 times	
Storage period	Before opening	Please use it within two years after manufacture.
	From opening to the 2nd reflow	Less than 8 days
	When the storage period after opening was exceeded	Please process within 8 days after baking (125 °C ± 3 °C, 24hrs + 2H/-0H) Baking can be performed up to two times.
Storage conditions	5 °C to 30 °C, 70%RH or less (the lowest possible humidity)	

[Parameters for Each Mounting Method]

IR (infrared reflow)



H rank : 260 °C Max

(a) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(b) Preliminary heating : Temperature 170 °C to 190 °C, 60s to 180s
(c) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(d) Actual heating : Temperature 260 °C Max; 255 °C or more, 10s or less
(d') : Temperature 230 °C or more, 40s or less
or
Temperature 225 °C or more, 60s or less
or
Temperature 220 °C or more, 80s or less
(e) Cooling : Natural cooling or forced cooling

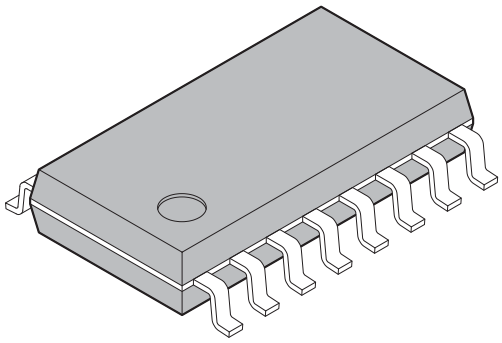
Note : Temperature : the top of the package body

Manual soldering (partial heating method)

Item	Condition	
Storage period	Before opening	Within two years after manufacture.
	Between opening and mounting	Within two years after manufacture. (No need to control moisture during the storage period because of the partial heating method.)
Storage conditions	5 °C to 30 °C, 70%RH or less (the lowest possible humidity)	
Mounting conditions	Temperature at the tip of a soldering iron: 400 °C max Time: Five seconds or below per pin*	

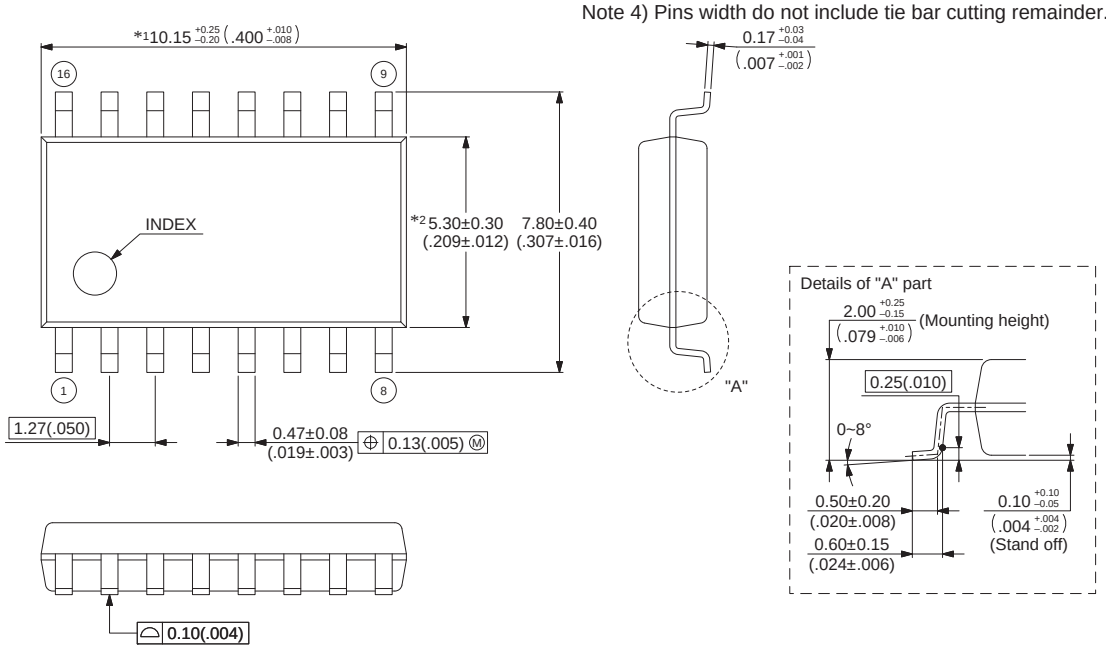
* : Make sure that the tip of a soldering iron does not come in contact with the package body.

■ PACKAGE DIMENSION

16-pin plastic SOP		
	Lead pitch	1.27 mm
	Package width × package length	5.3 × 10.15 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	2.25 mm MAX
	Weight	0.20 g
(FPT-16P-M06)	Code (Reference)	P-SOP16-5.3×10.15-1.27

16-pin plastic SOP
(FPT-16P-M06)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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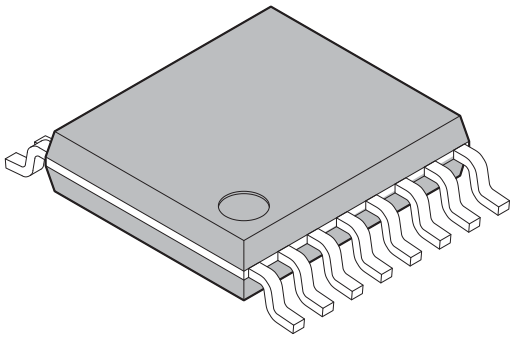
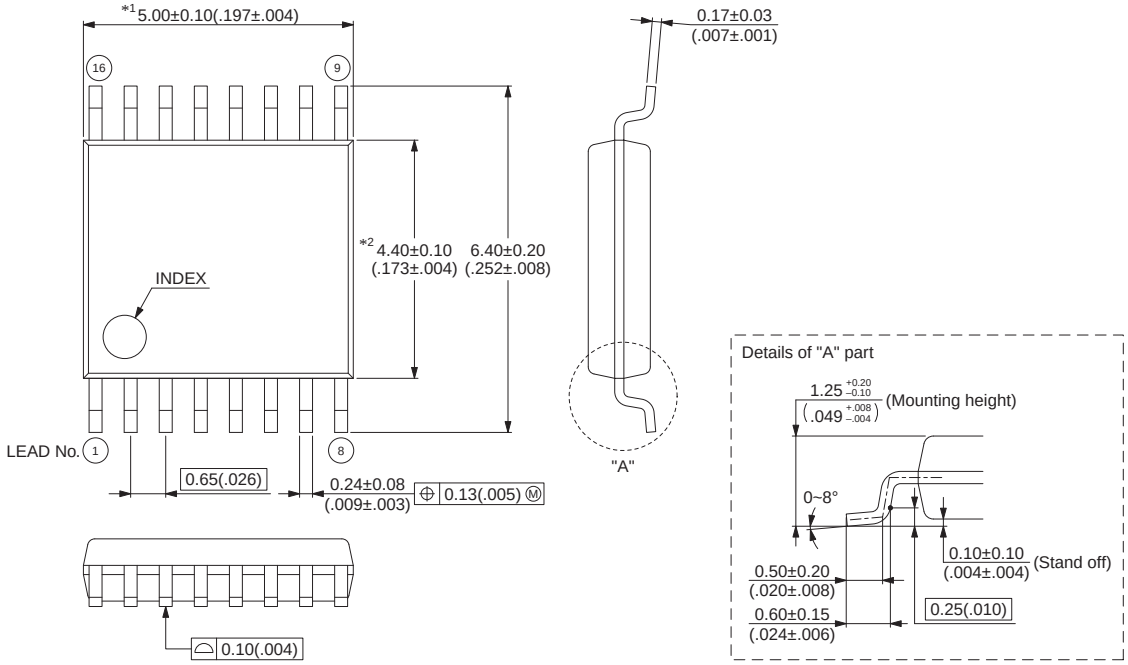
16-pin plastic SSOP		
	Lead pitch	0.65 mm
	Package width × package length	4.40 × 5.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.45mm MAX
	Weight	0.07g
(FPT-16P-M05)	Code (Reference)	P-SSOP16-4.4×5.0-0.65

16-pin plastic SSOP
(FPT-16P-M05)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

MEMO

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