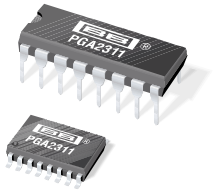


Stereo Audio Volume Control

FEATURES

- **DIGITALLY-CONTROLLED ANALOG VOLUME CONTROL**
  Two Independent Audio Channels
  Serial Control Interface
  Zero Crossing Detection
  Mute Function
- **WIDE GAIN AND ATTENUATION RANGE**
  +31.5dB to –95.5dB with 0.5dB Steps
- **LOW NOISE AND DISTORTION**
  120dB Dynamic Range
  0.0004% THD+N at 1kHz (U-Grade)
  0.0002% THD+N at 1kHz (A-Grade)
- **NOISE-FREE LEVEL TRANSITIONS**
- **LOW INTERCHANNEL CROSSTALK**
  –130dBFS
- **POWER SUPPLIES: ±5V Analog, +5V Digital**
- **AVAILABLE IN DIP-16 AND SOL-16 PACKAGES**
- **PIN AND SOFTWARE COMPATIBLE WITH THE CRYSTAL CS3310**

APPLICATIONS

- **AUDIO AMPLIFIERS**
- **MIXING CONSOLES**
- **MULTI-TRACK RECORDERS**
- **BROADCAST STUDIO EQUIPMENT**
- **MUSICAL INSTRUMENTS**
- **EFFECTS PROCESSORS**
- **A/V RECEIVERS**
- **CAR AUDIO SYSTEMS**

DESCRIPTION

The PGA2311 is a high–performance, stereo audio volume control designed for professional and high-end consumer audio systems. Using high performance operational amplifier stages internal to the PGA2311 yields low noise and distortion, while providing the capability to drive 600Ω loads directly without buffering. The 3-wire serial control interface allows for connection to a wide variety of host controllers, in addition to support for daisy-chaining of multiple PGA2311 devices.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V_A+	+5.5V
V_A–	–5.5V
V_D+	+5.5V
V_A+ to V_D+	< ± 0.3V
Analog Input Voltage	0V to V_A+, V_A–
Digital Input Voltage	–0.3V to V_D+
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Package Temperature (IR reflow, 10s)	+235°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE–LEAD	PACKAGE DESIGNATOR(1)	OPERATING TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
PGA2311 (U–Grade)	DIP–16	N	–40°C to +85°C	PGA2311P	PGA2311P	Rails
	SOL–16	DW		PGA2311U	PGA2311U	Rails
				PGA2311U	PGA2311U/1K	Tape and Reel, 1000
PGA2311 (A–Grade)	DIP–16	N	–40°C to +85°C	PGA2311PA	PGA2311PA	Rails
	SOL–16	DW		PGA2311UA	PGA2311UA	Rails
				PGA2311UA	PGA2311UA/1K	Tape and Reel, 1000

(1) For the most current specifications and package information, refer to our web site at www. ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_A+ = +5V, V_A– = –5V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 10Hz to 20kHz, unless otherwise noted.

PARAMETER	CONDITIONS	PGA2311P, U (U–Grade).			PGA2311PA, UA (A–Grade)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS								
Step Size	Gain Setting = 31.5dB		0.5			0.5		dB
Gain Error			±0.05			±0.05		dB
Gain Matching			±0.05			±0.05		dB
Input Resistance			10			10		kΩ
Input Capacitance			3			3		pF
AC CHARACTERISTICS								
THD+N	V_{IN} = 2Vrms, f = 1kHz		0.0004	0.001		0.0002	0.0004	%
Dynamic Range	V_{IN} = AGND, Gain = 0dB	116	120		116	120		dB
Voltage Range, Output		(V_A–) + 1.25		(V_A+) – 1.25	(V_A–) + 1.25		(V_A+) – 1.25	V
Voltage Range, Input (without clipping)			2.5			2.5		Vrms
Output Noise	V_{IN} = AGND, Gain = 0dB		2.5	4		2.5	4	µVrms
Interchannel Crosstalk	f = 1kHz		–130			–130		dBFS
OUTPUT BUFFER								
Offset Voltage	V_{IN} = AGND, Gain = 0dB		0.25	0.5		0.25	0.5	mV
Load Capacitance Stability			100			100		pF
Short–Circuit Current			50			50		mA
Unity–Gain Bandwidth, Small Signal			10			10		MHz

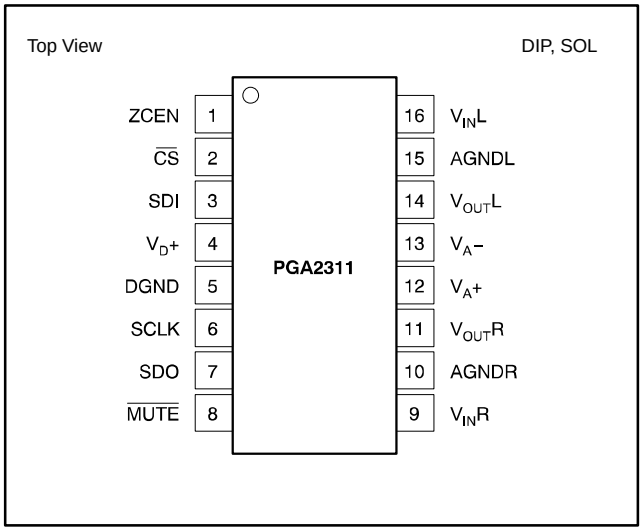
ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_A+ = +5V, V_A– = –5V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 10Hz to 20kHz, unless otherwise noted.

PARAMETER	CONDITIONS	PGA2311P, U (U–Grade)			PGA2311PA, UA (A–Grade)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL CHARACTERISTICS								
High–Level Input Voltage, V_{IH}		+2.0		V_D+	+2.0		V_D+	V
Low–Level Input Voltage, V_{IL}		–0.3		0.8	–0.3		0.8	V
High–Level Output Voltage, V_{OH}	I_O = 200µA	(V_A+) – 1.0			(V_D+) – 1.0			V
Low–Level Output Voltage, V_{OL}	I_O = –3.2mA			0.4			0.4	V
Input Leakage Current			1	10		1	10	µA
SWITCHING CHARACTERISTICS								
Serial Clock (SCLK) Frequency	f_{SCLK}	0		6.25	0		6.25	MHz
Serial Clock (SCLK) Pulse Width LOW	t_{PH}	80			80			ns
Serial Clock (SCLK) Pulse Width HIGH	t_{PL}	80			80			ns
$\overline{\text{MUTE}}$ Pulse Width LOW	t_{MI}	2.0			2.0			ms
Input Timing								
SDI Setup Time	t_{SDS}	20			20			ns
SDI Hold Time	t_{SDH}	20			20			ns
$\overline{\text{CS}}$ Falling to SCLK Rising	t_{CSCR}	90			90			ns
SCLK Falling to $\overline{\text{CS}}$ Rising	t_{CFCS}	35			35			ns
Output Timing								
$\overline{\text{CS}}$ LOW to SDO Active	t_{CSO}			35			35	ns
SCLK Falling to SDO Data Valid	t_{CFDO}			60			60	ns
$\overline{\text{CS}}$ HIGH to SDO High Impedance	t_{CSZ}			100			100	ns
POWER SUPPLY								
Operating Voltage								
V_A+		+4.75	+5	+5.25	+4.75	+5	+5.25	V
V_A–		–4.75	–5	–5.25	–4.75	–5	–5.25	V
V_D+		+4.75	+5	+5.25	+4.75	+5	+5.25	V
Quiescent Current								
I_A+	V_A+ = +5V		8	10		8	10	mA
I_A–	V_A– = –5V		10	12		10	12	mA
I_D+	V_D+ = +5V		0.5	1.0		0.5	1.0	mA
Power–Supply Rejection Ratio PSRR (250Hz)			100			100		dB
TEMPERATURE RANGE								
Operating Range		–40		+85	–40		+85	°C
Storage Range		–65		+150	–65		+150	°C
Thermal Resistance, $_{JC}$								
DIP–16			60			60		°C/W
SOL–16			50			50		°C/W

PIN CONFIGURATION

Top View DIP, SOL



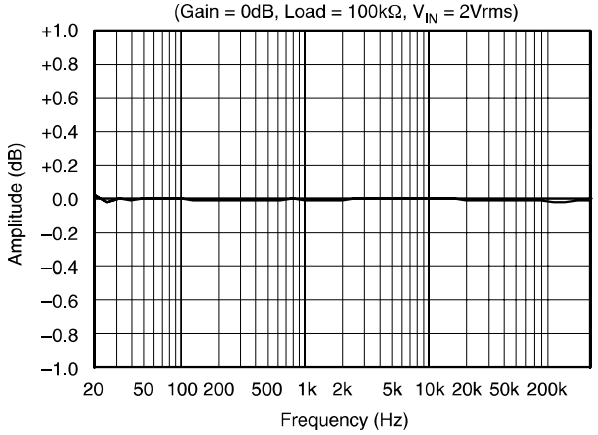
PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	ZCEN	Zero Crossing Enable Input (Active HIGH)
2	$\overline{CS}$	Chip Select Input (Active LOW)
3	SDI	Serial Data input
4	V_D+	Digital Power Supply, +5V
5	DGND	Digital Ground
6	SCLK	Serial Clock Input
7	SDO	Serial Data Output
8	$\overline{MUTE}$	Mute Control Input (Active LOW)
9	V_{IN}R	Analog Input, Right Channel
10	AGNDR	Analog Ground, Right Channel
11	V_{OUT}R	Analog Output, Right Channel
12	V_A+	Analog Power Supply, +5V
13	V_A–	Analog Power Supply, –5V
14	V_{OUT}L	Analog Output, Left Channel
15	AGNDL	Analog Ground, Left Channel
16	V_{IN}L	Analog Input, Left Channel

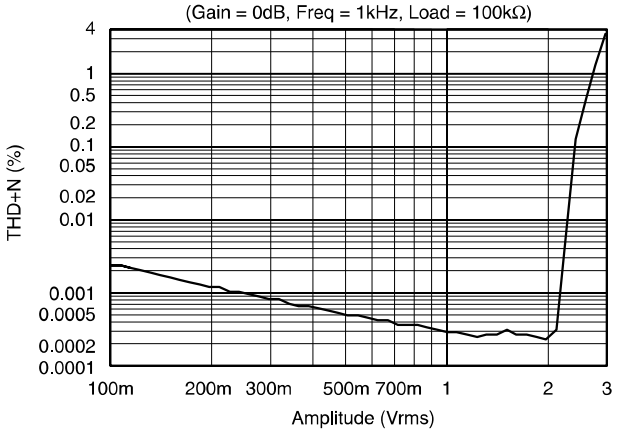
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_A+ = +5V, V_A– = –5V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 10Hz to 20kHz, unless otherwise noted.
(NOTE: All plots taken with PGA2311 A–Grade.)

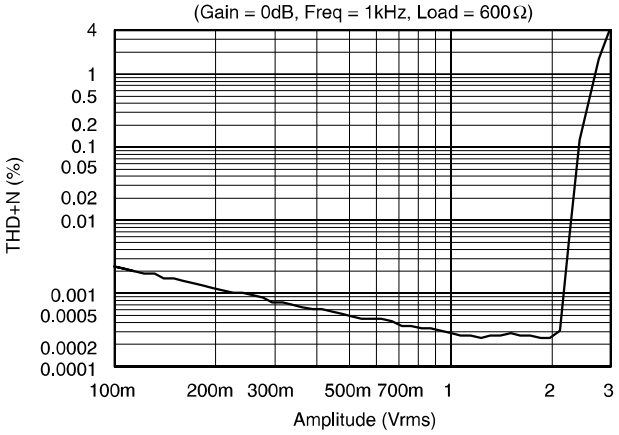
AMPLITUDE vs FREQUENCY
(Gain = 0dB, Load = 100kΩ, V_{IN} = 2Vrms)



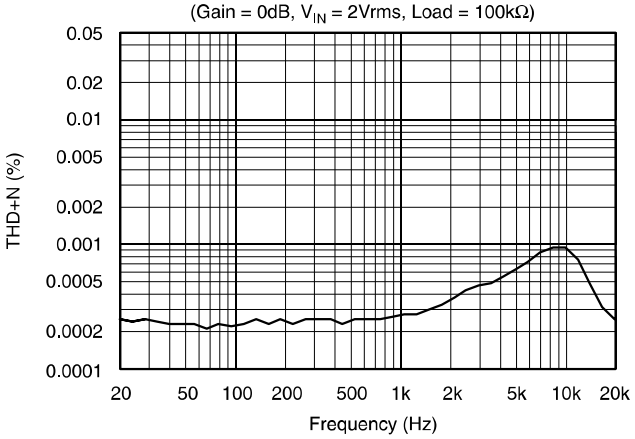
THD+N vs AMPLITUDE
(Gain = 0dB, Freq = 1kHz, Load = 100kΩ)



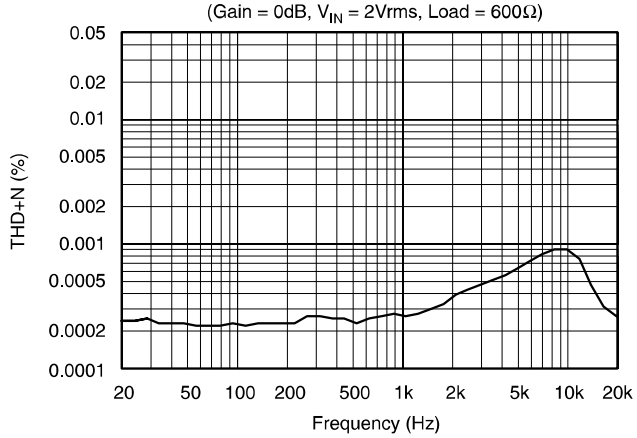
THD+N vs AMPLITUDE
(Gain = 0dB, Freq = 1kHz, Load = 600Ω)



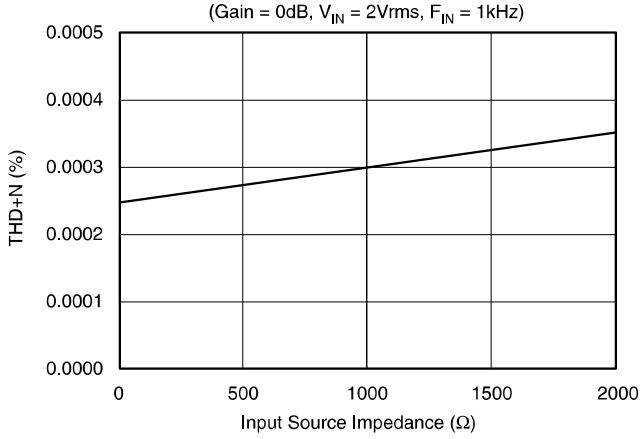
THD+N vs FREQUENCY
(Gain = 0dB, V_{IN} = 2Vrms, Load = 100kΩ)



THD+N vs FREQUENCY
(Gain = 0dB, V_{IN} = 2Vrms, Load = 600Ω)

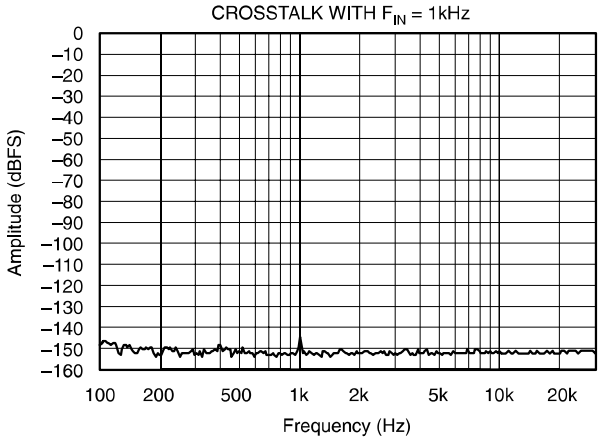


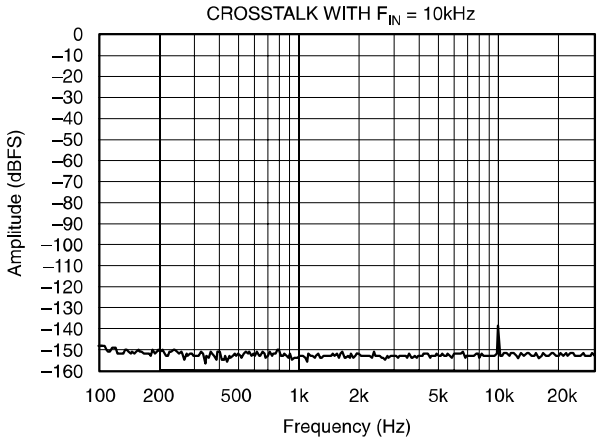
THD+N vs INPUT SOURCE IMPEDANCE
(Gain = 0dB, V_{IN} = 2Vrms, F_{IN} = 1kHz)

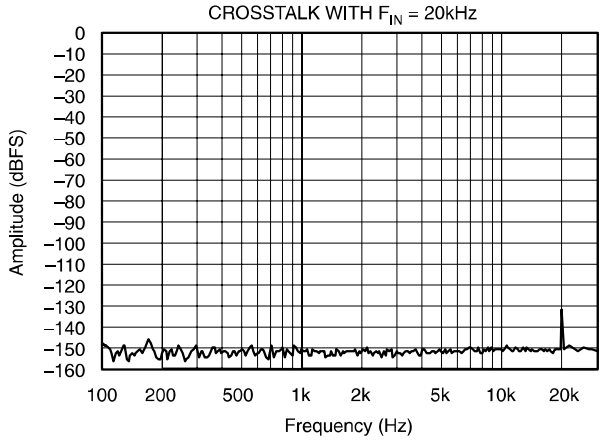


TYPICAL CHARACTERISTICS (CONT.)

At T_A = +25°C, V_A+ = +5V, V_A– = –5V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 10Hz to 20kHz, unless otherwise noted.
(NOTE: All plots taken with PGA2311 A–Grade.)







GENERAL DESCRIPTION

The PGA2311 is a stereo audio volume control. It may be used in a wide array of professional and consumer audio equipment. The PGA2311 is fabricated in a sub–micron CMOS process.

The heart of the PGA2311 is a resistor network, an analog switch array, and a high–performance op amp stage. The switches are used to select taps in the resistor network that, in turn, determine the gain of the amplifier stage. Switch selections are programmed using a serial control port. The serial port allows connection to a wide variety of host controllers. Figure 1 shows a functional block diagram of the PGA2311.

POWER–UP STATE

On power up, "power–up reset" is activated for about 100ms during which the circuit is in hardware $\overline{\text{MUTE}}$ state and all internal flip-flops are reset. At the end of this period, the offset calibration is initiated without any external signals. Once this has been completed, the gain byte value for both the left and right channels are set to 00_{HEX}, or the software $\overline{\text{MUTE}}$ condition. The gain will remain at this setting until the host controller programs new settings for for each channel via the serial control port.

If during normal operation the power supply voltage drops below ±3.2V, the circuit enters a hardware $\overline{\text{MUTE}}$ state. A power-up sequence will be initiated if the power supply voltage returns to greater than ±3.2V.

ANALOG INPUTS AND OUTPUTS

The PGA2311 includes two independent channels, referred to as the left and right channels. Each channel has a corresponding input and output pin. The input and output pins are unbalanced, or referenced to analog ground (either AGNDR or AGNDL). The inputs are named $V_{IN}R$ (pin 9) and $V_{IN}L$ (pin 16), while the outputs are named $V_{OUT}R$ (pin 11) and $V_{OUT}L$ (pin 14).

The input and output pins may swing within 1.25V of the analog power supplies, V_A+ (pin 12) and $V_A–$ (pin 13). Given V_A+ = +5V and $V_A–$ = –5V, the maximum input or output voltage range is 7.5Vp-p.

For optimal performance, it is best to drive the PGA2311 with a low source impedance. A source impedance of 600Ω or less is recommended. Source impedances up to 2kΩ will cause minimal degradation of THD+N. Please refer to the "THD+N vs Source Impedance" plot in the Typical Characteristics section of the datasheet.

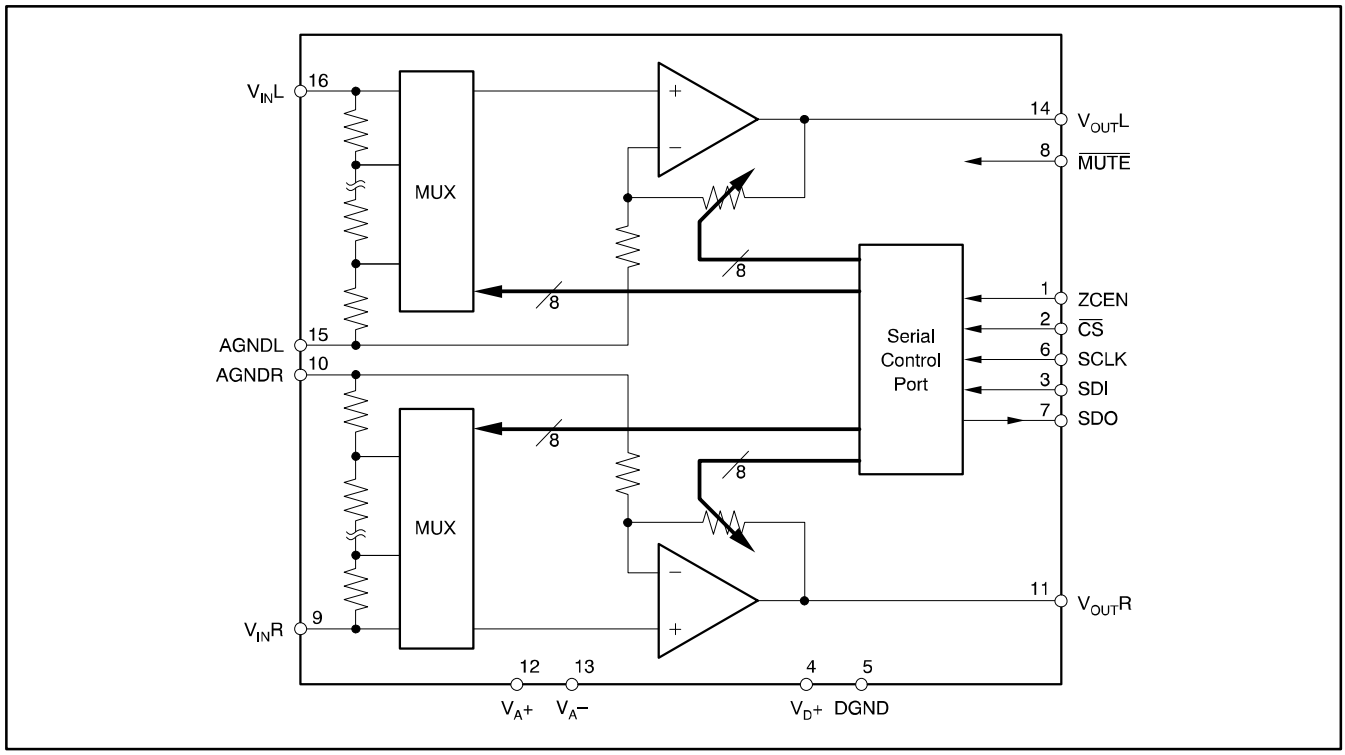


Figure 1. PGA2311 Block Diagram.

SERIAL CONTROL PORT

The serial control port is utilized to program the gain settings for the PGA2311. The serial control port includes three input pins and one output pin. The inputs include $\overline{CS}$ (pin 2), SDI (pin 3), and SCLK (pin 6). The sole output pin is SDO (pin 7).

The $\overline{CS}$ pin functions as the chip select input. Data may be written to the PGA2311 only when $\overline{CS}$ is LOW. SDI is the serial data input pin. Control data is provided as a 16-bit word at the SDI pin, 8 bits each for the left and right channel gain settings.

Data is formatted as MSB first, straight binary code. SCLK is the serial clock input. Data is clocked into SDI on the rising edge of SCLK.

SDO is the serial data output pin, and is used when daisy-chaining multiple PGA2311 devices. Daisy-chain operation is described in detail later in this section. SDO is a tri-state output, and assumes a high impedance state when $\overline{CS}$ is HIGH.

The protocol for the serial control port is shown in Figure 2. See Figure 3 for detailed timing specifications for the serial control port.

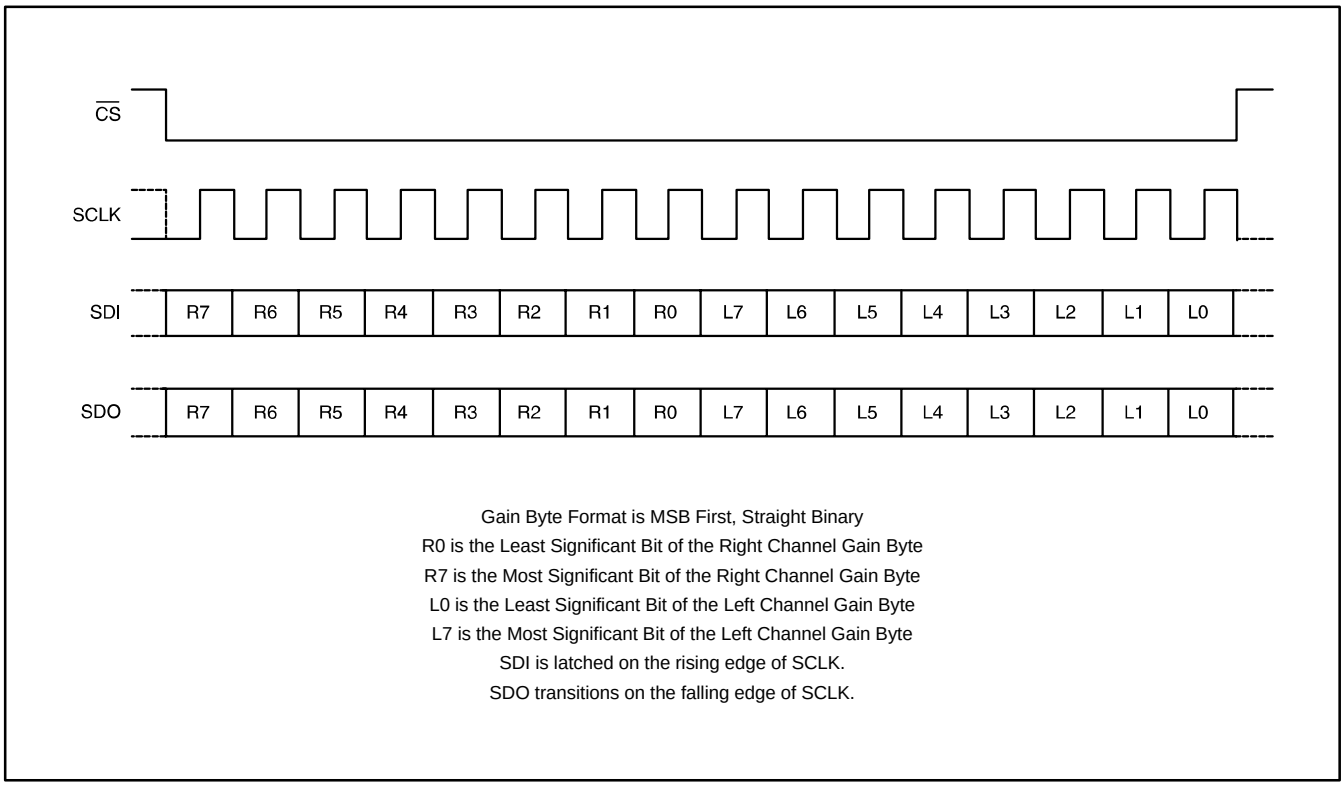


Figure 2. Serial Interface Protocol.

GAIN SETTINGS

The gain for each channel is set by its corresponding 8–bit code, either R[7:0] or L[7:0] (see Figure 2). The gain code data is straight binary format. If we let N equal the decimal equivalent of R[7:0] or L[7:0], then the following relationships exist for the gain settings:

For N = 0:

Mute Condition. The input multiplexer is connected to analog ground (AGNDR or AGNDL).

For N = 1 to 255:

Gain (dB) = 31.5 – [0.5 w (255 – N)]

This results in a gain range of +31.5dB (with N = 255) to –95.5dB (with N = 1).

Changes in gain setting may be made with or without zero crossing detection. The operation of the zero crossing detector and timeout circuitry is discussed later in this data sheet.

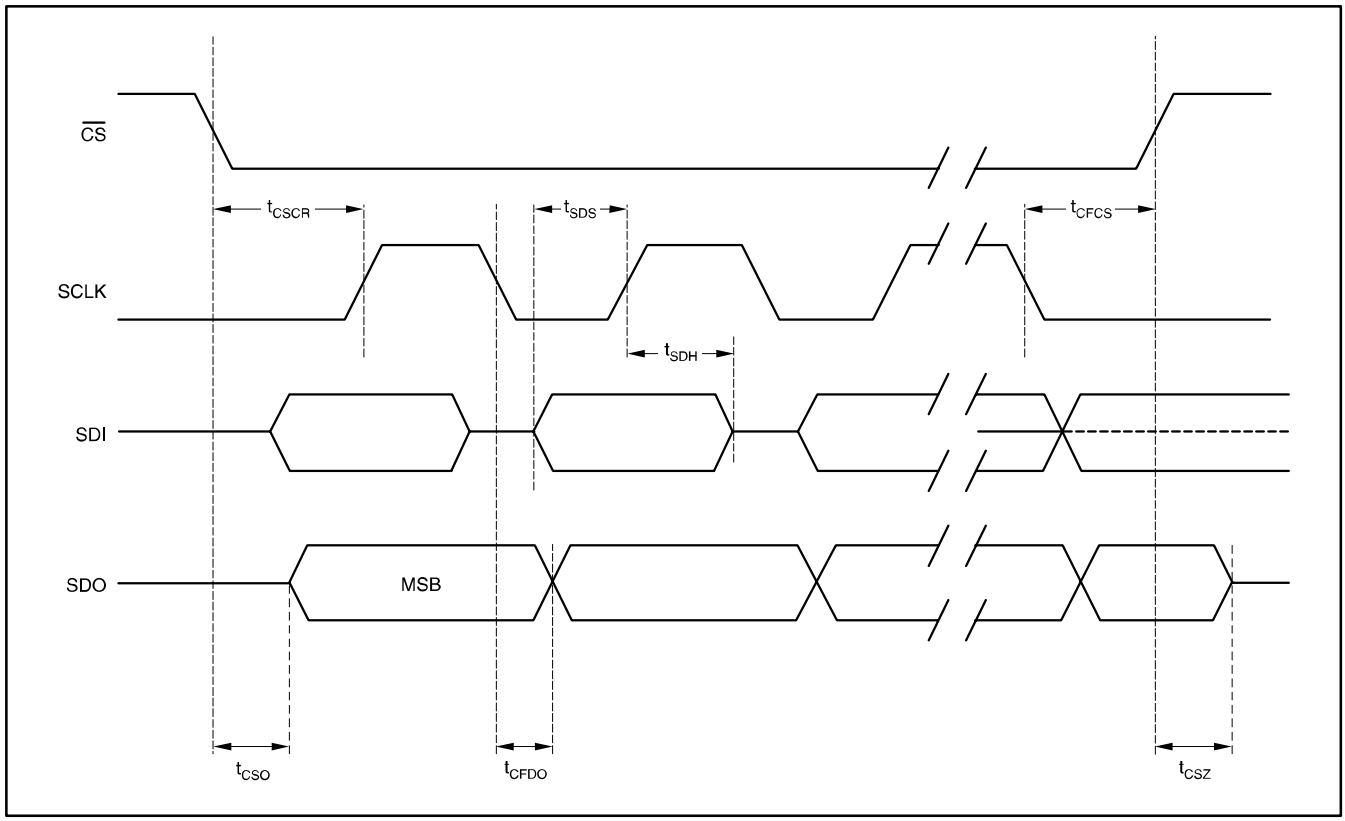


Figure 3. Serial Interface Timing Requirements.

DAISY-CHAINING MULTIPLE PGA2311 DEVICES

In order to reduce the number of control signals required to support multiple PGA2311 devices on a printed circuit board, the serial control port supports daisy-chaining of multiple PGA2311 devices. Figure 4 shows the connection requirements for daisy-chain operation. This arrangement allows a 3-wire serial interface to control many PGA2311 devices.

As shown in Figure 4, the SDO pin from device #1 is connected to the SDI input of device #2, and is repeated for additional devices. This in turn forms a large shift register, in which gain data may be written for all PGA2311s connected to the serial bus. The length of the shift register is 16 • N bits, where N is equal to the number of PGA2311 devices included in the chain. The $\overline{CS}$ input must remain LOW for 16 • N SCLK periods, where N is the number of devices connected in the chain, in order to allow enough SCLK cycles to load all devices.

ZERO CROSSING DETECTION

The PGA2311 includes a zero crossing detection function that can provide for noise-free level transitions. The concept is to change gain settings on a zero crossing of the input signal, thus minimizing audible glitches. This function is enabled or disabled using the ZCEN input (pin 1). When ZCEN is LOW, zero crossing detection is disabled. When ZCEN is HIGH, zero crossing detection will be enabled.

The zero crossing detection takes effect with a change in gain setting for a corresponding channel. The new gain setting will not be implemented until either positive slope zero crossing is detected or a time-out period of 16ms has elapsed. In the case of a time-out, the new gain setting takes effect with no attempt to minimize audible artifacts.

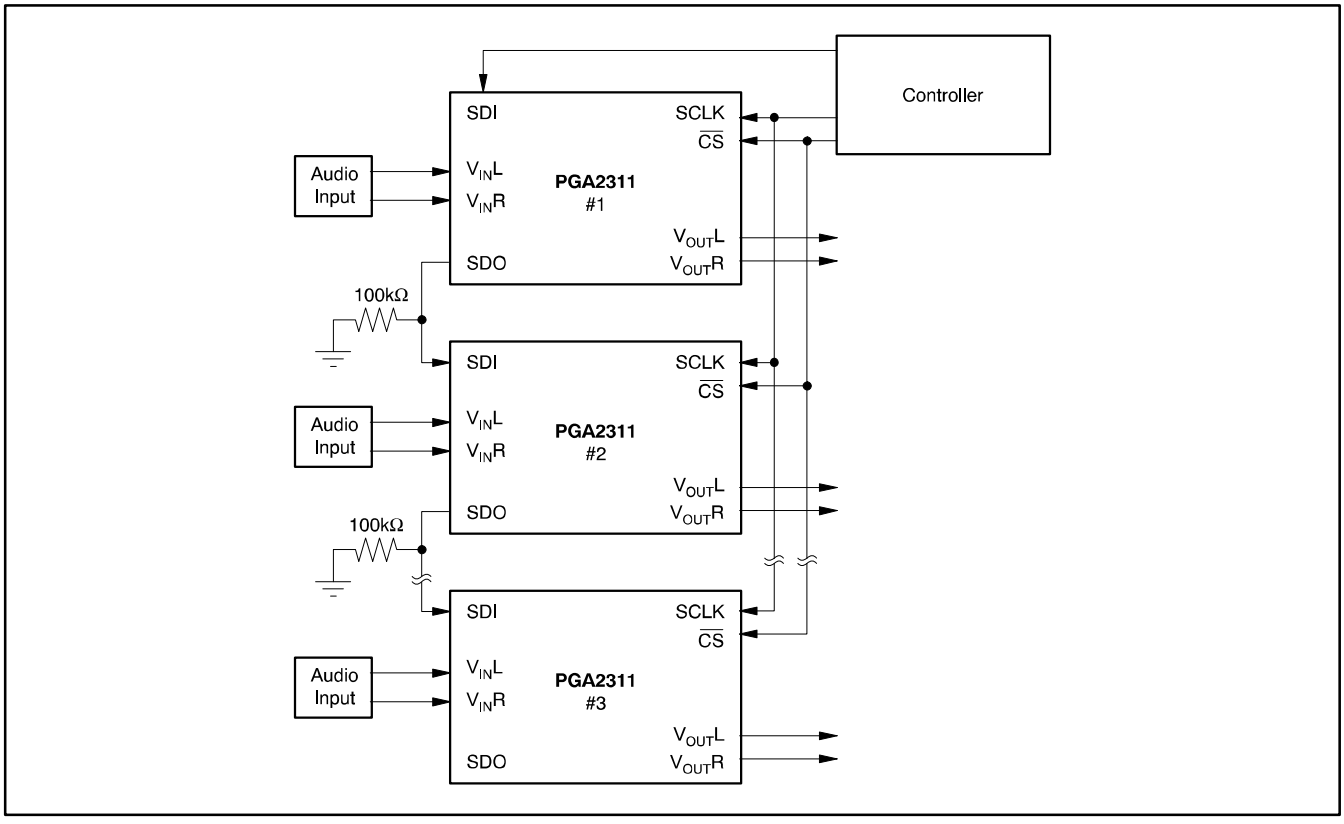


Figure 4. Daisy-Chaining Multiple PGA2311 Devices.

$\overline{\text{MUTE}}$ FUNCTION

Muting can be achieved by either hardware or software control. Hardware muting is accomplished via the $\overline{\text{MUTE}}$ input, and software muting by loading all zeroes into the volume control register.

$\overline{\text{MUTE}}$ disconnects the internal buffer amplifiers from the output pins and terminates $A_{OUT}L$ and $A_{OUT}R$ with 10kΩ resistors to ground. The mute is activated with a zero crossing detection (independent of the zero cross enable status) or an 16ms time-out to eliminate any audible “clicks” or “pops”. $\overline{\text{MUTE}}$ also initiates an internal offset calibration.

A software mute is implemented by loading all zeroes into the volume control register. The internal amplifier is set to unity gain with the amplifier input connected to AGND.

APPLICATIONS INFORMATION

This section includes additional information that is pertinent to designing the PGA2311 into an end application.

RECOMMENDED CONNECTION DIAGRAM

Figure 5 depicts the recommended connections for the PGA2311. Power-supply bypass capacitors should be placed as close to the PGA2311 package as physically possible.

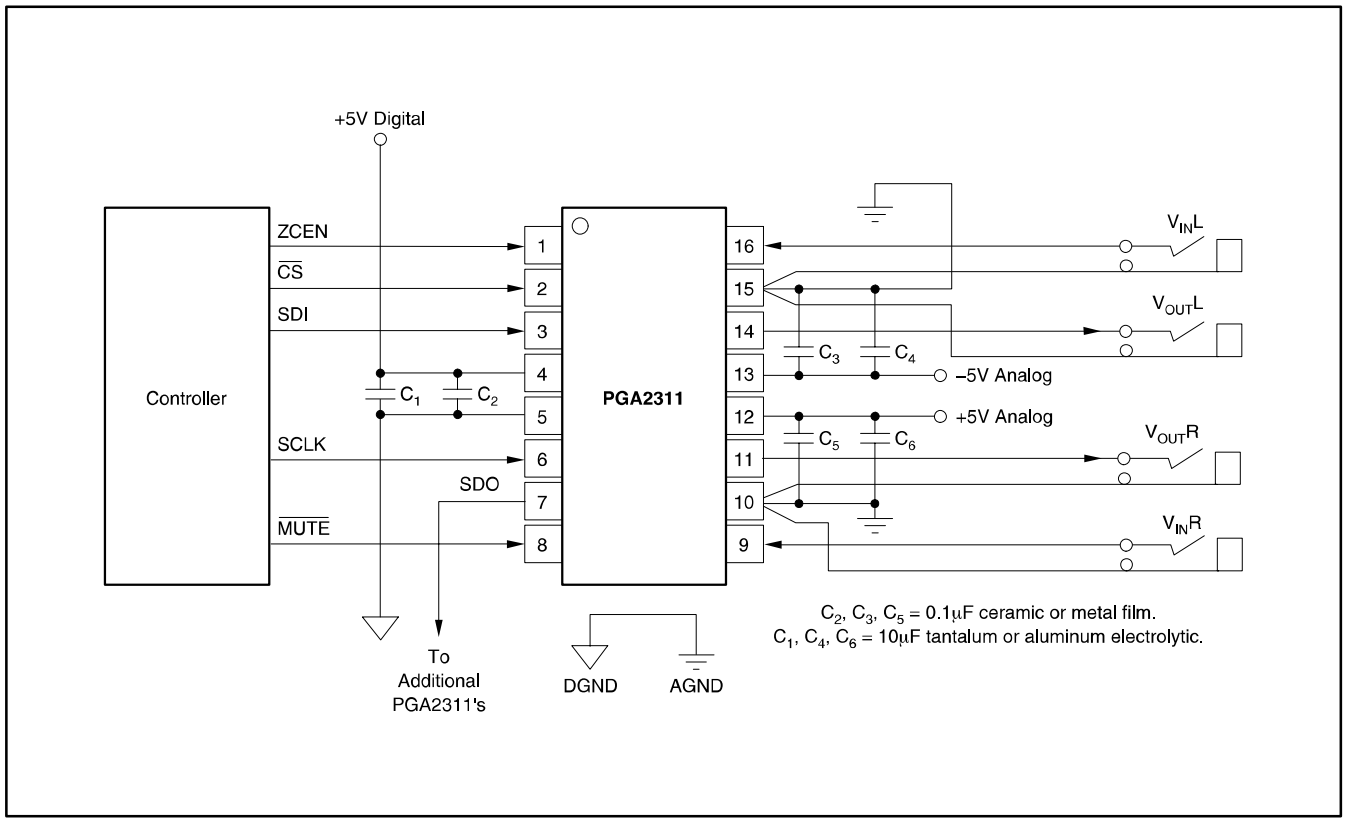


Figure 5. Recommended Connection Diagram.

PRINTED CIRCUIT BOARD (PCB) LAYOUT GUIDELINES

It is recommended that the ground planes for the digital and analog sections of the PCB be separate from one another. The planes should be connected at a single point. Figure 6 shows the recommended PCB floor plan for the PGA2311.

The PGA2311 is mounted so that it straddles the split between the digital and analog ground planes. Pins 1 through 8 are oriented to the digital side of the board, while pins 9 through 16 are on the analog side of the board.

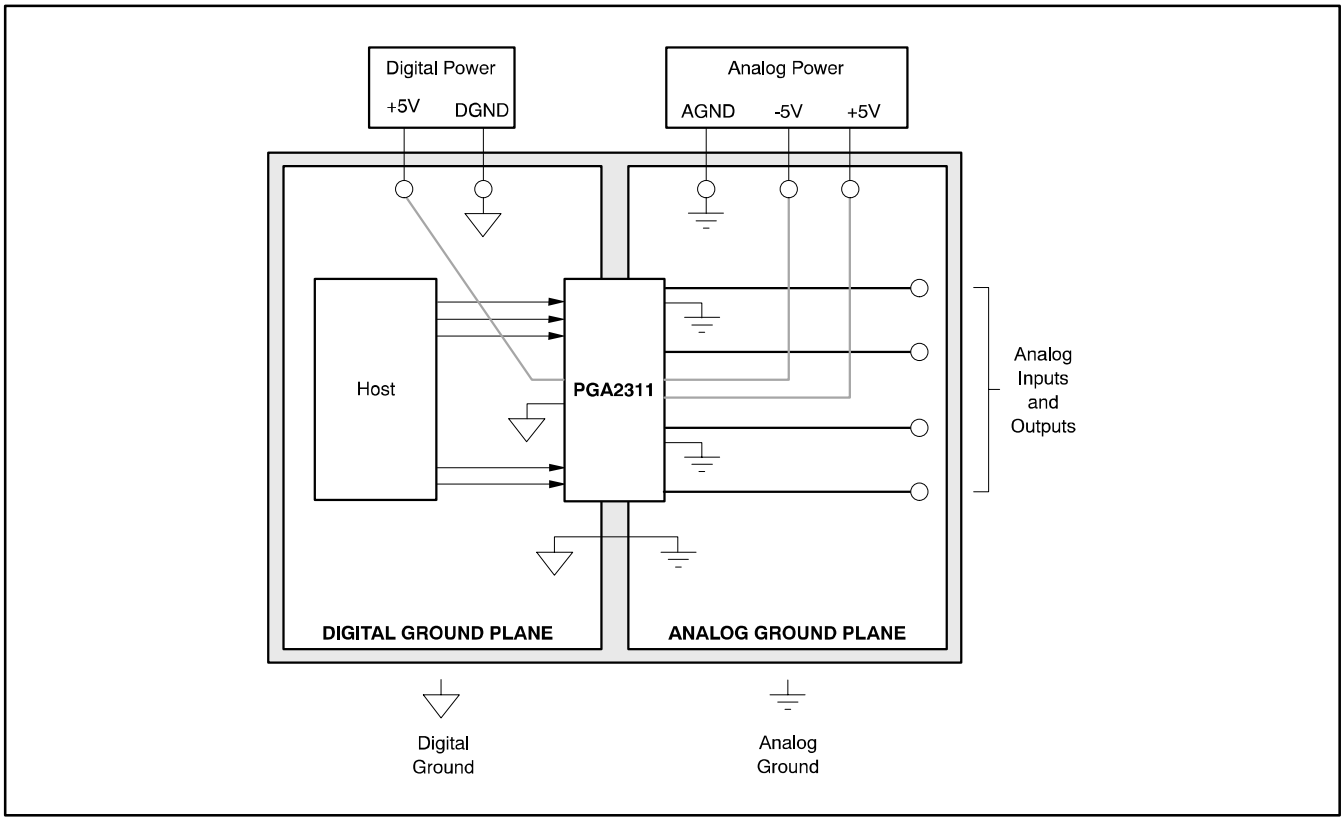


Figure 6. Typical PCB Layout Floor Plan.

PACKAGE DRAWINGS

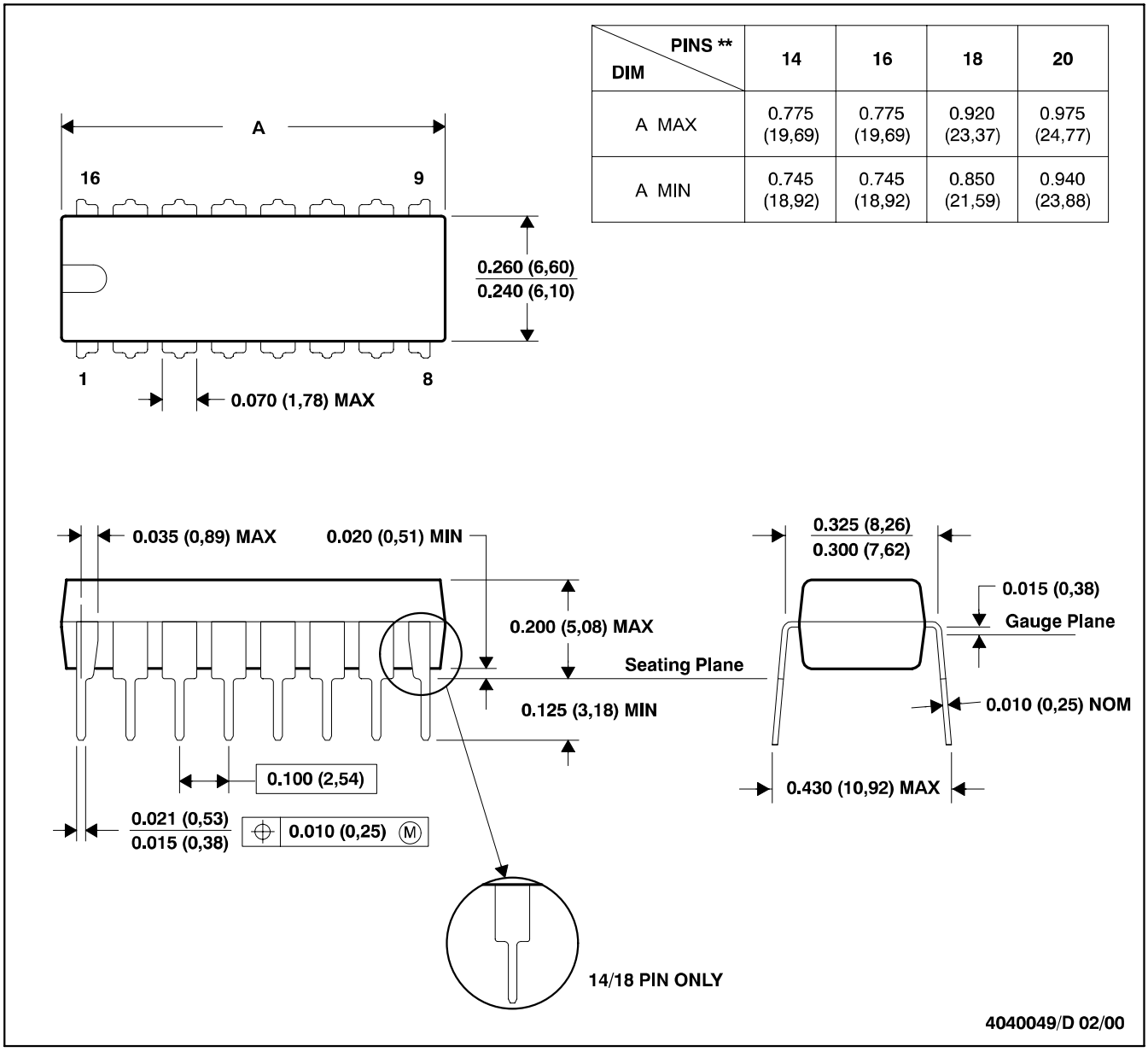
MPDI002B ± JANUARY 1995 ± REVISED FEBRUARY 2000

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)



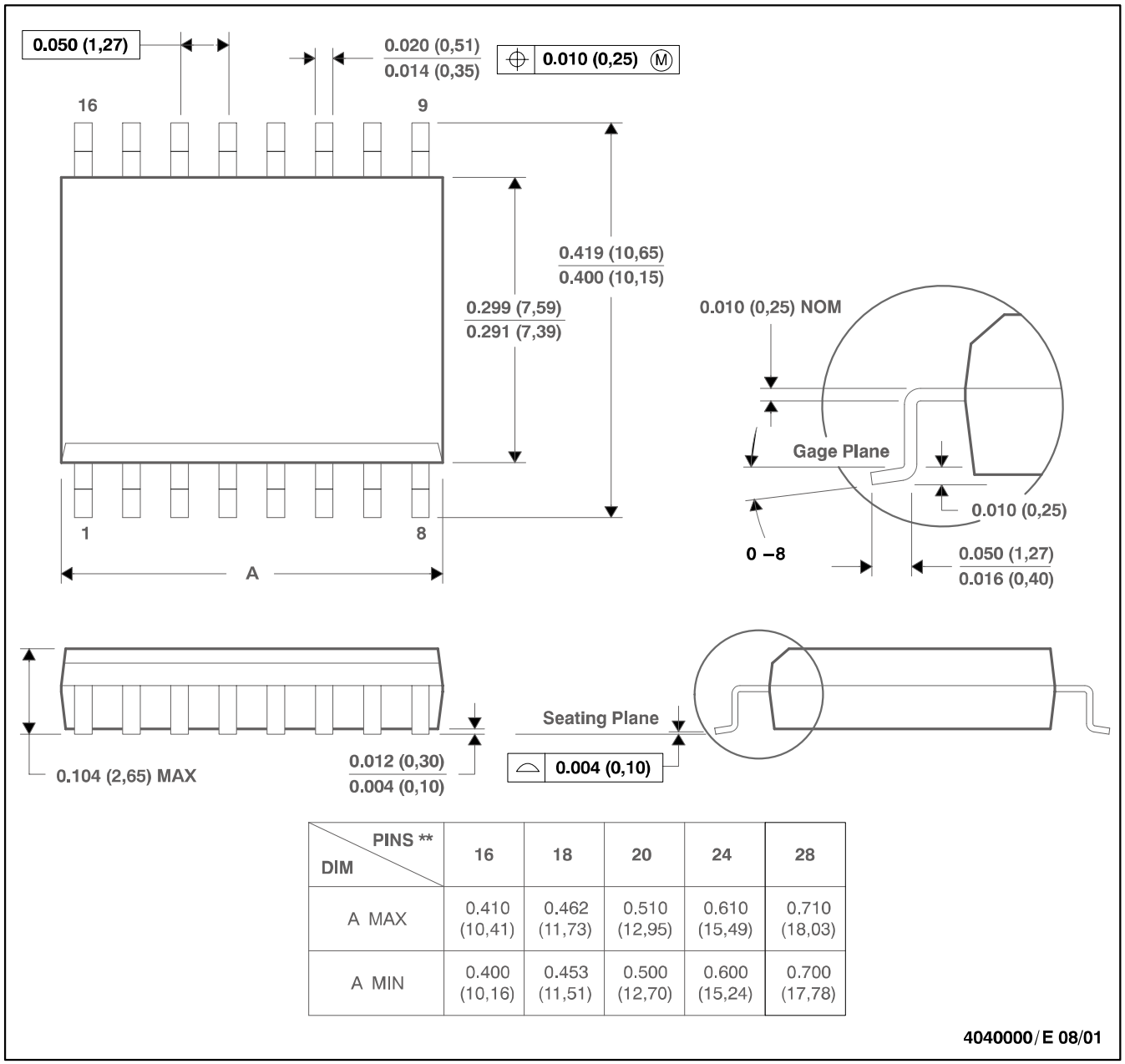
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

PACKAGE DRAWINGS (Cont.)

MSOI003E – JANUARY 1995 – REVISED SEPTEMBER 2001

DW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
PGA2311P	ACTIVE	PDIP	N	16	25
PGA2311PA	ACTIVE	PDIP	N	16	25
PGA2311U	ACTIVE	SOIC	DW	16	48
PGA2311U/1K	ACTIVE	SOIC	DW	16	1000
PGA2311UA	ACTIVE	SOIC	DW	16	48
PGA2311UA/1K	ACTIVE	SOIC	DW	16	1000

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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