Mini Router

The project consists in the design and the implementation, using VHDL, of a synchronous mini-router. The mini-router send to the output a selection between 2 input sources. The input data are represented on 8 bit, with 2 priority bit (0=minor priority, 3=maximum priority). The input data are valid when the correspondent req signal is hold to 1. req, grant and data set of signals (10 bit, which 8 bit for the data and 2 bit for the priority) is called "link".

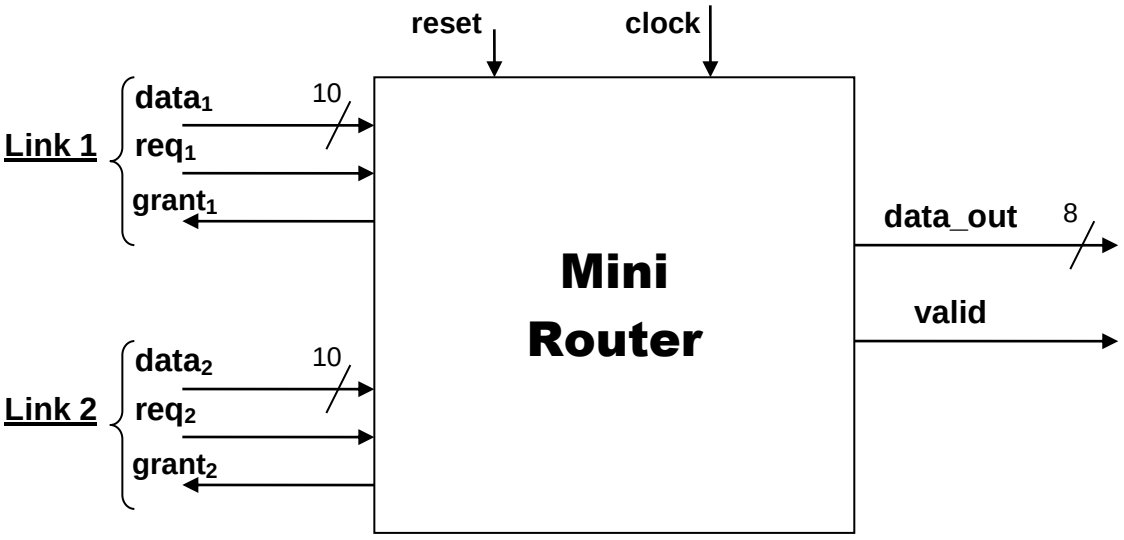
If in a clock cycle only one of the two req signals is high then the correspondent link's data are propagated to the output. Otherwise, if both of req signals are high, the mini-router has to select the link with the higher priority. If the link have the same priority (data conflict), then it is chosen one of the two following a Round Robin algorithm: after the reset, at the first conflict, it is selected the link 1, at the second conflict the link 2, at the third conflict the link 1, and so on…

The link selection and the possible conflict resolution is processed every clock cycle.

When the output data are presented, the correspondent grant signal of the selected link is set high, as the valid output, for 1 clock cycle. N.B. the output data are transmitted without the priority section.

The reset can be active high or active low as a choice of the VHDL designer.

The interface of the circuit to be designed is as follows:



You are requested to deal with the various possible error situations, documenting the choices made.

The final project report must contain:

- Introduction (circuit description, possible applications, possible architectures, etc.)
- Description of the architecture designed (block diagram, inputs/outputs, etc.)
- VHDL code (with detailed comments) to be attached to the report.
- Test strategy (Test-plan) and related Testbench for verification; a detailed, though not exhaustive, verification is required, including error situations and borderline cases of functioning
- Interpretation of the results obtained in the automatic synthesis/implementation on a Xilinx FPGA platform in terms of maximum clock frequency (critical path), elements used (slice, LUT, etc.) and estimated power consumption. Comment on any warning messages.
- Conclusions