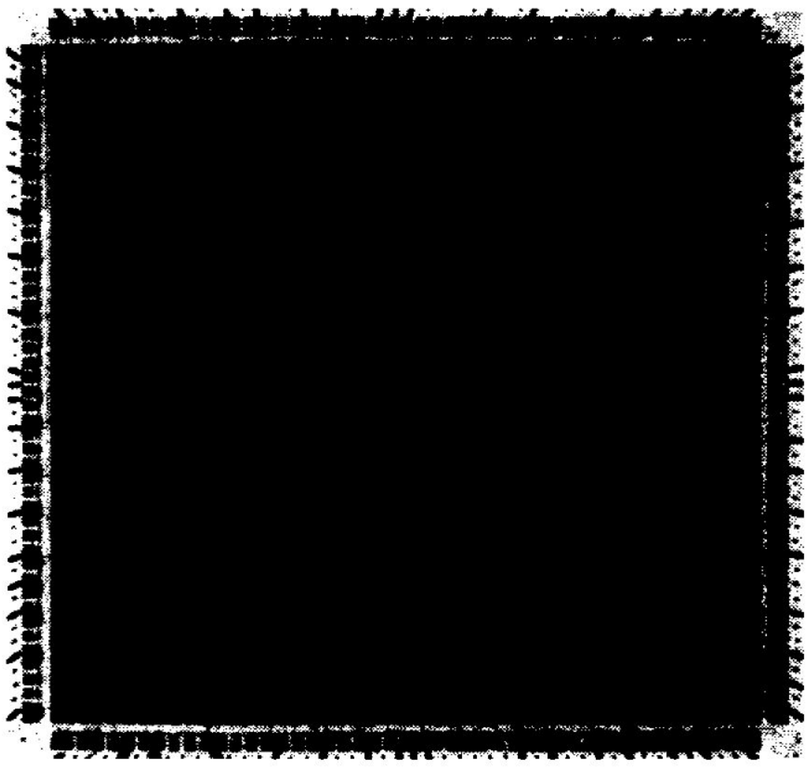
L64243
3 x 3 Multi-Bit Filter (MFIR3)

Description

The L64243 is a 9-tap high speed transversal filter processor consisting of a 9-tap section, with 8-bit wide coefficients and data. The processor can be configured as a 1-D (one-dimensional) filter for radar or other signal processing applications, or as a 2-D (two-dimensional) filter for image processing applications. The processor accepts 2-D data directly from a L64210/L64211 Variable-Length Video Shift Register or other video source. The coefficients can be changed to perform adaptive filtering and correlation.

The processor is ideally suited for real-time image processing applications such as video pattern matching, noise removal, inverse filtering, edge enhancement and edge detection. The maximum window size is 3 x 3 for a chip. Data throughput of 40 MHz makes the processor suitable for radar processing. The L64243 is implemented in a 1.5-micron drawn gate length (0.9-micron effective channel length) low power HCMOS technology.



L64243 Chip

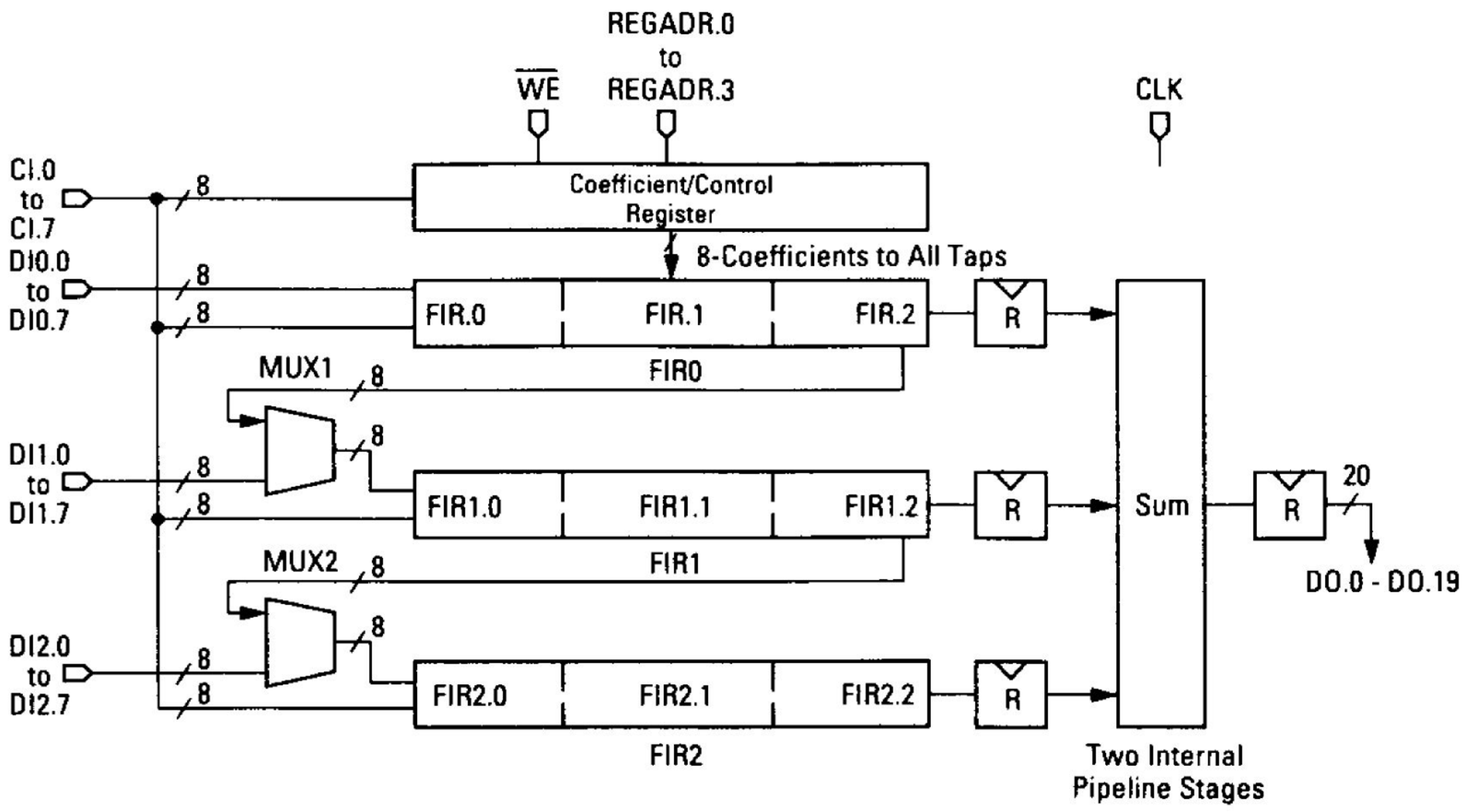
Features

- 9-taps, 8-bit data and coefficients
- Reconfigurable for 1-D and 2-D correlation/convolution
- Two's complement or unsigned 8-bit input data and coefficient
- Output precision up to 20 bits
- Double buffering of coefficients
- High speed operation

	Commercial	Military
L64243-40	40 MHz	40 MHz
L64243-30	30 MHz	30 MHz
L64243-20	20 MHz	20 MHz

- Available in 68-pin CPGA (Ceramic Pin Grid Array) or 68-pin PLDCC (Plastic Leaded Chip Carrier) package

Block Diagram



L64243
3 x 3 Multi-Bit Filter
(MFIR3)

LSI LOGIC

Architecture

The L64243 Multi-Bit Filter is a stand-alone FIR (finite impulse response) filter which can operate on either 1-D or 2-D data. It is easily reconfigurable to perform FIR filter operations with a variety of window sizes and shapes.

It operates at very high speeds and is useful in high-end applications such as radar signal processing, image processing, high speed data communications, and other areas where performance and processing power are important.

The L64243 performs convolution/correlation operations of the type:

$$\text{1-D: } y(n) = \sum_{l=0} hl \times (n-1)$$

$$\text{2-D: } y(n, m) = \sum_{l=0}^{L-1} \sum_{k=0}^{K-1} hl, k \times (n-1, m-k)$$

The device contains three individual 3rd order FIR filters (FIR0-FIR2). Each of the nine taps accepts two's complement or unsigned 8-bit integer data and coefficients. The L64243 has three separate input buses (DI0 through D12), one for each of the FIR sections. By controlling the input source to each 3-tap FIR section, the Multi-Bit Filter can be configured as a 9th order 1-D FIR filter or as a 2-D filter with a 3 x 3 window, both with 8-bit data and coefficients.

All coefficients are double-buffered. This allows the user to load a new set of coefficients while processing continues on the current set. Thus, the processor does not require the insertion of new control inputs at the same speed as the data rate.

The outputs of the three 3rd order filters are summed together and the result is latched in a pipeline register. Up to this stage no arithmetic overflow can occur regardless of the values of data, coefficients, and operating parameters.

A 20-bit output bus (DO) is available for both 1-D and 2-D configurations.

Pin Listing and Description

Note: For all buses, SIGNALY.X denotes the Xth bit of SIGNALY. The LSB of bus SIGNALY is SIGNALY.0.

DI0-DI2
Three individual data input buses, each eight bits wide. When the L64243 is used as a 1-D filter with 8-bit wide data, only pins DI0.0 to DI0.7 are used. The remaining data input pins are either left unconnected or used for other functions depending on the system configuration. When used as a 2-D filter processor with a 3 x 3 window, the L64243 operates with all 24 data input pins (DI0.0 to DI0.7 ... DI2.0 to DI2.7) active. DI0.0 to DI0.7, DI1.0 to DI1.7 and DI2.0 DI2.7 are unidirectional input pins. All DI inputs default to LOW when left unconnected.

CI.0 to CI.7
Coefficient/control input pins. An 8-bit coefficient can be loaded into any one of the nine filter taps by choosing the address of the destination filter cell with REGADR.0 to REGADR.3. CI.0 to CI.7 are used to input coefficients when decimal value of REGADR.0- REGADR.3 is less than nine. CI.0 to CI.7 are interpreted as control bits for setting filter processing parameters when REGADR.0 to REGADR.3 is 9. CI.0 to CI.7 are ignored when REGADR.0 - REGADR.3 are greater than nine during loading of coefficients and control bits.

BNKLDI
Input signal, set HIGH to bank load new coefficients and certain decoded internal control signals from master to slave registers. While asynchronously loading coefficients/controls with respect to CLK, BNKLDI is held LOW until bank loading accurs. When loading coefficient/control synchronous to CLK, BNKLDI is held HIGH.

$\overline{WE}$
Write enable input, active LOW, for enabling the loading of coefficients and decoded control signals into the destination latches selected by REGADR.0 to REGADR.3.

REGADR.0 to REGADR.3
Inputs indicating the destination address of the coefficients or control signals where they are loaded into master latches when WE is LOW. When (REGADR.0 - REGADR.3) are between 0 and 8 inclusive, CI.0 to CI.7 are interpreted as coefficients. When (REGADR.0 - REGADR.3) is nine, the CI inputs are interpreted as control signals. When (REGADR.0 - REGADR.3) > 9, the destination address is invalid.

CLK
System clock controls all positive edge-triggered master-slave flip-flops in the data path. When BNKLDI is HIGH, CLK enables the level-triggered slave latches of all coefficients.

DO.0 to DO.19
Multi-Bit filter data output.

Test
Internal LSI Logic test output. Should be left unconnected by user.

Pin Description and Summary

Pin	No. of Pins	I/O	Description
DI0.0 - DI0.7	8	I	Data input bus 0
DI1.0 - DI1.7	8	I	Data input bus 1 [2 - D]
DI2.0 - DI2.7	8	I	Data input bus 2 [2 - D]
CI.0 - CI.7	8	I	Coefficient/control input bus
DO.0 - DO.19	20	O	Filter output
CLK	1	I	System clock
BNKLDI	1	I	Bank loads
$\overline{WE}$	1	I	Write enable for coefficient/control registers
REGADR.0 - REGADR.3	4	I	Address of coefficient/control registers

Functional Overview

One-Dimensional Processing: The L64243 performs convolution/correlation of the form:

$$D0(n) = \sum_{i=0}^{8} hi\ DI0(n - i - 5)$$

D0(n) is the time domain filter output of a 9th order FIR filter.

DI0(n - i) is the delayed data input (the data value of the ith filter tap at time n). The position of the ith filter tap (FIRy.x) in the L64243 block diagram can be found by:

$i = 3y + x.$

hi is the active coefficient in the ith filter cell, which in this case is assumed to be time invariant. The sum of the nine products of data and coefficients in all the filter taps can be represented by:

$$\sum_{i=0}^{8} hi\ DI0(n - i).$$

Extra latency is introduced by certain factors. The data register in FIR0.0 and four pipeline registers introduce a total delay of five cycles. Taking these factors into consideration gives the filter output term:

$$\sum_{i=0}^{8} hi\ (DI0(n - i - 5)$$

Two Dimensional Processing: The L64243 performs convolution/correlation of the form:

$$D0(n) = \sum_{i=0}^{2} \sum_{j=0}^{2} hi,j\ DIi(n - j - 5)$$

In a typical system, DIi(n) is the ith output of the L64210/L64211 video shift register and D0(n), which represents the time-domain filter output, is the raster scanned video output from the Multi-Bit Filter. The value of n can be converted to a position in the video image of line length L by:

$n = Ly + x$

where x and y are coordinates of the pixel represented by D0 in the horizontal and vertical directions.

A 3 x 3 convolution of an image is considered in the equation, where i represents the row and j represents the column in the window in which a pixel is located. DIi(n - j) represents the pixel at location i,j in a moving window at time n. The latency (5) is the same as that explained in the 1-D case above. hi,j is the active coefficient in FIRi.j.

The familiar 2-D convolution equation:

$$D0(n) = \sum_{i=0}^{2} \sum_{j=0}^{2} hi,j\ DIi(n - j - 5)$$

Data I/O

The first 3-tap FIR filter section (FIR0) receives data directly from the first input bus (DI0). The other two 3-tap filter sections (FIR1–FIR2) receive 8-bit input data from either an external input bus or from the shift register output of the previous section. The multiplexer at the input to these sections determines the window shape of the filter. For example, if all multiplexers are set such that all sections receive input from the shift register output of the previous section, then the filter behaves as a 9-tap filter with only the DI0 bus active. When all multiplexers are set such that each of the three sections receives its input from the three input buses, then the filter behaves as a 3 x 3 2-D filter. Thus, by setting the multiplexers, it is possible to set the window shape to 1 x 9 or 3 x 3.

Two-Dimensional Configuration: Normally, an L64210/L64211 would be used to generate the multi-line data inputs required for 2-D operation.

Loading of Coefficients

The L64243 has an 8-bit coefficient input (CI.0 to CI.7) The location of the register into which the coefficient should be stored is selected by the pins REGADR.0 to REGADR.3. Coefficient loading occurs only when $\overline{WE}$ is set LOW. The coefficient destination address decoding scheme is summarized below:

Coefficient Address Decoding ($\overline{WE}$ = LOW)

REGADR.0 -REGADR.3	Coefficient (CI.0 - CI.7) Destination
0	FIR0.0
1	FIR0.1
2	FIR0.2
3	FIR1.0
4	FIR1.1
5	FIR1.2
6	FIR2.0
7	FIR2.1
8	FIR2.2

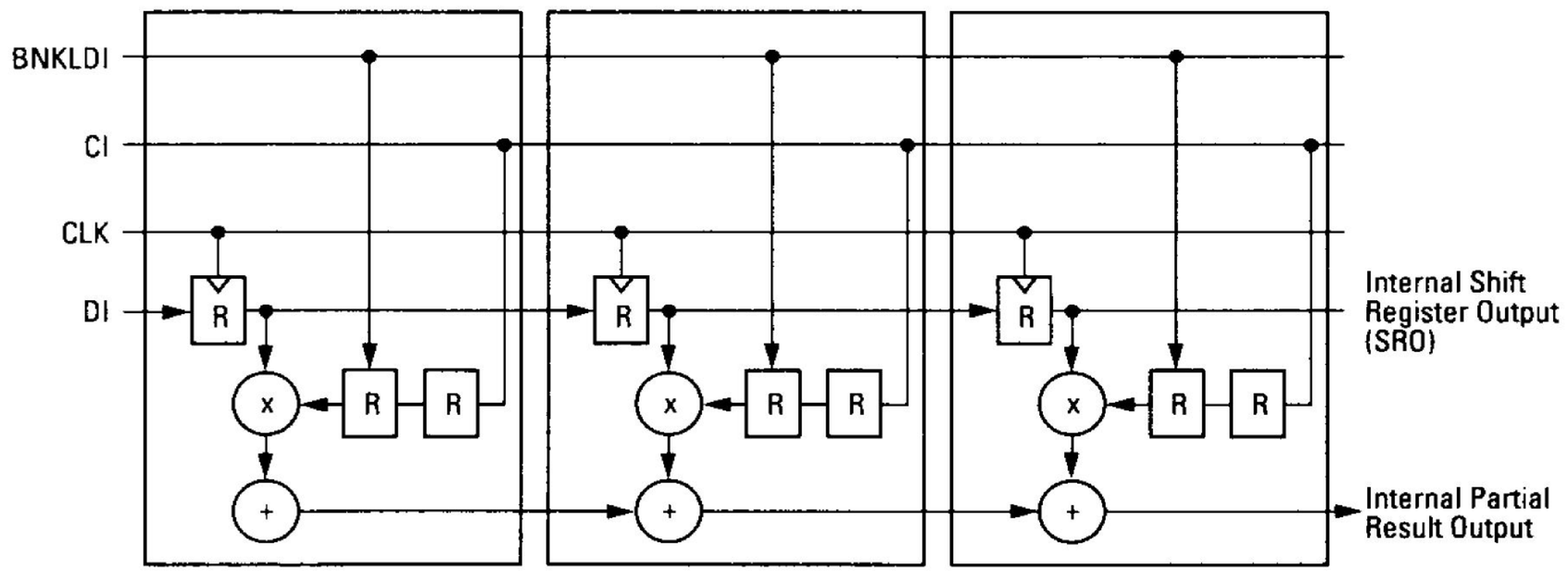
The diagram "3-Cell Filter Section" shows three taps that make up FIR0, FIR1 and FIR2. Coefficients are double-buffered with two level-triggered latches (master and slave) placed before the 8 x 8 multiplier of each cell The process of providing a valid coefficient to the multiplier of each filter cell consists of first loading the coefficient to the master latch, then transferring it to the slave latch. There are three methods of loading and transferring coefficients.

The first method is to load the coefficient into the master latch asynchronously to the system CLK and to transfer it to the slave latch in a manner synchronous to the CLK. The coefficient is loaded into the master latch at the filter location selected by the REGADR.0-REGADR.3 address and when $\overline{WE}$ is LOW. This is then repeated for each new coefficient for other filter cells in the processor. When the master latches of all the filter cells have been updated, the coefficients can be bank loaded simultaneously into the multipliers by enabling the slave latches when BNKLDI and CLK are HIGH. The transfer of coefficients from the master to the slave latches is synchronous to the CLK. This is illustrated in the diagram "AC Timing Waveforms – Bank Loading of Controls." This method provides flexibility in the loading of new coefficients into the processor without modifying the active set of coefficients.

The second method is to load and transfer coefficients synchronously to the system clock. This can be done with BNKLDI tied HIGH. $\overline{WE}$ is set from HIGH to LOW when CLK is LOW. During this time a new coefficient on bus CI is loaded into the master latch of the filter cell whose location has been determined by REGADR.0 - REGADR.3. On the next rising edge of CLK the coefficient is transferred to the slave latch, thus loading the active coefficient for the multiplier. In this way a new coefficient can replace the current one within one clock cycle.

The third method is to asynchronously load and transfer new coefficients over several cycles. This technique is used if it is not convenient to supply BNKLDI or $\overline{WE}$ signals synchronous to CLK. BNKLDI can be tied HIGH and $\overline{WE}$ operated asynchronously. In this case, every time a new coefficient is loaded the processor output could be invalid for up to 20 cycles after the rising edge of $\overline{WE}$.

3-Cell Filter Section



Loading of Control Bits

In addition to acting as input pins for coefficient loading, the bus pins CI.0 to CI.7 are also used for loading encoded control bits. $\overline{WE}$ must be LOW to load control bits into the processor. The decoding scheme for control bits is given below:

Control Bit Map ($\overline{WE}$ = LOW)

REGADR.0-REGADR.3	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
9	MUXCON	TCD	TCC	X	X	X	X	X

In the table above, REGADR > 9, generates invalid destination addresses. "X" means that the state of CI is ignored.

All internal signals are loaded directly. Hence, the loading of these controls is independent of CLK and BNKLDI. These parameters must be set during initialization. Whenever these parameters are changed during filter operation it significantly modifies the processor configuration. During such reconfiguration of the processor, the internal states may be corrupted and the output may not be valid for up to 20 cycles.

The internal signal MUXCON is the select line for MUX1 and MUX2. When MUXCON is HIGH, the corresponding MUX select line is set such that external data residing at the input bus pins is transferred to the corresponding 3-tap FIR block. When LOW, data is transferred from the previous FIR block to the output of the MUX. The table below summarizes the reconfiguration of the L64243 window, which must be set during initialization of the processor.

Window Shapes

MUXCON	Window Shape	Active Inputs
0	1 x 9	D0
1	3 x 3	D0, D1, D2

The L64243 supports two's complement, unsigned, or mixed-mode formats for operations with the data and coefficients. The interpretation of the formats is done in the following manner:

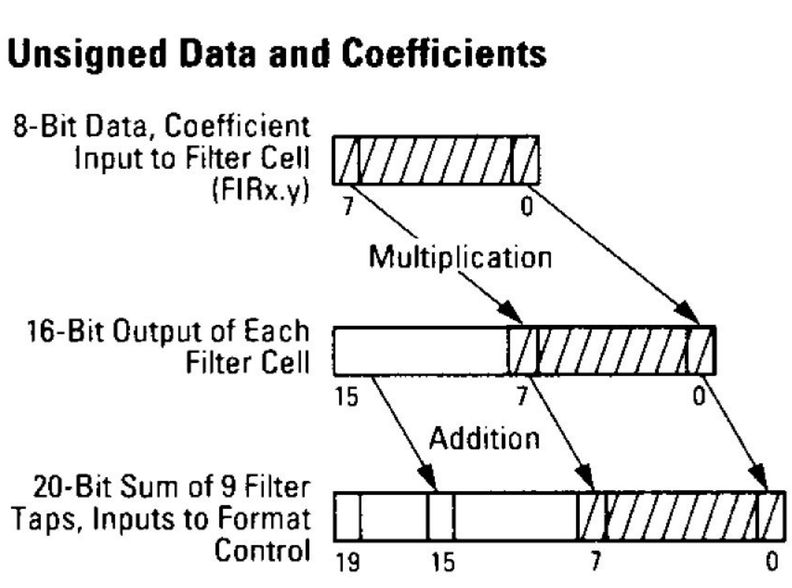
Data/Coefficient Formats

Internal Control Signal	State	Data/ Coefficient	Filter Cell Blocks	TC/ Unsigned
TCD	LOW	Data	FIR0 - FIR2	Unsigned
TCD	HIGH	Data	FIR0 - FIR2	TC
$\overline{TCC}$	HIGH	Coefficient	FIR0 - FIR2	Unsigned
$\overline{TCC}$	LOW	Coefficient	FIR0 - FIR2	TC

Internal Data Representations

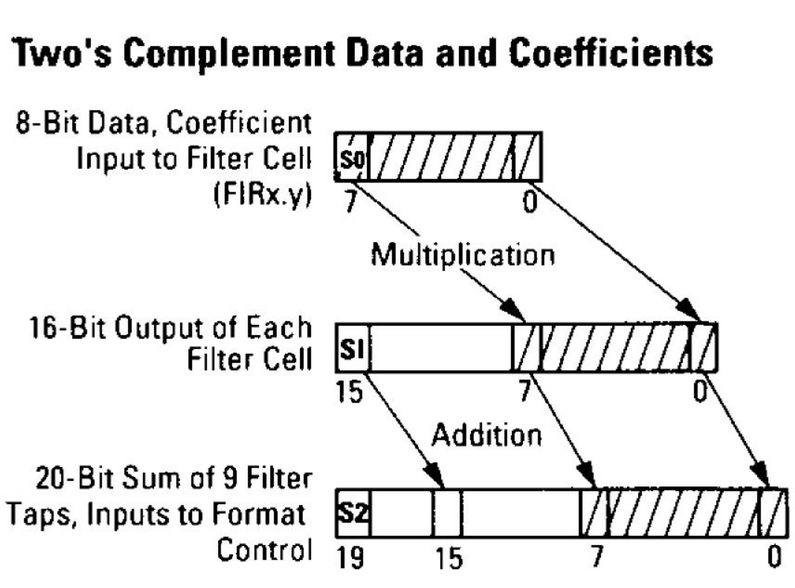
In this section, the size of the operands, filter cell outputs and filter output sums are illustrated in greater detail.

Unsigned Data and Coefficients



Traces the region of interest in the extreme case when the L64243 has only one filter cell with a non-zero coefficient. In this case, the non-zero coefficient has value 1.

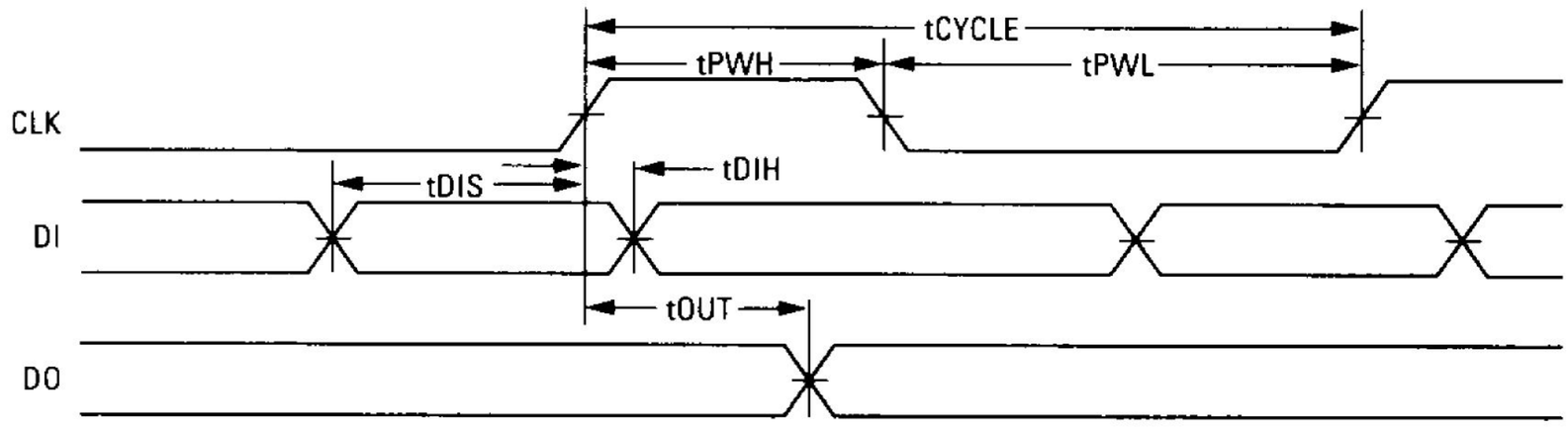
Two's Complement Data and Coefficients



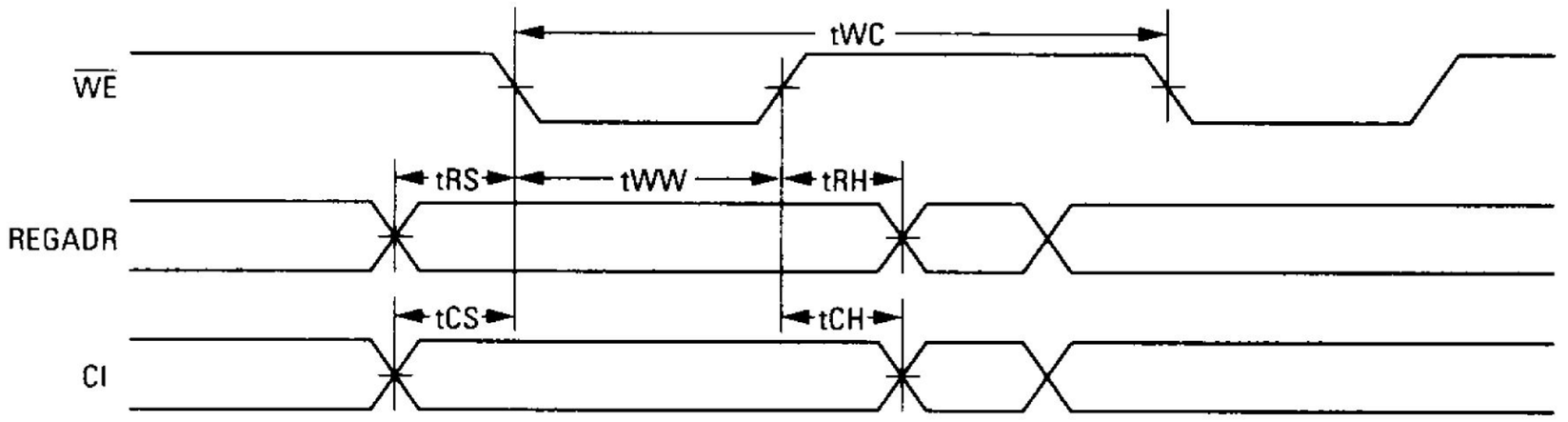
Same as previous diagram. In the case of only one non-zero coefficient, S2 = S1 = S0, sign extension is performed all the way to MSB at any stage.

AC Timing Waveforms

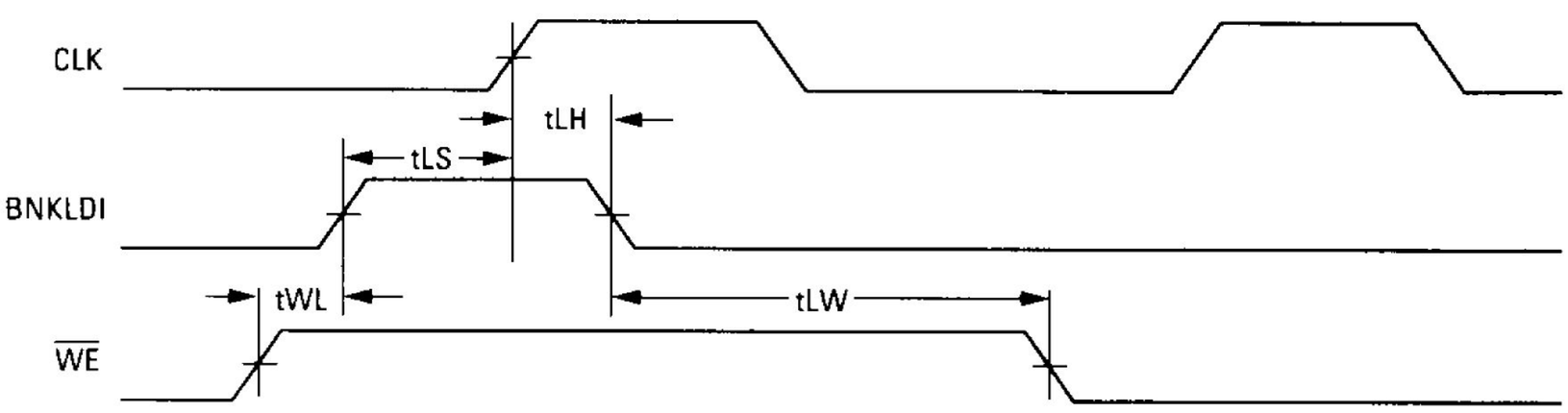
Normal Filter Operation



Loading Controls and Coefficients into Master Section (Methods I, II, III)

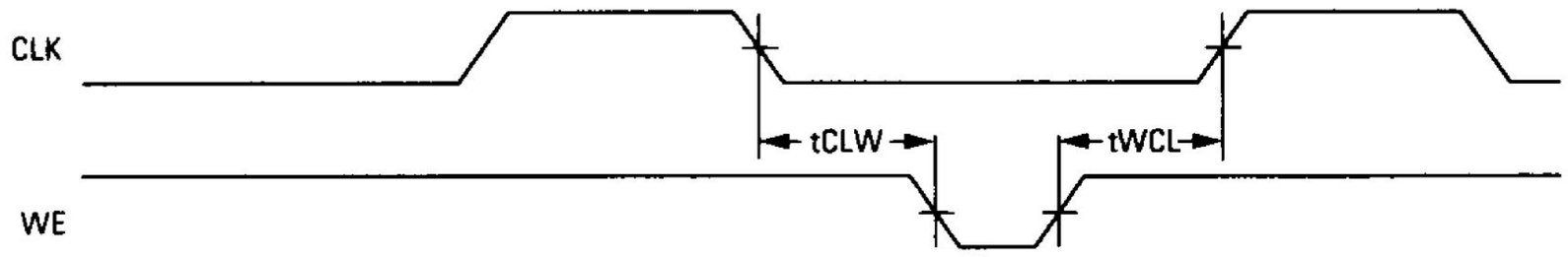


Bank Loading of Controls and Coefficients - Synchronous Transfer From Master to Slave Registers (Method I)

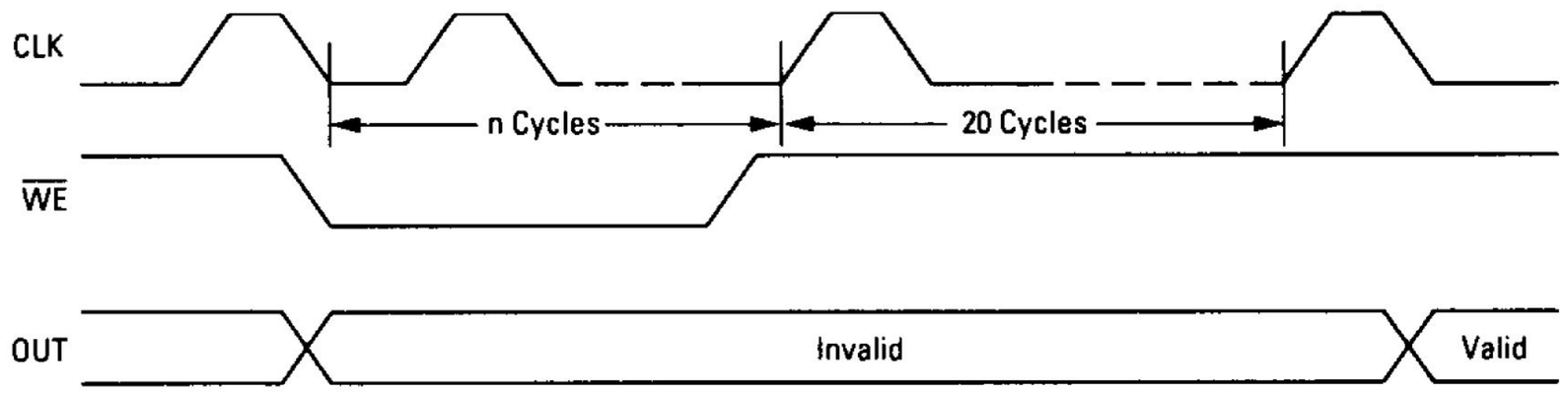


AC Timing Waveforms (Continued)

Synchronous Loading of Master Section and Synchronous Transfer to Slave Section with Bank Load HIGH (Method II)



Asynchronous Loading of Master Section and Asynchronous Transfer to Slave Section with Bank Load HIGH (Method III)



AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)
Military (TA = -55°C to 125°C, VDD = 4.5 V to 5.5 V)

Symbol	Parameter	L64243-40		L64243-30		L64243-20	
		Min	Max	Min	Max	Min	Max
tCYCLE	Minimum clock (CLK) cycle time	25		33		50	
tPWH	Minimum clock (CLK) pulse width HIGH	8		11		11	
tPWL	Minimum clock (CLK) pulse width LOW	8		11		11	
tDIS	Input data (DI) set-up time	7		10		10	
tDIH	Input data (DI) hold time	4		6		6	
tOUT	Output delay (DO) from CLK↑		20		27		27
tLS	BNKLDI set-up time with respect to CLK↑	7		10		10	
tLH	$\overline{\text{BNL}}$KDI hold time with respect to CLK↑	4		6		6	
tWL	$\overline{\text{WE}}$ set-up time with respect to BNKLDI↑	4		6		6	
tLW	WE hold time with respect to BNKLDI$\overline{\downarrow}$	15		20		20	
tRS	REGADR set-up time with respect to $\overline{\text{WE}}$↓	5		7		7	
tRH	REGADR hold time with respect to $\overline{\text{WE}}$↓	5		7		7	
tCS	CI set-up time with respect to $\overline{\text{WE}}$	8		11		11	
tCH	CI hold time with respect to WE	10		14		14	
tWW	Minimum $\overline{\text{WE}}$ pulse width LOW	8		11		11	
tWC	Minimum WE cycle time	25		33		33	
tCLW	CLK ↓ Before $\overline{\text{WE}}$↓	20		25		25	
tWCL	CLK ↑ After WE↓	20		25		25	

Note: All times are in ns.

Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to + 7	V
Input voltage	VIN	-0.3 to VDD + 0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to + 150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to + 6	V
Operating ambient temperature range			
Military	TA	-55 to +125	°C
Commercial	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges (1)

Symbol	Parameter	Condition			Min	Typ	Max	Units
VIL	LOW level input voltage						0.8	V
VIH	HIGH level input voltage Commercial temperature range Military temperature range				2.0 2.25			V V
IIN	Input current	VIN = VDD			-150		200	µA
VOH	HIGH level output voltage	IOH =	Comm -4 mA	Mil -3.2 mA	2.4	4.5		V
VOL	LOW level output voltage	IOL =	Comm 4 mA	Mil 3.2 mA		0.2	0.4	V
IOS	Output short circuit current(2)	VDD = Max, VO = VDD			15		130	mA
		VDD = Max, VO = 0V			-5		-100	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS					10	mA
IDD	Operating supply current(3)	tCYCLE = 25 ns				200		mA
CIN	Input capacitance	Any input				5		pF
COUT	Output capacitance	Any output				10		pF

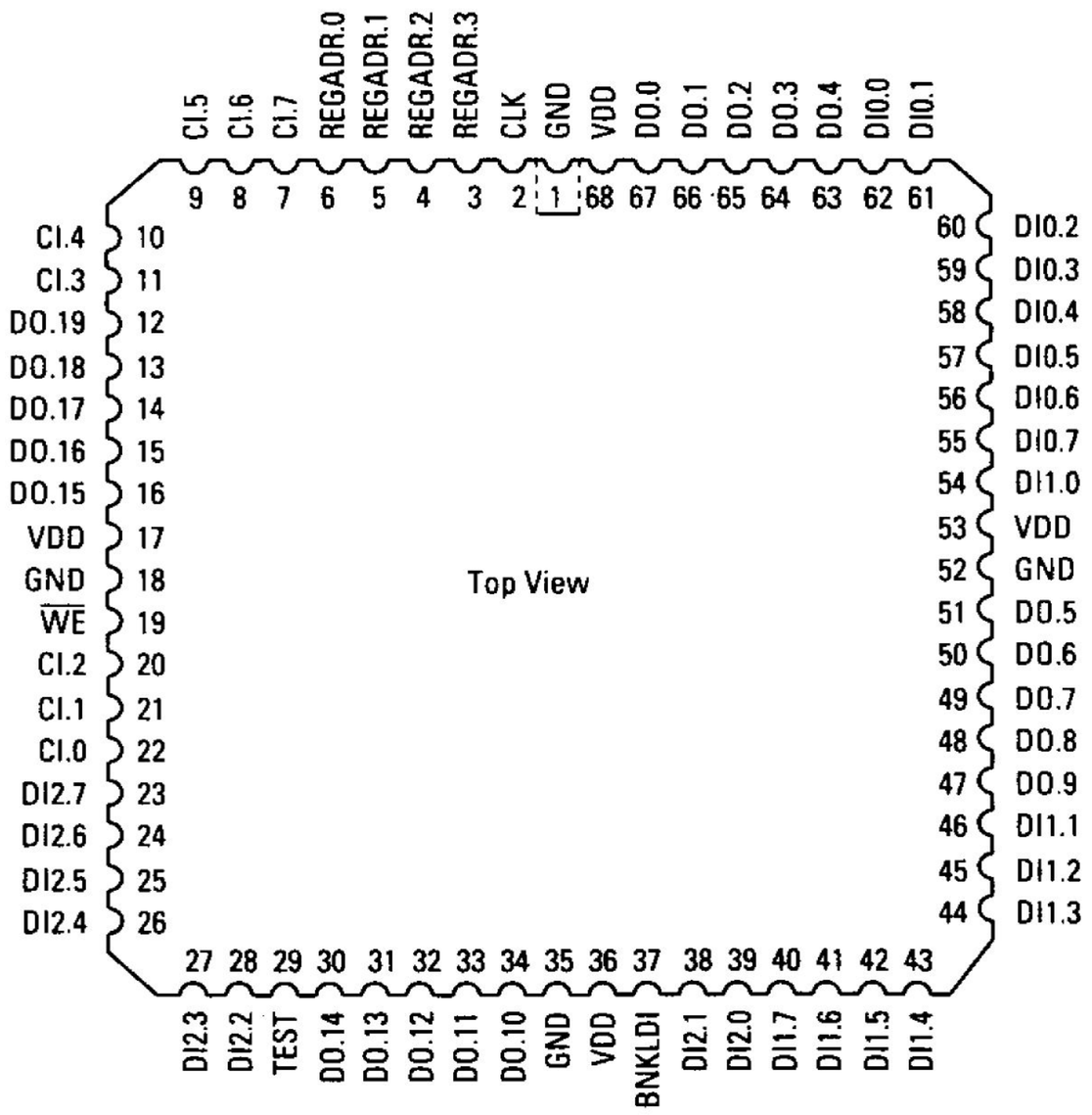
Notes:
1. Military temperature range is -55°C to +125°C, ±10% power supply; commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.
3. For 40 MHz device.

Pinout Diagram

68-Pin Ceramic Pin Grid Array (CPGA)

	1	2	3	4	5	6	7	8	9	10	11
A		CI.5	CI.6	REG-ADR.0	REG-ADR.2	CLK	VDD	DO.1	DO.3	DI0.0	
B	CI.3	CI.4	CI.7	REG-ADR.1	REG-ADR.3	GND	DO.0	DO.2	DO.4	DI0.1	DI0.2
C	DO.18	DO.19	X	← Extra Pin						DI0.4	DI0.3
D	DO.16	DO.17								DI0.6	DI0.5
E	VDD	DO.15								DI1.0	DI0.7
F	$\overline{WE}$	GND				Top View				GND	VDD
G	CI.1	CI.2								DO.6	DO.5
H	DI2.7	CI.0								DO.8	DO.7
J	DI2.5	DI2.6								DI1.1	DO.9
K	DI2.4	DI2.3	TEST	DO.13	DO.11	GND	BNKLDI	DI2.0	DI1.6	DI1.3	DI1.2
L		DI2.2	DO.14	DO.12	DO.10	VDD	DI2.1	DI1.7	DI1.5	DI1.4	

68-Pin Plastic Leaded Chip Carrier (PLCC)



LSI LOGIC

L64243
3 x 3 Multi-Bit Filter
(MFIR3)

Packaging

68-Pin Ceramic Pin Grid Array: See FB Package in Package Selector Guide
68-Pin Plastic Leaded Chip Carrier: See MC Package in Package Selector Guide

Ordering Information

L64243 G M -XX

- **-XX** — Speed in MHz
- **M** — Temperature Range/Flow Option
  - C = Commercial (0°C to 70°C)
  - M = Military (-55°C to + 125°C), Processed to MIL-STD-883C Level B
- **G** — Package Code
  - G = 68-Pin Ceramic Pin Grid Array
  - J = 68-Pin Plastic Leaded Chip Carrier
- **L64243** — Device Type
  - Multi-Bit Filter