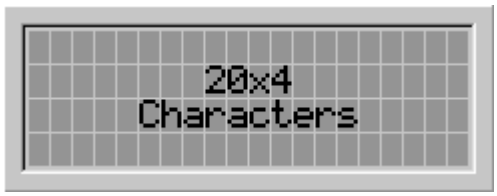
HD44780-Based LCD Modules

Hitachi LM018L

40 character x 2 lines • Built-in LSI HD44780 controller
+5volt single power supply • Display Colour: Grey
LM018L: Introduction • Interfacing • Display Pattern and Character Set
HD44780: Operation • Instruction Set • Initialisation

I have now obtained a number of



Three-Five Systems TLCM2040

pretty much the same specs as above

Introduction to the LM018L

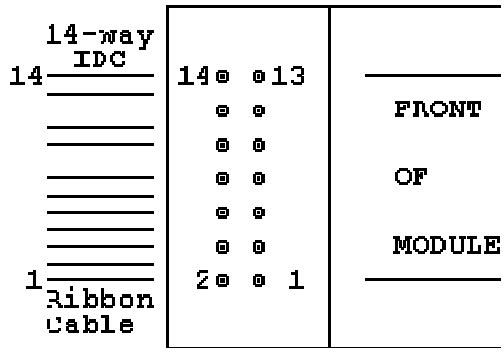
The Hitachi LM018L is a 40 character x 2 line reflective type Liquid Crystal character display module. It includes a built-in LSI controller HD44780 which provides a range of features, including

- 192 5x7-dot characters plus 8 user-defined characters.
- Instruction functions
  - Display Clear
  - Cursor Home
  - Display On/Off
  - Cursor On/Off
  - Character Display Blink
  - Cursor Shift
  - Display Shift

The module can be directly interfaced to a 4-bit or 8-bit MPU.

Interfacing to the LM018L

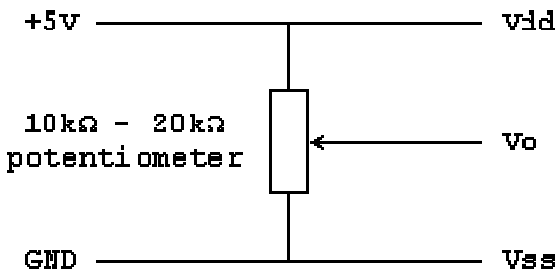
Pinout Diagram



Internal pin connections

Pin	Symbol	Level	Function
1	Vss	-	0v *** Reversing Vss and Vdd ***
2	Vdd	-	+5v *** will DESTROY the unit ***
3	Vo	-	*
4	RS	H/L	H: Data Input L: Instruction code input
5	R/W	H/L	H: Data Read (LCD module -> MPU) L: Data Write (LCD module <- MPU)
6	E	H,H->L	Enable Signal
7	DB0	H/L	D
8	DB1	H/L	A
9	DB2	H/L	T
10	DB3	H/L	A
11	DB4	H/L	
12	DB5	H/L	B
13	DB6	H/L	U
14	DB7	H/L	S

* Vo is between GND and 5V. The potentiometer is the contrast adjustment (or just tie Vo to GND).



Notes:
With the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8-bit MPUs.

- When the interface is 4 bits wide, data is transferred via DB4-DB7 only. DB0-DB3 are not used. Data transfer between the HD44780 and the MPU is complete when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB4-DB7 when interface is 8-

bits wide) is transferred first and then the lower order 4 bits (contents of DB0-DB3 when the interface is 8-bits wide).

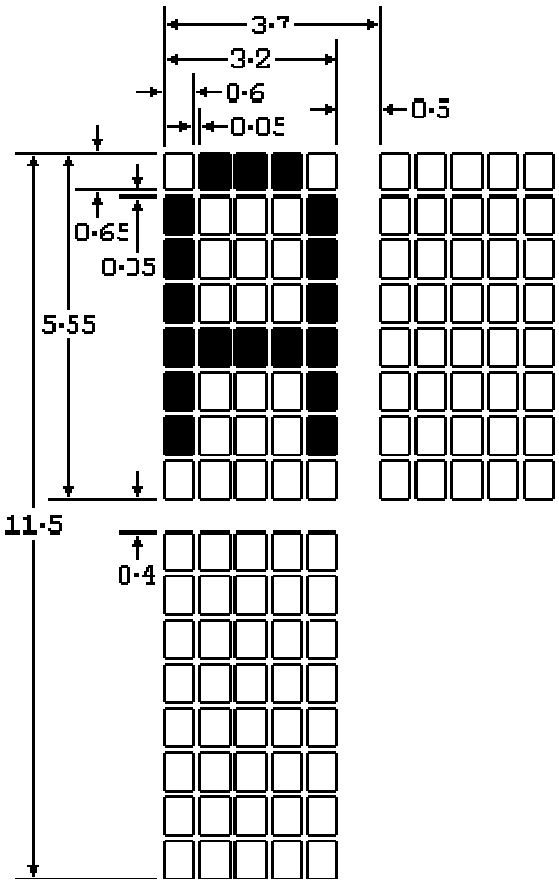
- When the interface is 8-bits wide, data is transferred using DB0-DB7.

```
Absolute Maximum Ratings
Power supply for logic (Vdd - Vss)  . . . . 0v min, 6.5v max
Power supply for LCD drive (Vdd - Vo) . . . 0v min, 6.5v max

Electrical Characteristics
 Input "high" voltage . . . . . 2.2v min
 Input  "low" voltage . . . . . 0.6v max
Output "high" voltage . . . . . 2.4v min
Output  "low" voltage . . . . . 0.4v max
Power supply current  . . . . . 2.0mA typ, 3.0mA max
```

LM018L Display Pattern and Character Set

Display Pattern (Unit: mm)



5x7 dot Character Set

Notes:
The first (blank) column corresponds to the Character Generator RAM. With a 5x7 dot display, this can hold 8 user-defined characters (numbered 0 - 7). The next 8 (numbered 8 - 15) simply *wrap round* onto the first 8.

Here's an example of using the 8 user-defined characters to create double-height digit characters, (now includes a demo program).

Characters numbered 16 - 31 and 128 - 159 are not available.

Operation of the HD44780

Registers
The HD44780 has two 8 bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from the DD RAM or the CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM by internal operation. The DR is also used for data storage when reading from the DD RAM or the CG RAM. When address information is written into the IR, data is read into the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

Register selection

RS	R/W	Enable	Operation
0	0	H,H->L	IR write as internal operation (Display clear, etc.)
0	1	H	Read busy flag (DB7) and address counter (DB0-DB6)
1	0	H,H->L	DR write as internal operation (DR to DD RAM or CG RAM)
1	1	H	DR read as internal operation (DD RAM or CG RAM to DR)

Busy Flag
When the busy flag is "1", the HD44780 is in the internal operation mode, and the next instruction will not be accepted. As the Register selection table above shows, the busy flag is output to DB7 when RS = 0 and R/W = 1. The next instruction must be written after ensuring that the busy flag is "0".
Address counter (AC)
The address counter (AC) assigns addresses to DD and CG RAMs. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.
After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented or decremented by 1. AC contents are output as DB0-DB6 when RS = 0 and R/W = 1, as shown in the Register selection table above.
Display Data RAM (DD RAM)
The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 x 8 bits, or 80 characters. On displays with fewer than 80 characters, any DD RAM that is not used for display can be used as a general data RAM. The relationship between DD RAM addresses and positions on the liquid crystal display are shown below. The DD RAM address is set in the Address Counter (AC) and is expressed in hexadecimal.

DD RAM addresses for a 40 character x 2 line display

	1	2		39	40	← display position
1st line	00	01	- - - - - - - - - -	26	27	← DD RAM address (Hex)
2nd line	40	41	- - - - - - - - - -	66	67	← DD RAM address (Hex)

With the 40 character x 2 line display provided by the LM018L, when a display shift is performed the display will "wrap round". A Left shift will cause the character previously at display position 1 to "drop off" the left end and reappear at display position 40. A Right shift will cause the character previously at display position 40 to "drop off" the right end and reappear at display position 1.
Character Generator ROM (CG ROM)
The Character Generator ROM generates 5 x 7 dot or 5 x 10 dot character patterns from 8-bit character codes. It contains 192 5 x 7 dot character patterns and 192 5 x 10 dot character patterns.
Character Generator RAM (CG RAM)
The Character Generator RAM is RAM with which the user can redefine character patterns in software. With 5 x 7 dots, 8 user-defined character patterns can be stored and with 5 x 10 dots, 4 user-defined character patterns can be stored.

HD44780 Instruction Set

Instruction	Code									
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Clear Display	0	0	0	0	0	0	0	0	0	1
Return Home	0	0	0	0	0	0	0	0	1	*
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S
Display ON/OFF	0	0	0	0	0	0	1	D	C	B
Cursor and Display Shift	0	0	0	0	0	1	S/C	R/L	*	*
Function Set	0	0	0	0	1	DL	N	F	*	*
Set CG RAM address	0	0	0	1	A	A	A	A	A	A
Set DD RAM address	0	0	1	A	A	A	A	A	A	A
Read busy flag and address	0	1	BF	A	A	A	A	A	A	A
Write data to CG or DD RAM	1	0	D	D	D	D	D	D	D	D
Read data from CG or DD RAM	1	1	D	D	D	D	D	D	D	D

Notes
* means 0 or 1 have no effect

Where execution times are given as A / B

A applies for 1/8 duty or 1/11 duty (1 display line)
B applies for 1/16 duty (2 display lines)

Initialisation of the HD44780

Initialising by internal reset circuit

The HD44780 automatically initialises (resets) when power is turned on using the internal reset circuit. The following instructions are executed in initialisation. The busy flag (BF) is kept in busy state until initialisation ends. The busy state (BF=1) is 10ms after Vcc rises to 4.5volts.

```
1. Display clear

2. Function set ..... DL = 1: 8 bit interface
                      N = 0: 1 line display
                      F = 0: 5 x 7 dot character font

3. Display ON/OFF ...  D = 0: Display OFF
                       C = 0: Cursor OFF
                       B = 0: Blink OFF

4. Entry mode set .. I/D = 1: +1 (increment)
                       S = 0: No shift

5. Write DD RAM
   When the rise time of power supply (0.2 -> 4.5) is out
   of the range 0.1ms - 10ms, or when the low level width
   of power OFF (less than 0.2) is less than 1ms, the
   internal reset circuit will not operate normally.
   In this case, initialisation will not be performed
   normally. Initialise by instruction, as detailed below.
```

If the power supply conditions for correctly operating the internal reset circuit are not met, initialisation by instruction is required.

Initialising by instruction

When interface is 8-bits wide

```
               [Power ON]

       [  Wait more than 15ms  ]
       [after Vdd rises to 4.5v]

RS  R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0  Can't check BF before this instruction
 0   0   0   0   1   1   *   *   *   *   Function set (8-bit interface)

        [Wait more than 4.1ms]

RS  R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0  Can't check BF before this instruction
 0   0   0   0   1   1   *   *   *   *   Function set (8-bit interface)

        [Wait more than 100us]

RS  R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0  Can't check BF before this instruction
 0   0   0   0   1   1   *   *   *   *   Function set (8-bit interface)

                                         BF can be checked after the following
                                         instructions. When BF is not checked,
                                         the waiting time between instructions
                                         is longer than the execution time.
                                         (See Instruction set)

RS  R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
 0   0   0   0   1   1   N   F   *   *   Function set  [8-bit Interface      ]
```

```
                                                          [Specify display lines]
RS  R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0                   [and character font   ]
 0   0   0   0   0   0   1   0   0   0   Display OFF       These cannot be
                                                           changed afterwards
RS  R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
 0   0   0   0   0   0   0   0   0   1   Display ON

RS  R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
 0   0   0   0   0   0   0   1  I/D  S   entry mode set

        [end of initialisation]
```

When interface is 4-bits wide

```
        [Power ON]

[  Wait more than 15ms  ]
[after Vdd rises to 4.5v]

RS  R/W DB7 DB6 DB5 DB4  Can't check BF before this instruction
 0   0   0   0   1   1   Function set (8-bit interface)

    [Wait more than]
    [     4.1ms    ]

RS  R/W DB7 DB6 DB5 DB4  Can't check BF before this instruction
 0   0   0   0   1   1   Function set (8-bit interface)

    [Wait more than]
    [     100us    ]

RS  R/W DB7 DB6 DB5 DB4  Can't check BF before this instruction
 0   0   0   0   1   1   Function set (8-bit interface)

                         BF can be checked after the following
                         instructions. When BF is not checked,
                         the waiting time between instructions
                         is longer than the execution time.
                         (See Instruction set)

RS  R/W DB7 DB6 DB5 DB4
 0   0   0   0   1   0   Function set (to 4-bit interface)

RS  R/W DB7 DB6 DB5 DB4
 0   0   0   0   1   0
 0   0   N   F   *   *   Function set  [4-bit Interface      ]
                                       [Specify display lines]
RS  R/W DB7 DB6 DB5 DB4                [and character font   ]
 0   0   0   0   0   0                  These cannot be
 0   0   1   0   0   0   Display OFF    changed afterwards

RS  R/W DB7 DB6 DB5 DB4
 0   0   0   0   0   0
 0   0   0   0   0   1   Display ON

RS  R/W DB7 DB6 DB5 DB4
 0   0   0   0   0   0
 0   0   0   1  I/D  S   entry mode set

[end of initialisation]
```

Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clears all display and returns the cursor to the home position (Address 0).

Details
Writes space code "20" (Hexadecimal) (character pattern for character code "20" must be blank pattern) into all DD RAM addresses. Sets DD RAM address to 0 in the address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the display (the first line if 2 lines are displayed). Set I/D = 1 (Increment Mode) of Entry mode. S of Entry Mode doesn't change.

Execution Time = 82µs-1.64ms / 120µs-4.9ms

Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	*

Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.

Details
Sets the DD RAM address to 0 in the address counter. Returns the display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

Execution Time = 40µs-1.6ms / 120µs-4.8ms

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data read and write.

Details
I/D: Increments (I/D = 1) or Decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing to and reading from the CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and the display moves.

Execution Time = 40µs / 120µs

Display ON/OFF

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Sets ON/OFF display, cursor and cursor position character (underscore) blink

Details
D: The display is ON when D = 1 and OFF when D = 0.
When off due to D = 0, display data remains in the DD RAM. It can be displayed immediately by setting D = 1.

C: The cursor displays when C = 1 and does not display when C = 0.
Even if the cursor disappears, the function of I/D, etc. does not change during display data write.
The cursor is displayed using 5 dots in the 8th line when the 5 x 7 dot character font is selected and 5 dots in the 11th line when the 5 x 10 dot character font is selected.

B: The character indicated by the cursor blinks when B = 1.
The blink is displayed by switching between all blank dots and display characters at 409.6 ms interval.

Execution Time = 40µs / 120µs

Cursor and Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	*	*

Moves the cursor and shifts the display without changing DD RAM contents

Details
Shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line position.

S/C	R/L	
0	0	Shifts the cursor position to the left (Address Counter is decremented by 1)
0	1	Shifts the cursor position to the right (Address Counter is incremented by 1)
1	0	Shifts the entire display to the left The cursor follows the display shift
1	1	Shifts the entire display to the right The cursor follows the display shift

Execution Time = 40µs / 120µs

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	*	*

Sets interface data length (DL), number of display lines (N) and character font (F)

Details
DL: Sets interface data length

Data is sent or received in 8 bit lengths (DB7-DB0) when DL = 1

Data is sent or received in 4 bit lengths (DB7-DB4) when DL = 0

When the 4 bit length is selected, data must be sent or received twice.

N: Sets number of display lines

F: Sets character font

Note
Perform the function at the start of the program before executing any instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

N	F	display lines	Character Font	Duty Factor	Remarks
0	0	1	5x 7 dots	1/8	-
0	1	1	5x10 dots	1/11	-
1	*	2	5x 7 dots	1/16	Cannot display 2 lines with 5x10 dot character font

Execution Time = 40µs / 120µs

Set CG RAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	A	A	A	A	A	A

Sets the CG RAM address. CG RAM data is sent after this setting

Details
Sets the CG RAM address into the address counter in binary AAAAAA. Data is then written to or read from the MPU for the CG RAM.

Execution Time = 40µs / 120µs

Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	A	A	A	A	A	A	A

Sets the DD RAM address. DD RAM data is sent after this setting

Details
Sets the DD RAM address into the address counter in binary AAAAAAA. Data is then written to or read from the MPU for the DD RAM.

However

when N = 0 (1 line display)

AAAAAAA is "00" - "4F" (Hex)

when N = 1 (2 line display)

AAAAAAA is "00" - "27" (Hex) for the first line and
AAAAAAA is "40" - "67" (Hex) for the second line.

Execution Time = 40µs / 120µs

Read busy flag and address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	A	A	A	A	A	A	A

Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents

Details
Reads the busy flag (BF) that indicates the system is now internally executing a previously received instruction. BF = 1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to "0". Check the BF status before the next wire operation.

At the same time, the value of the address counter expressed in AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses. Its current use is determined by the previous instruction.

Execution Time = 1µs

Write data to CG or DD RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D	D	D	D	D	D	D	D

Writes data into DD RAM or CG RAM

Details
Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM. Whether the CG or DD RAM is to be written is determined by the previous specification of CG RAM or DD RAM address setting. After the write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

Execution Time = 40µs / 120µs

Read data from CG or DD RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D	D	D	D	D	D	D	D

Reads data from DD RAM or CG RAM.

Details
Reads binary DDDDDDDD from the CG or DD RAM. The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. When serially executing the "read" instruction, the next address data is normally read from the second read. The "address set" instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift instruction operation is the same as that of the DD RAM's address set instruction.

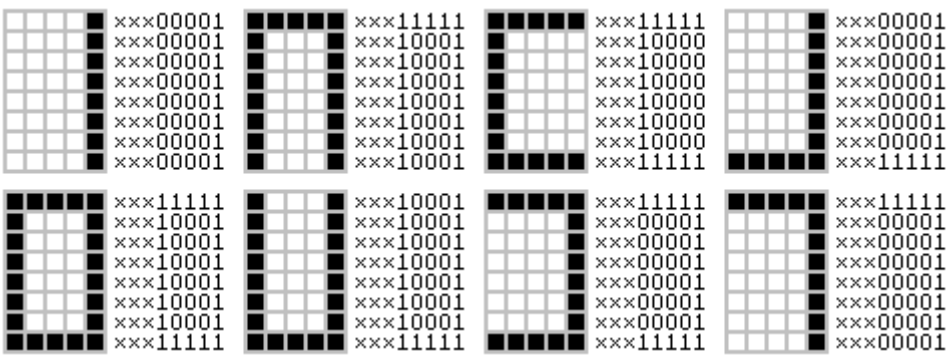
After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

Note:
The address counter (AC) is automatically incremented or decremented by 1 after "write" instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot them be read out even if "read" instructions are executed. The conditions for correct data read out are: execute either the address set instruction or cursor shift instruction (only with DD RAM), just before reading out execute the "read" instruction from the second time the "read" instruction is serial.

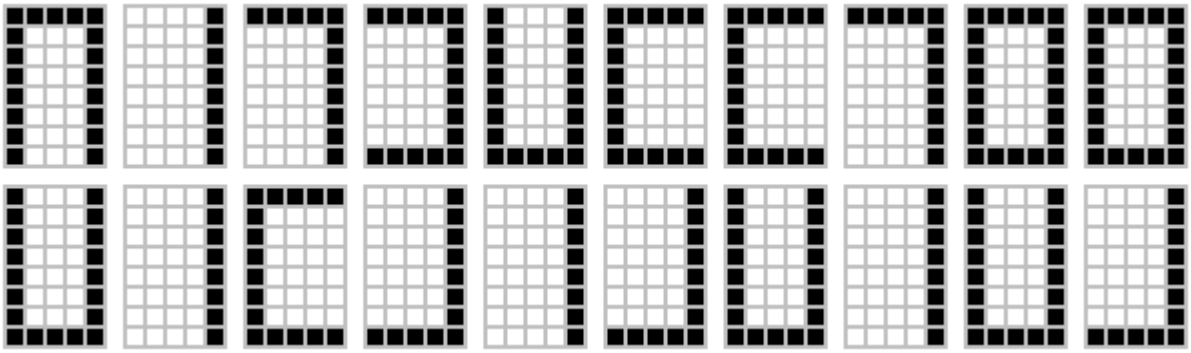
Execution Time = 40µs / 120µs

Double-Height Digit Characters

with these 8 patterns programmed into the Character Generator RAM -



it is possible to display double-height versions of the characters 0 to 9 -



(haven't you got any *imagination*?)

This works nicely in the Radio-controlled Digital Clock project
Here's an example program to illustrate the technique