SSD1303

Advance Information

132 x 64 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

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FIGURES

TABLES

1 GENERAL INFORMATION

The SSD1303 is a single-chip CMOS OLED/PLED driver with a controller for an organic or polymer light emitting diode dot-matrix graphic display system. It consists of 132 segments, 64 commons which support a maximum display resolution of 132x64. There are 4-color selections, supporting monochrome or area color OLED/PLED. This IC is designed for a Common Cathode type OLED panel.

The SSD1303 has contrast control, display RAM and an oscillator, reducing both the number of external components as well as power consumption. It is suitable for many compact, portable applications, including mobile phone sub-displays, calculators and MP3 players.

2 FEATURES

Supports maximum 132 x 64 dot matrix panel
Area color support with 4 Color Selection and 64 steps per color
Logic voltage supply: V_{DD} = 2.4V - 3.5V
High voltage supply: V_{CC} = 7.0V - 16.0V
Maximum segment output current: 320uA
Maximum common sink current: 45mA
Embedded with 132 x 64 bit SRAM display buffer
256-step Contrast Control on monochrome passive OLED panel
On-Chip Oscillator
Programmable Frame Frequency and Multiplexing Ratio
Pin selectable MCU interfaces:

- Serial Peripheral Interface
- 8-bit 6800-series Parallel Interface
- 8-bit 8080-series Parallel Interface
- I^2C Interface

Row Re-mapping and Column Re-mapping
Vertical Scrolling
Automatic horizontal scrolling function
Low power consumption
Wide range of operating temperatures: -40 to 90 °C

3 ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1303Z	132	64	Gold Bump Die	Page 7, 56	Die size: 9.22mm x 1.55mm Pad pitch: COM 51.8um SEG 52.2um
SSD1303T3R1	96	64	TAB	Page 44	• 35mm film • 4 sprocket hole • Folding TAB • 80 / 68 / SPI / I^2C interface • Output lead pitch 0.12974mm
SSD1303T6R1	132	64	TAB	Page 48	• 35mm film • 4 sprocket hole • Folding TAB • 80 / 68 / SPI / I^2C interface • Output lead pitch 0.11976
SSD1303T10R1	132	64	TAB	Page 52	• 48mm film • 5 sprocket hole • Folding TAB • 80 / 68 / SPI / I^2C interface • Output lead pitch 0.139825mm

4 BLOCK DIAGRAM

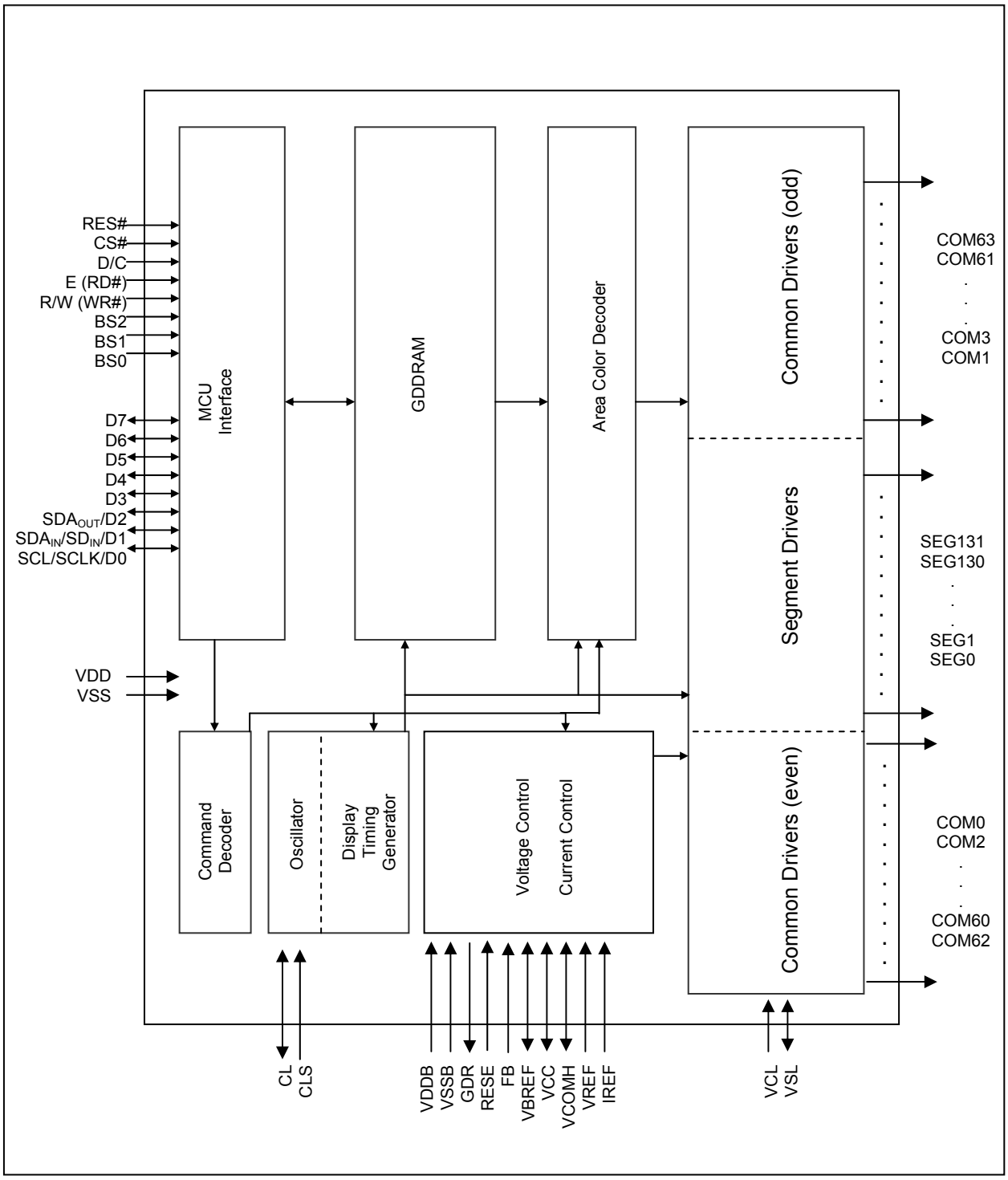
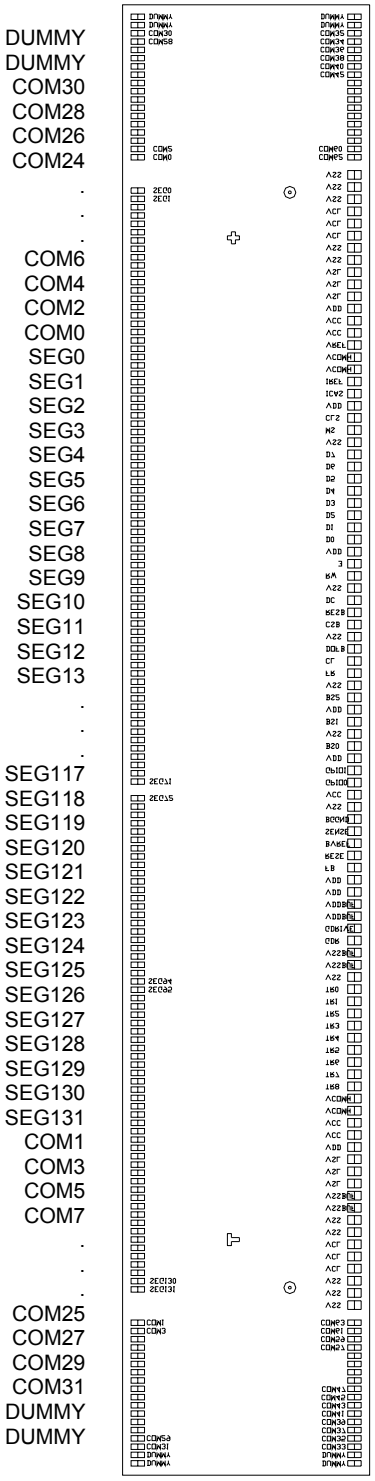


Figure 1 - Block Diagram

5 DIE PAD FLOOR PLAN

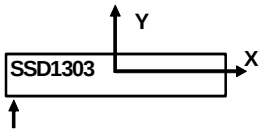
Figure 2 - SSD1303Z Pin Assignment



DUMMY
DUMMY
COM30
COM28
COM26
COM24
.
.
.
COM6
COM4
COM2
COM0
SEG0
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG7
SEG8
SEG9
SEG10
SEG11
SEG12
SEG13
.
.
.
SEG117
SEG118
SEG119
SEG120
SEG121
SEG122
SEG123
SEG124
SEG125
SEG126
SEG127
SEG128
SEG129
SEG130
SEG131
COM1
COM3
COM5
COM7
.
.
.
COM25
COM27
COM29
COM31
DUMMY
DUMMY

DUMMY (x2)
COM32
COM34
.
.
COM60
COM62
VSS (x3)
VCL (x3)
VSS (x2)
VSL (x3)
VDD
VCC (x2)
VREF
VCOMH (x2)
IREF
ICAS
VDD
CLS
M/S
VSS
D7
D6
D5
D4
D3
D2
D1
D0
VDD
E/RD
R/W
VSS
D/C
RES#
CS#
VSS
DOF#
CL
M
VSS
BS2
VDD
BS1
VSS
BS0
VDD
GPIO1
GPIO0
VCC
VSS
BGGND
SENSE
VBREF
RESE
FB
VDD (x2)
VDDB (x2)
GDR (x2)
VSSB (x2)
VSS
TR0
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
VCOMH (x2)
VCC (x2)
VDD
VSL (x3)
VSSB (x2)
VSS (x2)
VCL (x3)
VSS (x3)
COM63
COM61
.
.
COM35
COM33
DUMMY (x2)

PAD 1



Pad 1,2,3,? >130
Gold Bumps face up

Die size	9.22mm x 1.55mm
Die height	457 +/- 25um

Bump height	Nominal 18um
Bump size	
Pad 1-18, 113-298	34um x 84um
Pad 19-112	54um x 84um

Alignment mark		
T shape	(-3132.9, 79.5)	75um x 75um
+ shape	(3148.9, 79.5)	75um x 75um
Circle	(3433.9, -274.6)	R37.5um, inner 18um
Circle	(-3433.9, -274.6)	R37.5um, inner 18um

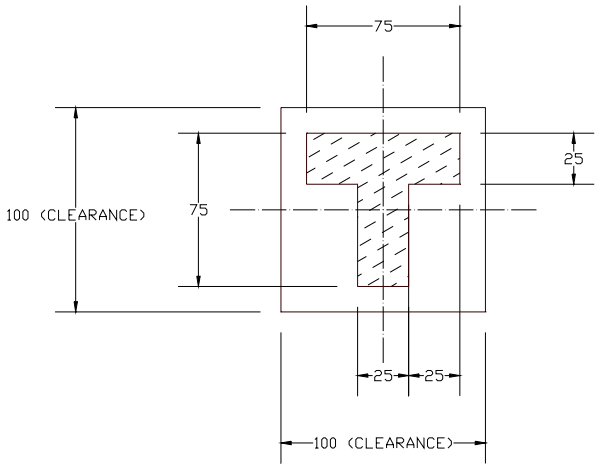
Table 2 - SSD1303Z Die Pad Coordinates

Pad no.	Pad Name	X-pos	Y-pos
1	NC	-4535.4	-679.6
2	NC	-4483.2	-679.6
3	COM33	-4431.0	-679.6
4	COM35	-4379.2	-679.6
5	COM37	-4327.4	-679.6
6	COM39	-4275.6	-679.6
7	COM41	-4223.8	-679.6
8	COM43	-4172.0	-679.6
9	COM45	-4120.2	-679.6
10	COM47	-4068.4	-679.6
11	COM49	-4016.6	-679.6
12	COM51	-3964.8	-679.6
13	COM53	-3913.0	-679.6
14	COM55	-3861.2	-679.6
15	COM57	-3809.4	-679.6
16	COM59	-3757.6	-679.6
17	COM61	-3705.8	-679.6
18	COM63	-3654.0	-679.6
19	VSS	-3543.3	-679.6
20	VSS	-3467.1	-679.6
21	VSS	-3390.9	-679.6
22	VCL	-3314.7	-679.6
23	VCL	-3238.5	-679.6
24	VCL	-3162.3	-679.6
25	VSS	-3086.1	-679.6
26	VSS	-3009.9	-679.6
27	VSSB	-2933.7	-679.6
28	VSSB	-2857.5	-679.6
29	VSL	-2781.3	-679.6
30	VSL	-2705.1	-679.6
31	VSL	-2628.9	-679.6
32	VDD	-2552.7	-679.6
33	VCC	-2476.5	-679.6
34	VCC	-2400.3	-679.6
35	VCOMH	-2324.1	-679.6
36	VCOMH	-2247.9	-679.6
37	TR8	-2171.7	-679.6
38	TR7	-2095.5	-679.6
39	TR6	-2019.3	-679.6
40	TR5	-1943.1	-679.6
41	TR4	-1866.9	-679.6
42	TR3	-1790.7	-679.6
43	TR2	-1714.5	-679.6
44	TR1	-1638.3	-679.6
45	TR0	-1562.1	-679.6
46	VSS	-1485.9	-679.6
47	VSSB	-1409.7	-679.6
48	VSSB	-1333.5	-679.6
49	GDR	-1257.3	-679.6
50	GDR	-1181.1	-679.6
51	VDDB	-1104.9	-679.6
52	VDDB	-1028.7	-679.6
53	VDD	-952.5	-679.6
54	VDD	-876.3	-679.6
55	FB	-800.1	-679.6
56	RESE	-723.9	-679.6
57	VBREF	-647.7	-679.6
58	SENSE	-571.5	-679.6
59	BGGND	-495.3	-679.6
60	VSS	-419.1	-679.6
61	VCC	-342.9	-679.6
62	GPIO0	-267.2	-679.6
63	GPIO1	-190.5	-679.6
64	VDD	-114.3	-679.6
65	BS0	-38.1	-679.6
66	VSS	38.1	-679.6
67	BS1	114.3	-679.6
68	VDD	190.5	-679.6
69	BS2	266.7	-679.6
70	VSS	342.9	-679.6
71	M	419.1	-679.6
72	CL	495.3	-679.6
73	DOF#	571.5	-679.6
74	VSS	647.7	-679.6
75	CS#	723.9	-679.6
76	RES#	800.1	-679.6
77	D/C	876.3	-679.6
78	VSS	952.5	-679.6
79	R/W	1028.7	-679.6
80	E/RD	1104.9	-679.6
81	VDD	1181.1	-679.6
82	D0	1257.3	-679.6
83	D1	1333.5	-679.6
84	D2	1409.7	-679.6
85	D3	1485.9	-679.6
86	D4	1562.1	-679.6
87	D5	1638.3	-679.6
88	D6	1714.5	-679.6
89	D7	1790.7	-679.6
90	VSS	1866.9	-679.6
91	M/S	1943.1	-679.6
92	CLS	2019.3	-679.6
93	VDD	2095.5	-679.6
94	ICAS	2171.7	-679.6
95	IREF	2247.9	-679.6
96	VCOMH	2324.1	-679.6
97	VCOMH	2400.3	-679.6
98	VREF	2476.5	-679.6
99	VCC	2552.7	-679.6
100	VCC	2628.9	-679.6
101	VDD	2705.1	-679.6
102	VSL	2781.3	-679.6
103	VSL	2857.5	-679.6
104	VSL	2933.7	-679.6
105	VSS	3009.9	-679.6
106	VSS	3086.1	-679.6
107	VCL	3162.3	-679.6
108	VCL	3238.5	-679.6
109	VCL	3314.7	-679.6
110	VSS	3390.9	-679.6
111	VSS	3467.1	-679.6
112	VSS	3543.3	-679.6
113	COM62	3654.0	-679.6
114	COM60	3705.8	-679.6
115	COM58	3757.6	-679.6
116	COM56	3809.4	-679.6
117	COM54	3861.2	-679.6
118	COM52	3913.0	-679.6
119	COM50	3964.8	-679.6
120	COM48	4016.6	-679.6
121	COM46	4068.4	-679.6
122	COM44	4120.2	-679.6
123	COM42	4172.0	-679.6
124	COM40	4223.8	-679.6
125	COM38	4275.6	-679.6
126	COM36	4327.4	-679.6
127	COM34	4379.2	-679.6
128	COM32	4431.0	-679.6
129	NC	4483.2	-679.6
130	NC	4535.4	-679.6
131	NC	4535.4	679.6
132	NC	4483.2	679.6
133	COM30	4431.0	679.6
134	COM28	4379.2	679.6
135	COM26	4327.4	679.6
136	COM24	4275.6	679.6
137	COM22	4223.8	679.6
138	COM20	4172.0	679.6
139	COM18	4120.2	679.6
140	COM16	4068.4	679.6
141	COM14	4016.6	679.6
142	COM12	3964.8	679.6
143	COM10	3913.0	679.6
144	COM8	3861.2	679.6
145	COM6	3809.4	679.6
146	COM4	3757.6	679.6
147	COM2	3705.8	679.6
148	COM0	3654.0	679.6
149	SEG0	3445.2	679.6
150	SEG1	3393.0	679.6
151	SEG2	3340.8	679.6
152	SEG3	3288.6	679.6
153	SEG4	3236.4	679.6
154	SEG5	3184.2	679.6
155	SEG6	3132.0	679.6
156	SEG7	3079.8	679.6
157	SEG8	3027.6	679.6
158	SEG9	2975.4	679.6
159	SEG10	2923.2	679.6
160	SEG11	2871.0	679.6
161	SEG12	2818.8	679.6
162	SEG13	2766.6	679.6
163	SEG14	2714.4	679.6
164	SEG15	2662.2	679.6
165	SEG16	2610.0	679.6
166	SEG17	2557.8	679.6
167	SEG18	2505.6	679.6
168	SEG19	2453.4	679.6
169	SEG20	2401.2	679.6
170	SEG21	2349.0	679.6
171	SEG22	2296.8	679.6
172	SEG23	2244.6	679.6
173	SEG24	2192.4	679.6
174	SEG25	2140.2	679.6
175	SEG26	2088.0	679.6
176	SEG27	2035.8	679.6
177	SEG28	1983.6	679.6
178	SEG29	1931.4	679.6
179	SEG30	1879.2	679.6
180	SEG31	1827.0	679.6

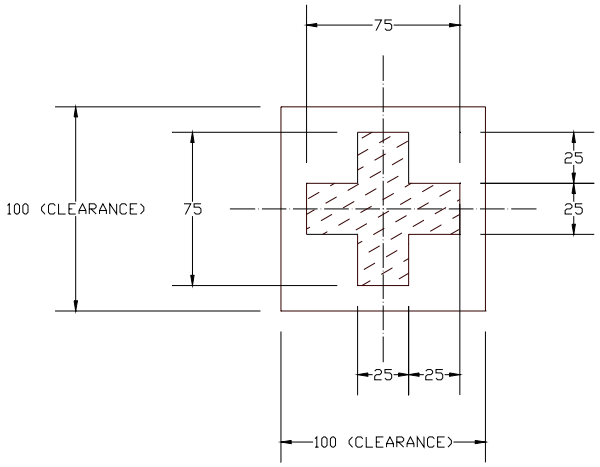
Pad no.	Pad Name	X-pos	Y-pos
181	SEG32	1774.8	679.6
182	SEG33	1722.6	679.6
183	SEG34	1670.4	679.6
184	SEG35	1618.2	679.6
185	SEG36	1566.0	679.6
186	SEG37	1513.8	679.6
187	SEG38	1461.6	679.6
188	SEG39	1409.4	679.6
189	SEG40	1357.2	679.6
190	SEG41	1305.0	679.6
191	SEG42	1252.8	679.6
192	SEG43	1200.6	679.6
193	SEG44	1148.4	679.6
194	SEG45	1096.2	679.6
195	SEG46	1044.0	679.6
196	SEG47	991.8	679.6
197	SEG48	939.6	679.6
198	SEG49	887.4	679.6
199	SEG50	835.2	679.6
200	SEG51	783.0	679.6
201	SEG52	730.8	679.6
202	SEG53	678.6	679.6
203	SEG54	626.4	679.6
204	SEG55	574.2	679.6
205	SEG56	522.0	679.6
206	SEG57	469.8	679.6
207	SEG58	417.6	679.6
208	SEG59	365.4	679.6
209	SEG60	313.2	679.6
210	SEG61	261.0	679.6
211	SEG62	208.8	679.6
212	SEG63	156.6	679.6
213	SEG64	104.4	679.6
214	SEG65	52.2	679.6
215	SEG66	0.0	679.6
216	SEG67	-52.2	679.6
217	SEG68	-104.4	679.6
218	SEG69	-156.6	679.6
219	SEG70	-208.8	679.6
220	SEG71	-261.0	679.6
221	SEG72	-365.4	679.6
222	SEG73	-417.6	679.6
223	SEG74	-469.8	679.6
224	SEG75	-522.0	679.6
225	SEG76	-574.2	679.6
226	SEG77	-626.4	679.6
227	SEG78	-678.6	679.6
228	SEG79	-730.8	679.6
229	SEG80	-783.0	679.6
230	SEG81	-835.2	679.6
231	SEG82	-887.4	679.6
232	SEG83	-939.6	679.6
233	SEG84	-991.8	679.6
234	SEG85	-1044.0	679.6
235	SEG86	-1096.2	679.6
236	SEG87	-1148.4	679.6
237	SEG88	-1200.6	679.6
238	SEG89	-1252.8	679.6
239	SEG90	-1305.0	679.6
240	SEG91	-1357.2	679.6

Pad no.	Pad Name	X-pos	Y-pos
241	SEG92	-1409.4	679.6
242	SEG93	-1461.6	679.6
243	SEG94	-1513.8	679.6
244	SEG95	-1566.0	679.6
245	SEG96	-1618.2	679.6
246	SEG97	-1670.4	679.6
247	SEG98	-1722.6	679.6
248	SEG99	-1774.8	679.6
249	SEG100	-1827.0	679.6
250	SEG101	-1879.2	679.6
251	SEG102	-1931.4	679.6
252	SEG103	-1983.6	679.6
253	SEG104	-2035.8	679.6
254	SEG105	-2088.0	679.6
255	SEG106	-2140.2	679.6
256	SEG107	-2192.4	679.6
257	SEG108	-2244.6	679.6
258	SEG109	-2296.8	679.6
259	SEG110	-2349.0	679.6
260	SEG111	-2401.2	679.6
261	SEG112	-2453.4	679.6
262	SEG113	-2505.6	679.6
263	SEG114	-2557.8	679.6
264	SEG115	-2610.0	679.6
265	SEG116	-2662.2	679.6
266	SEG117	-2714.4	679.6
267	SEG118	-2766.6	679.6
268	SEG119	-2818.8	679.6
269	SEG120	-2871.0	679.6
270	SEG121	-2923.2	679.6
271	SEG122	-2975.4	679.6
272	SEG123	-3027.6	679.6
273	SEG124	-3079.8	679.6
274	SEG125	-3132.0	679.6
275	SEG126	-3184.2	679.6
276	SEG127	-3236.4	679.6
277	SEG128	-3288.6	679.6
278	SEG129	-3340.8	679.6
279	SEG130	-3393.0	679.6
280	SEG131	-3445.2	679.6
281	COM1	-3654.0	679.6
282	COM3	-3705.8	679.6
283	COM5	-3757.6	679.6
284	COM7	-3809.4	679.6
285	COM9	-3861.2	679.6
286	COM11	-3913.0	679.6
287	COM13	-3964.8	679.6
288	COM15	-4016.6	679.6
289	COM17	-4068.4	679.6
290	COM19	-4120.2	679.6
291	COM21	-4172.0	679.6
292	COM23	-4223.8	679.6
293	COM25	-4275.6	679.6
294	COM27	-4327.4	679.6
295	COM29	-4379.2	679.6
296	COM31	-4431.0	679.6
297	NC	-4483.2	679.6
298	NC	-4535.4	679.6

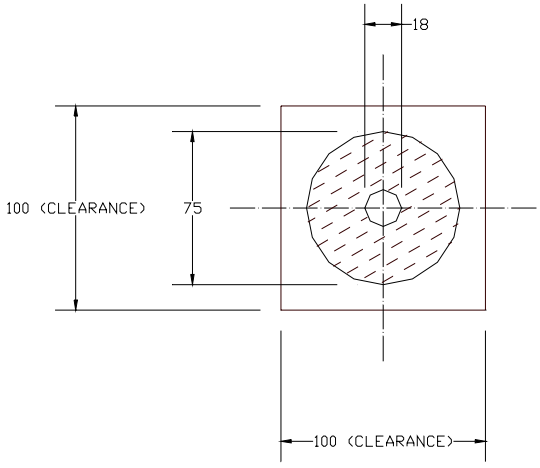
Figure 3 - SSD1303Z Alignment mark dimensions



T shape



+ shape



Circle

Unit in um

6 PIN DESCRIPTION

CL
This pin is the system clock input. When the internal clock is enabled this pin should be left open, as the internal clock is the output from this pin. When the internal oscillator is disabled this pin receives the display clock signal from the external clock source.

CLS
This is the internal clock enable pin. When it is pulled HIGH the internal clock is enabled. When it is pulled LOW the internal clock is disabled and an external clock source must be connected to the CL pin for normal operation.

BS0, BS1, BS2
These are the MCU interface input selection pins. See the table below for selecting different interfaces:

	6800-parallel interface	8080-parallel interface	Serial interface	I^2C interface
BS0	0	0	0	0
BS1	0	1	0	1
BS2	1	1	0	0

CS#
This pin is the chip select input. The chip is enabled for MCU communication only when the CS# is pulled low.

RES#
This is a reset signal input pin. When it is pulled LOW initialization of the chip is executed.

D/C
This is the Data/Command control pin. When it is pulled HIGH, the input at D_7-D_0 is treated as data. When it is pulled LOW, the input at D_7-D_0 is transferred to the command registers. For details of the relationship to MCU interface signals please refer to the Timing Characteristics Diagrams.

When the pin is pulled high and serial interface mode is selected, the data at SD_{IN} is treated as data. When the pin is pulled low, the data at SD_{IN} will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection.

R/W (WR#)
This is a MCU interface input pin. When the 6800-series Parallel Interface mode is selected, this pin is used as the Read/Write (R/W) selection input. Pull this pin to HIGH is for read mode and to LOW is for write mode.
When the 8080-series Parallel Interface mode is selected this pin is used as Write (WR#) selection input. Pull this pin to LOW is for write mode. Data write operation is initiated when this pin is pulled LOW and the CS# is also pulled LOW.

E (RD#)
This is a MCU interface input pin. When the 6800-series Parallel Interface is selected this pin is used as the Enable (E) signal. Read/Write operation is initiated when this pin is pulled HIGH and the CS# pin is pulled LOW. When the 8080-series Parallel Interface is selected this pin is used to receive the Read Data (RD#) signal. Data read operation is initiated when this pin is pulled LOW and the CS# pin is also pulled LOW.

D_7-D_0
These is 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D1 will be the serial data input, SD_{IN}, and D_0 will be the serial clock input, SCLK. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.

VDD
This is a voltage supply pin. It must be connected to an external source.

VSS
This is a ground pin. It also acts as a reference for the logic pins and the OLED driving voltages. It must be connected to an external ground.

BGGND
This is a ground pin for analog circuits. It must be connected to an external ground

VCC
This is the most positive voltage supply pin of the chip. It can be supplied externally.

VREF
This is a voltage reference pin for pre-charge voltage to drive the OLED device. The voltage should be set to match the OLED driving voltage in its current drive phase. It can either be supplied externally, or by connecting to the VCC.

IREF
This is a segment current reference pin. A resistor should be connected between this pin and the V_{SS} and the current set at 10uA.

VCOMH
This is an input pin for high-level voltage output for COM signals. A capacitor should be connected between this pin and the VSS.

VDDB This is a power supply pin for the internal buffer of the DC-DC voltage converter. It must be connected to the V_{DD} when the converter is used.

VSSB
This is a ground pin for the internal buffer of the DC-DC voltage converter. It must be connected to the V_{SS} when the converter is used.

GDR
This is an output pin which drives the gate of the external NMOS of the booster circuit.

RESE
This is a source current pin for the external NMOS of the booster circuit.

VB_{REF}
This is an internal voltage reference pin for the booster circuit. A stabilization capacitor, type 1uF, should be connected to the Vss.

FB
This is a feedback resistor input pin for the booster circuit. It is used to adjust the booster output voltage level for the Vcc.

COM0-COM63
These pins provide the Common switch signals to the OLED panel. They are in a state of high impedance when the display is OFF.

SEG0-SEG131
These pins provide the Segment switch signals to the OLED panel. They are in a state of high impedance when the display is OFF.

TR0-TR8, GPIO0, GPIO1, ICAS, M and DOF#
These are reserved pins. No connection is necessary and they should be left open individually.

VSL
This is a segment voltage reference pin. This pin should be connected to the VSS externally.

VCL
This is a common voltage reference pin. This pin should be connected to the VSS externally.

M/S
This pin must be connected to the VDD to enable the chip.

NC
Dummy pad. Do not group or short the NC pins together.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 Oscillator Circuit and Display Time Generator

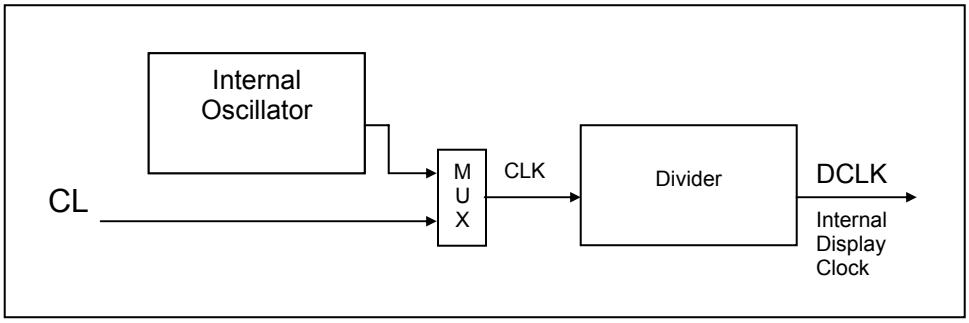


Figure 4 - Oscillator Circuit

This module is an On-Chip, low power, RC oscillator circuit (Figure 4). The oscillator generates the clock for the Display Timing Generator.

7.2 Reset Circuit

When RES# pin is pulled LOW the chip is initialized with the following status:

1. Display is OFF
2. 132 x 64 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 is mapped to column address 00H and COM0 is mapped to row address 00H)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80H
9. DC/DC enabled

7.3 Command Decoder and Command Interface

This module determines if the input data is interpreted as data, or a command. When the D/C# pin is pulled HIGH the inputs at D_7-D_0 are interpreted as data and will be written to Graphic Display Data RAM (GDDRAM). When it is pulled LOW the inputs at D_7-D_0 are interpreted as a command and will be decoded and written to the corresponding command registers.

7.4 MPU I^2C interface

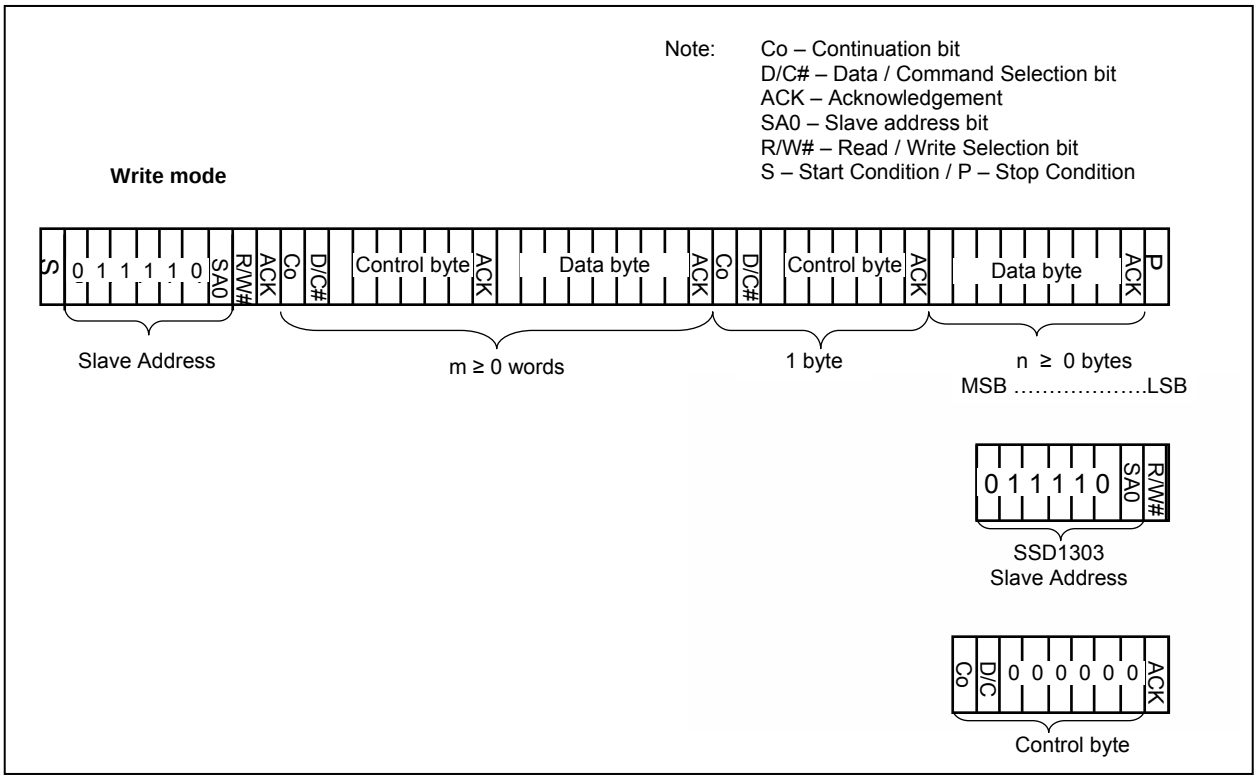
The I^2C communication interface consists of slave address bit SA0, I^2C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I^2C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
   SSD1303 has to recognize the slave address before transmitting or receiving any information by the I^2C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,
   b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
   0 1 1 1 1 0 SA0 R/W#
   "SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1303. D/C pin acts as SA0 for slave address selection.
   "R/W#" bit is used to determine the operation mode of the I^2C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.
b) I^2C-bus data signal (SDA)
   SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.
   It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".
   "SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I^2C-bus.
c) I^2C-bus clock signal (SCL)
   The transmission of information in the I^2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 5 for the write mode of I²C-bus in chronological order.

Figure 5 - I²C-bus data format



Write mode for I^2C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 6. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1303, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic “0”.
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 7 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.
    a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 6. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

Figure 6 - Definition of the Start and Stop Condition

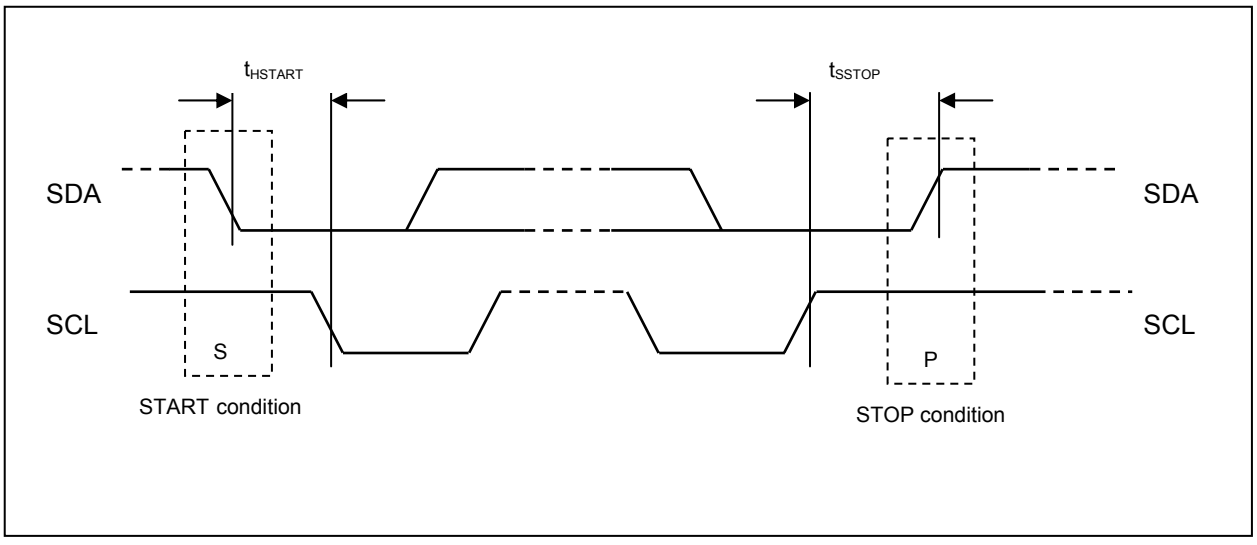
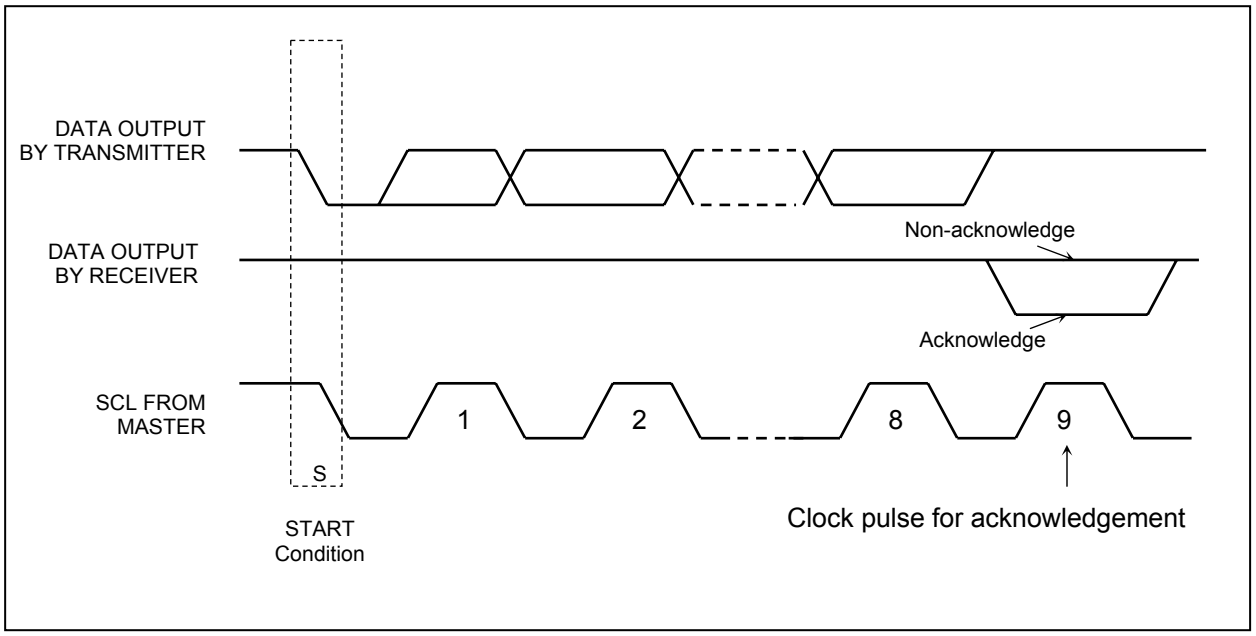


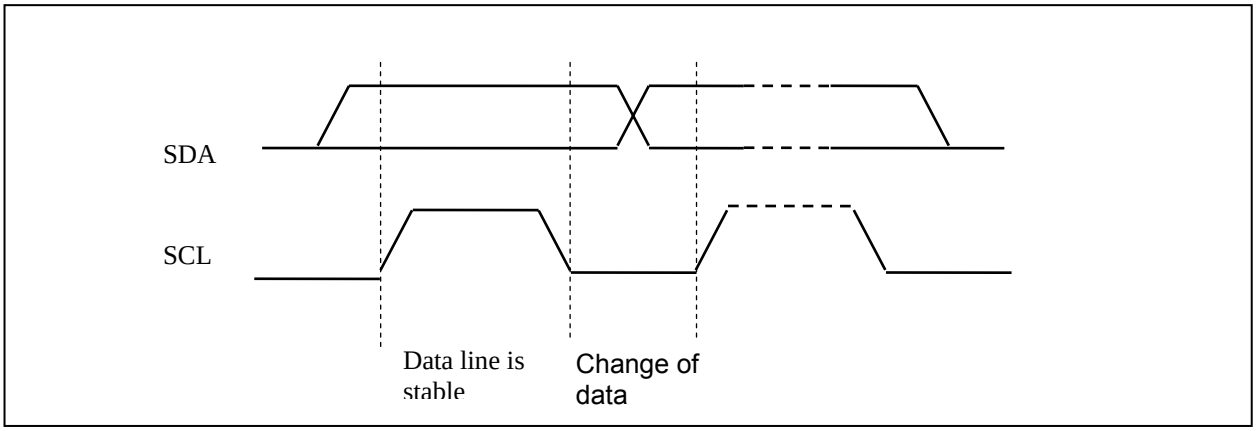
Figure 7 - Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 8 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 8 - Definition of the data transfer condition



7.5 MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins: (D_7-D_0), R/W (WR#), E (RD#), D/C, CS#. When the R/W (WR#) pin is pulled HIGH Read operation from the Graphic Display Data RAM (GDDRAM), or the status register, occurs. When the R/W (WR#) pin is pulled LOW Write operation to the Display Data RAM, or Internal Command Registers, occurs, depending on the status of the D/C input. The E (RD#) input serves as the data latch signal (clock) when on HIGH, provided the CS# is pulled LOW. Please refer to the Parallel Interface Timing Diagram of the 6800-series microprocessors.
In order to match the operating frequency of the display RAM with that of the microprocessor, some pipeline processing is performed internally, which requires the insertion of a dummy read before the first actual display data read. See Figure 5 below.

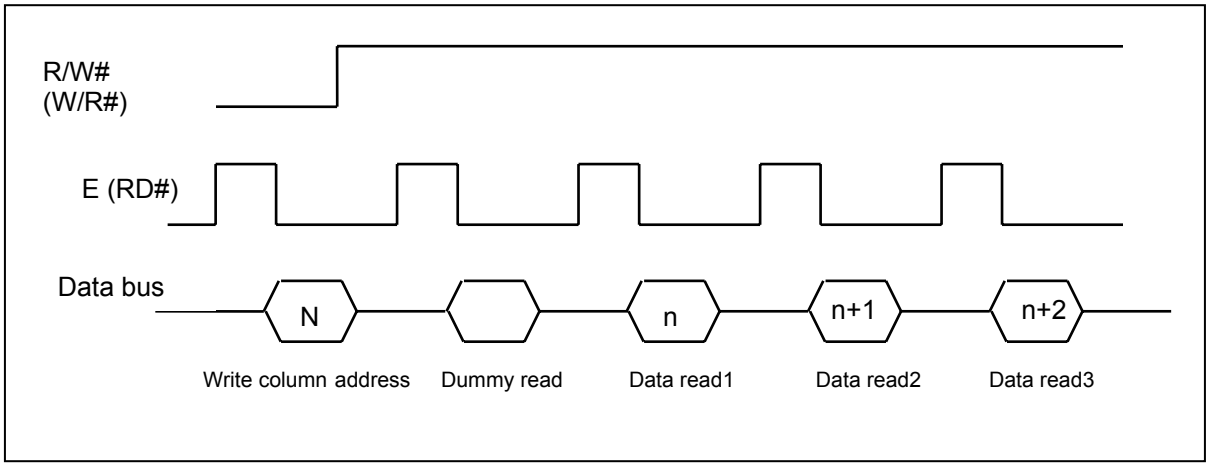


Figure 9 - Display data read back procedure - insertion of dummy read

7.6 MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), R/W (WR#), E (RD#), D/C, CS#. The E (RD#) input serves as the data read latch signal (clock) when on LOW, provided the CS# is also pulled LOW. Display data, or status register read, is controlled by the D/C signal.
R/W (WR#) input serves as the data write latch signal (clock) when on HIGH, provided the CS# is also pulled LOW. Display data, or command register write, is controlled by the D/C. Please refer to Parallel Interface Timing Diagram of the 8080-series microprocessors. Similar to the 6800-series interface, a dummy read is also required before the first, actual display data read.

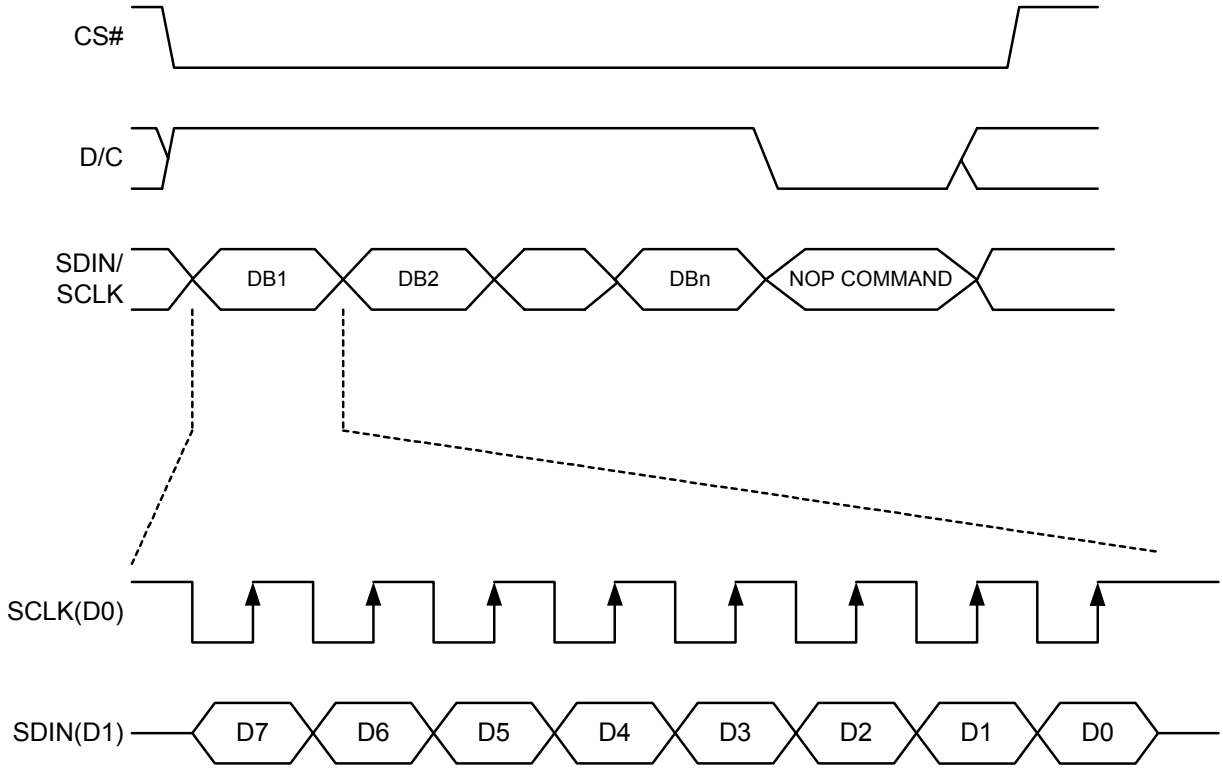
7.7 MPU Serial Interface

The serial interface consists of the serial clock SCLK and serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK and D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins fromD3 to D7, E and R/W can be connected to an external ground.

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D_7, D_6, ... D_0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM, or command register, in the same clock.

During data writing an additional NOP command should be inserted before the CS# is pulled HIGH. See Figure 10 below.

Figure 10 – Display data write procedure in SPI mode



7.8 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 x 64 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.
For vertical scrolling of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display.

7.9 Current Control and Voltage Control

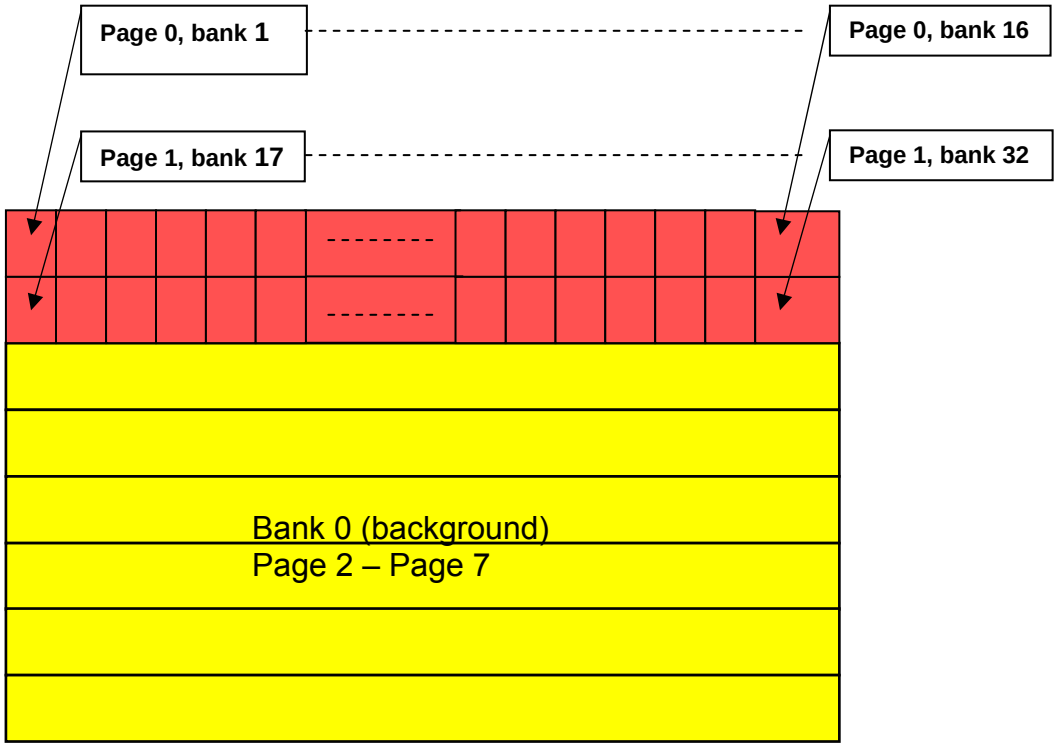
This block is used to divide the incoming power sources into different levels of internal use voltage and current. VCC and VDD are external power supplies. VREF is a reference voltage, used to derive the driving voltage for both segments and commons. IREF is a reference current source for the segment current drivers.

7.10 Segment Drivers / Common Drivers

Segment drivers deliver 132 current sources to drive the OLED panel. The driving current can be adjusted from 0 to 300uA with 256 steps. Common drivers generate voltage-scanning pulses.

7.11 Area Color Decoder

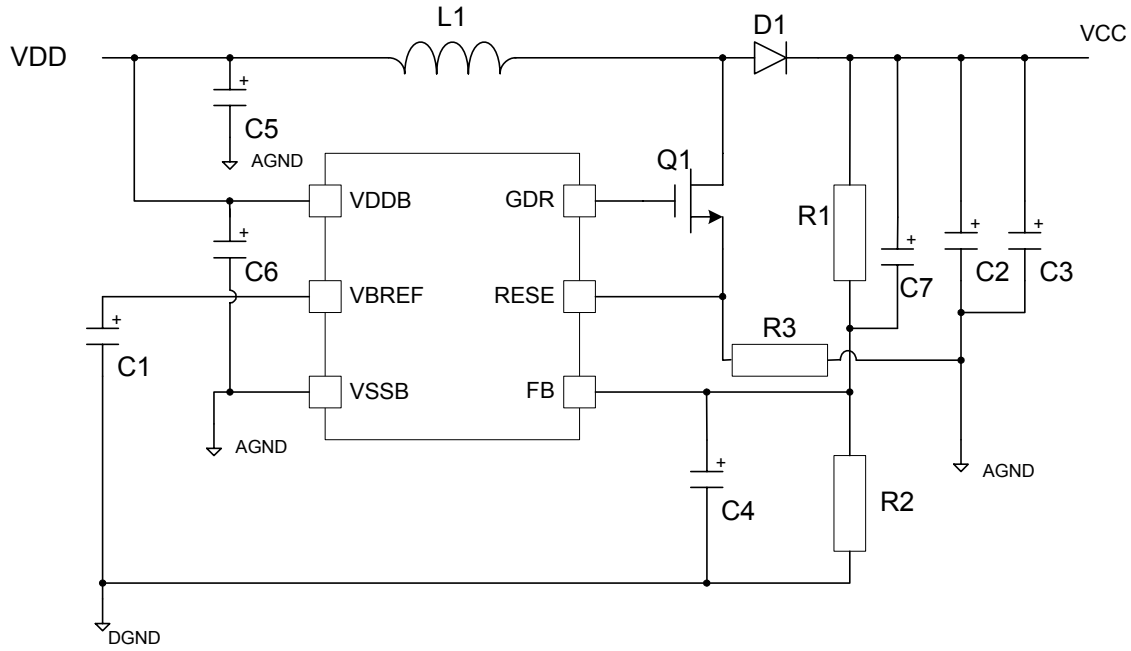
Page 0 and Page 1 of the display are divided into 32 banks. Bank16 and Bank32 consist of a display area of 12 x 8 pixels. Other banks (0~15 & 17~31) have matrices of 8 x 8 pixels. Each bank can be programmed to any one of the four colors (color A, B, C and D). Detailed operation can be referred to the Command Table.



7.12 DC-DC Voltage Converter

This is a switching voltage generator circuit, designed for handheld applications. In the SSD1303 an internal DC-DC voltage converter accompanying an external application circuit (See Figure 7 below) can generate a high voltage supply, $V_{CC,}$ from a low voltage supply input, V_{DD}. The V_{CC} is the voltage supply to the OLED driver block. Below is an example application circuit for the input voltage of 3V VDD to generate V_{CC} of 12V @0mA ~ 20mA application.

Figure 11 - DC-DC voltage converter circuit



Remark:

1. VSSB is tied to VSS in the SSD1303T3 package.
2. L1, D1, Q1, C5 should be grouped close together on PCB layout.
3. R1, R2, C1, C4 should be grouped close together on PCB layout.
4. The VCC output voltage level can be adjusted by R1and R2, the reference formula is:
   VCC = 1.2 x (R1+R2) / R2
   The value of (R1+R2) should be between 500k to 1M Ohm.

Table 3 - Passive component selection:

Components	Typical Value	Remark
L1	Inductor, 22μH	LP04815-223KXB [Coilcraft] - Low DCR - Over 0.5A current rating
D1	Schottky diode	MBR0520 [On Semi] - 0.5A
Q1	MOSFET	NTA4153N [On Semi] - Low Rds - Over 0.5A current rating
R1	Resistor, 510k	1%
R2	Resistor, 56k	1%
R3	Resistor, 1.2Ω	1%, 1/8W
C1	Capacitor, 1μF	6V
C2	Capacitor, 10μF	25V
C3	Capacitor, 1μF	25V
C4	Capacitor, 15nF	16V
C5	Capacitor, 10μF	6V
C6	Capacitor, 10μF	6V
C7	Capacitor, 15nF	6V

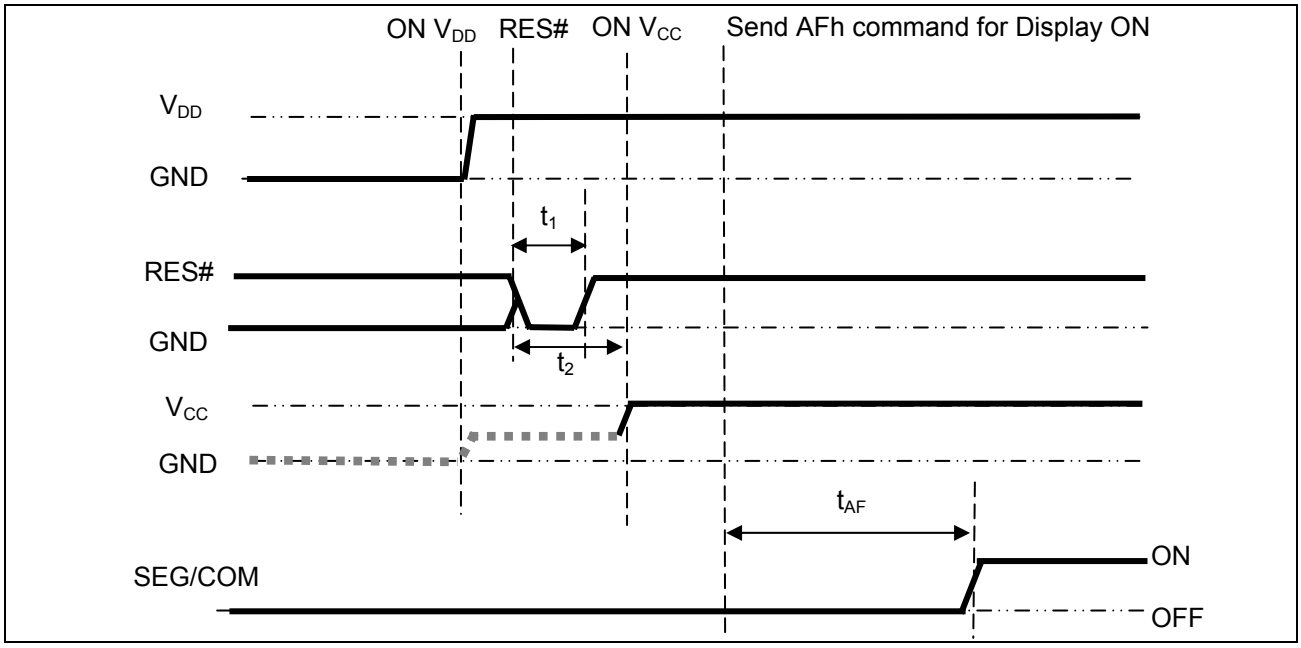
7.13 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1303.

Power ON sequence:

1. Power ON $V_{DD.}$
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON $V_{CC.}$ (1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

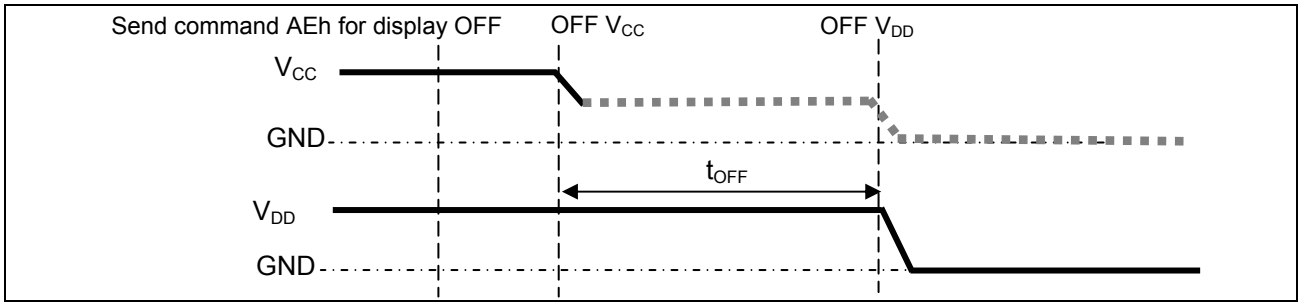
Figure 12 - The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF $V_{CC.}$ (1), (2)
4. Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=0ms, Typical t_{OFF}=100ms)

Figure 13 - The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 12 and Figure 13.

(2) V_{CC} should be kept float (disable) when it is OFF.

8 COMMAND TABLE

Table 4 - Command table

(D/C =0, R/W (WR#)=0, E (RD#)=1)
Note: commands marked with "**" are compatible with theSSD1301

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Address **	Set the lower nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after RESET.
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Address **	Set the higher nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after RESET.
0	26	0	0	1	0	0	1	1	0	Horizontal scroll setup	A[2:0] Set the number of column scroll per step
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		Valid value: 001b, 010b, 011b, 100b
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		B[2:0] Define start page address
0	C[1:0]	*	*	*	*	*	*	C_1	C_0		C[1:0] Set time interval between each scroll step in terms of frame frequency
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		00b – 12 frame 01b – 64 frames 10b – 128 frames 11b – 256 frames D[2:0] Define end page address Set the value of D[2:0] larger or equal to B[2:0]
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Start horizontal scrolling
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Stop horizontal scrolling
0	40-7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000 during RESET
0	81	1	0	0	0	0	0	0	1	Set Contrast Control Register **	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 80h)
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	82	1	0	0	0	0	0	1	0	Brightness for color banks	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases. (RESET = 80h)
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	91	1	0	0	1	0	0	0	1	Set Look Up Table (LUT)	Set current drive pulse width of Bank 0, Color A, B and C.
0	X[5:0]	*	*	X_5	X_4	X_3	X_2	X_1	X_0		Bank 0: X[5:0] = 31… 63; for pulse width set to 32 ~ 64 clocks (RESET = 110001b)
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		Color A: A[5:0] same as above (RESET = 111111b)
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		Color B: B[5:0] same as above (RESET = 111111b)
0	C[5:0]	*	*	C_5	C_4	C_3	C_2	C_1	C_0		Color C: C[5:0] same as above (RESET =111111b) Note: color D pulse width is fixed at 64 clocks pulse.

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	92	1	0	0	1	0	0	1	0	Set bank color of for bank 1-16 (Page 0)	A[1:0] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 1
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[3:2] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 2
0	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		:
0	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		:
0	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		D[7:6]: 00, 01, 10, or 11 for Color = A, B, C or D of bank 16
0	93	1	0	0	1	0	0	1	1	Set bank color of for bank 17-32 (Page 1)	A[1:0] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 17
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[3:2] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 18
0	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		:
0	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		:
0	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		D[7:6]: 00, 01, 10, or 11 for Color = A, B, C or D of bank 32
0	A0~ A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map **	X_0=0: column address 0 is mapped to SEG0 (RESET) X_0=1: column address 131 is mapped to SEG0
0	A4~A5	1	0	1	0	0	1	0	X_0	Set Entire Display ON/OFF **	X_0=0: normal display (RESET) X_0=1: entire display ON
0	A6~A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display **	X_0=0: normal display (RESET) X_0=1: inverse display
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio **	The next command, A[5:0] determines multiplex ratio N from 16MUX-64MUX, RESET= 64MUX
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	AA	1	0	1	0	1	0	1	0	NOP	Reserved, do not use
0	AB	1	0	1	0	1	0	1	1	NOP	Reserved, do not use
0 0	AD	1 1	0 0	1 0	0 0	1 1	1 0	0 1	1 X_0	Set DC-DC on/off	X_0 : 1 DC-DC will be turned on when display on (RESET) 0 DC-DC is disable
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF **	X_0=0: turns OFF OLED panel (RESET) X_0=1: turns ON OLED panel
0	B0~BF	1	0	1	1	X_3	X_2	X_1	X_0	Set Page Address **	Set GDDRAM Page Address (0~7) for read/write using $X_3X_2X_1X_0$
0	C0/C8	1	1	0	0	X_3	*	*	*	Set COM Output Scan Direction **	X_3=0: normal mode (RESET) Scan from COM 0 to COM [N –1] X_3=1: remapped mode. Scan from COM [N-1] to COM0 Where N is the Multiplex ratio.
0	D0-D1	1	1	0	1	0	0	0	X_0	Reserved	Reserved, do not use

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	D3	1	1	0	1	0	0	1	1	Set Display Offset **	Set vertical scroll by COM from 0-63.
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		The value is reset to 00H after RESET.
0	D5	1	1	0	1	0	1	0	1	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] Define the divide ratio of the display clocks (DCLK):
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] Set the Oscillator Frequency. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 0111b
0	D8	1	1	0	1	1	0	0	0	Set area color mode on/off & low power display mode	X_5X_4= 00 (RESET) : mono mode
0		0	0	X_5	X_4	0	X_2	0	X_0		X_5X_4= 11 Area Color enable X_2=0 and X_0=0: Normal (RESET) power mode X_2=1 and X_0=1: Set low power save mode
0	D9	1	1	0	1	1	0	0	1	Set Pre-charge period**	A[3:0] Phase 1 period of up to 15 dclk clocks [RESET=2h]; 0 is invalid entry
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:4] Phase 2 period of up to 15 dclk clocks [RESET=2h]; 0 is invalid entry
0	DA	1	1	0	1	1	0	1	0	Set COM pins hardware configuration	X_4=0, Sequential COM pin configuration
0		0	0	0	X_4	0	0	1	0		(i.e. COM31, 30, 29….0 ; SEG0-132; COM31,32….62,63) X_4=1(RESET), Alternative COM pin configuration (i.e. COM62,60,58,…2,0; SEG0-132; COM1,3,5…61,63)
0	DB	1	1	0	1	1	0	1	1	Set VCOM Deselect Level	A[5:0] 000000 low VCOM deselect level (~ 0.43 Vref)
0	A[6:0]	0	0	A_5	A_4	A_3	A_2	A_1	A_0		110101 normal VCOM deselect level (~ 0.77*Vref (RESET))
0	E2	1	1	1	0	0	0	1	0	Reserved	Reserved
0	E3	1	1	1	0	0	0	1	1	NOP **	Command for No Operation
0	F*	1	1	1	1	*	*	*	*	Reserved	Reserved, do not use

Note: Remark "*" stands for "Don't Care"

Table 5 - Read command table

(D/C=0, R/W (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read *	D_7 : Reserve D_6 : "1" for display OFF / "0" for display ON D_5 : Reserve D_4 : Reserve D_3 : Reserve D_2 : Reserve D_1 : Reserve D_0 : Reserve

Note: Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

8.1 Data Read / Write

To read data from the GDD RAM, select HIGH for both the R/W (WR#) pin and the D/C pin for 6800-series parallel mode and select LOW for the E (RD#) pin and HIGH for the D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.
In normal data read mode the GDD RAM column address pointer will be increased automatically by one after each data read.
Also, a dummy read is required before the first data read. See Figure 5 in the Functional Block Description.
To write data to the GDD RAM, select LOW for the R/W (WR#) pin and HIGH for the D/C pin for both 6800-series parallel mode and 8080-series parallel mode. The serial interface mode is always in write mode. The GDD RAM column address pointer will be increased automatically by one after each data write.

Table 6 - Address increment table (Automatic)

D/C	R/W (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes*1

9 COMMAND DESCRIPTIONS

Set Lower Column Address
This command specifies the lower nibble of the 8-bit column address for the display data RAM. The column address will be incremented by each data access, after it is pre-set by the MCU.

Set Higher Column Address
This command specifies the higher nibble of the 8-bit column address for the display data RAM. The column address will be incremented by each data access, after it is pre-set by the MCU.

Activate Horizontal Scroll
This command starts the motion of horizontal scrolling and should only be issued after the Horizontal scroll setup parameters have been defined.

The following actions are prohibited after the horizontal scroll is activated
1. RAM access (Data write or read)
2. Changing the horizontal scroll setup parameters

The SSD1303 horizontal scroll is designed for 128 columns scrolling only. The 4 remaining columns are reserved for computation and should be left open.

With column address 0 mapped to SEG0 (Segment remap setting = A0h), the 4 open columns will be SEG128, SEG129, SEG130 and SEG131.

With column address 0 mapped to SEG131 (Segment remap setting = A1h), the 4 open columns will be SEG0, SEG1, SEG2 and SEG3.

Figure 14 - Horizontal scroll direction

REMAP SETTING	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	⋯	⋯	⋯	SEG126	SEG127	SEG128	SEG129	SEG130	SEG131
A0	A	B	C	D	E	F	→	→	→	Y	Z	Invalid data			
A1	Invalid data				Z	Y	←	←	←	F	E	D	C	B	A

Scroll direction

Deactivate Horizontal Scroll
This command stops the motion of horizontal scrolling.

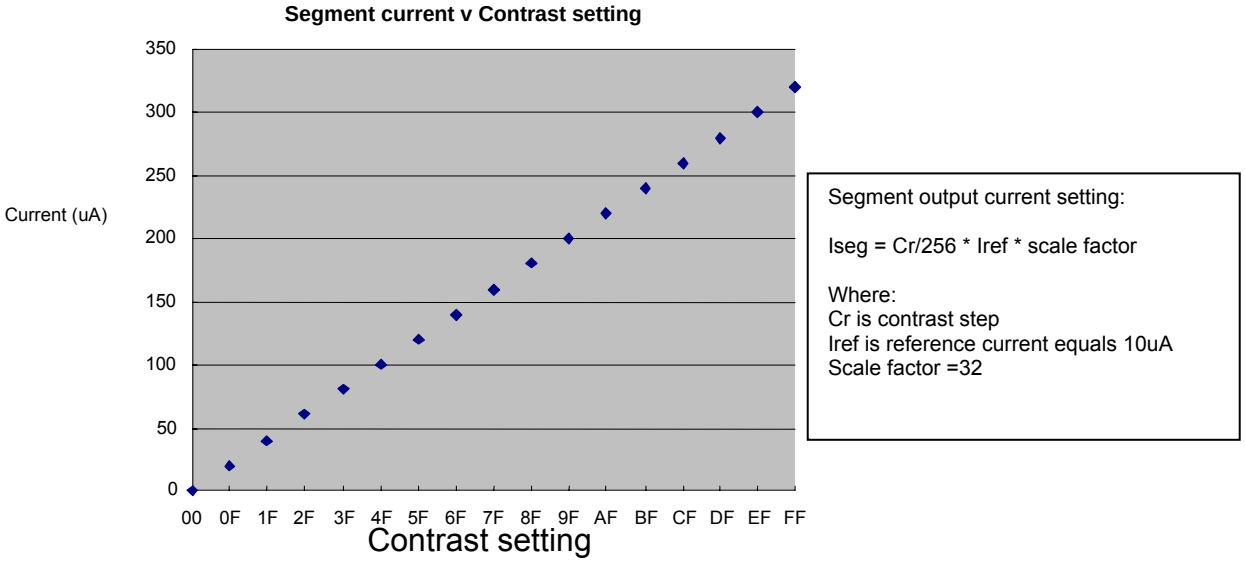
Horizontal Scroll Setup
This command consists of 5 consecutive bytes to set up the horizontal scroll parameters and determines the scrolling start page, end page and scrolling speed.

Before issuing this command the horizontal scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

Set Display Start Line
This command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 63. With value equal to 0, D_0 of Page 0 is mapped to COM0. With value equal to 1, D_1 of Page0 is mapped to COM0. The display start line values of 0 to 63 are assigned to Page 0 to Page 7.

Set Contrast Control Register
This command sets the Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases. See Figure 15 below.

Figure 15 - Segment current v Contrast setting



Set Brightness for Color Banks
This command sets the Brightness Setting of the display for the area color banks (except bank 0). The chip has 256 brightness steps from 00 to FF. The segment output current increases as the brightness step value increases

Set Look Up Table (LUT)
The SSD1303 provides 4 color (pulse width) settings - Colors A, B, C and D. The color intensity (or grey scale) is defined by the current drive pulse width. The pulse width of colors A, B, C is programmable from 32 to 64 DCLK* duration. The color D is fixed at 64 DCLK pulse width. This color setting must be stored in the Look Up Table (LUT).
For the background color, the color intensity is defined by a variable X[5:0].

Set LUT command: 10010001
X[5:0]
A[5:0]
B[5:0]
C[5:0]

	Description	Number of DCLKs
Bank 0	Set background color	X[5:0]
Color A	Set Pulse Width A	A[5:0]
Color B	Set Pulse Width B	B[5:0]
Color C	Set Pulse Width C	C[5:0]
Color D	Pulse width D is fixed to 64 DCLK	64 (fixed)

DCLK: Internal Display Clock
Set bank color of bank 1-16 (Page 0) and bank color of bank 17-32 (Page 1)

The next step is to define the color of each display area. The 132x64 display matrix is divided into 8 pages of 8 commons per page. The first two pages, page 0 and page 1, are divided into 32 banks: Bank16 and Bank32 consists of a display area of 12x8 pixels. Other banks (0~15 & 17~31) have matrices of 8x8 pixels. Each bank can be programmable to any one of the 4 colors (A, B, C and D). The user can select 92h and 93h commands for the bank color setting but this is only applicable in area color mode.

Set Segment Re-map
This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. Please refer to the Command Table.

Set Entire Display ON/OFF
This command forces the entire display to be “ON”, regardless of the contents of the display data RAM. This command has priority over normal/reverse display and can be used with “Set Display ON/OFF” command to form a combined command for engaging power save mode.

Set Normal/Inverse Display
This command sets the display to be either normal or inverse. In normal display a RAM data of 1 indicates an “ON” pixel while in inverse display a RAM data of 0 indicates an “ON” pixel.

Set Multiplex Ratio
This command switches the default 63 multiplex mode to any multiplex ratio, ranging from 2 to 63. The output pads COM0-COM63 will be switched to the corresponding COM signal.

Set DC-DC on/off
This command controls the DC-DC voltage converter, which will be turned on by issuing this command then the DISPLAY ON command. The panel display must be off while issuing this command.
For RESET the DC-DC will be turned on.

Set Display ON/OFF
This command turns the display ON or OFF. When the display is OFF the segment and common output are in a state of high impedance.

Set Page Address
This command positions the page address from 0 to 7 in GDD RAM. Please refer to the Command Table.

Set COM Output Scan Direction
This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display then the graphic display will be vertically flipped.

Set Display Offset
This is a double byte command. The second command specifies the mapping of the display start line to one of COM0-63 (assuming that COM0 is the display start line then the display start line register is equal to 0). For example, to move the COM16 towards the COM0 direction by 16 lines the 6-bit data in the second byte should be given as 010000. To move in the opposite direction by 16 lines the 6-bit data should be given by 64 – 16, so the second byte would be 100000.

	Output												
	64		64		64		56		56		56		Set MUX ratio(A8)
	Normal		Normal		Normal		Normal		Normal		Normal		COM Normal / Remapped (C0 / C8)
Hardware	0		8		0		0		8		0		Display offset (D3)
pin name	0		0		8		0		0		8		Display start line (40 - 7F)
COM0	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row0	RAM0	Row8	RAM8	Row0	RAM8	
COM1	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row1	RAM1	Row9	RAM9	Row1	RAM9	
COM2	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row2	RAM2	Row10	RAM10	Row2	RAM10	
COM3	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row3	RAM3	Row11	RAM11	Row3	RAM11	
COM4	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row4	RAM4	Row12	RAM12	Row4	RAM12	
COM5	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row5	RAM5	Row13	RAM13	Row5	RAM13	
COM6	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row6	RAM6	Row14	RAM14	Row6	RAM14	
COM7	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row7	RAM7	Row15	RAM15	Row7	RAM15	
COM8	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row8	RAM8	Row16	RAM16	Row8	RAM16	
COM9	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row9	RAM9	Row17	RAM17	Row9	RAM17	
COM10	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row10	RAM10	Row18	RAM18	Row10	RAM18	
COM11	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row11	RAM11	Row19	RAM19	Row11	RAM19	
COM12	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row12	RAM12	Row20	RAM20	Row12	RAM20	
COM13	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row13	RAM13	Row21	RAM21	Row13	RAM21	
COM14	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row14	RAM14	Row22	RAM22	Row14	RAM22	
COM15	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row15	RAM15	Row23	RAM23	Row15	RAM23	
COM16	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row16	RAM16	Row24	RAM24	Row16	RAM24	
COM17	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row17	RAM17	Row25	RAM25	Row17	RAM25	
COM18	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row18	RAM18	Row26	RAM26	Row18	RAM26	
COM19	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row19	RAM19	Row27	RAM27	Row19	RAM27	
COM20	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row20	RAM20	Row28	RAM28	Row20	RAM28	
COM21	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row21	RAM21	Row29	RAM29	Row21	RAM29	
COM22	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row22	RAM22	Row30	RAM30	Row22	RAM30	
COM23	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row23	RAM23	Row31	RAM31	Row23	RAM31	
COM24	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row24	RAM24	Row32	RAM32	Row24	RAM32	
COM25	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row25	RAM25	Row33	RAM33	Row25	RAM33	
COM26	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row26	RAM26	Row34	RAM34	Row26	RAM34	
COM27	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row27	RAM27	Row35	RAM35	Row27	RAM35	
COM28	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row28	RAM28	Row36	RAM36	Row28	RAM36	
COM29	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row29	RAM29	Row37	RAM37	Row29	RAM37	
COM30	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row30	RAM30	Row38	RAM38	Row30	RAM38	
COM31	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row31	RAM31	Row39	RAM39	Row31	RAM39	
COM32	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row32	RAM32	Row40	RAM40	Row32	RAM40	
COM33	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row33	RAM33	Row41	RAM41	Row33	RAM41	
COM34	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row34	RAM34	Row42	RAM42	Row34	RAM42	
COM35	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row35	RAM35	Row43	RAM43	Row35	RAM43	
COM36	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row36	RAM36	Row44	RAM44	Row36	RAM44	
COM37	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row37	RAM37	Row45	RAM45	Row37	RAM45	
COM38	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row38	RAM38	Row46	RAM46	Row38	RAM46	
COM39	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row39	RAM39	Row47	RAM47	Row39	RAM47	
COM40	Row40	RAM40	Row48	RAM48	Row40	RAM48	Row40	RAM40	Row48	RAM48	Row40	RAM48	
COM41	Row41	RAM41	Row49	RAM49	Row41	RAM49	Row41	RAM41	Row49	RAM49	Row41	RAM49	
COM42	Row42	RAM42	Row50	RAM50	Row42	RAM50	Row42	RAM42	Row50	RAM50	Row42	RAM50	
COM43	Row43	RAM43	Row51	RAM51	Row43	RAM51	Row43	RAM43	Row51	RAM51	Row43	RAM51	
COM44	Row44	RAM44	Row52	RAM52	Row44	RAM52	Row44	RAM44	Row52	RAM52	Row44	RAM52	
COM45	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row45	RAM45	Row53	RAM53	Row45	RAM53	
COM46	Row46	RAM46	Row54	RAM54	Row46	RAM54	Row46	RAM46	Row54	RAM54	Row46	RAM54	
COM47	Row47	RAM47	Row55	RAM55	Row47	RAM55	Row47	RAM47	Row55	RAM55	Row47	RAM55	
COM48	Row48	RAM48	Row56	RAM56	Row48	RAM56	Row48	RAM48	-	-	Row48	RAM56	
COM49	Row49	RAM49	Row57	RAM57	Row49	RAM57	Row49	RAM49	-	-	Row49	RAM57	
COM50	Row50	RAM50	Row58	RAM58	Row50	RAM58	Row50	RAM50	-	-	Row50	RAM58	
COM51	Row51	RAM51	Row59	RAM59	Row51	RAM59	Row51	RAM51	-	-	Row51	RAM59	
COM52	Row52	RAM52	Row60	RAM60	Row52	RAM60	Row52	RAM52	-	-	Row52	RAM60	
COM53	Row53	RAM53	Row61	RAM61	Row53	RAM61	Row53	RAM53	-	-	Row53	RAM61	
COM54	Row54	RAM54	Row62	RAM62	Row54	RAM62	Row54	RAM54	-	-	Row54	RAM62	
COM55	Row55	RAM55	Row63	RAM63	Row55	RAM63	Row55	RAM55	-	-	Row55	RAM63	
COM56	Row56	RAM56	Row0	RAM0	Row56	RAM0	-	-	Row0	RAM0	-	-	
COM57	Row57	RAM57	Row1	RAM1	Row57	RAM1	-	-	Row1	RAM1	-	-	
COM58	Row58	RAM58	Row2	RAM2	Row58	RAM2	-	-	Row2	RAM2	-	-	
COM59	Row59	RAM59	Row3	RAM3	Row59	RAM3	-	-	Row3	RAM3	-	-	
COM60	Row60	RAM60	Row4	RAM4	Row60	RAM4	-	-	Row4	RAM4	-	-	
COM61	Row61	RAM61	Row5	RAM5	Row61	RAM5	-	-	Row5	RAM5	-	-	
COM62	Row62	RAM62	Row6	RAM6	Row62	RAM6	-	-	Row6	RAM6	-	-	
COM63	Row63	RAM63	Row7	RAM7	Row63	RAM7	-	-	Row7	RAM7	-	-	

	Output														
	64		64		64		48		48		48		48		Set MUX ratio(A8)
	Remap		Remap		Remap		Remap		Remap		Remap		Remap		COM Normal / Remapped (C0 / C8)
Hardware	0		8		0		0		8		0		8		Display offset (D3)
pin name	0		0		8		0		0		8		16		Display start line (40 - 7F)
COM0	Row63	RAM63	Row7	RAM7	Row63	RAM7	Row47	RAM47	-	-	Row47	RAM41	-	-	
COM1	Row62	RAM62	Row6	RAM6	Row62	RAM6	Row46	RAM46	-	-	Row46	RAM40	-	-	
COM2	Row61	RAM61	Row5	RAM5	Row61	RAM5	Row45	RAM45	-	-	Row45	RAM41	-	-	
COM3	Row60	RAM60	Row4	RAM4	Row60	RAM4	Row44	RAM44	-	-	Row44	RAM42	-	-	
COM4	Row59	RAM59	Row3	RAM3	Row59	RAM3	Row43	RAM43	-	-	Row43	RAM43	-	-	
COM5	Row58	RAM58	Row2	RAM2	Row58	RAM2	Row42	RAM42	-	-	Row42	RAM44	-	-	
COM6	Row57	RAM57	Row1	RAM1	Row57	RAM1	Row41	RAM41	-	-	Row41	RAM45	-	-	
COM7	Row56	RAM56	Row0	RAM0	Row56	RAM0	Row40	RAM40	-	-	Row40	RAM46	-	-	
COM8	Row55	RAM55	Row63	RAM63	Row55	RAM63	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row47	RAM63	
COM9	Row54	RAM54	Row62	RAM62	Row54	RAM62	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row46	RAM62	
COM10	Row53	RAM53	Row61	RAM61	Row53	RAM61	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row45	RAM61	
COM11	Row52	RAM52	Row60	RAM60	Row52	RAM60	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row44	RAM60	
COM12	Row51	RAM51	Row59	RAM59	Row51	RAM59	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row43	RAM59	
COM13	Row50	RAM50	Row58	RAM58	Row50	RAM58	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row42	RAM58	
COM14	Row49	RAM49	Row57	RAM57	Row49	RAM57	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row41	RAM57	
COM15	Row48	RAM48	Row56	RAM56	Row48	RAM56	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row40	RAM56	
COM16	Row47	RAM47	Row55	RAM55	Row47	RAM55	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row39	RAM55	
COM17	Row46	RAM46	Row54	RAM54	Row46	RAM54	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row38	RAM54	
COM18	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row37	RAM53	
COM19	Row44	RAM44	Row52	RAM52	Row44	RAM52	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row36	RAM52	
COM20	Row43	RAM43	Row51	RAM51	Row43	RAM51	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row35	RAM51	
COM21	Row42	RAM42	Row50	RAM50	Row42	RAM50	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row34	RAM50	
COM22	Row41	RAM41	Row49	RAM49	Row41	RAM49	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row33	RAM49	
COM23	Row40	RAM40	Row48	RAM48	Row40	RAM48	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row32	RAM48	
COM24	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row31	RAM47	
COM25	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row30	RAM46	
COM26	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row29	RAM45	
COM27	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row28	RAM44	
COM28	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row27	RAM43	
COM29	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row26	RAM42	
COM30	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row25	RAM41	
COM31	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row24	RAM40	
COM32	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row23	RAM39	
COM33	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row22	RAM38	
COM34	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row21	RAM37	
COM35	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row20	RAM36	
COM36	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row19	RAM35	
COM37	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row18	RAM34	
COM38	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row17	RAM33	
COM39	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row16	RAM32	
COM40	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row15	RAM31	
COM41	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row14	RAM30	
COM42	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row13	RAM29	
COM43	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row12	RAM28	
COM44	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row11	RAM27	
COM45	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row10	RAM26	
COM46	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row9	RAM25	
COM47	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row8	RAM24	
COM48	Row15	RAM15	Row23	RAM23	Row15	RAM23	-	-	Row7	RAM7	-	-	Row7	RAM23	
COM49	Row14	RAM14	Row22	RAM22	Row14	RAM22	-	-	Row6	RAM6	-	-	Row6	RAM22	
COM50	Row13	RAM13	Row21	RAM21	Row13	RAM21	-	-	Row5	RAM5	-	-	Row5	RAM21	
COM51	Row12	RAM12	Row20	RAM20	Row12	RAM20	-	-	Row4	RAM4	-	-	Row4	RAM20	
COM52	Row11	RAM11	Row19	RAM19	Row11	RAM19	-	-	Row3	RAM3	-	-	Row3	RAM19	
COM53	Row10	RAM10	Row18	RAM18	Row10	RAM18	-	-	Row2	RAM2	-	-	Row2	RAM18	
COM54	Row9	RAM9	Row17	RAM17	Row9	RAM17	-	-	Row1	RAM1	-	-	Row1	RAM17	
COM55	Row8	RAM8	Row16	RAM16	Row8	RAM16	-	-	Row0	RAM0	-	-	Row0	RAM16	
COM56	Row7	RAM7	Row15	RAM15	Row7	RAM15	-	-	-	-	-	-	-	-	
COM57	Row6	RAM6	Row14	RAM14	Row6	RAM14	-	-	-	-	-	-	-	-	
COM58	Row5	RAM5	Row13	RAM13	Row5	RAM13	-	-	-	-	-	-	-	-	
COM59	Row4	RAM4	Row12	RAM12	Row4	RAM12	-	-	-	-	-	-	-	-	
COM60	Row3	RAM3	Row11	RAM11	Row3	RAM11	-	-	-	-	-	-	-	-	
COM61	Row2	RAM2	Row10	RAM10	Row2	RAM10	-	-	-	-	-	-	-	-	
COM62	Row1	RAM1	Row9	RAM9	Row1	RAM9	-	-	-	-	-	-	-	-	
COM63	Row0	RAM0	Row8	RAM8	Row0	RAM8	-	-	-	-	-	-	-	-	

Set Display Clock Divide Ratio/ Oscillator Frequency

This command sets the frequency of the internal display clocks -DCLKs. It is defined as the divide ratio (Value from 1 to 16) which is also used to divide the oscillator frequency. RESET is 1. Frame frequency is then determined by the divide ratio, the number of display clocks per row, the MUX ratio and oscillator frequency.

Set Area Color Mode ON/OFF

This command is used to enable area color mode. RESET is mono mode.

Set Low Power Display Mode
This is a double byte command and reduces power consumption during IC operation.

Set Pre-charge period
This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK, where RESET equals 2 DCLK.

Set COM pins hardware configuration
This command sets the COM signals pin configuration (sequential or alternative) to match the OLED panel hardware layout.

Sequential COM pin configuration:

COM31, 30, 29…0	**9.1.1.1.1.1 131**	**SEG0, 1, 2…**	**COM32, 33, 34…63**

Alternative COM pin configuration (RESET):

COM62, 60, 58…0	**9.1.1.1.1.2 131**	**SEG0, 1, 2…**	**COM1, 3, 5…63**

Set VCOM deselect level
This command sets the COM pin output voltage level at deselect stage.

NOP
No Operation Command

Status register Read
This command is issued by setting D/C# on LOW during a data read (See Figure 16 and Figure 17 for parallel interface waveform). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

10 MAXIMUM RATINGS

Table 7 - Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{CC}		0.0 to 18.0	V
V_{REF}		0.0 to 18.0	V
V_{COMH}	Supply Voltage/Output voltage	0.0 to 18.0	V
-	SEG/COM output voltage	0.0 to 18.0	V
V_{in}	Input voltage	V_{SS} -0.3 to V_{DD} +0.3	V
T_A	Operating Temperature	-40 to +90	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

Maximum Ratings are those beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 DC CHARACTERISTICS

Table 8 - DC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	7	12	16	V
V_{DD}	Logic Supply Voltage	-	2.4	-	3.5	V
V_{DD}	Logic Supply Voltage (internal DC/DC enable)	-	3.0	-	3.5	V
V_{OH}	High Logic Output Level	IOUT = 100uA, 3.3MHz	0.9*V_{DD}	-	V_{DD}	V
V_{OL}	Low Logic Output Level	IOUT = 100uA, 3.3MHz	0	-	0.1*V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8*V_{DD}	-	V_{DD}	V
V_{IL}	Low Logic Input Level	-	0	-	0.2*V_{DD}	V
I_{IL} /I_{IH}	Logic Input Current	-	-1	-	1	uA
$I_{CC, SLEEP}$	Sleep mode Current	V_{DD} =2.7V, display OFF, No panel attached	-10	-	+10	uA
$I_{DD, SLEEP}$	Sleep mode Current	V_{DD} =2.7V, display OFF, No panel attached	-10	-	+10	uA
I_{CC}	V_{CC} Supply Current V_{DD} = 2.7V, V_{CC} = 12V, I_{REF} = 10uA No loading, Display ON, All ON	Contrast = FF	-	550	1000	uA
I_{DD}	V_{DD} Supply Current V_{DD} = 2.7V, V_{CC} = 12V, I_{REF} = 10uA No loading, Display ON, All ON	Contrast = FF	-	190	300	uA
I_{SEG}	Segment Output Current V_{DD} = 2.7V, V_{CC} =12V, I_{REF} =10uA, Display ON, Segment pin under test is connected with a 20K resistive load to V_{SS}	Contrast=FF	285	320	355	uA
		Contrast=AF	-	220	-	
		Contrast=5F	-	120	-	
		Contrast=0F	-	20	-	
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:131] = Segment current at contrast = FF	-	-	±3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-	±2.0	-	%
Vcc	DC-DC converter output voltage	V_{DD} input=3V, L=22uH; R1=450Kohm; R2=50Kohm; Icc = 20mA(loading)	11.0	12.0	13.0	V
		-	7	-	16	
Pwr	DC-DC converter output power	V_{DD} input=3V, L=22uH; V_{CC} = 12V	-	-	400	mW

12 AC CHARACTERISTICS

Table 9 - AC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.7V	315	360	420	kHz
F_{FRM}	Frame Frequency for 64 MUX Mode	132x64 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} X 1/(D*K*64)	-	Hz
RES#	Reset low pulse width	-	3	-	-	us
	Reset complete time	-	-	-	2	us

D: divide ratio (default value = 1)
K: number of display clocks (default value = 54)
Please refer to the command table (set display clock divide ratio/oscillator freq) for detailed description
F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command D5h A[7:4] is in default value.

Table 10 - 6800-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

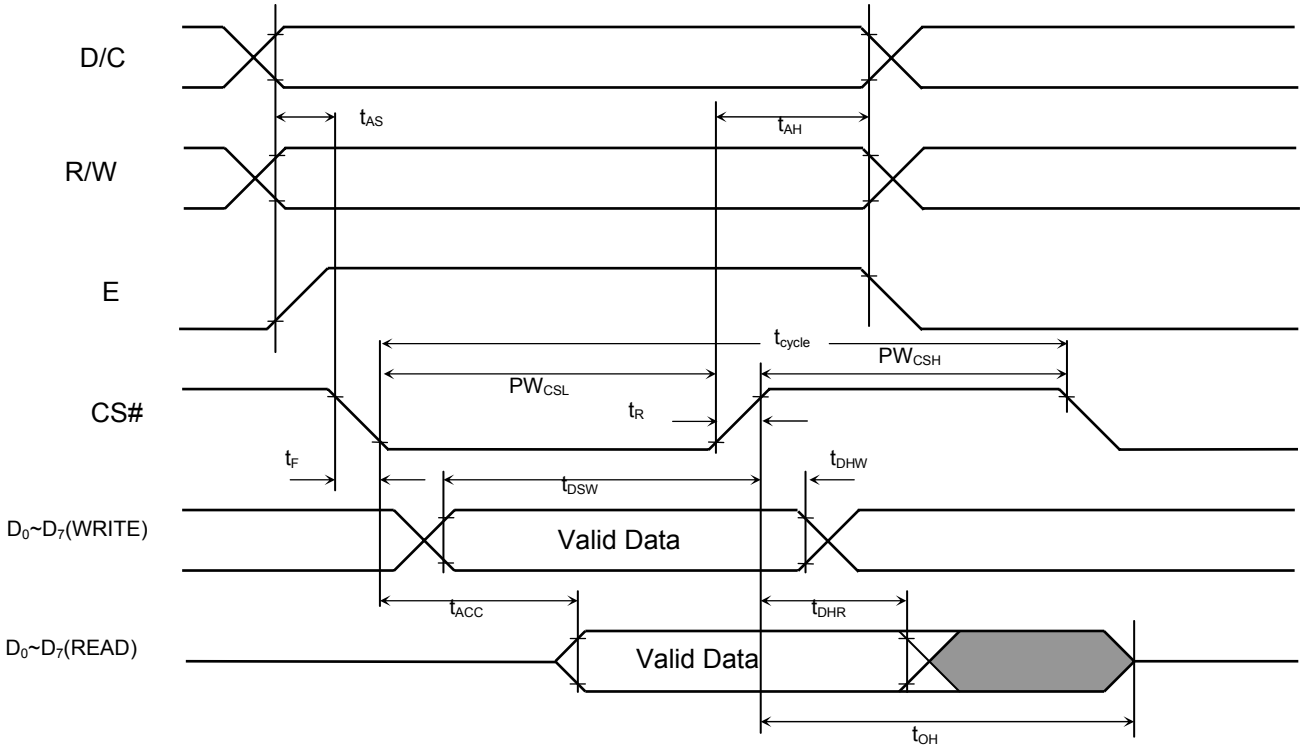


Figure 16 - 6800-series MPU parallel interface characteristics

Table 11 - 8080-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	150 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

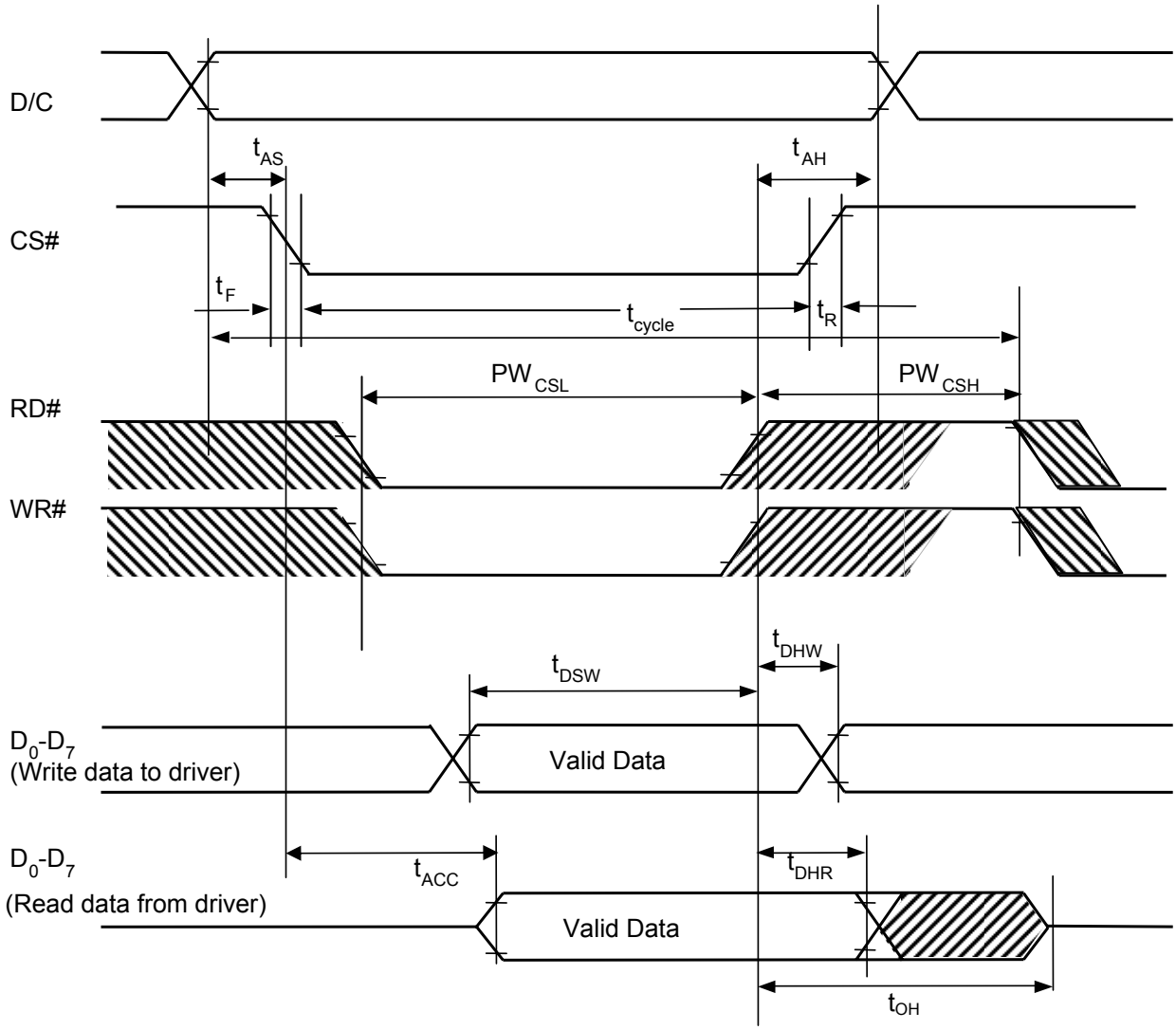


Figure 17 - 8080-series MPU parallel interface characteristics

Table 12 - Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

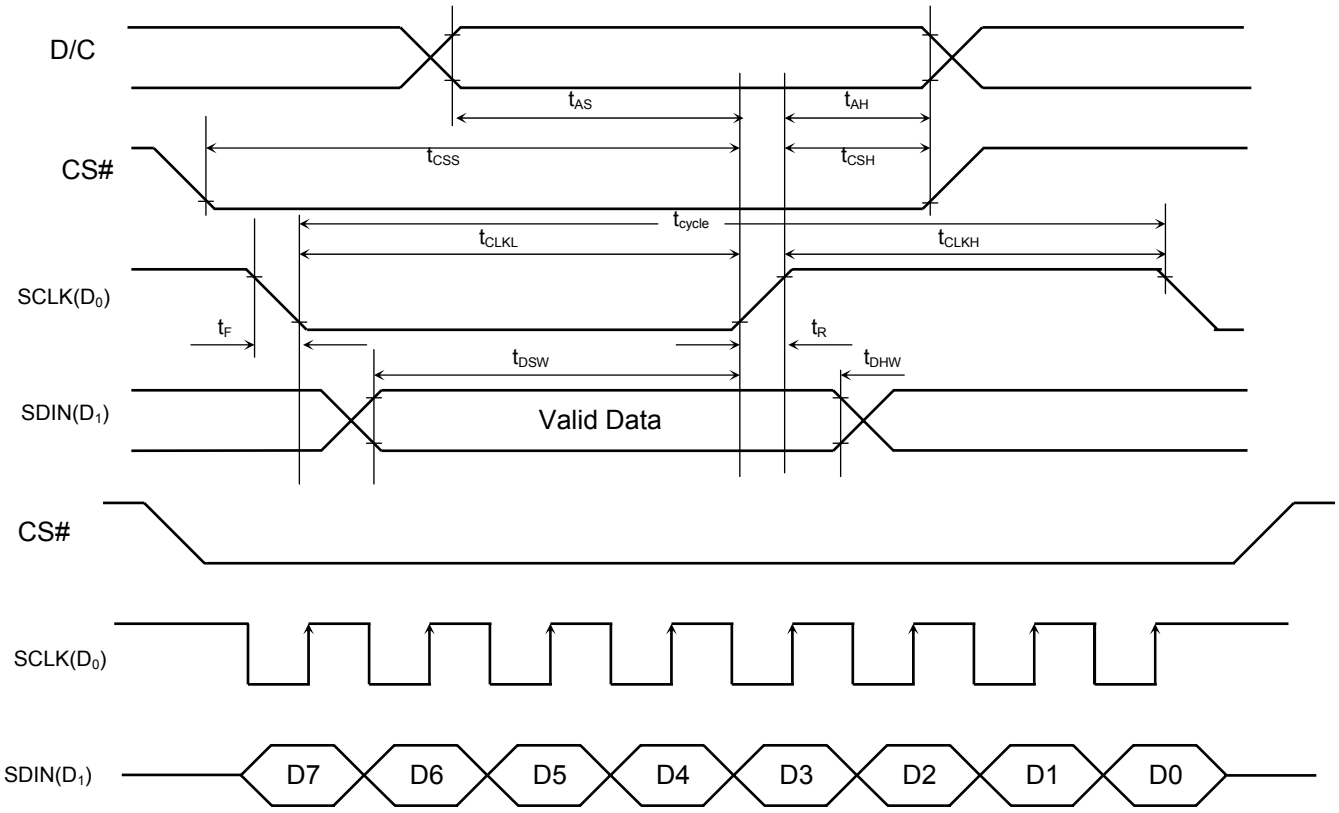


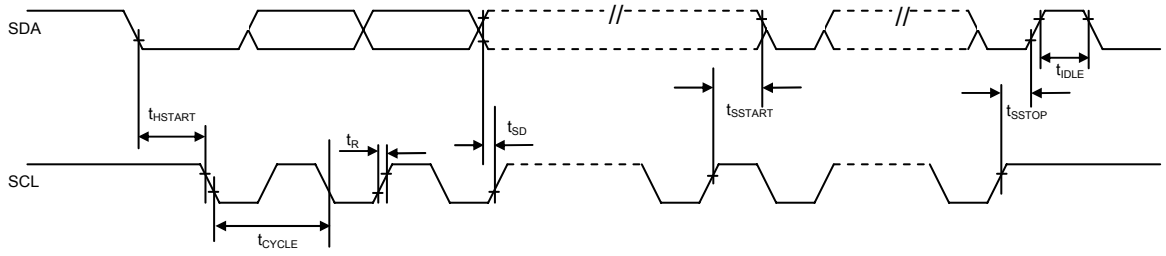
Figure 18 - Serial interface characteristics

Table 13 - I^2C Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

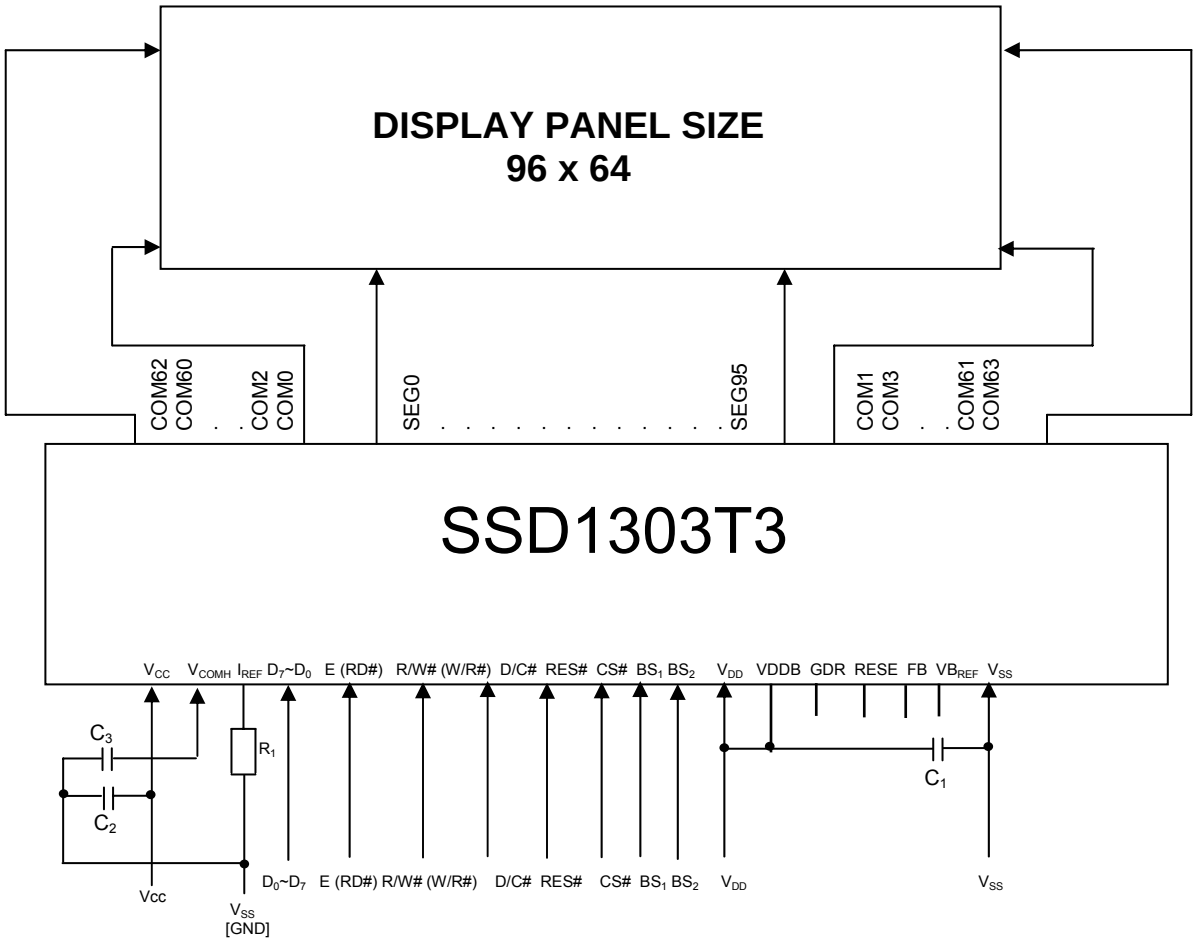
Figure 19 - I^2C Interface Timing Characteristics



13 APPLICATION EXAMPLE

Figure 20 - Application Example (Block Diagram of SSD1303T3)

The configuration for 6800-parallel interface mode, external V_{CC} is shown in the following diagram:
(V_{DD}=2.7V, V_{CC}=V_{REF}=12V, I_{REF}=10uA)



Pin connected to MCU interface: D0~D7, E, R/W#, D/C#, CS#, RES#
Pin externally connected to VSS: BS0, VSSB
Pin internally connected to VCC: VREF
GDR, RESE, VB_{REF}, FB should be left open individually;
C_1 : 4.7uF [(1)]
C_2 : 4.7uF [(1)]
C_3 : 4.7uF [(1)]
R1: 910kΩ, R_1= (Voltage at I_{REF} pin-VSS)/I_{REF}
Voltage at I_{REF} pin = V_{CC} -3V

Note
[(1)] The capacitor value is recommended value. Select appropriate value against module application.

14 SSD1303T3R1 PACKAGE DETAILS

SSD1303T3R1 Pin Assignment

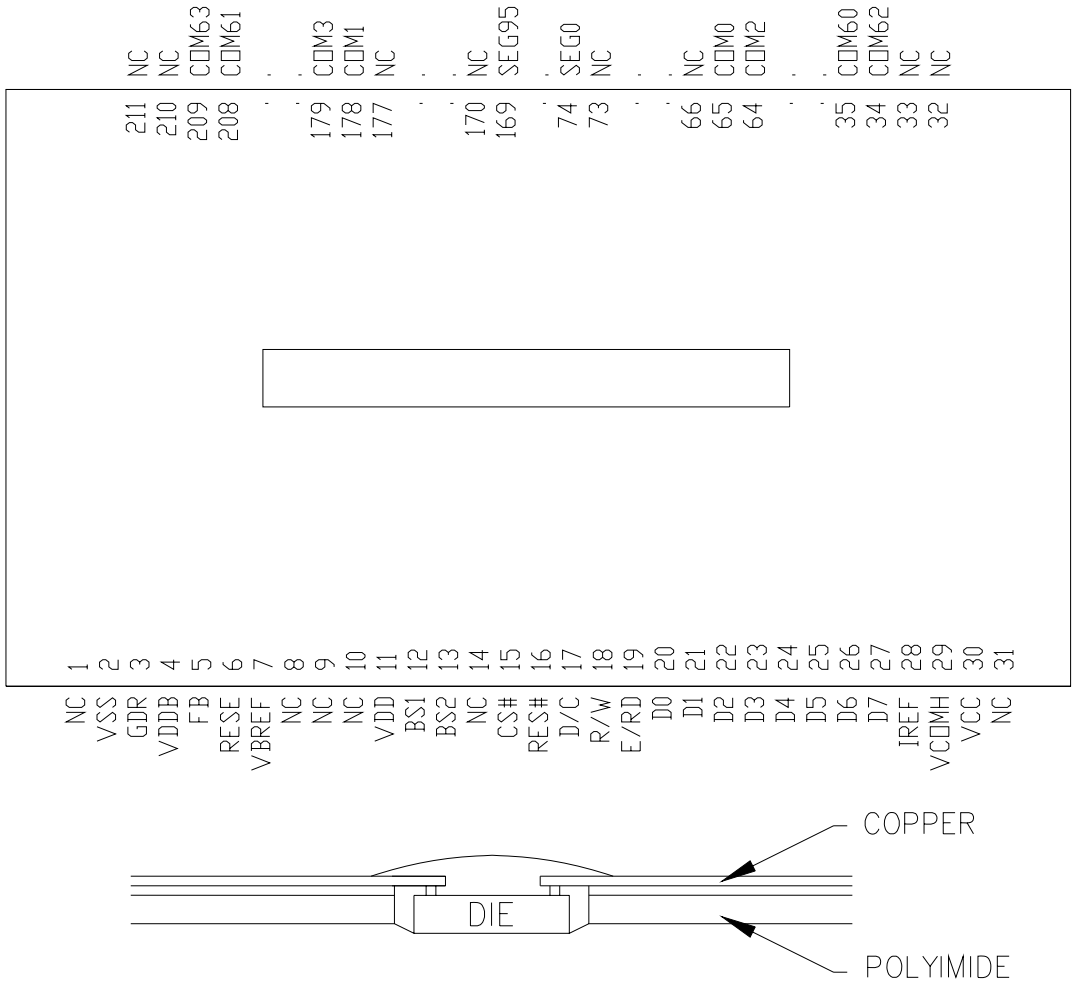


Figure 21 - SSD1303T3R1 pin assignment (Copper view, Normal TAB design)

Remark:
Use internal clock
VREF is connected to VCC
Support MCU interface: 8-bit 6800/8080 parallel interface and SPI
VSSB, BGGND are connected to VSS
BS0 is connected to VSS

Table 14 - SSD1303T3R1 pin assignment

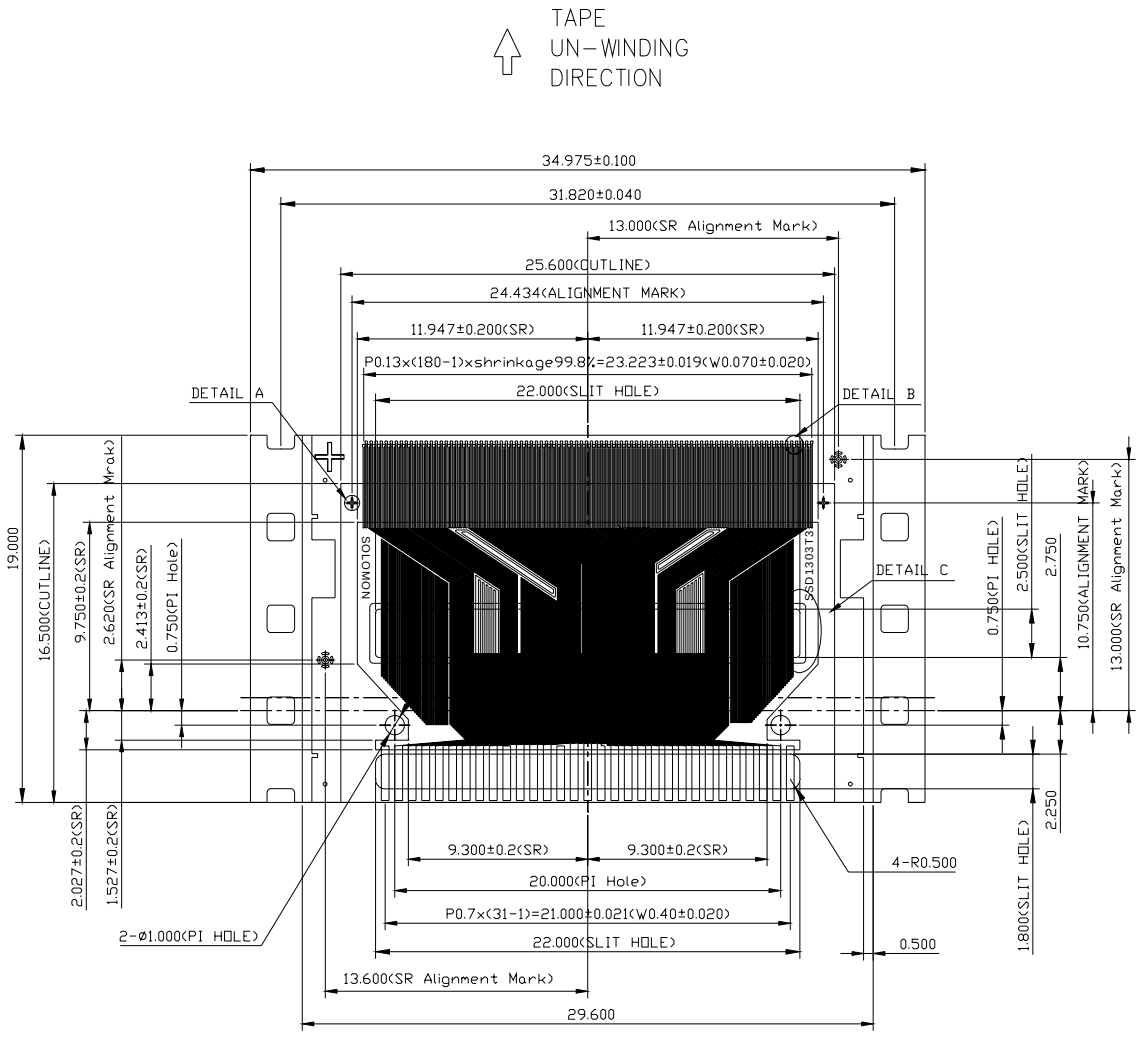
Pin no.	Pin name
1	NC
2	VSS
3	GDR
4	VDDB
5	FB
6	RESE
7	VBREF
8	GP0
9	GP1
10	NC
11	VDD1
12	BS1
13	BS2
14	NC
15	CS#
16	RES#
17	D/C
18	R/W
19	E/RD
20	D0
21	D1
22	D2
23	D3
24	D4
25	D5
26	D6
27	D7
28	IREF
29	VCOMH
30	VCC
31	NC
32	NC
33	NC
34	COM62
35	COM60
36	COM58
37	COM56
38	COM54
39	COM52
40	COM50
41	COM48
42	COM46
43	COM44
44	COM42
45	COM40
46	COM38
47	COM36
48	COM34
49	COM32
50	COM30
51	COM28
52	COM26
53	COM24
54	COM22
55	COM20
56	COM18
57	COM16
58	COM14
59	COM12
60	COM10

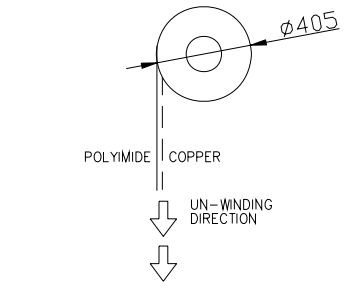
Pin no.	Pin name
61	COM8
62	COM6
63	COM4
64	COM2
65	COM0
66	NC
67	NC
68	NC
69	NC
70	NC
71	NC
72	NC
73	NC
74	SEG0
75	SEG1
76	SEG2
77	SEG3
78	SEG4
79	SEG5
80	SEG6
81	SEG7
82	SEG8
83	SEG9
84	SEG10
85	SEG11
86	SEG12
87	SEG13
88	SEG14
89	SEG15
90	SEG16
91	SEG17
92	SEG18
93	SEG19
94	SEG20
95	SEG21
96	SEG22
97	SEG23
98	SEG24
99	SEG25
100	SEG26
101	SEG27
102	SEG28
103	SEG29
104	SEG30
105	SEG31
106	SEG32
107	SEG33
108	SEG34
109	SEG35
110	SEG36
111	SEG37
112	SEG38
113	SEG39
114	SEG40
115	SEG41
116	SEG42
117	SEG43
118	SEG44
119	SEG45
120	SEG46

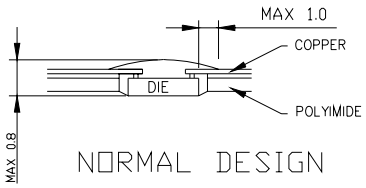
Pin no.	Pin name
121	SEG47
122	SEG48
123	SEG49
124	SEG50
125	SEG51
126	SEG52
127	SEG53
128	SEG54
129	SEG55
130	SEG56
131	SEG57
132	SEG58
133	SEG59
134	SEG60
135	SEG61
136	SEG62
137	SEG63
138	SEG64
139	SEG65
140	SEG66
141	SEG67
142	SEG68
143	SEG69
144	SEG70
145	SEG71
146	SEG72
147	SEG73
148	SEG74
149	SEG75
150	SEG76
151	SEG77
152	SEG78
153	SEG79
154	SEG80
155	SEG81
156	SEG82
157	SEG83
158	SEG84
159	SEG85
160	SEG86
161	SEG87
162	SEG88
163	SEG89
164	SEG90
165	SEG91
166	SEG92
167	SEG93
168	SEG94
169	SEG95
170	NC
171	NC
172	NC
173	NC
174	NC
175	NC
176	NC
177	NC
178	COM1
179	COM3
180	COM5

Pin no.	Pin name
181	COM7
182	COM9
183	COM11
184	COM13
185	COM15
186	COM17
187	COM19
188	COM21
189	COM23
190	COM25
191	COM27
192	COM29
193	COM31
194	COM33
195	COM35
196	COM37
197	COM39
198	COM41
199	COM43
200	COM45
201	COM47
202	COM49
203	COM51
204	COM53
205	COM55
206	COM57
207	COM59
208	COM61
209	COM63
210	NC
211	NC

SSD1303T3R1 TAB PACKAGE DIMENSIONS

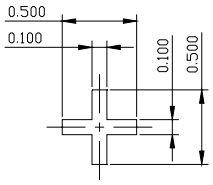




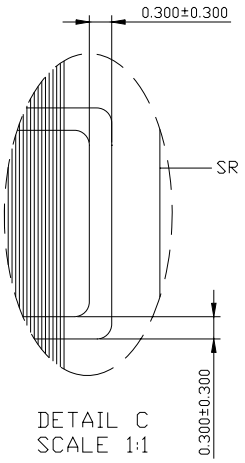


NORMAL DESIGN

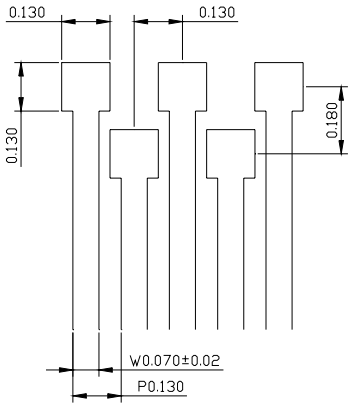
NOTE:
1. GENERAL TOLERANCE: ±0.05MM
2. MATERIAL
   PI: 75±6um
   CU: 18um
   SR: 26±14um
3. SN PLATING: 0.200±0.05um
4. TAPESITE: 4 SPH,19mm



DETAIL A
SCALE 2:1



DETAIL C
SCALE 1:1

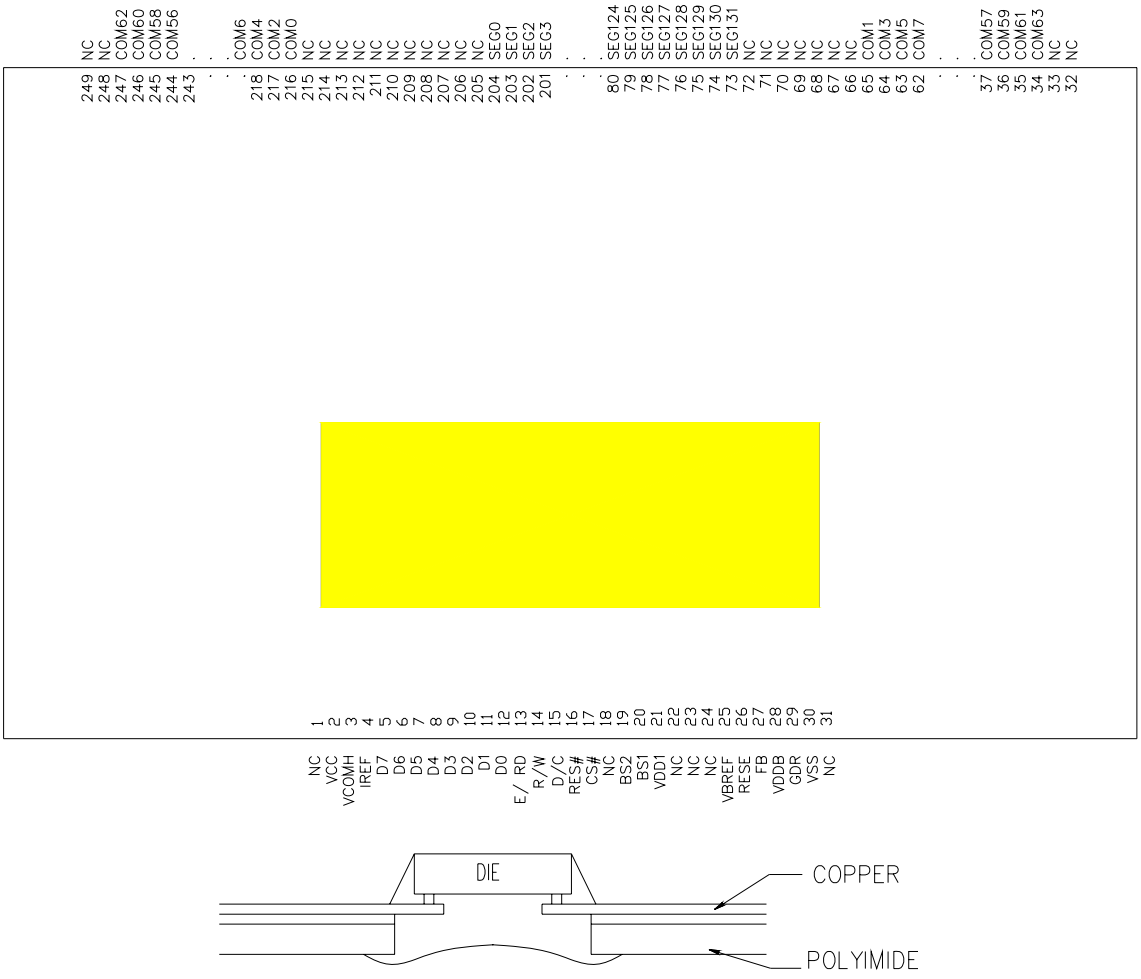


DETAIL B
SCALE 5:1

15 SSD1303T6R1 PACKAGE DETAILS

SSD1303T6R1 Pin Assignment

Figure 22 - SSD1303T6R1 pin assignment (Copper view)

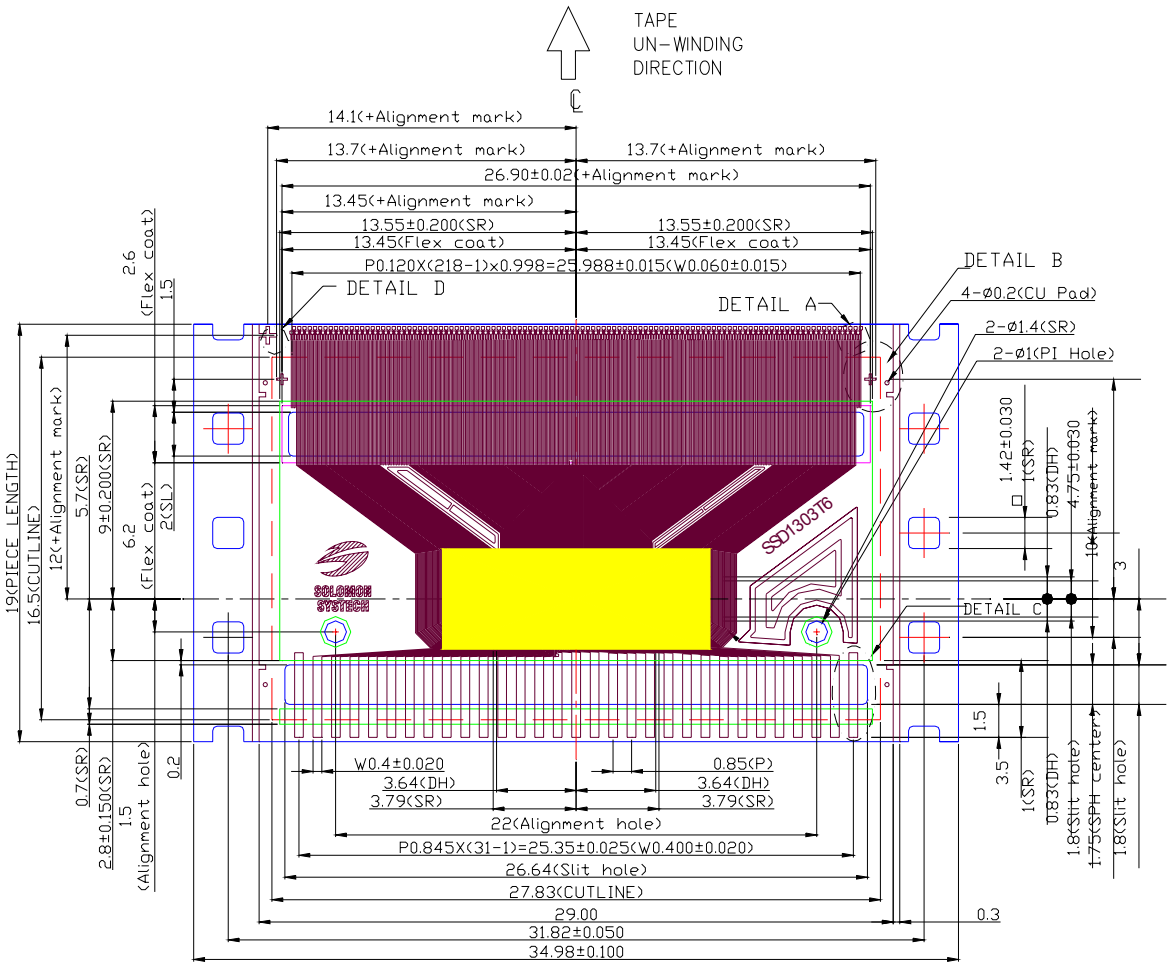


Remark:
Use internal clock
VREF is connected to VCC
Support MCU interface: 8-bit 6800/8080 parallel interface and SPI
VSSB, BGGND are connected to VSS
BS0 is connected to VSS

Table 15 - SSD1303T6R1 pin assignment

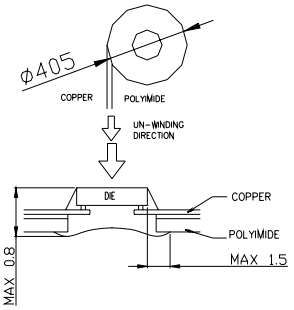
Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
1	NC	61	COM9	121	SEG83	181	SEG23	241	COM50
2	VCC	62	COM7	122	SEG82	182	SEG22	242	COM52
3	VCOMH	63	COM5	123	SEG81	183	SEG21	243	COM54
4	IREF	64	COM3	124	SEG80	184	SEG20	244	COM56
5	D7	65	COM1	125	SEG79	185	SEG19	245	COM58
6	D6	66	NC	126	SEG78	186	SEG18	246	COM60
7	D5	67	NC	127	SEG77	187	SEG17	247	COM62
8	D4	68	NC	128	SEG76	188	SEG16	248	NC
9	D3	69	NC	129	SEG75	189	SEG15	249	NC
10	D2	70	NC	130	SEG74	190	SEG14		
11	D1	71	NC	131	SEG73	191	SEG13		
12	D0	72	NC	132	SEG72	192	SEG12		
13	E/RD	73	SEG131	133	SEG71	193	SEG11		
14	R/W	74	SEG130	134	SEG70	194	SEG10		
15	D/C	75	SEG129	135	SEG69	195	SEG9		
16	RES#	76	SEG128	136	SEG68	196	SEG8		
17	CS#	77	SEG127	137	SEG67	197	SEG7		
18	NC	78	SEG126	138	SEG66	198	SEG6		
19	BS2	79	SEG125	139	SEG65	199	SEG5		
20	BS1	80	SEG124	140	SEG64	200	SEG4		
21	VDD	81	SEG123	141	SEG63	201	SEG3		
22	NC	82	SEG122	142	SEG62	202	SEG2		
23	NC	83	SEG121	143	SEG61	203	SEG1		
24	NC	84	SEG120	144	SEG60	204	SEG0		
25	VBREF	85	SEG119	145	SEG59	205	NC		
26	RESE	86	SEG118	146	SEG58	206	NC		
27	FB	87	SEG117	147	SEG57	207	NC		
28	VDDB	88	SEG116	148	SEG56	208	NC		
29	GDR	89	SEG115	149	SEG55	209	NC		
30	VSS	90	SEG114	150	SEG54	210	NC		
31	NC	91	SEG113	151	SEG53	211	NC		
32	NC	92	SEG112	152	SEG52	212	NC		
33	NC	93	SEG111	153	SEG51	213	NC		
34	COM63	94	SEG110	154	SEG50	214	NC		
35	COM61	95	SEG109	155	SEG49	215	NC		
36	COM59	96	SEG108	156	SEG48	216	COM0		
37	COM57	97	SEG107	157	SEG47	217	COM2		
38	COM55	98	SEG106	158	SEG46	218	COM4		
39	COM53	99	SEG105	159	SEG45	219	COM6		
40	COM51	100	SEG104	160	SEG44	220	COM8		
41	COM49	101	SEG103	161	SEG43	221	COM10		
42	COM47	102	SEG102	162	SEG42	222	COM12		
43	COM45	103	SEG101	163	SEG41	223	COM14		
44	COM43	104	SEG100	164	SEG40	224	COM16		
45	COM41	105	SEG99	165	SEG39	225	COM18		
46	COM39	106	SEG98	166	SEG38	226	COM20		
47	COM37	107	SEG97	167	SEG37	227	COM22		
48	COM35	108	SEG96	168	SEG36	228	COM24		
49	COM33	109	SEG95	169	SEG35	229	COM26		
50	COM31	110	SEG94	170	SEG34	230	COM28		
51	COM29	111	SEG93	171	SEG33	231	COM30		
52	COM27	112	SEG92	172	SEG32	232	COM32		
53	COM25	113	SEG91	173	SEG31	233	COM34		
54	COM23	114	SEG90	174	SEG30	234	COM36		
55	COM21	115	SEG89	175	SEG29	235	COM38		
56	COM19	116	SEG88	176	SEG28	236	COM40		
57	COM17	117	SEG87	177	SEG27	237	COM42		
58	COM15	118	SEG86	178	SEG26	238	COM44		
59	COM13	119	SEG85	179	SEG25	239	COM46		
60	COM11	120	SEG84	180	SEG24	240	COM48		

SSD1303T6R1 TAB Package Dimensions

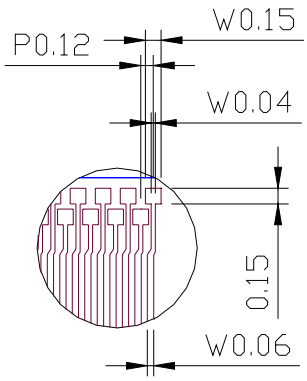


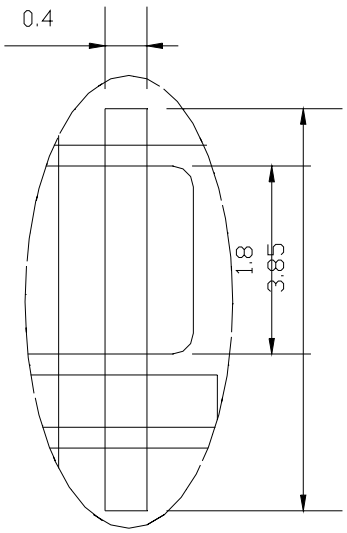
NOTE:

1. GENERAL TOLERANCE: ±0.05MM
2. MATERIAL
   PI: UPILEX-S 75±6um
   ADHESIVE:12±2um
   CU: 18um
   SR: 26±14um
   TOLERANCE±0.200
3. SN PLATING: 0.200±0.05um
4. TAPESITE: 4 SPH,19mm

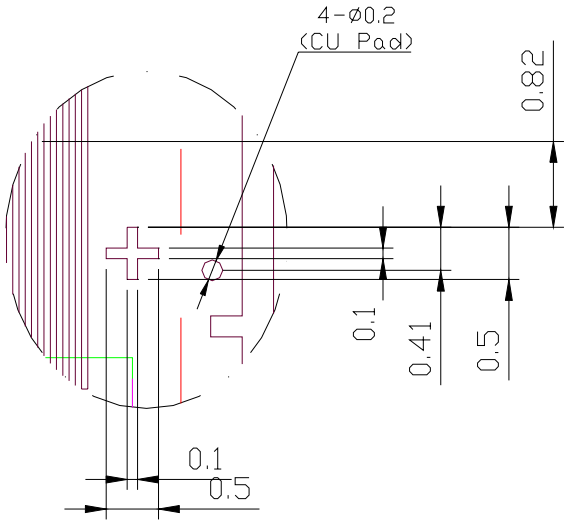


MIRROR DESIGN

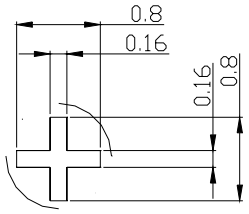




DETAIL C



DETAIL B



DETAIL D

16 SSD1303T10R1 PACKAGE DETAILS

SSD1303T10R1 Pin Assignment

Figure 23 - SSD1303T10R1 pin assignment

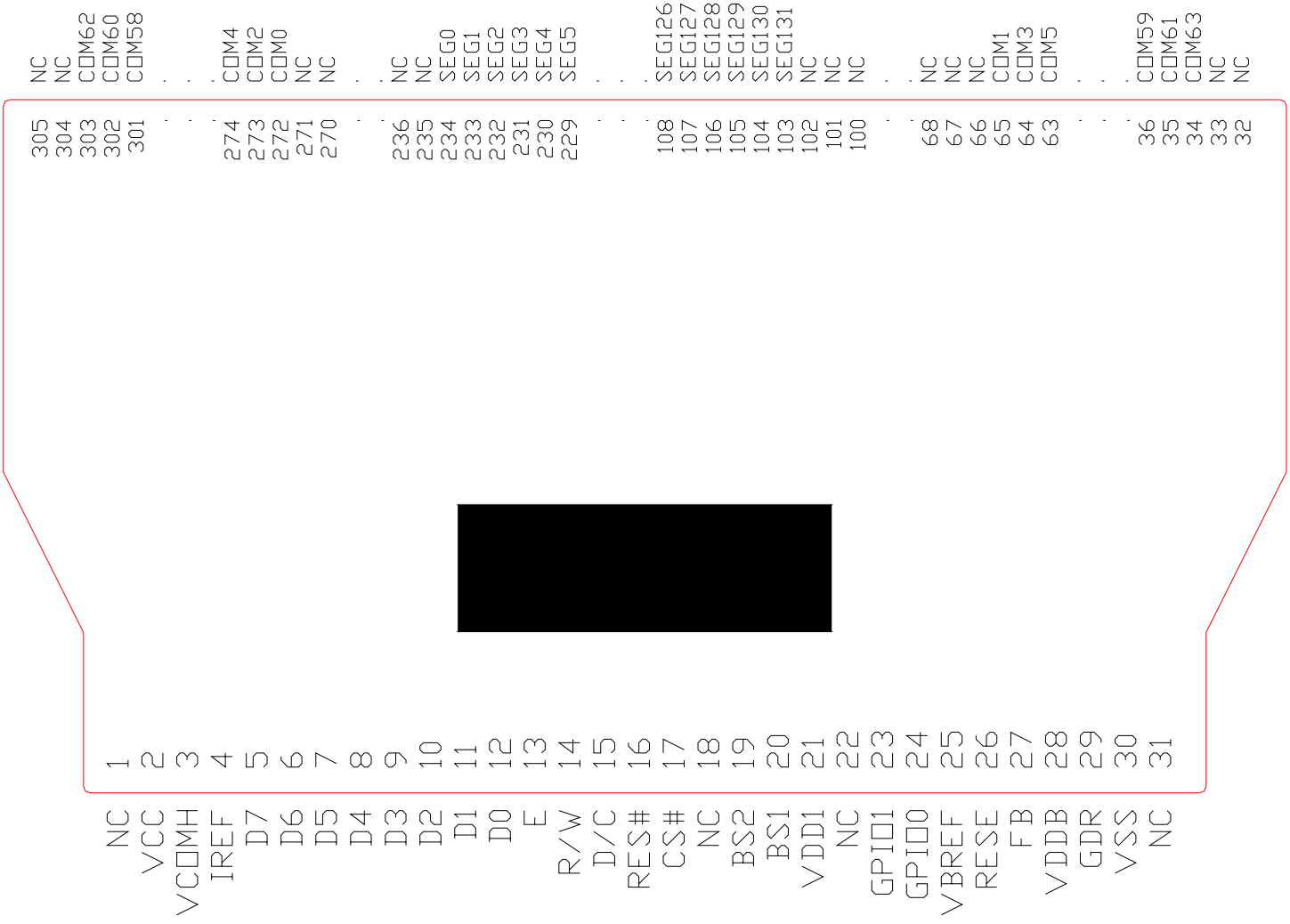


Table 16 : SSD1303T10R1 pin assignment

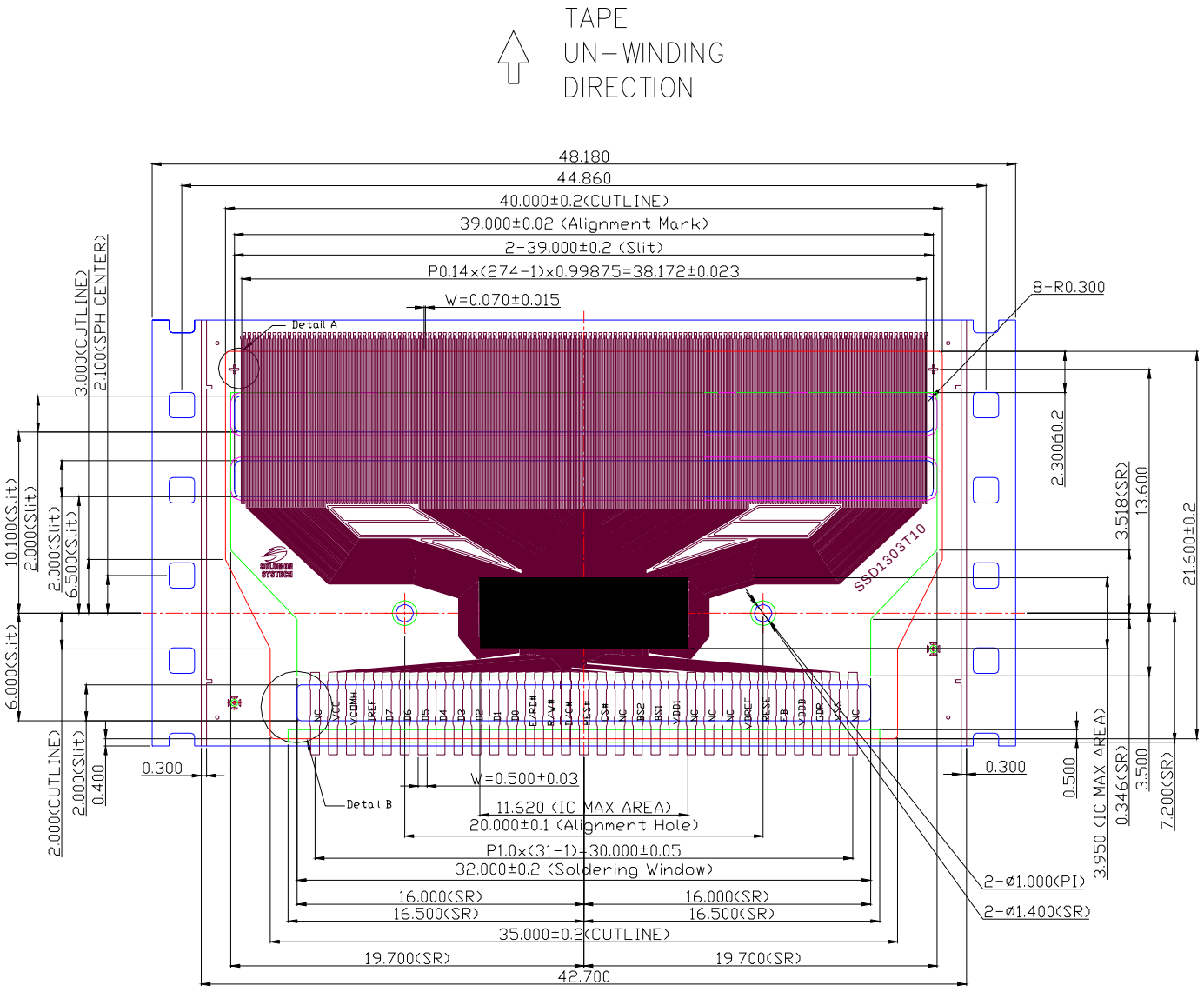
Pin no	Pin name
1	NC
2	VCC
3	VCOMH
4	IREF
5	D7
6	D6
7	D5
8	D4
9	D3
10	D2
11	D1
12	D0
13	E/RD
14	R/W
15	D/C
16	RES#
17	CS#
18	NC
19	BS2
20	BS1
21	VDD
22	NC
23	NC
24	NC
25	VBREF
26	RESE
27	FB
28	VDDB
29	GDR
30	VSS
31	NC
32	GPIO1
33	GPIO0
34	COM63
35	COM61
36	COM59
37	COM57
38	COM55
39	COM53
40	COM51
41	COM49
42	COM47
43	COM45
44	COM43
45	COM41
46	COM39
47	COM37
48	COM35
49	COM33
50	COM31
51	COM29
52	COM27
53	COM25
54	COM23
55	COM21
56	COM19
57	COM17
58	COM15
59	COM13
60	COM11
61	COM9
62	COM7
63	COM5
64	COM3
65	COM1
66	NC
67	NC
68	NC
69	NC
70	NC
71	NC
72	NC
73	NC
74	NC
75	NC
76	NC
77	NC
78	NC
79	NC
80	NC

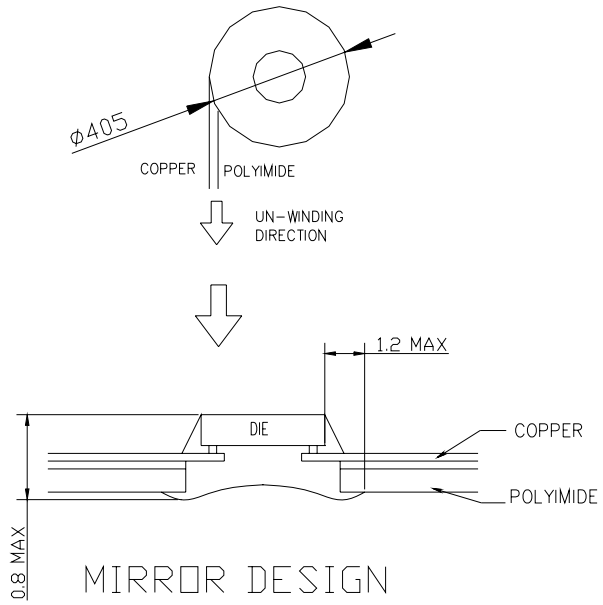
Pin no	Pin name
81	NC
82	NC
83	NC
84	NC
85	NC
86	NC
87	NC
88	NC
89	NC
90	NC
91	NC
92	NC
93	NC
94	NC
95	NC
96	NC
97	NC
98	NC
99	NC
100	NC
101	NC
102	NC
103	SEG131
104	SEG130
105	SEG129
106	SEG128
107	SEG127
108	SEG126
109	SEG125
110	SEG124
111	SEG123
112	SEG122
113	SEG121
114	SEG120
115	SEG119
116	SEG118
117	SEG117
118	SEG116
119	SEG115
120	SEG114
121	SEG113
122	SEG112
123	SEG111
124	SEG110
125	SEG109
126	SEG108
127	SEG107
128	SEG106
129	SEG105
130	SEG104
131	SEG103
132	SEG102
133	SEG101
134	SEG100
135	SEG99
136	SEG98
137	SEG97
138	SEG96
139	SEG95
140	SEG94
141	SEG93
142	SEG92
143	SEG91
144	SEG90
145	SEG89
146	SEG88
147	SEG87
148	SEG86
149	SEG85
150	SEG84
151	SEG83
152	SEG82
153	SEG81
154	SEG80
155	SEG79
156	SEG78
157	SEG77
158	SEG76
159	SEG75
160	SEG74

Pin no	Pin name
161	SEG73
162	SEG72
163	SEG71
164	SEG70
165	SEG69
166	SEG68
167	SEG67
168	SEG66
169	SEG65
170	SEG64
171	SEG63
172	SEG62
173	SEG61
174	SEG60
175	SEG59
176	SEG58
177	SEG57
178	SEG56
179	SEG55
180	SEG54
181	SEG53
182	SEG52
183	SEG51
184	SEG50
185	SEG49
186	SEG48
187	SEG47
188	SEG46
189	SEG45
190	SEG44
191	SEG43
192	SEG42
193	SEG41
194	SEG40
195	SEG39
196	SEG38
197	SEG37
198	SEG36
199	SEG35
200	SEG34
201	SEG33
202	SEG32
203	SEG31
204	SEG30
205	SEG29
206	SEG28
207	SEG27
208	SEG26
209	SEG25
210	SEG24
211	SEG23
212	SEG22
213	SEG21
214	SEG20
215	SEG19
216	SEG18
217	SEG17
218	SEG16
219	SEG15
220	SEG14
221	SEG13
222	SEG12
223	SEG11
224	SEG10
225	SEG9
226	SEG8
227	SEG7
228	SEG6
229	SEG5
230	SEG4
231	SEG3
232	SEG2
233	SEG1
234	SEG0
235	NC
236	NC
237	NC
238	NC
239	NC
240	NC

Pin no	Pin name
241	NC
242	NC
243	NC
244	NC
245	NC
246	NC
247	NC
248	NC
249	NC
250	NC
251	NC
252	NC
253	NC
254	NC
255	NC
256	NC
257	NC
258	NC
259	NC
260	NC
261	NC
262	NC
263	NC
264	NC
265	NC
266	NC
267	NC
268	NC
269	NC
270	NC
271	NC
272	COM0
273	COM2
274	COM4
275	COM6
276	COM8
277	COM10
278	COM12
279	COM14
280	COM16
281	COM18
282	COM20
283	COM22
284	COM24
285	COM26
286	COM28
287	COM30
288	COM32
289	COM34
290	COM36
291	COM38
292	COM40
293	COM42
294	COM44
295	COM46
296	COM48
297	COM50
298	COM52
299	COM54
300	COM56
301	COM58
302	COM60
303	COM62
304	NC
305	NC

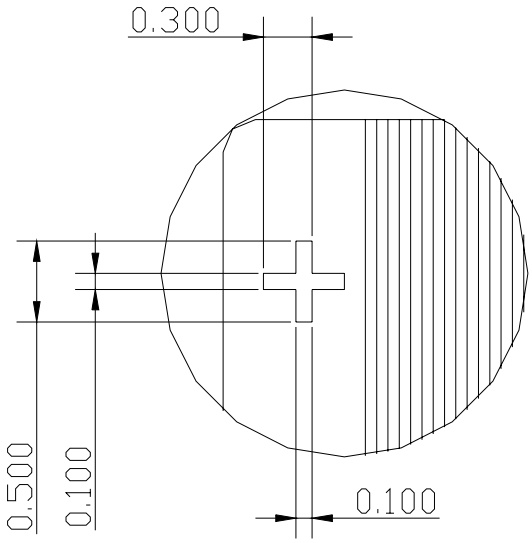
SSD1303T10R1 TAB Package Dimensions



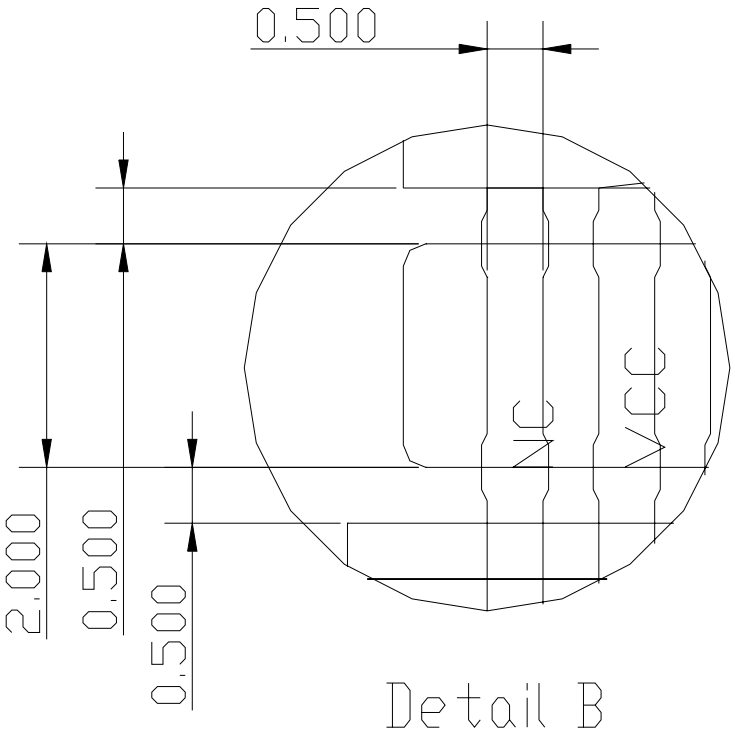


MIRROR DESIGN

1. GENERAL TOLERANCE: ±0.05MM
2. MATERIAL
   PI: 75±6um
   CU: 18±5um
   SR: 26±14 um
   TOLERANCE±0.200
   FC: MIN10um
   ADHESIVE: 12±2um
3. SN PLATING: 0.200±0.05um



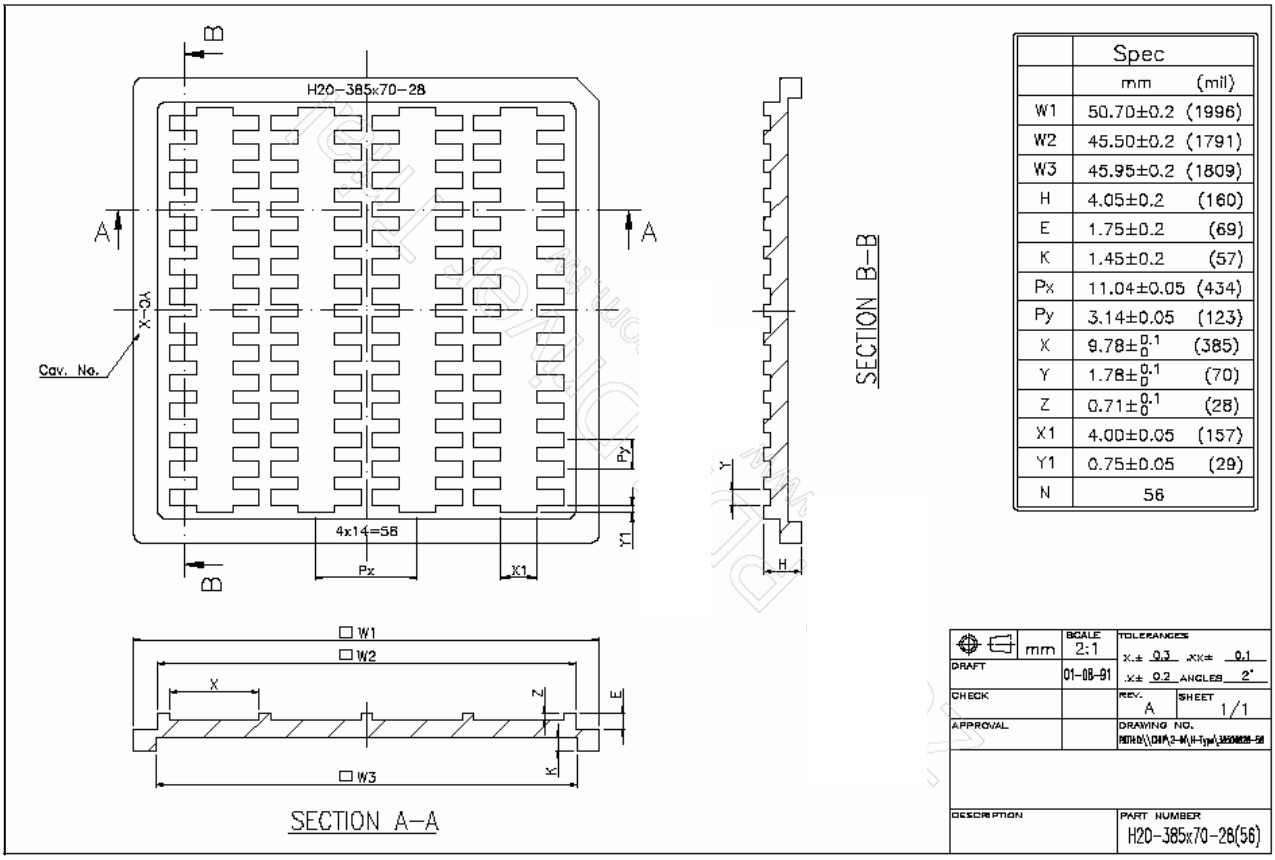
Detail A
Tolerance : ±0.02mm



Detail B

17 SSD1303Z PACKAGE DETAILS

DIE TRAY DIMENSIONS



	Spec	
	mm	(mil)
W1	50.70±0.2	(1996)
W2	45.50±0.2	(1791)
W3	45.95±0.2	(1809)
H	4.05±0.2	(160)
E	1.75±0.2	(69)
K	1.45±0.2	(57)
Px	11.04±0.05	(434)
Py	3.14±0.05	(123)
X	$9.78^{0}_{-0.1}$	(385)
Y	$1.78^{0}_{-0.1}$	(70)
Z	$0.71^{0}_{-0.1}$	(28)
X1	4.00±0.05	(157)
Y1	0.75±0.05	(29)
N	56	

All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) “Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)” and China standard “电子信息产品污染控制标识要求 (SJ/T11364-2006)” with control Marking Symbol  . Hazardous Substances test report is available upon requested.

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