DATA SHEET

TDA5051A
Home automation modem

Product specification
Supersedes data of 1997 Sep 19
File under Integrated Circuits, IC11

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Philips
Semiconductors

PHILIPS

FEATURES

- Full digital carrier generation and shaping
- Modulation/demodulation frequency set by clock adjustment, from microcontroller or on-chip oscillator
- High clock rate of 6-bit A/D (Digital to Analog) converter for rejection of aliasing components
- Fully integrated output power stage with overload protection
- Automatic Gain Control (AGC) at receiver input
- 8-bit A/D (Analog to Analog) converter and narrow digital filtering
- Digital demodulation delivering baseband data
- Easy compliance with EN50065-1 with simple coupling network
- Few external components for low cost applications
- SO16 plastic package.

APPLICATIONS

- Home appliance control (air conditioning, shutters, lighting, alarms and so on)
- Energy/heating control
- Amplitude Shift Keying (ASK) data transmission using the home power network.

GENERAL DESCRIPTION

The TDA5051A is a modem IC, specifically dedicated to ASK transmission by means of the home power supply network, at 600 or 1200 baud data rate. It operates from a single 5 V supply.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.75	5.0	5.25	V
$I_{DD(tot)}$	total supply current	f_{osc} = 8.48 MHz				
	reception mode		–	28	38	mA
	transmission mode ($\overline{DATA}_{IN}$ = 0)	Z_L = 30 Ω	–	47	68	mA
	power-down mode		–	19	25	mA
f_{cr}	carrier frequency	note 1	95	132.5	148.5	kHz
f_{osc}	oscillator frequency		6.08	8.48	9.504	MHz
$V_{o(rms)}$	output carrier signal on CISPR16 load (RMS value)		120	–	122	dBμV
$V_{i(rms)}$	input signal (RMS value)	note 2	82	–	122	dBμV
THD	total harmonic distortion on CISPR16 load with coupling network		–	–55	–	dB
Z_L	load impedance		1	30	–	Ω
BR	baud rate		–	600	1200	bits/s
T_{amb}	ambient temperature		0	–	70	°C

Notes

1. Frequency range corresponding to the EN50065-1 band. However, the modem can operate at any lower oscillator frequency.
2. The minimum value can be improved by using an external amplifier, see application diagrams Figs 22 and 23.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5051AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

BLOCK DIAGRAM

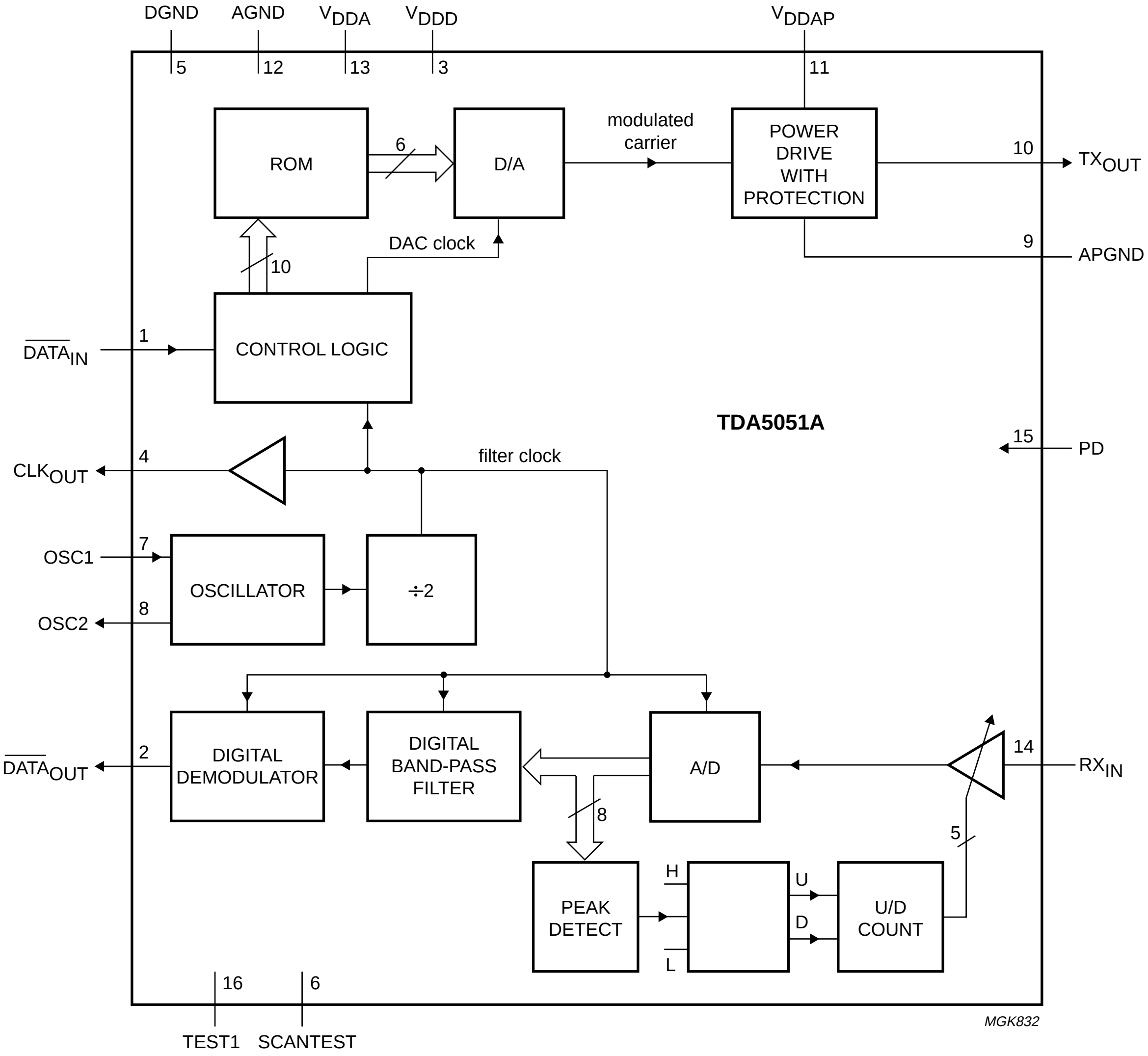


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{\text{DATA}}_{\text{IN}}$	1	digital data input (active LOW)
$\overline{\text{DATA}}_{\text{OUT}}$	2	digital data output (active LOW)
V_{DDD}	3	digital supply voltage
CLK_{OUT}	4	clock output
DGND	5	digital ground
SCANTEST	6	test input (LOW in application)
OSC1	7	oscillator input
OSC2	8	oscillator output
APGND	9	analog ground for power amplifier
TX_{OUT}	10	analog signal output
V_{DDAP}	11	analog supply voltage for power amplifier
AGND	12	analog ground
V_{DDA}	13	analog supply voltage
RX_{IN}	14	analog signal input
PD	15	power-down input (active HIGH)
TEST1	16	test input (HIGH in application)

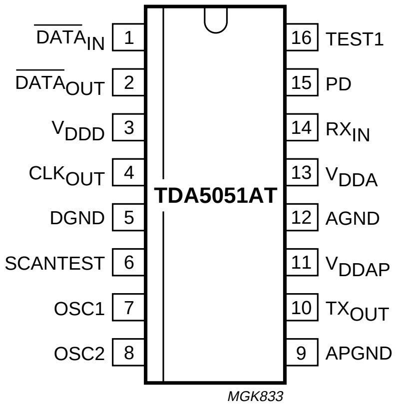


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Both transmission and reception stages are controlled either by the master clock of the microcontroller or by the on-chip reference oscillator connected to a crystal. This ensures the accuracy of the transmission carrier and the exact trimming of the digital filter, thus making the performance totally independent of application disturbances such as component spread, temperature, supply drift and so on.

The interface with the power network is made by means of an LC network (see Fig.18). The device includes a power output stage that feeds a 120 dBμV (RMS) signal on a typical 30 Ω load.

To reduce power consumption, the IC is disabled by a power-down input (pin PD): in this mode, the on-chip oscillator remains active and the clock continues to be supplied at pin CLK_{OUT}. For low-power operation in reception mode, this pin can be dynamically controlled by the microcontroller, see Section “Power-down mode”.

When the circuit is connected to an external clock generator (see Fig.6), the clock signal must be applied at pin OSC1 (pin 7); OSC2 (pin 8) must be left open-circuit. Fig.7 shows the use of the on-chip clock circuit.

All logic inputs and outputs are compatible with TTL/CMOS levels, providing an easy connection to a standard microcontroller I/O port.

The digital part of the IC is fully scan-testable. Two digital inputs, SCANTEST and TEST1, are used for production test: these pins must be left open-circuit in functional mode (correct levels are internally defined by pull-up or pull-down resistors).

Transmission mode

To provide strict stability with respect to environmental conditions, the carrier frequency is generated by scanning the ROM memory under the control of the microcontroller clock or the reference frequency provided by the on-chip oscillator. High frequency clocking rejects the aliasing components to such an extent that they are filtered by the coupling LC network and do not cause any significant disturbance. The data modulation is applied through pin $\overline{\text{DATA}}_{\text{IN}}$ and smoothly applied by specific digital circuits to the carrier (shaping). Harmonic components are limited in this process, thus avoiding unacceptable disturbance of the transmission channel (according to CISPR16 and EN50065-1 recommendations). A –55 dB Total Harmonic Distortion (TDH) is reached when the typical LC coupling network (or an equivalent filter) is used.

The DAC and the power stage are set in order to provide a maximum signal level of 122 dBμV (RMS) at the output.

The output of the power stage (TX_{OUT}) must **always** be connected to a decoupling capacitor, because of a DC level of $0.5V_{DD}$ at this pin, which is present even when the device is not transmitting. This pin must also be **protected against overvoltage and negative transient signals**. The DC level of TX_{OUT} can be used to bias a unipolar transient suppressor, as shown in the application diagram; see Fig.18.

Direct connection to the mains is done through an LC network for low-cost applications. However, a HF signal transformer could be used when power-line insulation has to be performed.

CAUTION
In transmission mode, the receiving part of the circuit is **not disabled** and the detection of the transmitted signal is normally performed. In this mode, the gain chosen before the beginning of the transmission is stored, and the **AGC is internally set to –6 dB** as long as $\overline{DATA}_{IN}$ is LOW. Then, the old gain setting is **automatically restored**.

Reception mode

The input signal received by the modem is applied to a wide range input amplifier with AGC (–6 to +30 dB). This is basically for noise performance improvement and signal level adjustment, which ensures a maximum sensitivity of the ADC. An 8-bit conversion is then performed, followed by digital band-pass filtering, to meet the CISPR normalization and to comply with some additional limitations met in current applications.

After digital demodulation, the baseband data signal is made available after pulse shaping.

The signal pin (RX_{IN}) is a high-impedance input which has to be protected and DC decoupled for the same reasons as with pin TX_{OUT}. The high sensitivity (82 dBμV) of this input requires an efficient 50 Hz rejection filter (realized by the LC coupling network), which also acts as an anti-aliasing filter for the internal digital processing; see Fig.18.

Data format

TRANSMISSION MODE

The data input ($\overline{DATA}_{IN}$) is active LOW: this means that a burst is generated on the line (pin TX_{OUT}) when $\overline{DATA}_{IN}$ pin is LOW.

Pin TX_{OUT} is in a high-impedance state as long as the device is not transmitting. Successive logic 1s are treated in a Non-Return-to-Zero (NRZ) mode, see pulse shapes in Figs 8 and 9.

RECEPTION MODE

The data output (pin $\overline{DATA}_{OUT}$) is active LOW; this means that the data output is LOW when a burst is received. Pin $\overline{DATA}_{OUT}$ remains LOW as long as a burst is received.

Power-down mode

Power-down input (pin PD) is active HIGH; this means that the power consumption is minimum when pin PD is HIGH. Now, all functions are disabled, except clock generation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.5	V
f_{osc}	oscillator frequency	–	12	MHz
T_{stg}	storage temperature	–50	+150	°C
T_{amb}	ambient temperature	–10	+80	°C
T_j	junction temperature	–	125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

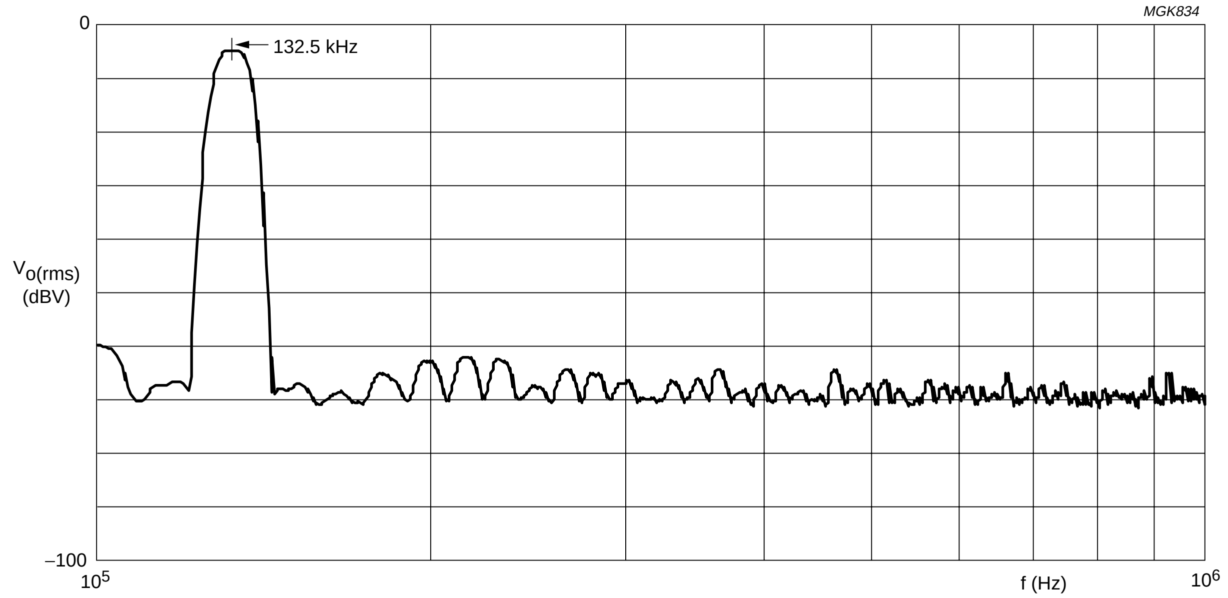
CHARACTERISTICS

$V_{DDD} = V_{DDA} = 5$ V ±5%; $T_{amb} = 0$ to 70 °C; V_{DDD} connected to V_{DDA}; DGND connected to AGND.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.75	5	5.25	V
$I_{DD(RX/TX)(tot)}$	total analog + digital supply current	$V_{DD} = 5$ V ±5% TX or RX mode	–	28	38	mA
$I_{DD(PD)(tot)}$	total analog + digital supply current;	$V_{DD} = 5$ V ±5%; PD = HIGH Power-down mode	–	19	25	mA
$I_{DD(PAMP)}$	power amplifier supply current	$V_{DD} = 5$ V ±5%; $Z_L = 30\ \Omega$; $\overline{DATA}_{IN}$ = LOW in transmission mode	–	19	30	mA
$I_{DD(PAMP)(max)}$	maximum power amplifier supply current	$V_{DD} = 5$ V ±5%; $Z_L = 1\ \Omega$; $\overline{DATA}_{IN}$ = LOW in transmission mode	–	76	–	mA
$\overline{DATA}_{IN}$ and PD inputs: $\overline{DATA}_{OUT}$ and CLK_{OUT} outputs						
V_{IH}	HIGH-level input voltage		$0.2V_{DD} + 0.9$	–	$V_{DD} + 0.5$	V
V_{IL}	LOW-level input voltage		–0.5	–	$0.2V_{DD} – 0.1$	V
V_{OH}	HIGH-level output voltage	$I_{OH} = –1.6$ mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	$I_{OL} = 1.6$ mA	–	–	0.45	V
OSC1 input and OSC2 output (OSC2 only used for driving external quartz crystal; must be left open-circuit when using an external clock generator)						
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.5$	V
V_{IL}	LOW-level input voltage		–0.5	–	$0.2V_{DD} – 0.1$	V
V_{OH}	HIGH-level output voltage	$I_{OH} = –1.6$ mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	$I_{OL} = 1.6$ mA	–	–	0.45	V
Clock						
f_{osc}	oscillator frequency		6.080	–	9.504	MHz
$\frac{f_{osc}}{f_{cr}}$	ratio between oscillator and carrier frequency		–	64	–	
$\frac{f_{osc}}{f_{CLKOUT}}$	ratio between oscillator and clock output frequency		–	2	–	
Transmission mode						
f_{cr}	carrier frequency	$f_{osc} = 8.48$ MHz	–	132.5	–	kHz
t_{su}	set-up time of the shaped burst	$f_{osc} = 8.48$ MHz; see Fig.8	–	170	–	µs
t_h	hold time of the shaped burst	$f_{osc} = 8.48$ MHz; see Fig.8	–	170	–	µs

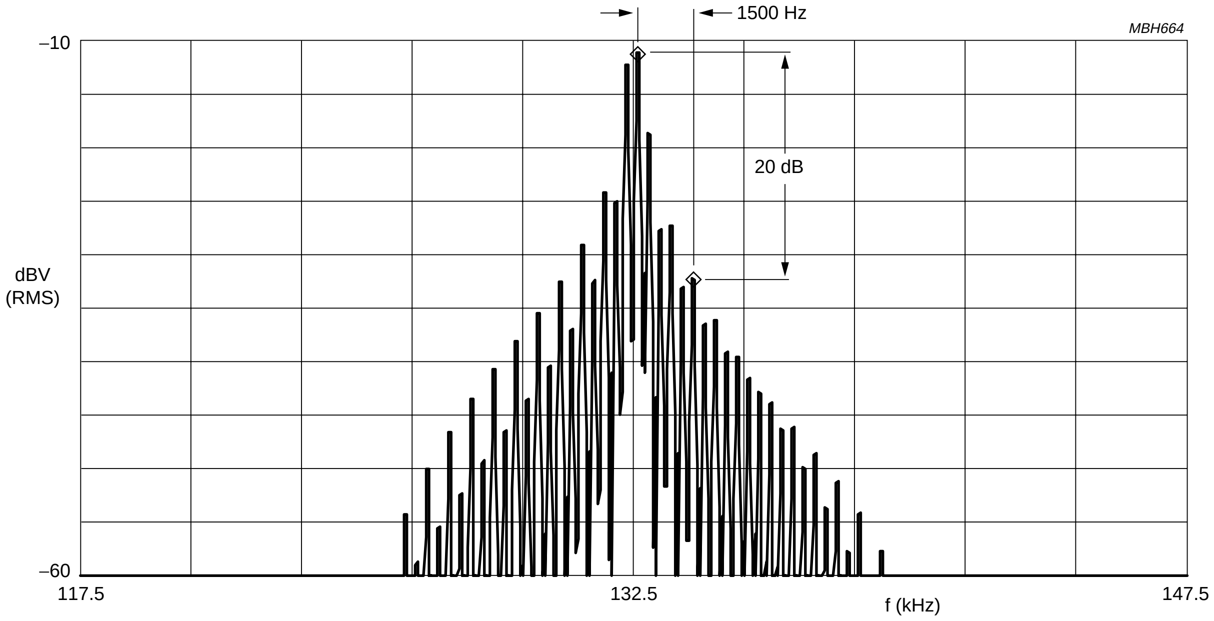
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{W(DI)(min)}$	minimum pulse width of $\overline{\text{DATA}}_{\text{IN}}$ signal	f_{osc} = 8.48 MHz; see Fig.8	–	190	–	µs
$V_{o(rms)}$	output carrier signal (RMS value)	Z_L = CISPR16; $\overline{\text{DATA}}_{\text{IN}}$ = LOW	120	–	122	dBµV
$I_{o(max)}$	power amplifier maximum output current (peak value)	Z_L = 1 Ω; $\overline{\text{DATA}}_{\text{IN}}$ = LOW	–	160	–	mA
Z_o	output impedance of the power amplifier		–	5	–	Ω
V_O	output DC level at pin TX_{OUT}		–	2.5	–	V
THD	total harmonic distortion on CISPR16 load with the coupling network (measured on the first ten harmonics)	$V_{o(rms)}$ = 121 dBµV on CISPR16 load; f_{osc} = 8.48 MHz; $\overline{\text{DATA}}_{\text{IN}}$ = LOW (no modulation); see Figs 3 and 16	–	–55	–	dB
B_{-20dB}	bandwidth of the shaped output signal (at –20 dB) on CISPR16 load with the coupling network	$V_{o(rms)}$ = 121 dBµV on CISPR16 load; f_{osc} = 8.48 MHz; $\overline{\text{DATA}}_{\text{IN}}$ = 300 Hz; duty factor = 50%; see Fig.4	–	3000	–	Hz
Reception mode						
$V_{i(rms)}$	analog input signal (RMS value)		82	–	122	dBµV
V_I	DC level at pin RX_{IN}		–	2.5	–	V
Z_i	RX_{IN} input impedance		–	50	–	kΩ
R_{AGC}	AGC range		–	36	–	dB
$t_{c(AGC)}$	AGC time constant	f_{osc} = 8.48 MHz; see Fig.5	–	296	–	µs
$t_{d(dem)(su)}$	demodulation delay set-up time	f_{osc} = 8.48 MHz; see Fig.15	–	350	400	µs
$t_{d(dem)(h)}$	demodulation delay hold time	f_{osc} = 8.48 MHz; see Fig.15	–	420	470	µs
B_{det}	detection bandwidth	f_{osc} = 8.48 MHz	–	3	–	kHz
BER	bit error rate	f_{osc} = 8.48 MHz; 600 baud; S/N = 35 dB; signal 76 dBµV; see Fig.17	–	1	–	1×10^{-4}

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-up timing						
$t_{d(pu)(TX)}$	delay between power-up and $\overline{\text{DATA}}_{\text{IN}}$ in transmission mode	XTAL = 8.48 MHz; C1 = C2 = 27 pF; R_p = 2.2 MΩ; see Fig.10	–	1	–	µs
$t_{d(pu)(RX)}$	delay between power-up and $\overline{\text{DATA}}_{\text{OUT}}$ in reception mode	XTAL = 8.48 MHz; C1 = C2 = 27 pF; R_p = 2.2 MΩ; f_{RXIN} = 132.5 kHz; 120 dBµV sine wave; see Fig.11	–	1	–	µs
Power-down timing						
$t_{d(pd)(TX)}$	delay between PD = 0 and $\overline{\text{DATA}}_{\text{IN}}$ in transmission mode	f_{osc} = 8.48 MHz; see Fig.12	–	10	–	µs
$t_{d(pd)(RX)}$	delay between PD = 0 and $\overline{\text{DATA}}_{\text{OUT}}$ in reception mode	f_{osc} = 8.48 MHz; f_{RXIN} = 132.5 kHz; 120 dBµV sine wave; see Fig.13	–	500	–	µs
$t_{active(min)}$	minimum active time with T = 10 ms power-down period in reception mode	f_{osc} = 8.48 MHz; f_{RXIN} = 132.5 kHz; 120 dBµV sine wave; see Fig.14	–	1	–	µs



Resolution bandwidth = 9 kHz; top: 0 dBV (RMS) = 120 dBµV (RMS); marker at –5 dBV (RMS) = 115 dBµV (RMS); the CISPR16 network provides an attenuation of 6 dB, so the signal amplitude is 121 dBµV (RMS).

Fig.3 Carrier spectrum.



Resolution bandwidth = 100 Hz; B_{-20dB} = 3000 Hz (2 × 1500 Hz).

Fig.4 Shaped signal spectrum.

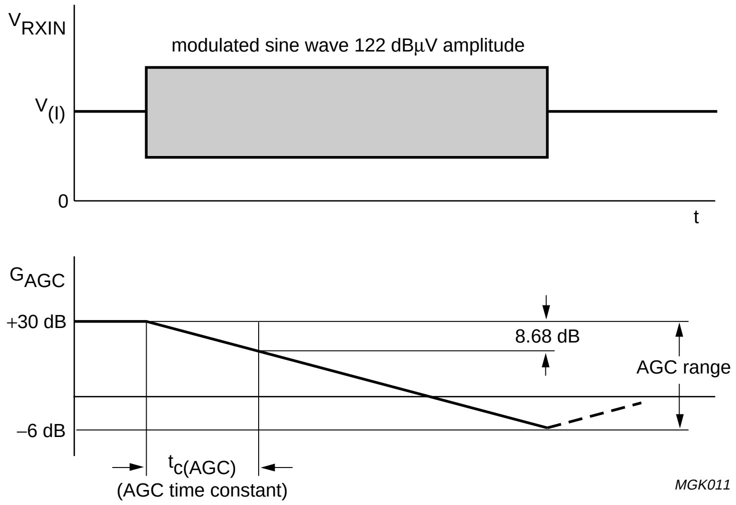
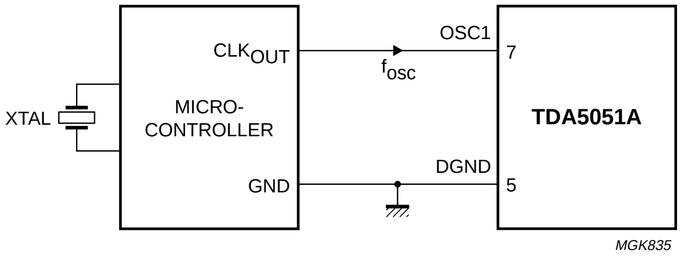


Fig.5 AGC time constant definition (not to scale).

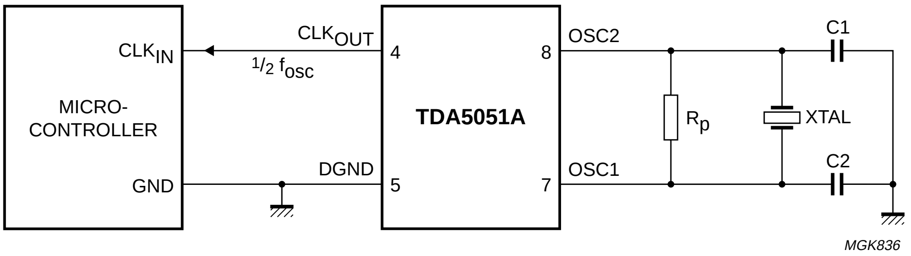
TIMING

Configuration for clock



For parameter description, see Table 1.

Fig.6 External clock.



For parameter description, see Table 1.

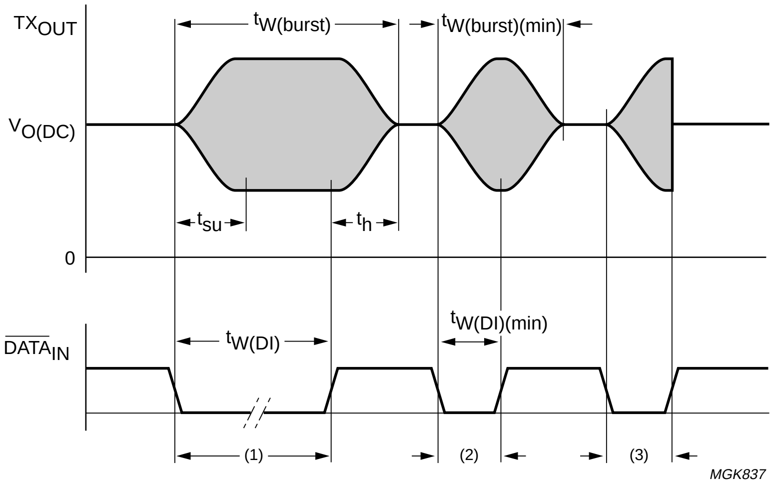
Fig.7 Typical configuration for on-chip clock circuit.

Table 1 Clock oscillator parameters

OSCILLATOR FREQUENCY f_{osc}	**CARRIER FREQUENCY f_{cr}**	**CLOCK OUTPUT FREQUENCY $\frac{1}{2}f_{osc}$**	**EXTERNAL COMPONENTS**
6.080 to 9.504 MHz	95 to 148.5 kHz	3.040 to 4.752 MHz	C1 = C2 = 27 to 47 pF; R_p = 2.2 to 4.7 MΩ; XTAL = standard quartz crystal

Table 2 Calculation of parameters depending on the clock frequency

SYMBOL	PARAMETER	CONDITIONS	UNIT
f_{osc}	oscillator frequency	with on-chip oscillator: frequency of the crystal quartz; with external clock: frequency of the signal applied at OSC1	Hz
f_{CLKOUT}	clock output frequency	$\frac{1}{2}f_{osc}$	Hz
f_{cr}	carrier frequency/digital filter tuning frequency	$\frac{1}{64}f_{osc}$	Hz
t_{su}	set-up time of the shaped burst	$\frac{23}{f_{cr}}$ or $\frac{1472}{f_{osc}}$	s
t_h	hold time of the shaped burst	$\frac{23}{f_{cr}}$ or $\frac{1472}{f_{osc}}$	s
$t_{W(DI)(min)}$	minimum pulse width of $\overline{DATA}_{IN}$ signal	$t_{su} + \frac{1}{f_{cr}}$	s
$t_{W(burst)(min)}$	minimum burst time of $V_{O(DC)}$ signal	$t_{W(DI)(min)} + t_h$	s
$t_{c(AGC)}$	AGC time constant	$\frac{2514}{f_{osc}}$	s
$t_{su(demod)}$	demodulation set-up time	$\frac{3200}{f_{osc}}$ (≈max.)	s
$t_{h(demod)}$	demodulation hold time	$\frac{3800}{f_{osc}}$ (≈max.)	s



(1) $t_{W(DI)} > t_{W(DI)(min)}$.

(2) $t_{W(DI)(min)} = t_{su} + \frac{1}{f_{cr}}$

(3) $t_{W(DI)(min)} < t_{su}$; wrong operation.

Fig.8 Relationship between $\overline{DATA}_{IN}$ and TX_{OUT} (see Table 3).

Table 3 Relationship between $\overline{DATA}_{IN}$ and TX_{OUT}

PD	$\overline{DATA}_{IN}$	TX_{OUT}
1	X(1)	high-impedance
0	1	high-impedance (after t_h)
0	0	active with DC offset

Note

1. X = don’t care.

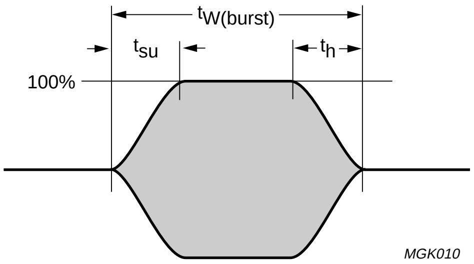
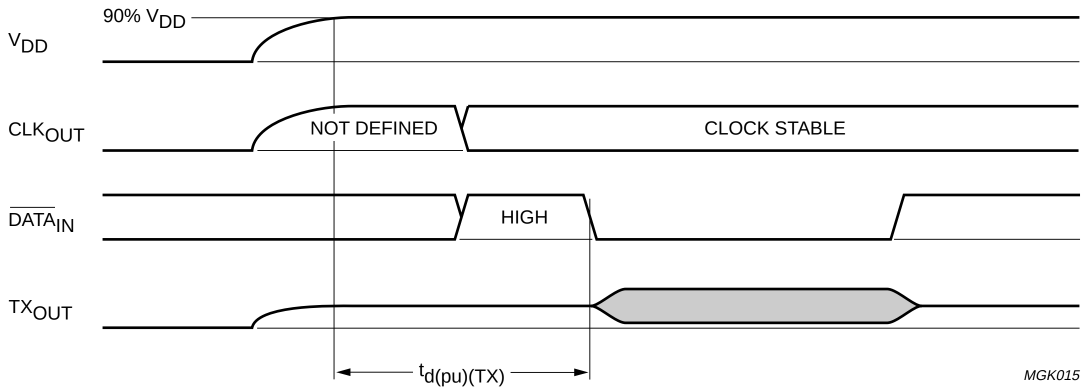


Fig.9 Pulse shape characteristics.

Timing diagrams



$\overline{DATA}_{IN}$ is an edge-sensitive input and must be HIGH before starting a transmission.

Fig.10 Timing diagram during power-up in transmission mode.

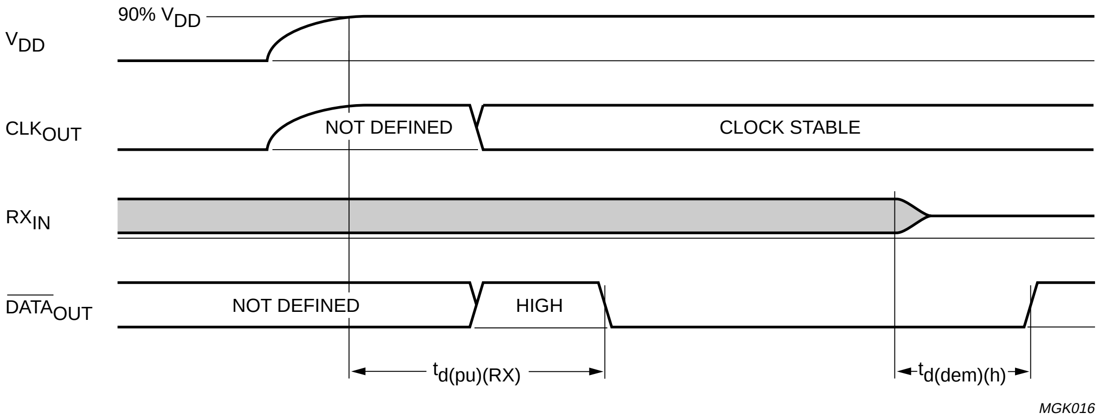


Fig.11 Timing diagram during power-up in reception mode.

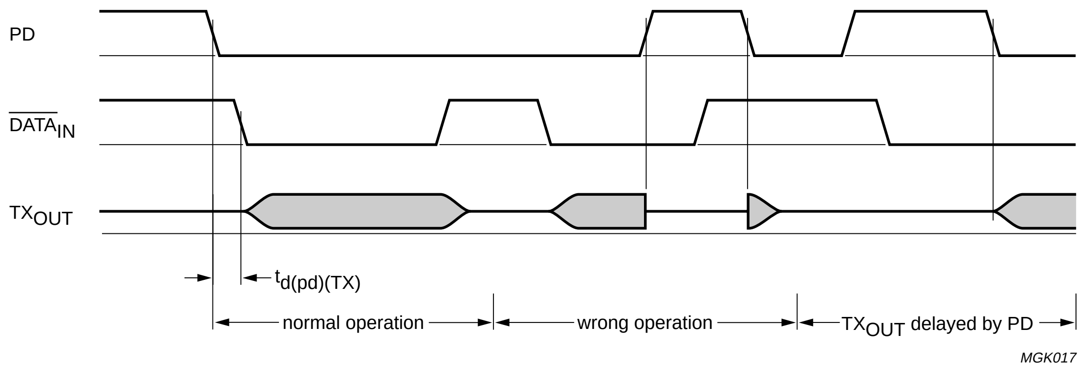


Fig.12 Power-down sequence in transmission mode.

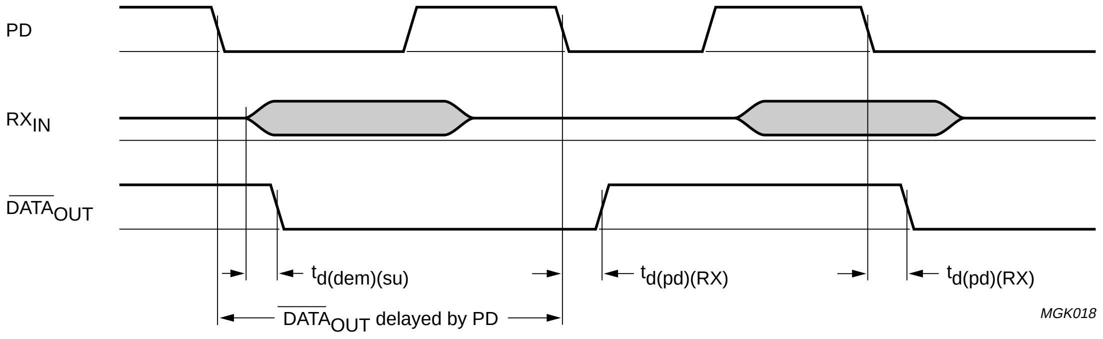


Fig.13 Power-down sequence in reception mode.

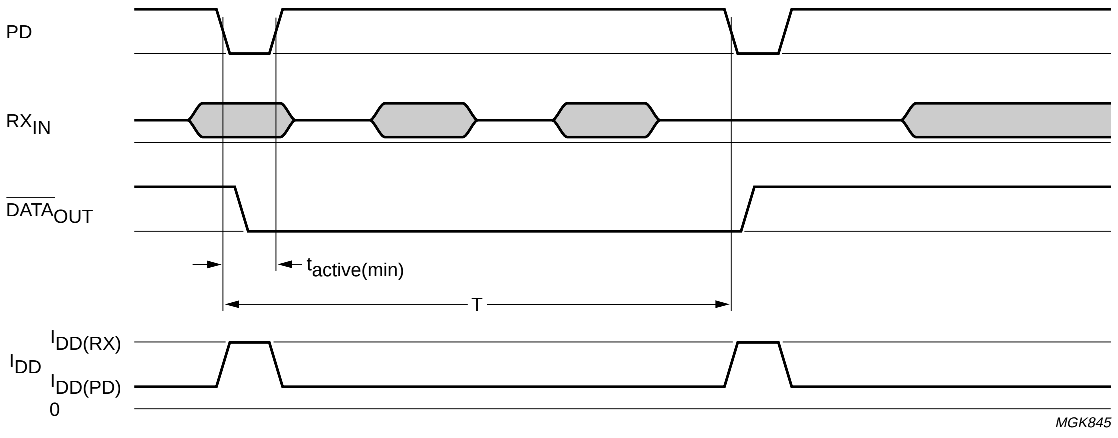


Fig.14 Power saving by dynamic control of power-down.

TEST INFORMATION

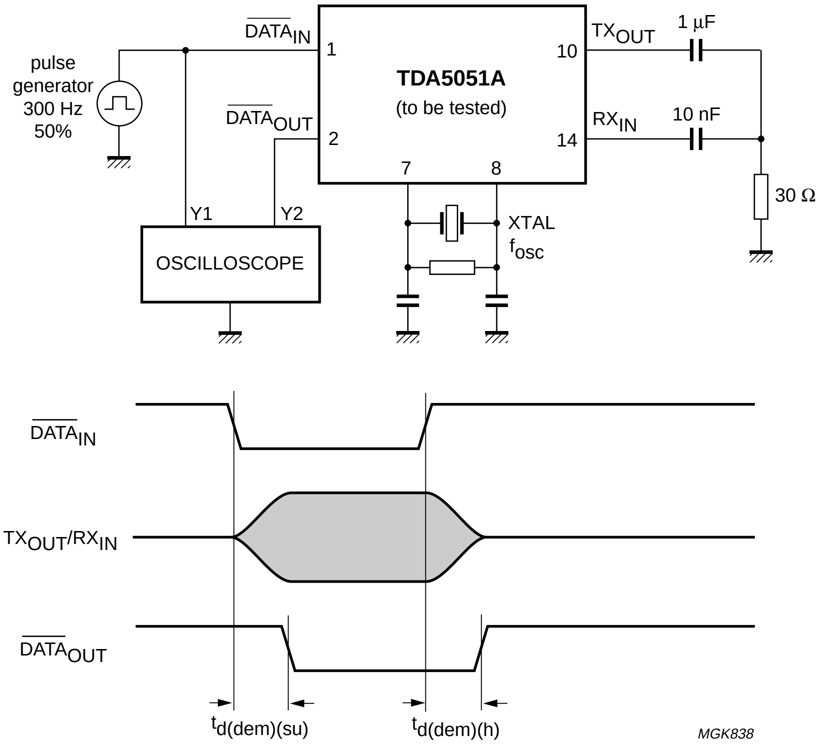
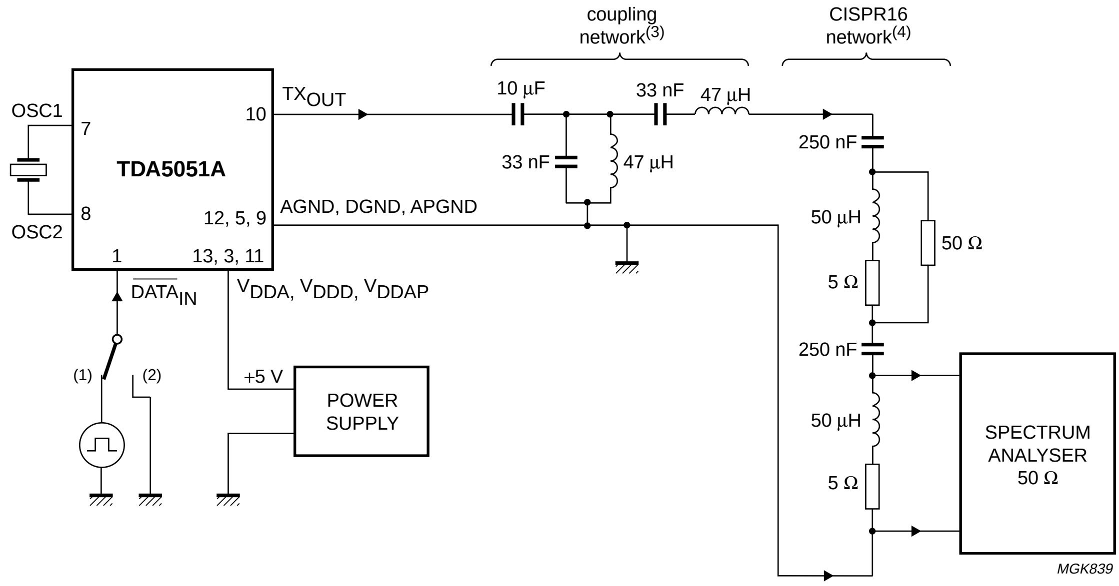


Fig.15 Test set-up for measuring demodulation delay.



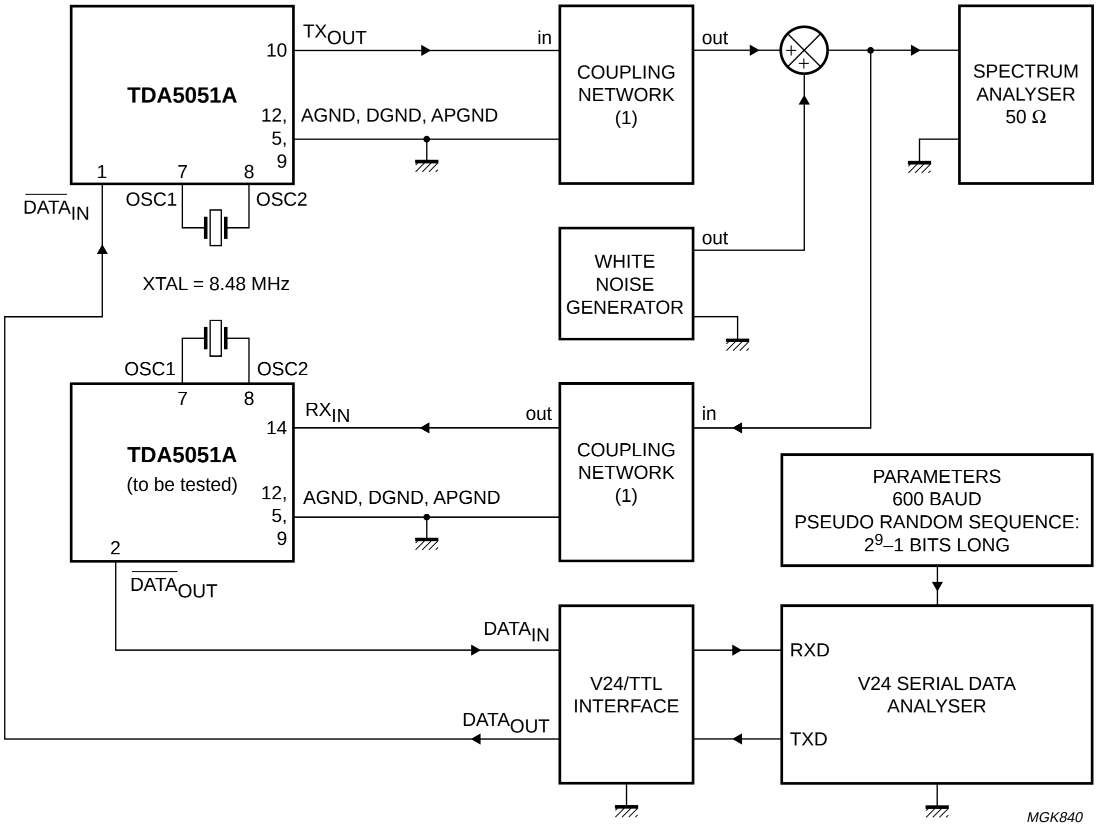
(1) Square wave TTL signal 300 Hz, duty factor = 50% for measuring signal bandwidth (see spectrum Fig.3).

(2) $\overline{\text{DATA}}_{\text{IN}}$ = LOW for measuring total harmonic distortion (see spectrum Fig.3).

(3) Tuned for f_{cr} = 132.5 kHz.

(4) The CISPR16 network provides a −6 dB attenuation.

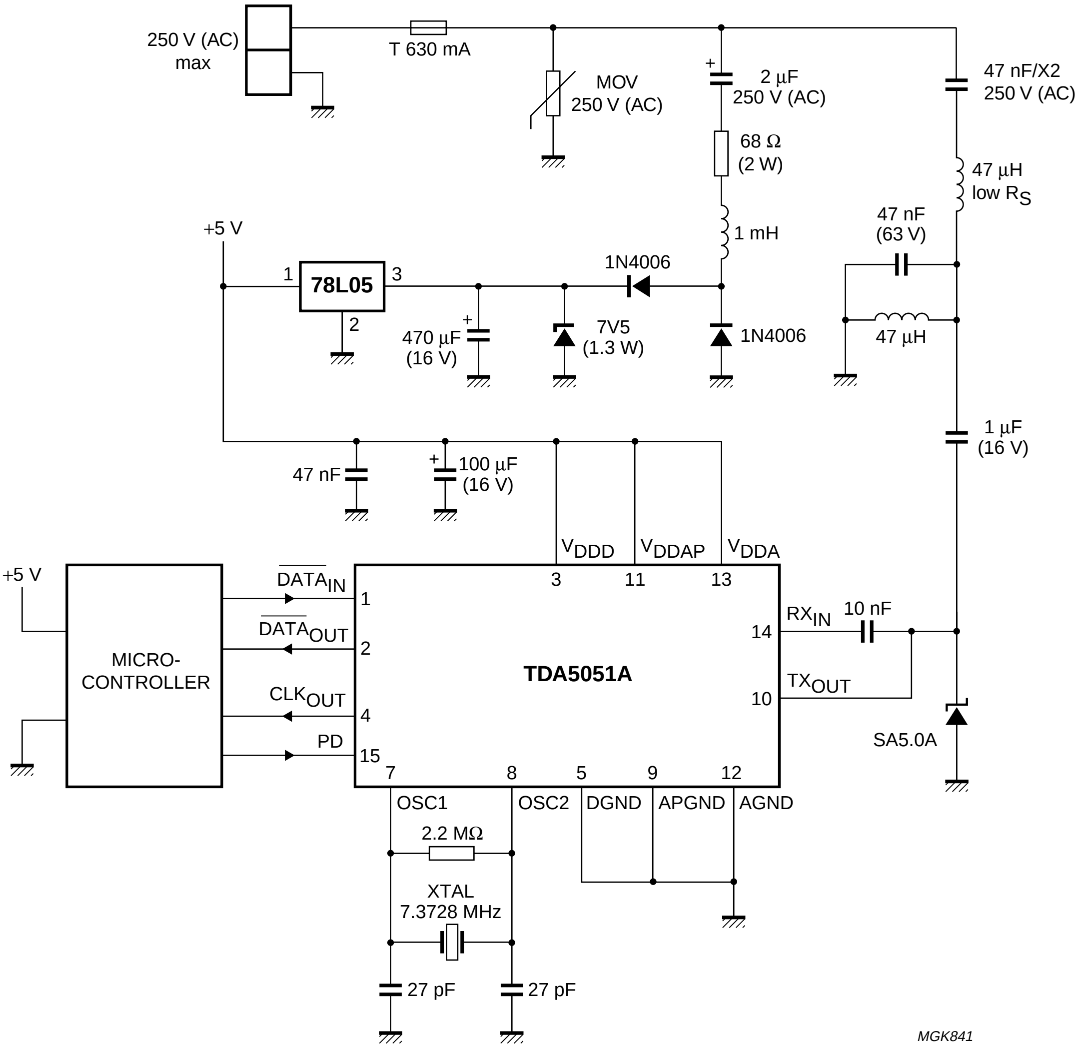
Fig.16 Test set-up for measuring THD and bandwidth of the TX_{OUT} signal.



(1) See Fig.16.

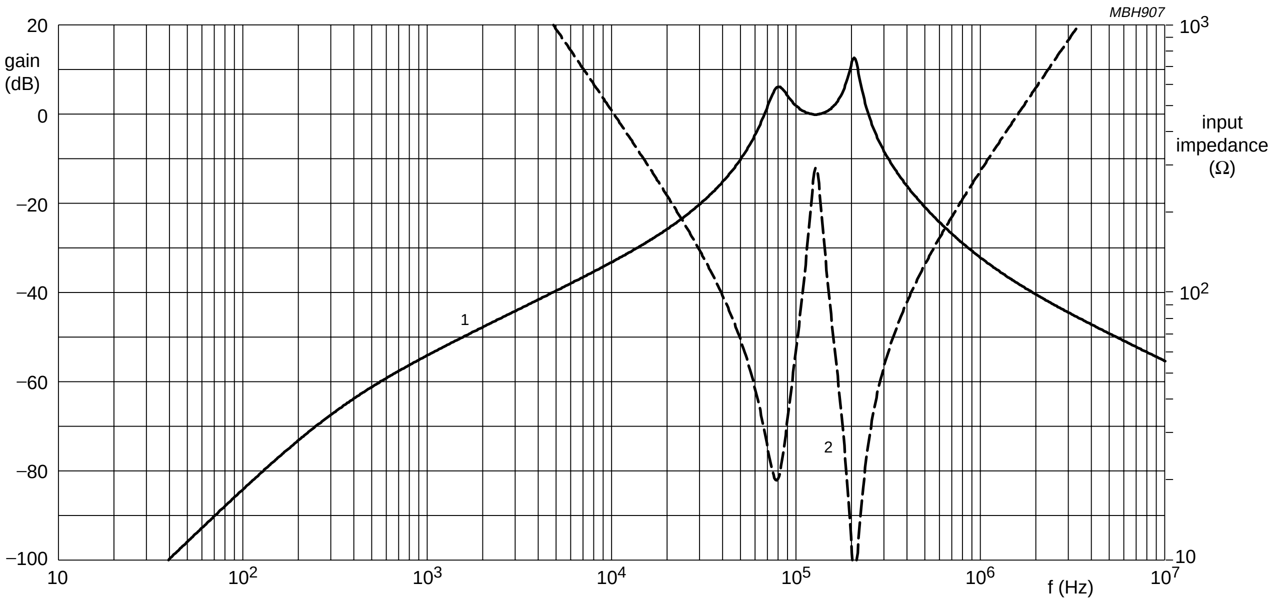
Fig.17 Test set-up for measuring Bit Error Rate (BER).

APPLICATION INFORMATION



f_{cr} = 115.2 kHz for a XTAL = 7.3728 MHz standard crystal.

Fig.18 Application diagram without power line insulation.



Main features of the coupling network: 50 Hz rejection >80 dB; anti-aliasing for the digital filter >50 dB at the sampling frequency (½f_{osc}). Input impedance always higher than 10 Ω within the 95 to 148.5 kHz band.

Fig.19 Gain (curve 1) and input impedance (curve 2) of the coupling network (f_{cr} = 115.2 kHz; L = 47 µH; C = 47 nF).

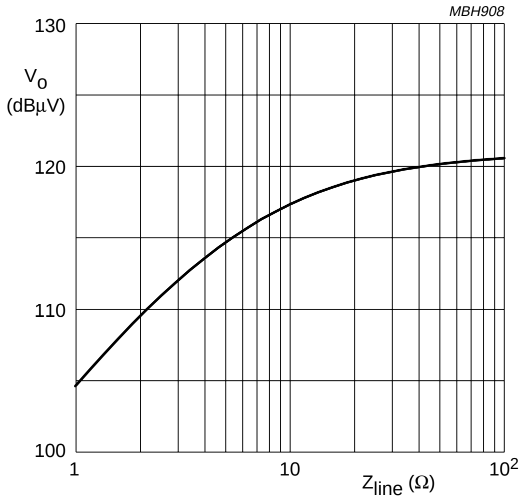
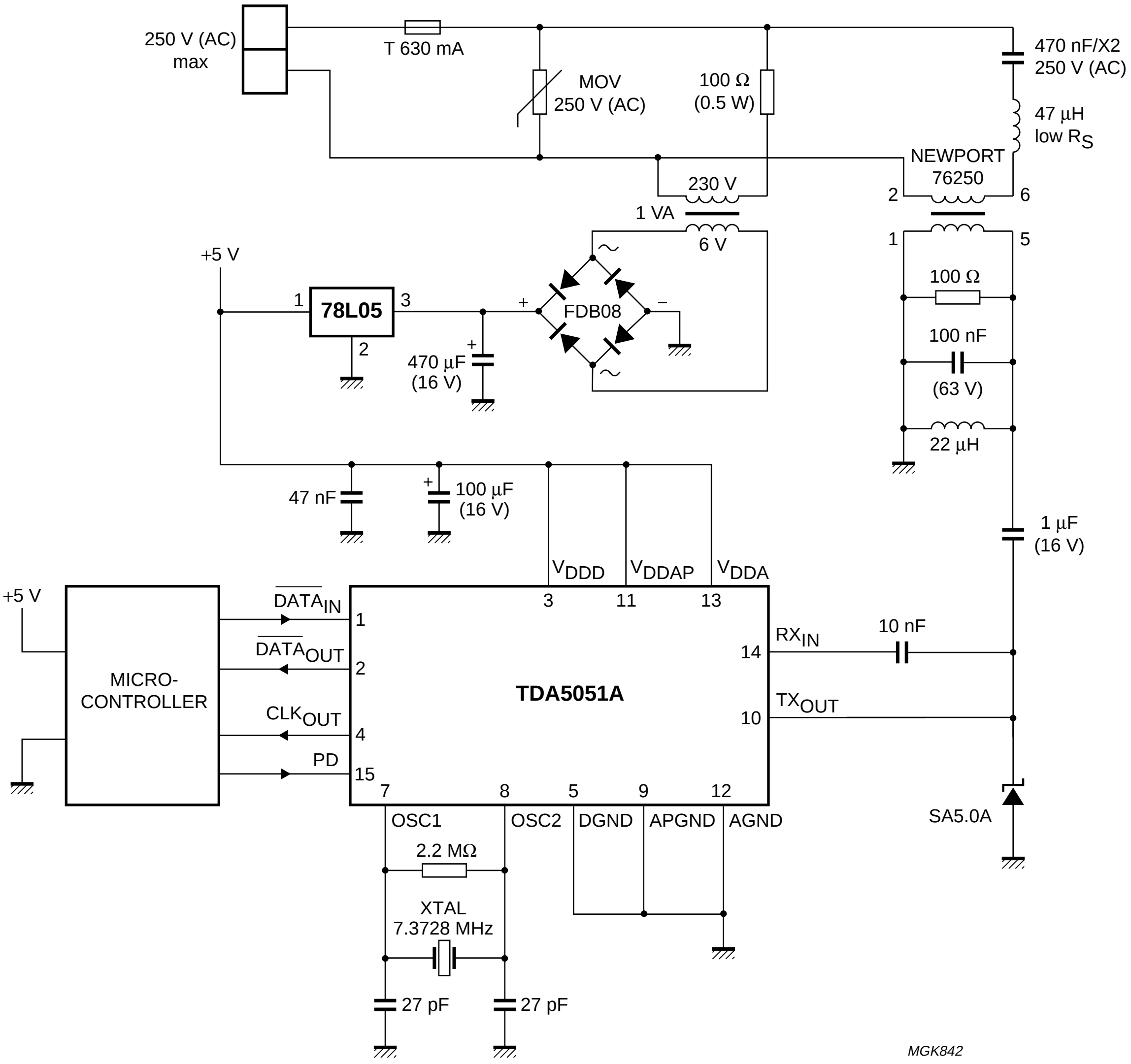
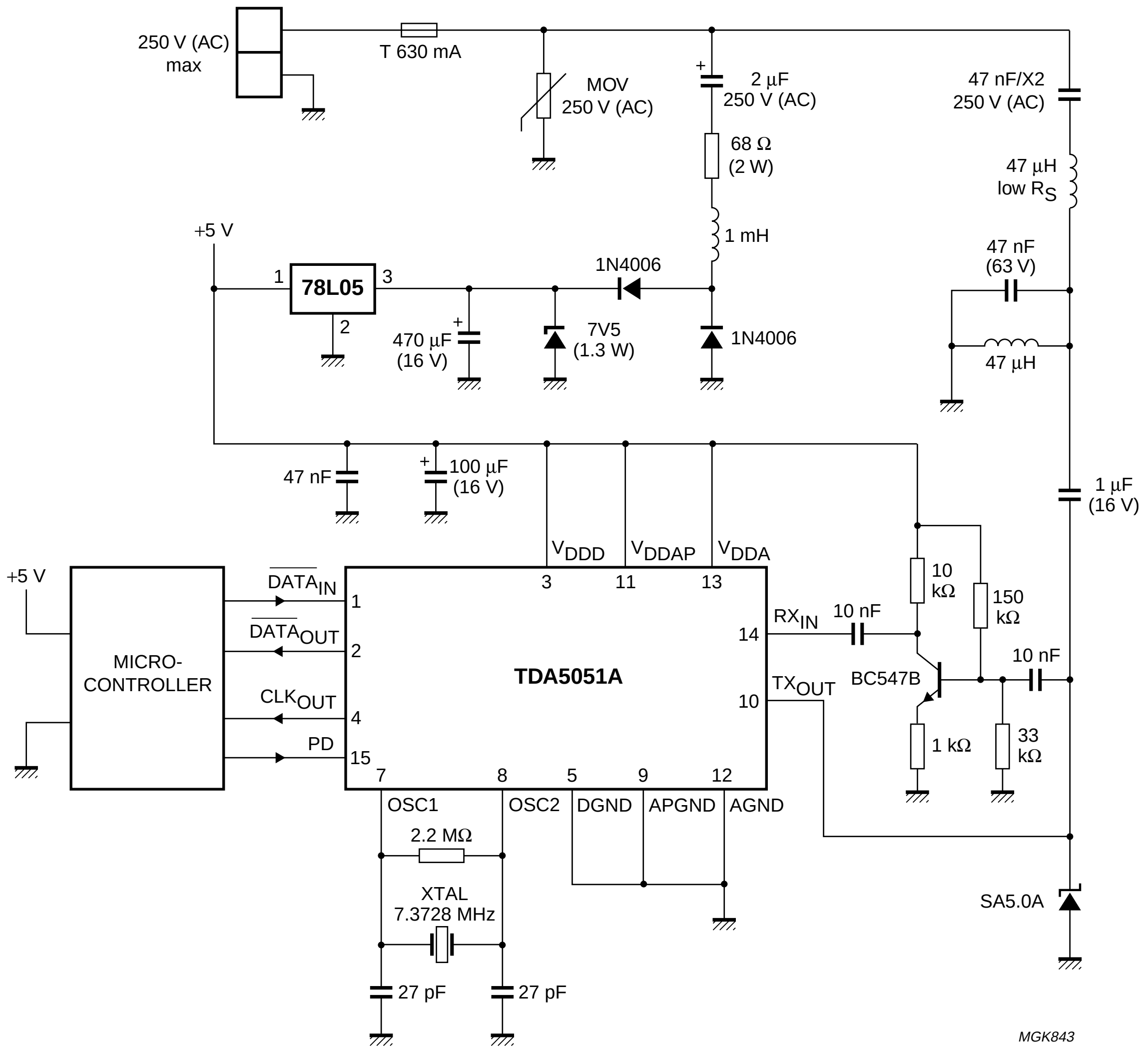


Fig.20 Output voltage as a function of line impedance (with coupling network; L = 47 µH; C = 47 nF).



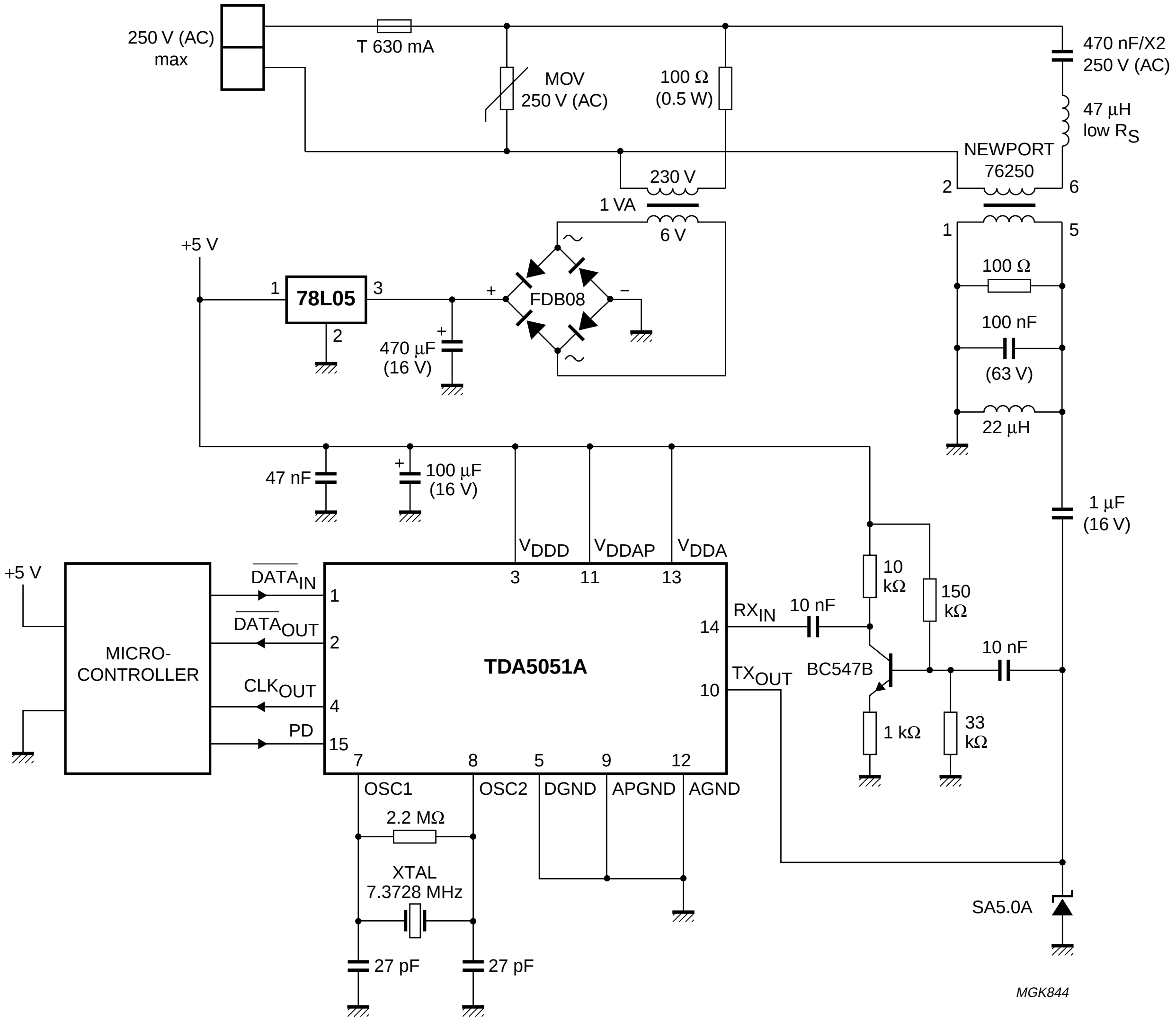
f_{cr} = 115.2 kHz for a XTAL = 7.3728 MHz standard crystal.

Fig.21 Application diagram with power line insulation.



f_{cr} = 115.2 kHz for a XTAL = 7.3728 MHz standard crystal.

Fig.22 Application diagram without power line insulation, with improved sensitivity (68 dBµV typ.).

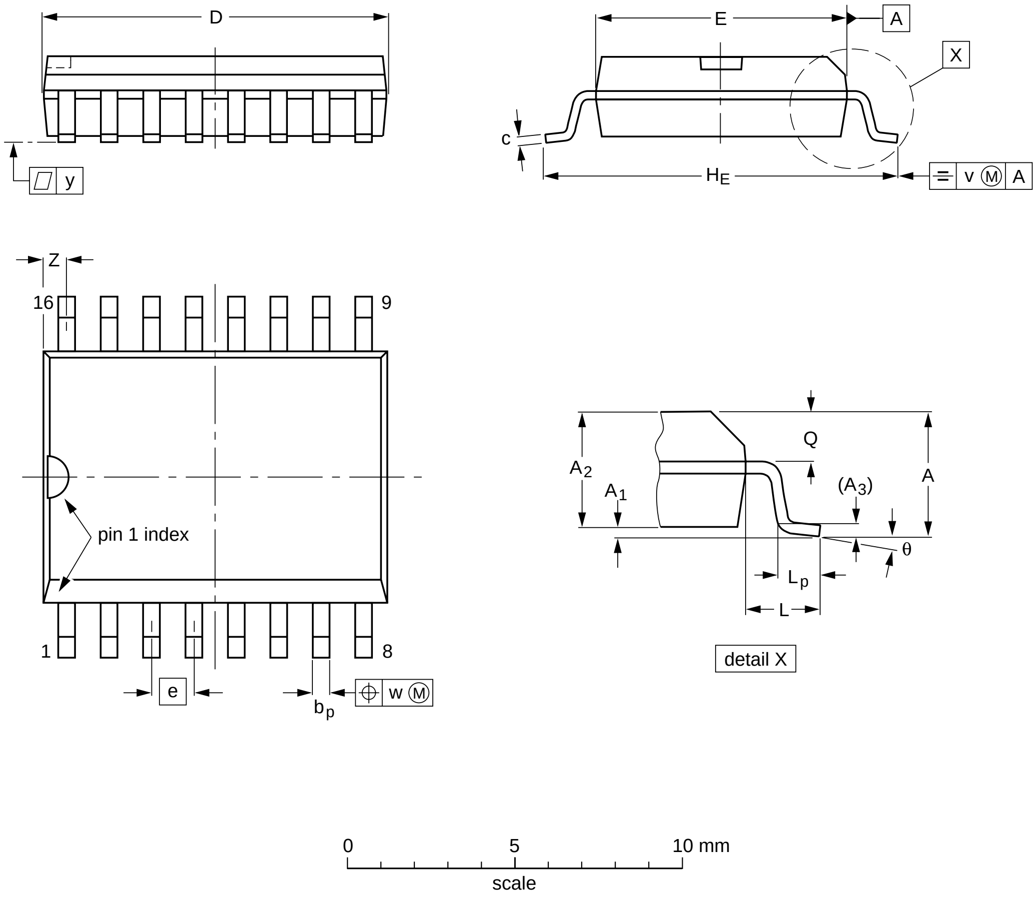


f_{cr} = 115.2 kHz for a XTAL = 7.3728 MHz standard crystal.

Fig.23 Application diagram with power line insulation, with improved sensitivity (68 dBµV typ.).

PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 7.5 mm SOT162-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	**REFLOW**(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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