SGS-THOMSON MICROELECTRONICS

TECHNICAL NOTE

AN ECONOMIC MOTOR DRIVE WITH VERY FEW COMPONENTS

INTRODUCTION

The main objectives of this design are the economy and circuit simplicity which enable costs to be reduced to a minimum. For this reason the design is particulary suitable for domestic appliances powered by the 220 V AC mains. In this area, characteristics such as low cost, simplicity (and consequently greater reliability) have priority.

With these objectives the choice of the power switch is very important because the complexity of the drive circuit, the number and the power of the auxiliary supplies and the protection networks, depend on its characteristics. These factors lead to the decision to use a HIMOS device (an IGBT) as a power switch. The main characteristics of a HIMOS device are that:

- It switches high current with very low ON resistance, similar to a BJT (bipolar junction transistor).
- It is very rugged and has very large safe operating areas similar to Power MOSFETs.
- It has high overload current capability.
- It is easy to drive (like Power MOSFETs) consequently it is possible to drive it directly by means of popular linear IC.

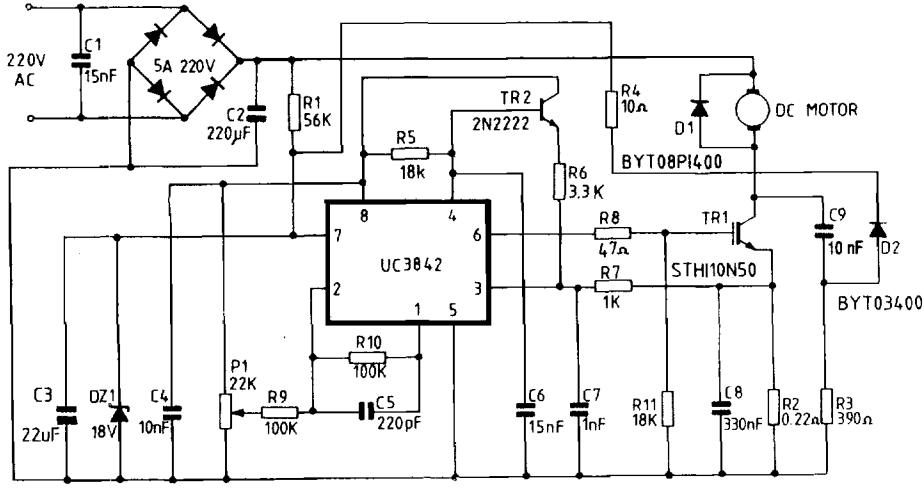
These characteristics are very suitable for motor drive applications in general and make HIMOS the new way of power switching in this area. An additional factor is that a HIMOS device has a smaller chip area than Power MOSFETs, or bipolar transistors with the same ratings ($V_{(BR)\,DSS}$ and $I_{DS\,max}$).

CIRCUIT DESCRIPTION

This DC motor drive circuit has a single switch topology and works in current mode; an STHI10N50 HIMOS is used as the power switch. The complete circuit schematic is shown in figure 1. Its main features are as follows:

- 300V, 4A DC permanent magnet step down motor drive
- Current mode PWM control
- Output current adjustable pulse by pulse from 0 to 4A
- 220 AC ± 10% supply voltage
- 6KHz switching frequency
- From 6% to 95% operating duty cycle

Fig. 1 - Circuit diagram of the HIMOS motor drive



The PWM controller IC used is STUC3842. It is a popular, economic eight pin IC widely used for off-line and DC to DC converters. STUC3842 provides the features necessary to implement fixed frequency current mode control scheme with a minimal external parts count.

Internally implemented circuits include under voltage lockout featuring start-up current less than 1mA, a precision reference, logic to insure latched operation, a PWM comparator which provides current limit control and a totem pole output stage. It can directly drive the gate of the 500V 10A HIMOS switch STHI10N50. The choice of this IC and its current mode working matches the requirements of economy and simplicity of this application.

Fig. 2 - STHI10N50 output characteristics (I step = 6V)

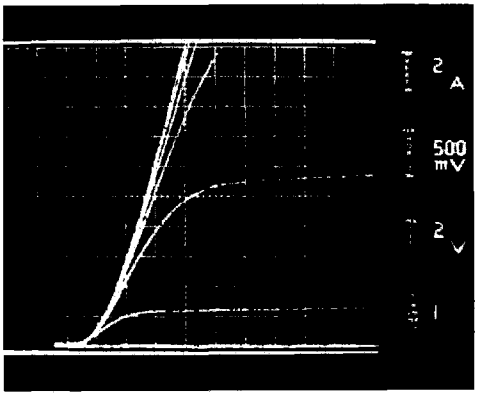
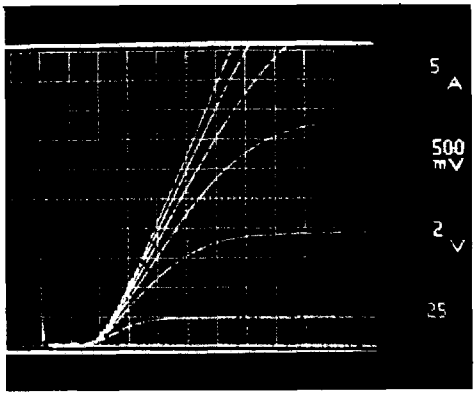


Fig. 3 - STHI20N50 output characteristics (I step = 6V)



The motor speed is controlled by the error voltage which is variable from OV to +5V, and is applied to pin 2 of the IC by means of R9. This voltage sets a constant current level at which the IC interrupts, pulse by pulse, the current in the power switch: the PWM control is therefore a "current mode" type. The HIMOS switch used is STHI10N50, for higher power motors STHI20N50 can be used simply by changing resistors R2 and R6 and free-wheeling diode D1. Figures 2 and 3 show respectively the output characteristics of STHI10N50 and STHI20N50 devices.

An important part of the circuit is the snubber consisting of R3, C9, D2. This accomplishes two functions:

a) it provides power for the UC3842 using the charge current of C9 during the STHI10N50 turn-off; infact the IC requires about 20 mA DC as supply current and cannot be biased simply through resistor R1 which should be 10Kohm 10W. Instead, using this active snubber, R1 can be set to a value of 56Kohm 2W in order to apply the start up power to the UC3842.

b) it reduces the energy dissipated in the power switch during turn-off; consequently a smaller heatsink can be used for STHI10N50 giving additional cost reduction.

To insure a continuous power supply to the IC, using the active snubber C9, R3, D2, it is necessary that the capacitor C9 must be completely discharged before turn-off. Because C9 is discharged by means of R3 during the ON phase of the power switch, there is a limit to the minimum ON time which cannot be less than 8 μs, consequently the minimum duty-cycle is 6%.

Considering a peak current I_p = 4A, a fall time t_f = 1.5 μs and the minimum ON time of 8 μs, the values of the snubber components are calculated as follows:

$$C9 = (I_p \cdot t_f)/2V_{cc} = 10\ nF$$

$$R3 = T_{on\ (min)}/2 \cdot C9 = 400ohm$$

The power dissipated across R3 is:

$$P = 1/2 \cdot C9 \cdot V^2 \cdot f = 3W$$

The adoption of this snubber does not affect the efficiency of the circuit during normal operation because its power dissipation is very low and it has the additional benefit of using this energy to supply the IC so reducing the dissipation in the power switch. The extra cost is negligible with respect to the cost of a transformer for supplying the low voltage power to the IC.

The network of Tr2 and R6 adds a fraction of the ramp oscillator voltage to the "current sense" si-

gnal at pin 3 of the IC (via transistor Tr2 2N2222) to allow slope compensation. Consequently duty-cycles as high as 50% can be obtained.

Diodes D1 (BYT08PI400) and D2 (BYT03400) are fast recovery types and have been used in order to minimize stresses on the power switch.

MEASUREMENTS ON THE CIRCUIT

The DC motor drive was tested in several operating conditions. These were maximum and rated output current and in blocked rotor conditions.

The waveforms of the drain voltage, V_{DS}, drain current, I_D, and gate voltage, V_G, both with and without the snubber can be seen in figures 5 and 6 respectively.

Fig. 4 - STHI10N50 turn-off with snubber I_d= 1A/div, V_{ds}= V50/div, V_g=5V/div

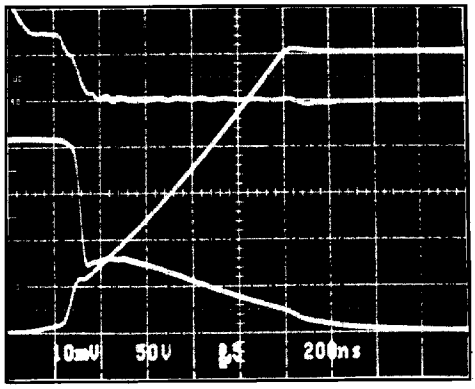
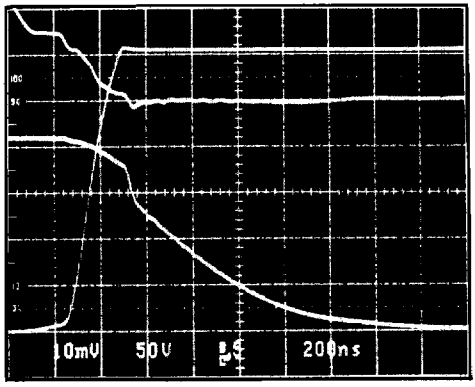


Fig. 5 - STHI10N50 turn-off without snubber I_d= 1A/div, V_{ds}= 50V/div, V_g= 5V/div



Here you can see the typical behaviour of a HIMOS device at the turn-off when typical features of both Power MOSFET and BJT are involved. The storage phase of the turn-off is dependent on the MOS behaviour as the base collector junction of the PNP transistor is reversed biased: the gate voltage decreases to a point where the Miller effect begins to control the current in the drain and V_{DS} start to rise. The fall time phase can be divided into two parts: the first part is the MOS turn-off and is very fast, the second is slow and starts when the MOS channel is closed and the PNP transistor has an open base turn-off and is dominated by recombination of excess carriers. Therefore the first part of the time is controlled by the gate drive circuit, the second part is dependent on the PNP transistor life-time and gain.

Since the PNP gain increases as V_{DS} increase, the fall time consequently varies with V_{DS}. Therefore, when the snubber is used and the V_{DS} slope is dominated by the capacitance, the fall time region due to the MOS is more evident (figure 6).

Figure 6 shows the turn-on behaviour of the HIMOS: it very fast (t-rise 30ns) and, as with Power MOS devices, is a function of the impedance of the driver circuit and the applied gate voltage.

Fig. 6 - STHI10N50 turn-on I_d= 1A/div, V_{ds}=50V/div

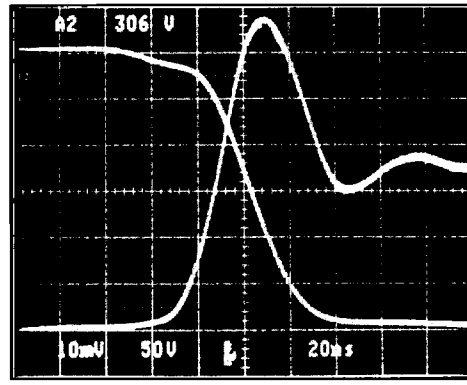
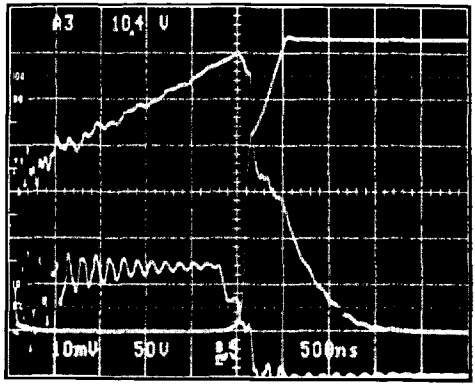


Figure 7 shows the behaviour in the case of a blocked rotor and with the current control set at the maximum 4A. This condition was simulated, as worst case, with and inductance of 300uH and a resistance of 1 Ω: the current does not exceed 6A. The overcurrent of 2A, with respect the control current of 4A, is due to the delay introduced by the network

of R7, C7 of about 2 μs. This filter network is necessary to suppress the leading edge spikes on the IC current sense comparator input.

Fig. 7 - Blocked rotor' beheaviour I_d= 1A/div, V_{ds}= 50V/div, V_g= 5V/div



The losses in the circuit, for the maximum rating of each component are approximately as follows: P(R1) = 2W, P(R3) = 3W, P(R2) = 3W, P(D1) = 4W, P(Tr1) = 7W.

CONCLUSION

A 300V 4A DC permanent magnet single quadrant motor drive was developed with objectives of maximum circuit simplicity and economy. Consequently a current mode PWM control with a popular IC was adopted and an STHI10N50 HIMOS (an IGBT) was used.

The low drive energy requirement due to the high input impedance of the HIMOS allows substantial cost reduction in the control circuit. Conductivity modulation of the drain produces a low ON resistance, an essential feature to work with high peak currents in the switching element. The ruggedness, due to the excellent safe operating areas, is especially relevant for motor control applications.

The easy drive, high current handling and excellent ruggedness make HIMOS the new way of power switching in the motor control field.