Tabelle1

C.4 Connector Pin Assignment for Digital and Analog Input/Output Modules

	Slots 0 to 8 (right)*	
	a b	
1	M	Gnd
2	+5V	+5v
3	PESP	Memory I/O Select; is generated every time peripheral memory is accessed.
4	ADB0	Ad0
5	RESET	Reset
6	ADB1	Ad1
7	/ MRD	Memory Read; is generated on every Read access.
8	ADB2	Ad2
9	/ MWR	Memory Write is generated on every write access.
10	ADB3	Ad3
11	/ RDY	Ready; signal acknowledging MRD or MWR access.
12	ADB4	Ad4
13	DB0	D0
14	ADB5	Ad5
15	DB1	D1
16	ADB6	Ad6
17	DB2	D2
18	ADB7	Ad7
19	DB3	D3
20	ADB8	Ad8
21	DB4	D4
22	ADB9	Ad9
23	DB5	D5
24	ADB10	Ad10
25	DB6	D6
26	ADB11	Ad11
27	DB7	D7
28	BASP	Command output disable. The signal disables the digital output modules.
29	/ PRAL	Process interrupt; hardware interrupt signal from a digital I/O
30	M	Gnd module.
31	/ ASG	Interface module plugged in
32	/ FX**	** Enabling lines of the individual slots (X=0 to 8)

Adress range starting at f000H