PIC16F/LF1847/PIC12F/LF1840 Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC12F1840
- PIC12LF1840
- PIC16F1847
- PIC16LF1847

1.0 OVERVIEW

The PIC16F/LF1847 and PIC12F/LF1840 devices can be programmed using either the high-voltage In-Circuit Serial Programming™ (ICSP™) method or the low-voltage ICSP™ method.

1.1 Hardware Requirements

1.1.1 HIGH-VOLTAGE ICSP PROGRAMMING

In High-Voltage ICSP™ mode, these devices require two programmable power supplies: one for V_{DD} and one for the $\overline{MCLR}/V_{PP}$ pin.

1.1.2 LOW-VOLTAGE ICSP PROGRAMMING

In Low-Voltage ICSP™ mode, these devices can be programmed using a single V_{DD} source in the operating range. The $\overline{MCLR}/V_{PP}$ pin does not have to be brought to a different voltage, but can instead be left at the normal operating voltage.

1.1.2.1 Single-Supply ICSP Programming

The LVP bit in Configuration Word 2 enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled) from the factory. The LVP bit may only be programmed to '0' by entering the High-Voltage ICSP mode, where the $\overline{MCLR}/V_{PP}$ pin is raised to V_{IHH}. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

> **Note 1:** The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying V_{IHH} to the $\overline{MCLR}/V_{PP}$ pin.
>
> **2:** While in Low-Voltage ICSP mode, $\overline{MCLR}$ is always enabled, regardless of the MCLRE bit, and the port pin can no longer be used as a general purpose input.

1.2 Pin Utilization

Five pins are needed for ICSP™ programming. The pins are listed in Table 1-1 and Table 1-2.

TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING – PIC16F/LF1847

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6	ICSPCLK	I	Clock Input – Schmitt Trigger Input
RB7	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
RA5/$\overline{MCLR}$/VPP	Program/Verify mode	P(1)	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: In the PIC12F/LF1840 and PIC16F/LF1847, the programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{MCLR}$ input. Since the $\overline{MCLR}$ is used for a level source, $\overline{MCLR}$ does not draw any significant current.

TABLE 1-2: PIN DESCRIPTIONS DURING PROGRAMMING – PIC12F/LF1840

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RA1	ICSPCLK	I	Clock Input – Schmitt Trigger Input
RA0	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
RA3/$\overline{MCLR}$/VPP	Program/Verify mode	P(1)	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: In the PIC12F/LF1840 and PIC16F/LF1847, the programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{MCLR}$ input. Since the $\overline{MCLR}$ is used for a level source, $\overline{MCLR}$ does not draw any significant current.

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2.0 DEVICE PINOUTS

The pin diagrams for the PIC16F/LF1847 and PIC12F/LF1840 family are shown in Figure 2-1 through Figure 2-5. The pins that are required for programming are listed in Table 1-1 and shown in bold lettering in the pin diagrams.

FIGURE 2-1: 18-PIN DIAGRAM FOR PIC16F1847 AND PIC16LF1847

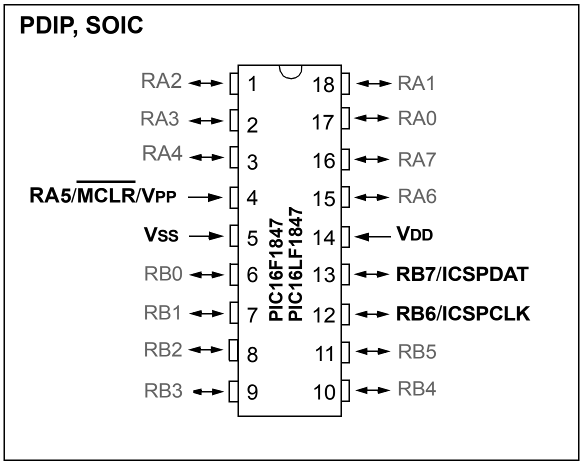


FIGURE 2-2: 20-PIN DIAGRAM FOR PIC16F1847 AND PIC16LF1847

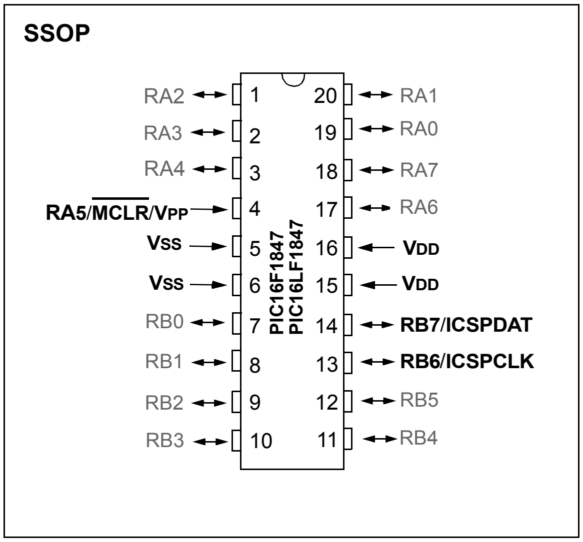


FIGURE 2-3: 28-PIN DIAGRAM FOR PIC16F1847 AND PIC16LF1847

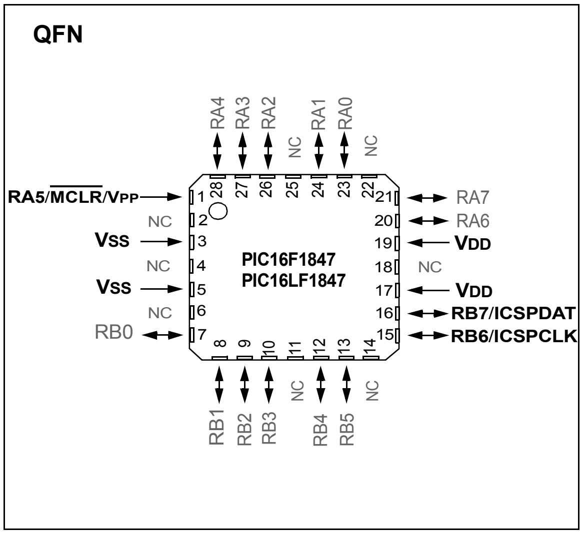


FIGURE 2-4: 8-PIN DIAGRAM FOR PIC12F1840/PIC12LF1840

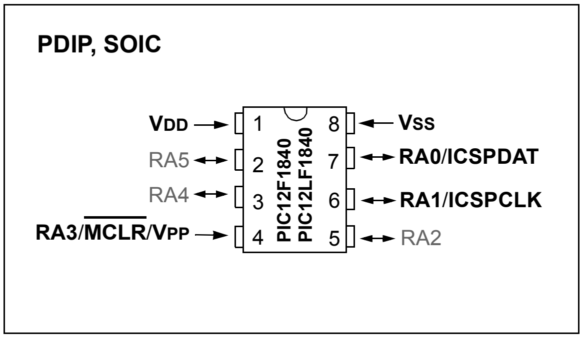
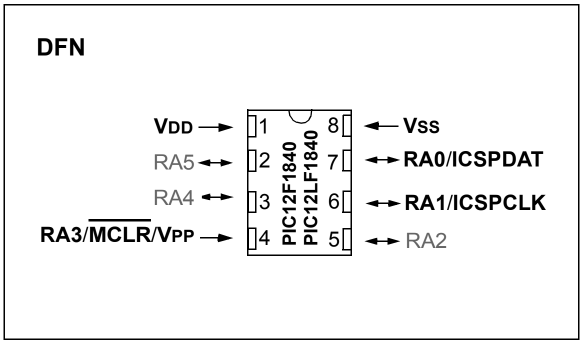


FIGURE 2-5: 8-PIN DIAGRAM FOR PIC12F1840/PIC12LF1840



3.0 MEMORY MAP

The memory for the PIC16F/LF1847 and PIC12F/LF1840 devices is broken into two sections: program memory and configuration memory. Only the size of the program memory changes between devices, the configuration memory remains the same.

FIGURE 3-1: PIC12F/LF1840 PROGRAM MEMORY MAPPING

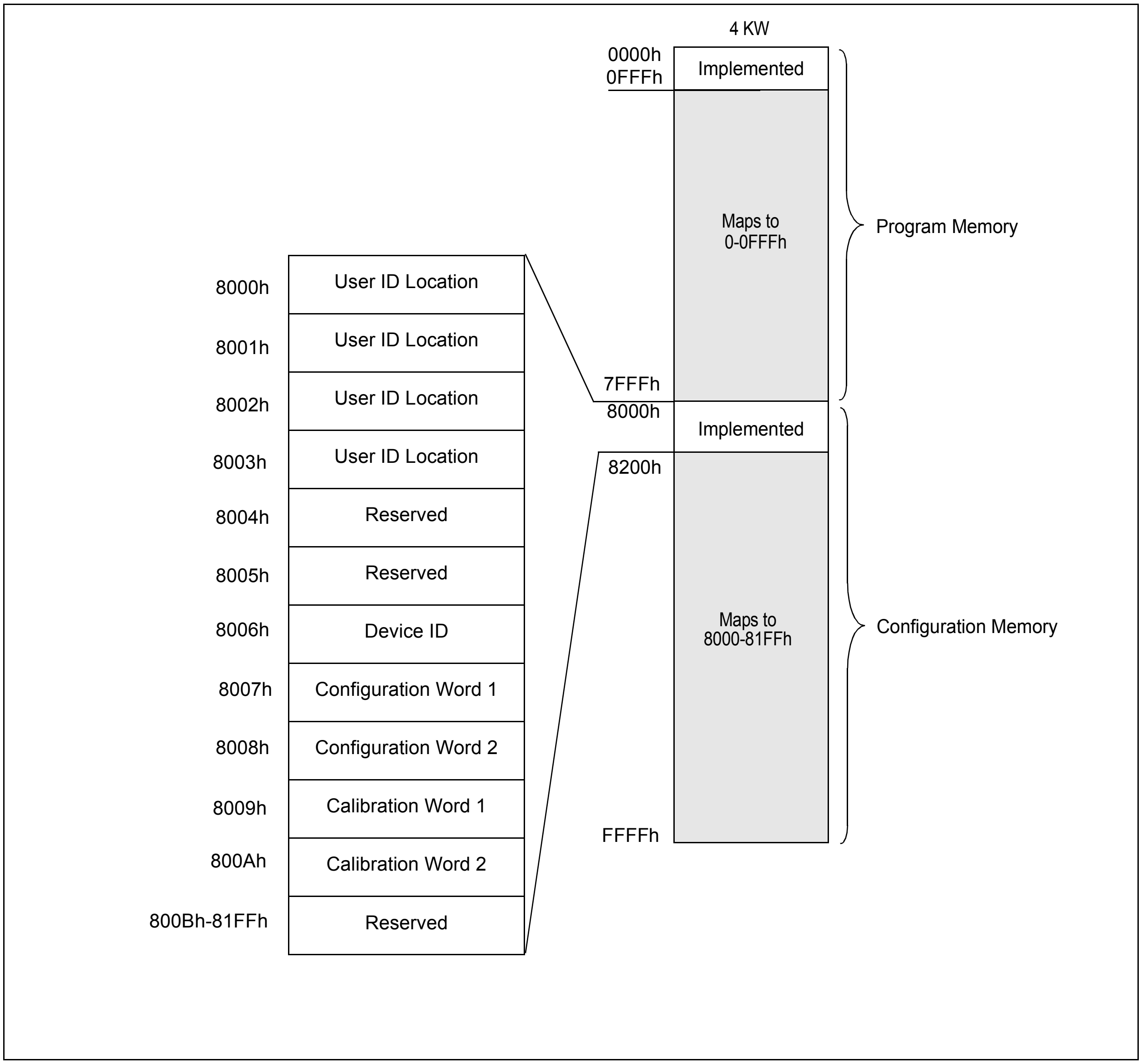


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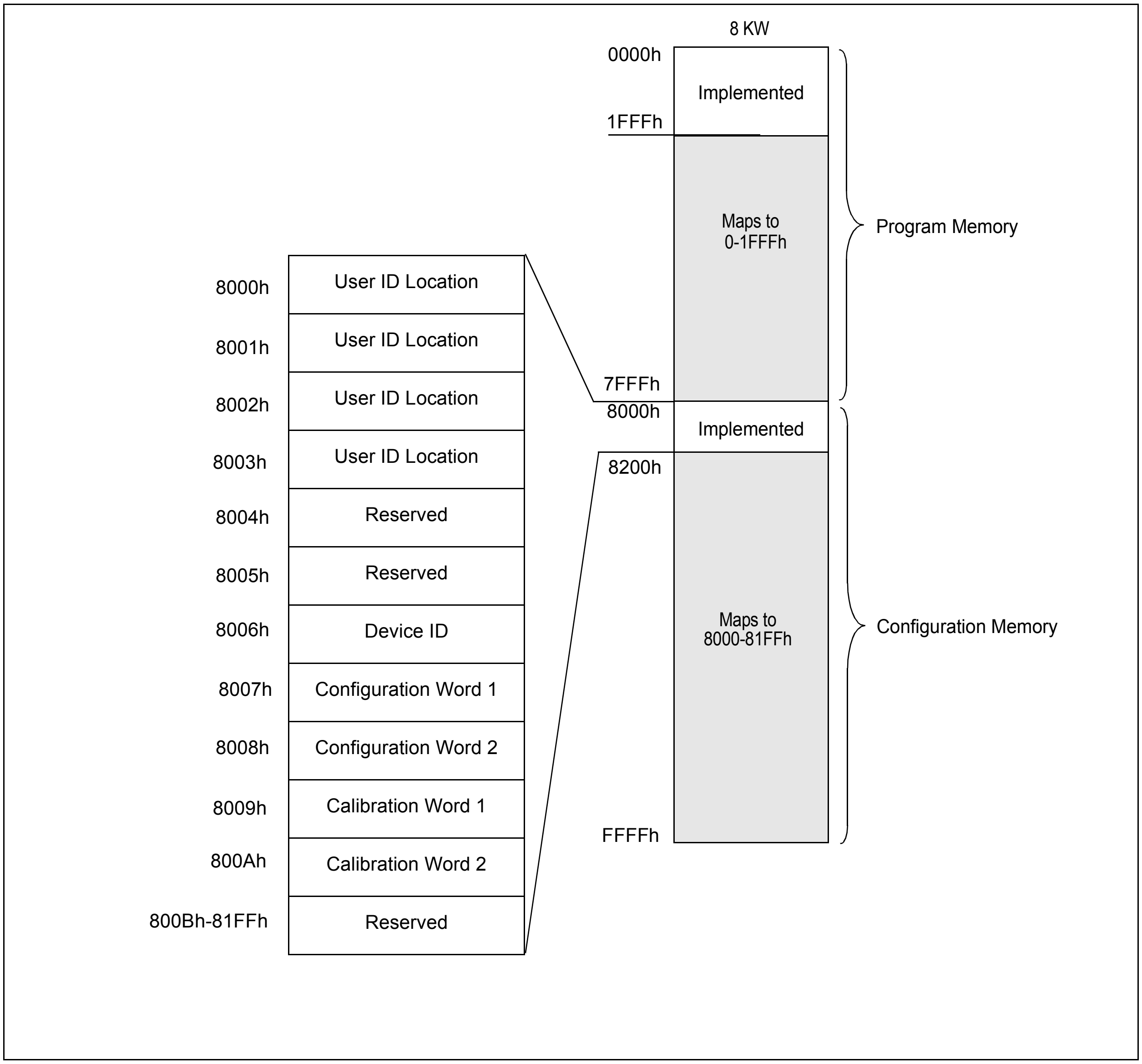
FIGURE 3-2: PIC16F/LF1847 PROGRAM MEMORY MAPPING



3.1 User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

> **Note:** MPLAB® IDE only displays the 7 Least Significant bits (LSb) of each user ID location, the upper bits are not read. It is recommended that only the 7 LSbs be used if MPLAB IDE is the primary tool used to read these addresses.

3.2 Device ID

The device ID word is located at 8006h. This location is read-only and cannot be erased or modified.

REGISTER 3-1: DEVICE ID: DEVICE ID REGISTER(1)

R	R	R	R	R	R	R
DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	DEV2
bit 13						bit 7

R	R	R	R	R	R	R
DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 6						bit 0

Legend:	P = Programmable bit	U = Unimplemented bit, read as ‘0’
R = Readable bit	W = Writable bit	‘0’ = Bit is cleared
-n = Value at POR	‘1’ = Bit is set	x = Bit is unknown

bit 13-5 **DEV<8:0>:** Device ID bits
These bits are used to identify the part number.

bit 4-0 **REV<4:0>:** Revision ID bits
These bits are used to identify the revision.

Note 1: This location cannot be written.

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TABLE 3-1: DEVICE ID VALUES

DEVICE	DEVICE ID VALUES	
	DEV	REV
PIC16F1847	01 0100 100	x xxxx
PIC16LF1847	01 0100 101	x xxxx
PIC12F1840	01 1011 100	x xxxx
PIC12LF1840	01 1011 110	x xxxx

3.3 Configuration Words

There are two Configuration Words, Configuration Word 1 (8007h) and Configuration Word 2 (8008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

3.4 Calibration Words

The internal calibration values are factory calibrated and stored in Calibration Words 1 and 2 (8009h, 800Ah).

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

REGISTER 3-2: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN1	BOREN0	$\overline{\text{CPD}}$	$\overline{\text{CP}}$
bit 13						bit 7

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
MCLRE	$\overline{\text{PWRTE}}$	WDTE1	WDTE0	FOSC2	FOSC1	FOSC0
bit 6						bit 0

Legend:	W = Writable bit	‘0’ = Bit is cleared
R = Readable bit	‘1’ = Bit is set	x = Bit is unknown
-n = Value at POR	U = Unimplemented bit, read as ‘0’	P = Programmable Bit

bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled

bit 12 **IESO:** Internal External Switchover bit
1 = Internal/External Switchover mode is enabled
0 = Internal/External Switchover mode is disabled

bit 11 **$\overline{\text{CLKOUTEN}}$:** Clock Out Enable bit
1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
0 = CLKOUT function is enabled on CLKOUT pin

bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits(1)
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit of the BORCON register
00 = BOR disabled

bit 8 **$\overline{\text{CPD}}$:** Data Code Protection bit(2)
1 = Data memory code protection is disabled
0 = Data memory code protection is enabled

bit 7 **$\overline{\text{CP}}$:** Code Protection bit(3)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 6 **MCLRE:** $\overline{\text{MCLR}}$/VPP Pin Function Select bit
<u>If LVP bit = 1:</u>
This bit is ignored.
<u>If LVP bit = 0:</u>
1 = $\overline{\text{MCLR}}$/VPP pin function is $\overline{\text{MCLR}}$; Weak pull-up enabled.
0 = $\overline{\text{MCLR}}$/VPP pin function is digital input; $\overline{\text{MCLR}}$ internally disabled; Weak pull-up under control of WPUA register.

bit 5 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
11 = WDT enabled
10 = WDT enabled while running and disabled in Sleep
01 = WDT controlled by the SWDTEN bit in the WDTCON register
00 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 = ECH: External Clock, High-Power mode: on CLKIN pin
110 = ECM: External Clock, Medium-Power mode: on CLKIN pin
101 = ECL: External Clock, Low-Power mode: on CLKIN pin
100 = INTOSC oscillator: I/O function on OSC1 pin
011 = EXTRC oscillator: RC function on OSC1 pin
010 = HS oscillator: High-speed crystal/resonator on OSC2 pin and OSC1 pin
001 = XT oscillator: Crystal/resonator on OSC2 pin and OSC1 pin
000 = LP oscillator: Low-power crystal on OSC2 pin and OSC1 pin

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire data EEPROM will be erased when the code protection is turned off during an erase.
3: The entire program memory will be erased when the code protection is turned off.

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REGISTER 3-3: CONFIGURATION WORD 2

R/P-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	U-1
LVP	$\overline{\text{DEBUG}}$	—	BORV	STVREN	PLLEN	—
bit 13						bit 7

U-1	U-1	R-1	U-1	U-1	R/P-1	R/P-1
—	—	RESERVED(2)	—	—	WRT1	WRT0
bit 6						bit 0

Legend:	W = Writable bit	'0' = Bit is cleared
R = Readable bit	'1' = Bit is set	x = Bit is unknown
-n = Value at POR	U = Unimplemented bit, read as '0'	P = Programmable Bit

bit 13 **LVP:** Low-Voltage Programming Enable bit(1)
1 = Low-voltage programming enabled
0 = HV on $\overline{\text{MCLR}}$/VPP must be used for programming

bit 12 **$\overline{\text{DEBUG}}$:** In-Circuit Debugger Mode bit
1 = In-Circuit Debugger disabled, ICSPCLK and ICSPDAT are general purpose I/O pins
0 = In-Circuit Debugger enabled, ICSPCLK and ICSPDAT are dedicated to the debugger

bit 11 **Unimplemented:** Read as '1'

bit 10 **BORV:** Brown-out Reset Voltage Selection bit
1 = Brown-out Reset voltage set to 1.9V
0 = Brown-out Reset voltage set to 2.5V

bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
1 = Stack Overflow or Underflow will cause a Reset
0 = Stack Overflow or Underflow will not cause a Reset

bit 8 **PLLEN:** PLL Enable bit
1 = 4xPLL enabled
0 = 4xPLL disabled

bit 7-5 **Unimplemented:** Read as '1'

bit 4 **Reserved:** Read as '1'(2)

bit 3-2 **Unimplemented:** Read as '1'

bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits
8 kW Flash memory (PIC16F1847/PIC16LF1847):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 1FFFh may be modified by EECON control
01 = 000h to FFFh write-protected, 1000h to 1FFFh may be modified by EECON control
00 = 000h to 1FFFh write-protected, no addresses may be modified by EECON control
4 kW Flash memory (PIC12F1840/PIC12LF1840):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to FFFh may be modified by EECON control
01 = 000h to 7FFh write-protected, 800h to FFFh may be modified by EECON control
00 = 000h to FFFh write-protected, no addresses may be modified by EECON control

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.
2: This bit must be programmed as a '1'.

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/ Verify mode via high-voltage:

- VPP – First entry mode
- VDD – First entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on MCLR from 0V to VIHH.
3. Raise the voltage on VDD FROM 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when Configuration Word 1 has MCLR disabled (MCLRE = 0), the power-up time is disabled (PWRTE = 0), the internal oscillator is selected (FOSC = 100), and ICSPCLK and ICSPDAT pins are driven by the user application, the device will execute code. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in Figure 8-2.

4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on MCLR from VDD or below to VIHH.

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 8-1.

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take MCLR to VDD or lower (VIL). See Figures 8-3 and 8-4.

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the PIC16F/LF1847 and PIC12F/LF1840 devices to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. MCLR is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, MCLR must be held at VIL for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figure 8-8 and Figure 8-9.

Exiting Program/Verify mode is done by no longer driving MCLR to VIL. See Figure 8-8 and Figure 8-9.

Note:	To enter LVP mode, the LSB of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.

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4.3 Program/Verify Commands

The PIC16F/LF1847 and PIC12F/LF1840 implement 13 programming commands; each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of T_{DLY} between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 4-1: COMMAND MAPPING

Command	Mapping							Data/Note
	Binary (MSb … LSb)						Hex	
Load Configuration	x	0	0	0	0	0	00h	0, data (14), 0
Load Data For Program Memory	x	0	0	0	1	0	02h	0, data (14), 0
Load Data For Data Memory	x	0	0	0	1	1	03h	0, data (8), zero (6), 0
Read Data From Program Memory	x	0	0	1	0	0	04h	0, data (14), 0
Read Data From Data Memory	x	0	0	1	0	1	05h	0, data (8), zero (6), 0
Increment Address	x	0	0	1	1	0	06h	—
Reset Address	x	1	0	1	1	0	16h	—
Begin Internally Timed Programming	x	0	1	0	0	0	08h	—
Begin Externally Timed Programming	x	1	1	0	0	0	18h	—
End Externally Timed Programming	x	0	1	0	1	0	0Ah	—
Bulk Erase Program Memory	x	0	1	0	0	1	09h	Internally Timed
Bulk Erase Data Memory	x	0	1	0	1	1	0Bh	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	11h	Internally Timed

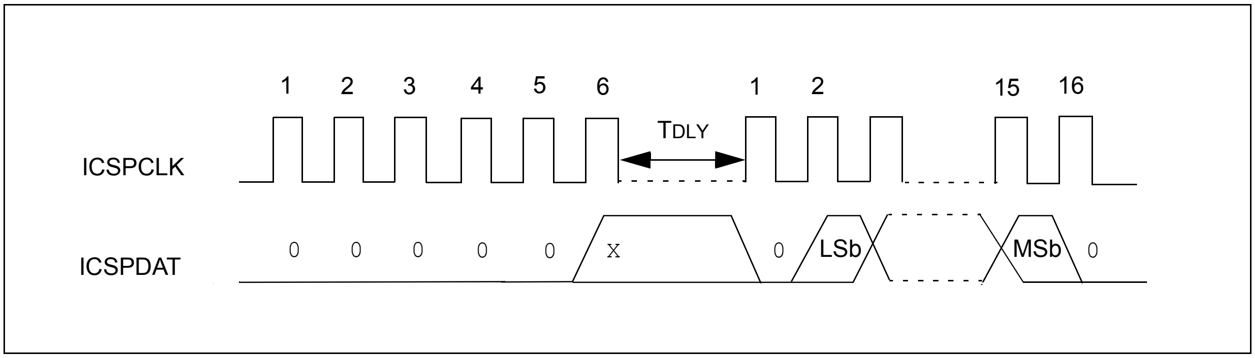
4.3.1 LOAD CONFIGURATION

The Load Configuration command is used to access the configuration memory (User ID Locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 4-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

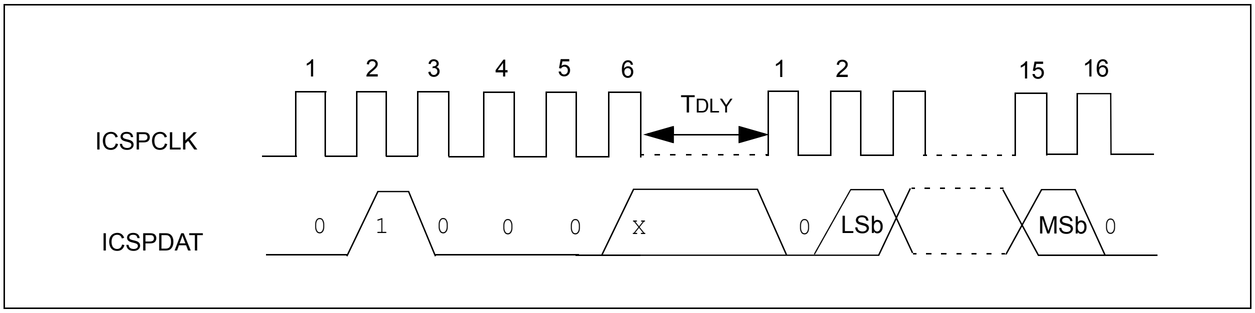
FIGURE 4-1: LOAD CONFIGURATION



4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY



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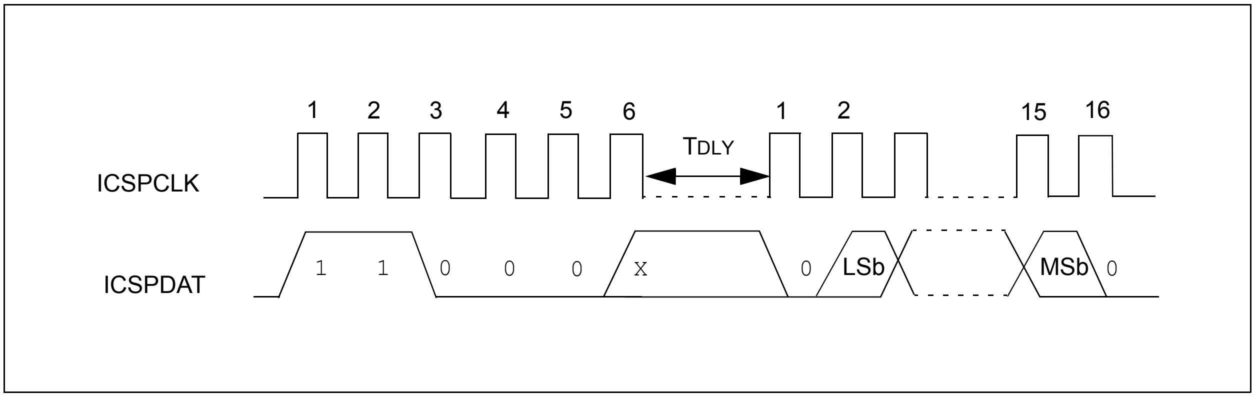
4.3.3 LOAD DATA FOR DATA MEMORY

The Load Data for Data Memory command will load a 14-bit "data word" when 16 cycles are applied. However, the data memory is only 8 bits wide and thus, only the first 8 bits of data after the Start bit will be programmed into the data memory. It is still necessary to cycle the clock the full 16 cycles in order to allow the internal circuitry to reset properly (see Figure 4-3).

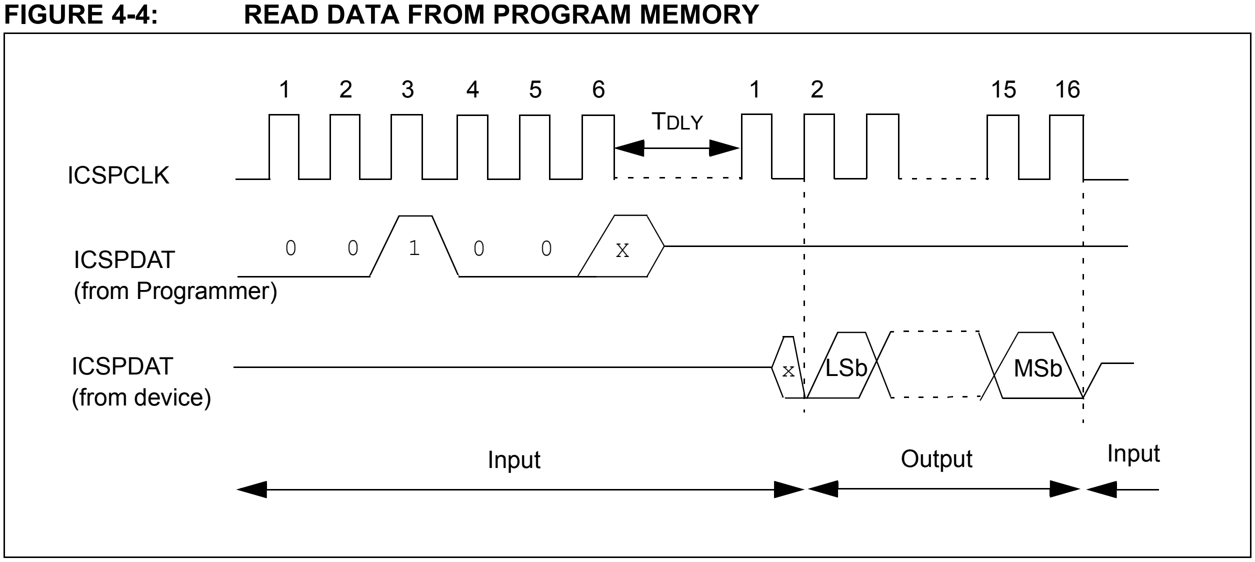
FIGURE 4-3: LOAD DATA FOR DATA MEMORY COMMAND



4.3.4 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ($\overline{\text{CP}}$), the data will be read as zeros (see Figure 4-4).

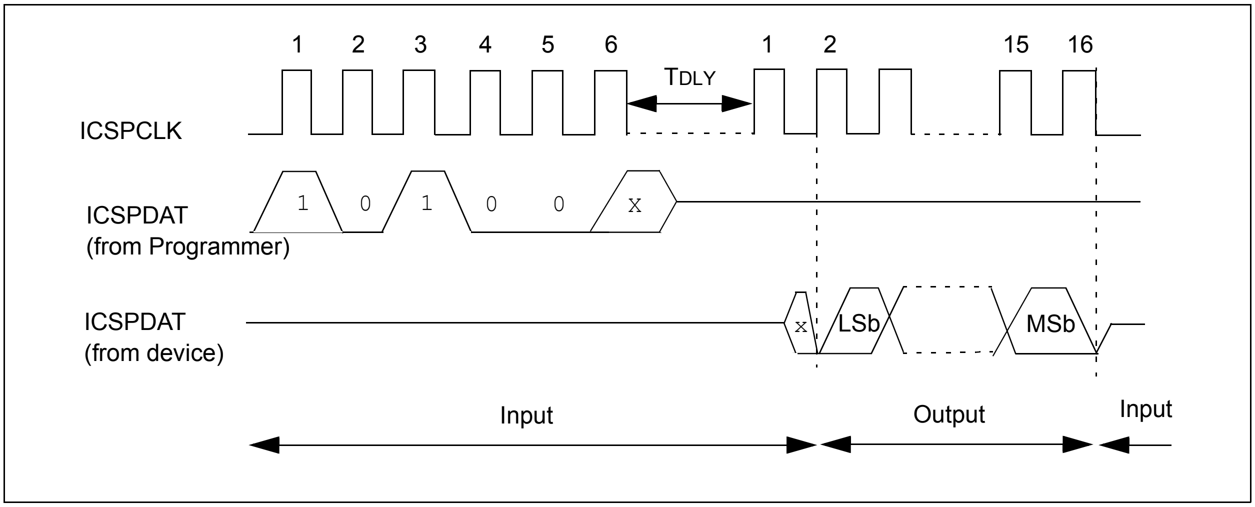
FIGURE 4-4: READ DATA FROM PROGRAM MEMORY



4.3.5 READ DATA FROM DATA MEMORY

The Read Data from Data Memory command will transmit data bits out of the data memory starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the second rising edge, and it will revert to Input mode (high-impedance) after the 16th rising edge. The data memory is 8 bits wide, and therefore, only the first 8 bits that are output are actual data. If the data memory is code-protected, the data is read as all zeros. A timing diagram of this command is shown in Figure 4-5.

FIGURE 4-5: READ DATA FROM DATA MEMORY COMMAND

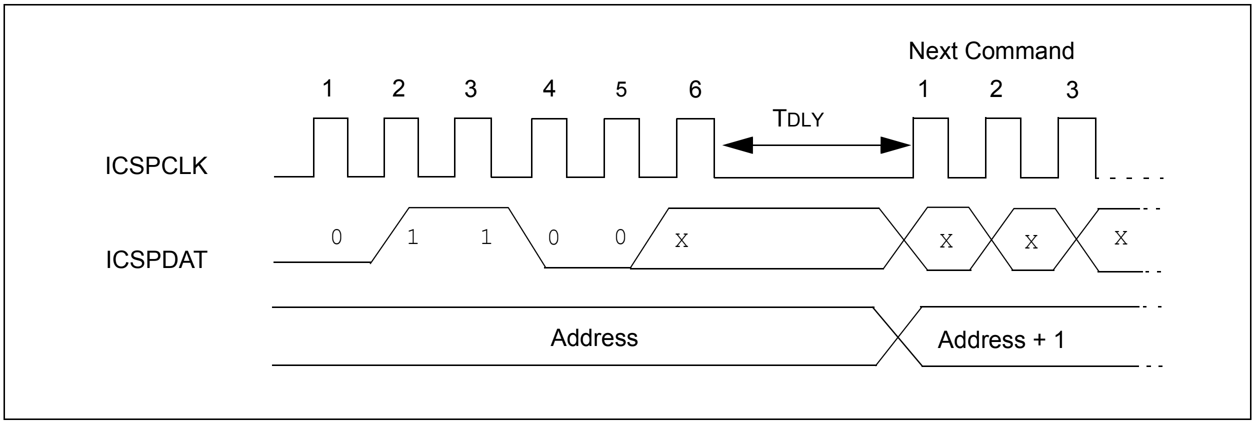


4.3.6 INCREMENT ADDRESS

The address is incremented when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Reset Address command or exit Program/Verify mode and re-enter it.

If the address is incremented from address 7FFFh, it will wrap-around to location 0000h. If the address is incremented from FFFFh, it will wrap-around to location 8000h.

FIGURE 4-6: INCREMENT ADDRESS



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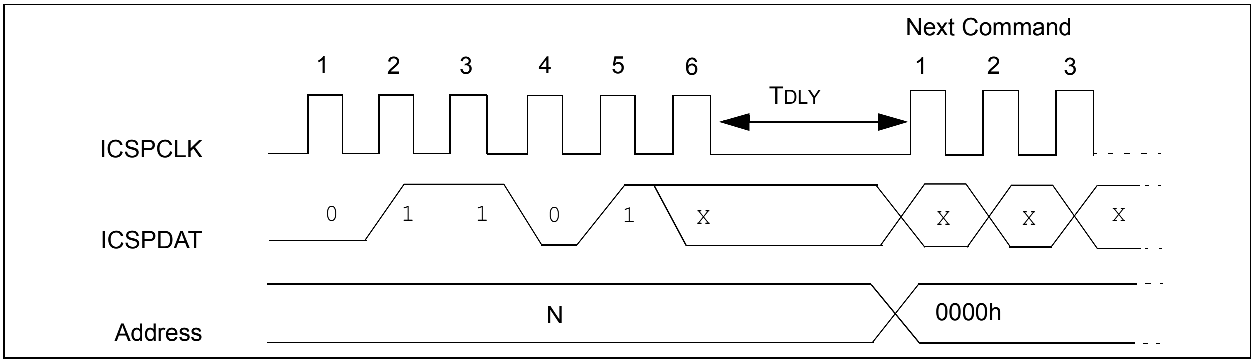
4.3.7 RESET ADDRESS

The Reset Address command will reset the address to 0000h, regardless of the current value. The address is used in program memory or the configuration memory.

FIGURE 4-7: RESET ADDRESS



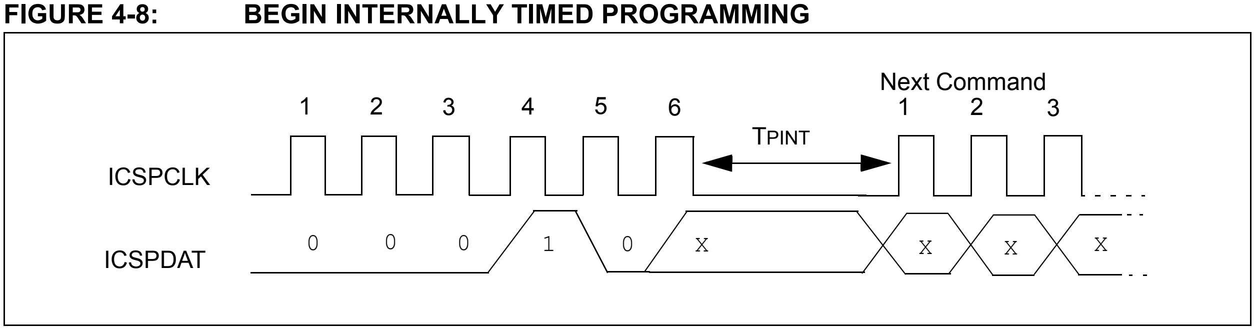
4.3.8 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, TPINT, for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed. However, the EEPROM memory address that is being programmed is erased prior to being programmed with internally timed programming.

FIGURE 4-8: BEGIN INTERNALLY TIMED PROGRAMMING

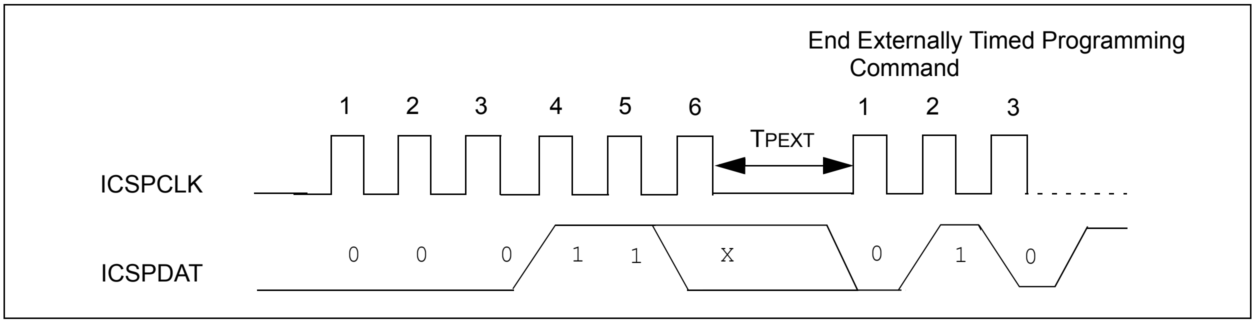


4.3.9 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration, Load Data for Program Memory or Load Data for Data Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming the End Externally Timed Programming command must be sent in the specified time window defined by TPEXT. No internal erase is performed for the data EEPROM, therefore, the device should be erased prior to executing this command.

The Begin Externally Timed Programming command cannot be used for programming the Configuration Words (see Figure 4-9).

FIGURE 4-9: BEGIN EXTERNALLY TIMED PROGRAMMING

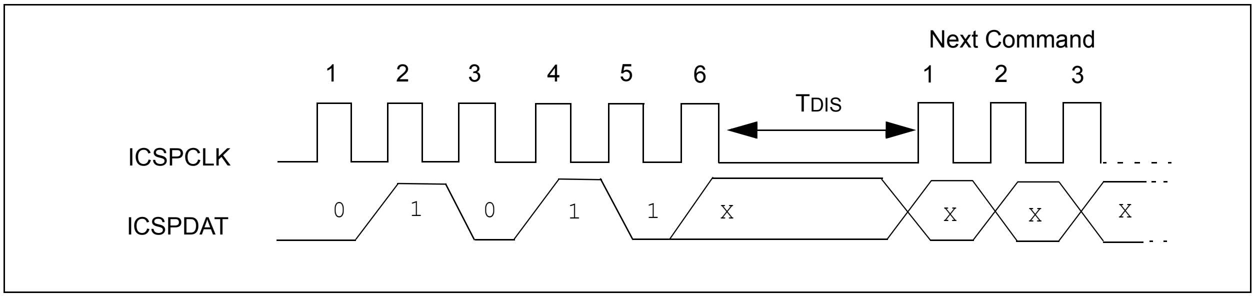


4.3.10 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by TPEXT after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (TDIS) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands (see Figure 4-10).

FIGURE 4-10: END EXTERNALLY TIMED PROGRAMMING



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4.3.11 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions dependent on the current state of the address.

Address 0000h-7FFFh:

- Program Memory is erased
- Configuration Words are erased
- If $\overline{CPD}$ = 0, Data Memory is erased

Address 8000h-8008h:

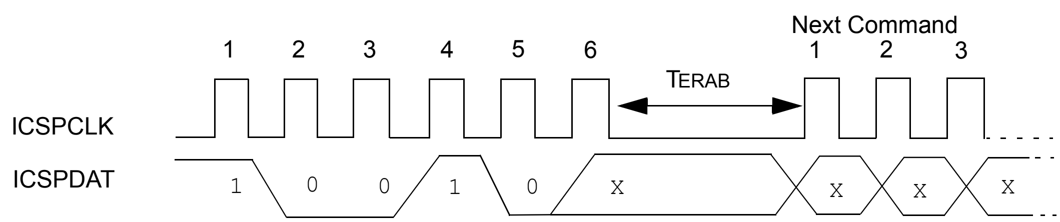
- Program Memory is erased
- Configuration Words are erased
- User ID Locations are erased
- If $\overline{CPD}$ = 0, Data Memory is erased

A Bulk Erase Program Memory command should not be issued when the address is greater than 8008h.

After receiving the Bulk Erase Program Memory command the erase will not complete until the time interval, TERAB, has expired.

Note:	The code protection Configuration bit ($\overline{CP}$) has no effect on the Bulk Erase Program Memory command.

FIGURE 4-11: BULK ERASE PROGRAM MEMORY



4.3.12 BULK ERASE DATA MEMORY

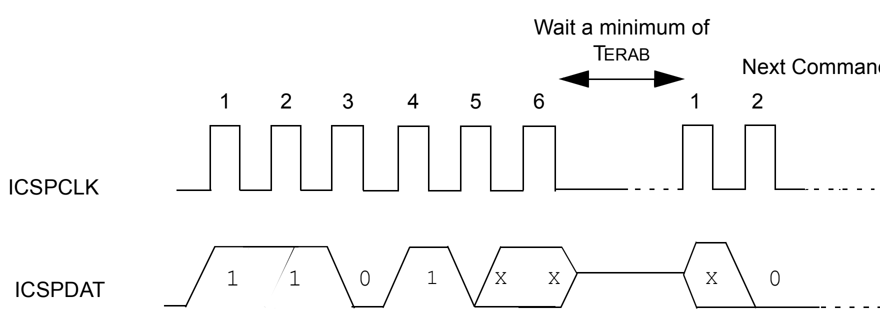
To perform an erase of the data memory, after a Bulk Erase Data Memory command, wait a minimum of TERAB to complete Bulk Erase.

To erase data memory when data code-protect is active ($\overline{CPD}$ = 0), the Bulk Erase Program Memory command should be used.

After receiving the Bulk Erase Data Memory command, the erase will not complete until the time interval, TERAB, has expired.

Note:	Data memory will not erase if code-protected ($\overline{CPD}$ = 0).

FIGURE 4-12: BULK ERASE DATA MEMORY COMMAND



4.3.13 ROW ERASE PROGRAM MEMORY

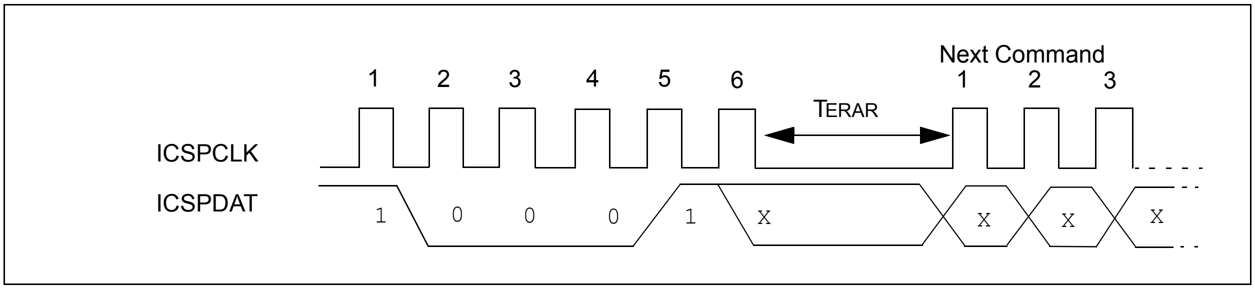
The Row Erase Program Memory command will erase an individual row. Refer to Table 4-2 for row sizes of specific devices and the PC bits used to address them. If the program memory is code-protected the Row Erase Program Memory command will be ignored. When the address is 8000h-8008h the Row Erase Program Memory command will only erase the user ID locations regardless of the setting of the $\overline{CP}$ Configuration bit.

After receiving the Row Erase Program Memory command the erase will not complete until the time interval, TERAR, has expired.

TABLE 4-2: PROGRAMMING ROW SIZE AND LATCHES

Devices	PC	Row Size	Number of Latches
PIC12F/LF1840	<15:5>	32	32
PIC16F/LF1847	<15:5>	32	32

FIGURE 4-13: ROW ERASE PROGRAM MEMORY



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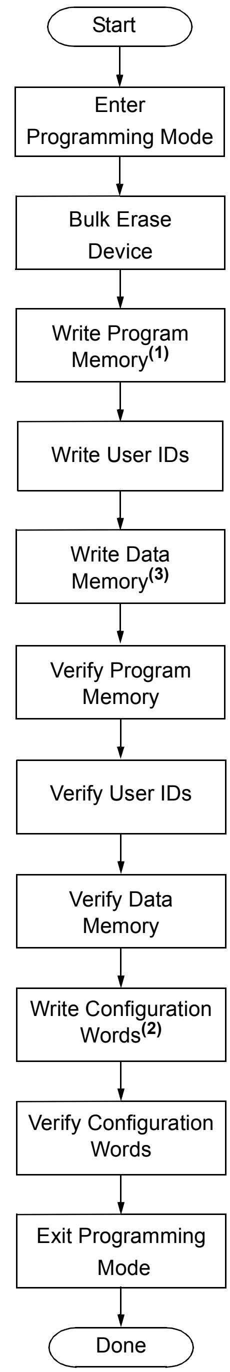
5.0 PROGRAMMING ALGORITHMS

The PIC16F/LF1847/PIC12F/LF1840 devices use internal latches to temporarily store the 14-bit words used for programming. Refer to Table 4-2 for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The PC's address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which location(s) in memory are written. Writes cannot cross the physical boundary. For example, with the PIC16F1847, attempting to write from address 0002h-0021h will result in data being written to 0020h-003Fh.

If more than the maximum number of data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.

FIGURE 5-1: DEVICE PROGRAM/VERIFY FLOWCHART



Note 1: See Figure 5-2.
2: See Figure 5-5.
3: See Figure 5-6.

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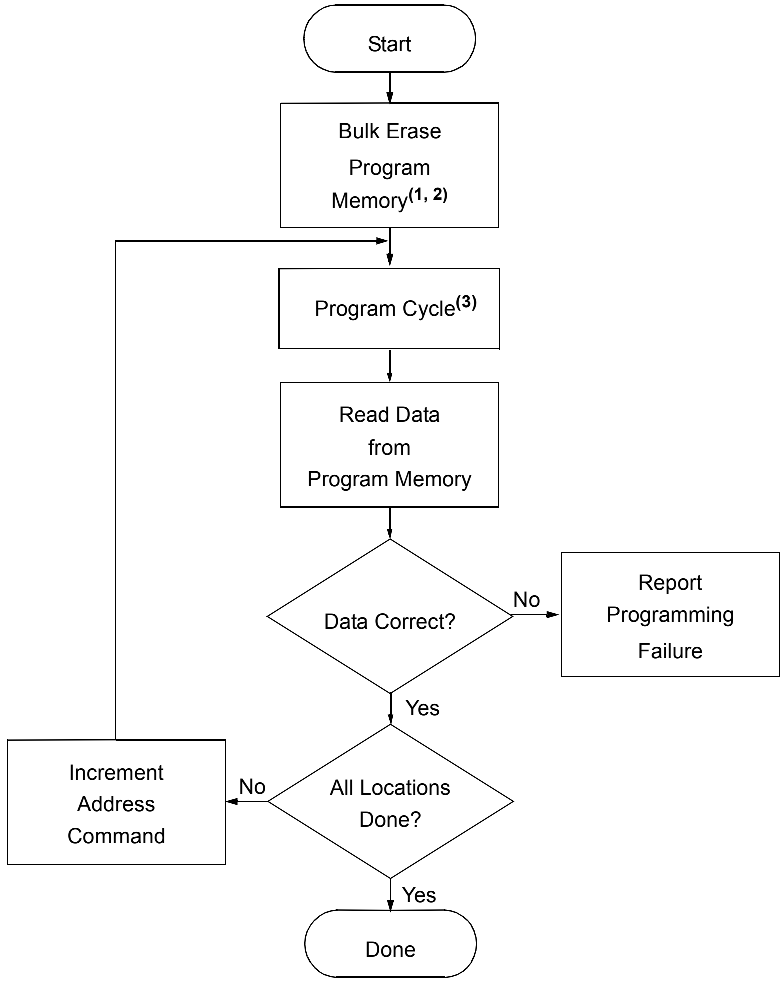
FIGURE 5-2: PROGRAM MEMORY FLOWCHART



Note 1: This step is optional if device has already been erased or has not been previously programmed.

2: If the device is code-protected or must be completely erased, then Bulk Erase device per Figure 5-8.

3: See Figure 5-3 or Figure 5-4.

FIGURE 5-3: ONE-WORD PROGRAM CYCLE

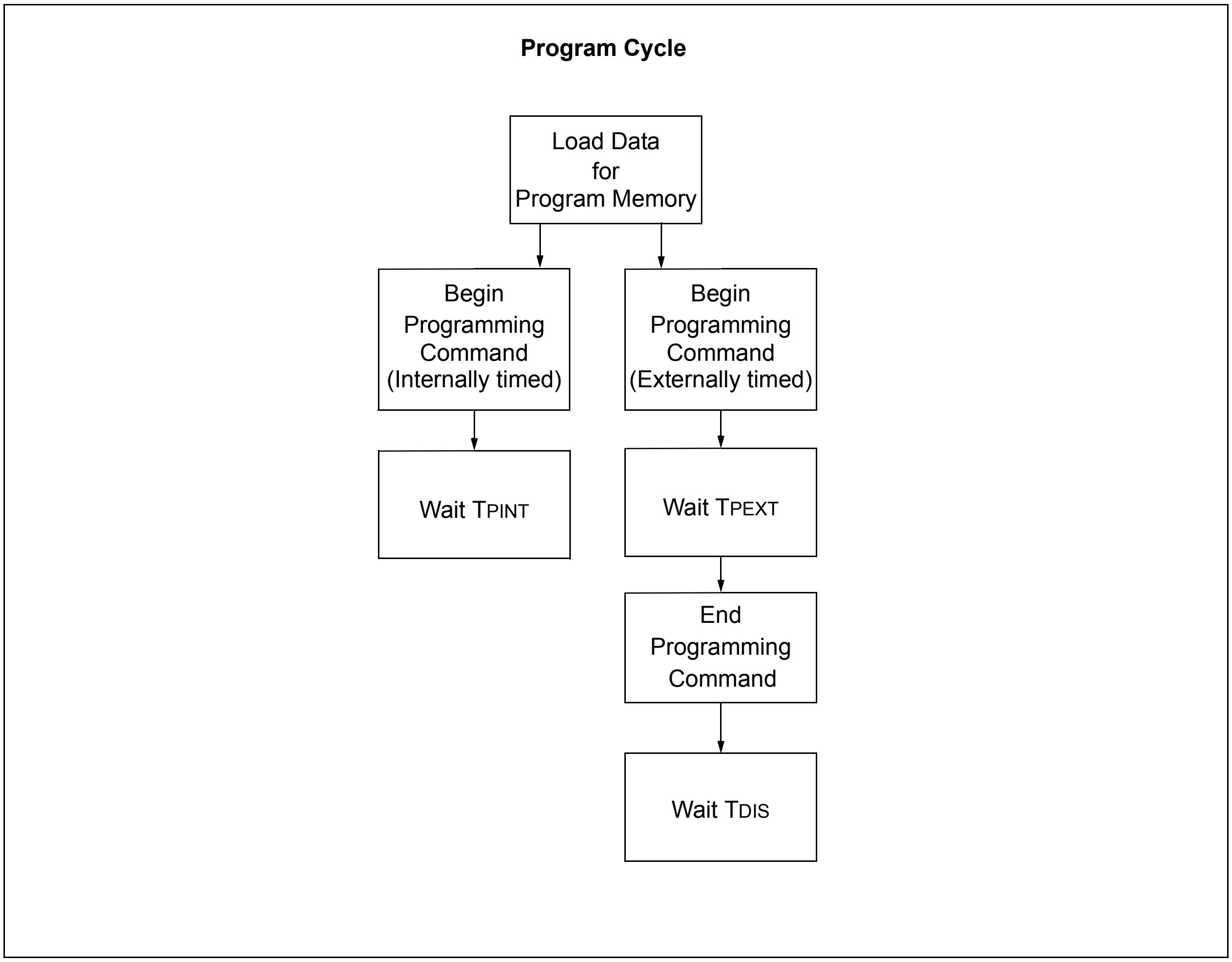


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FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE

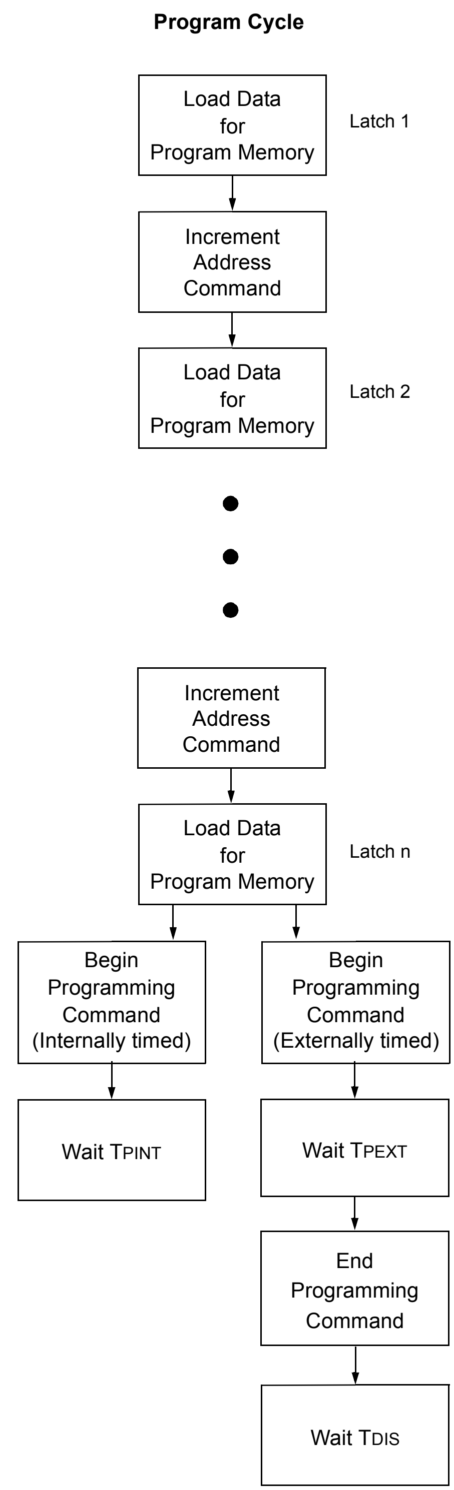
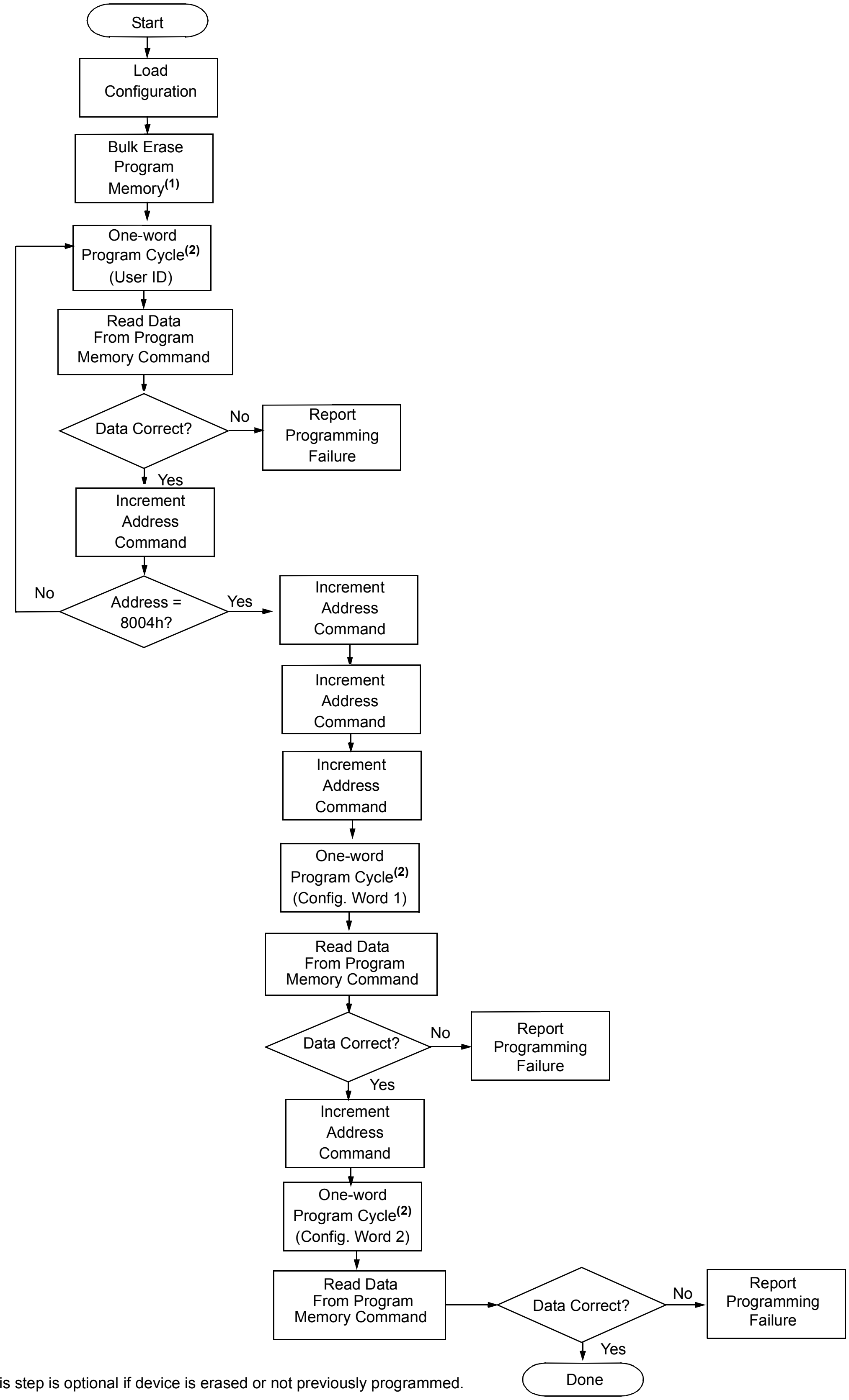


FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART



Note 1: This step is optional if device is erased or not previously programmed.
2: See Figure 5-3.

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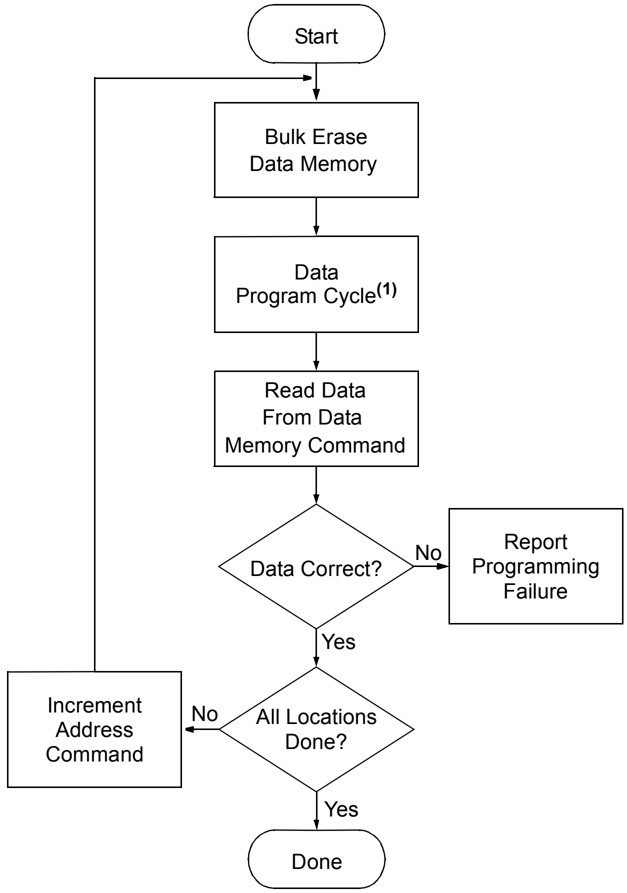
FIGURE 5-6: DATA MEMORY PROGRAM FLOWCHART



Note 1: See Figure 5-7.

FIGURE 5-7: DATA MEMORY PROGRAM CYCLE

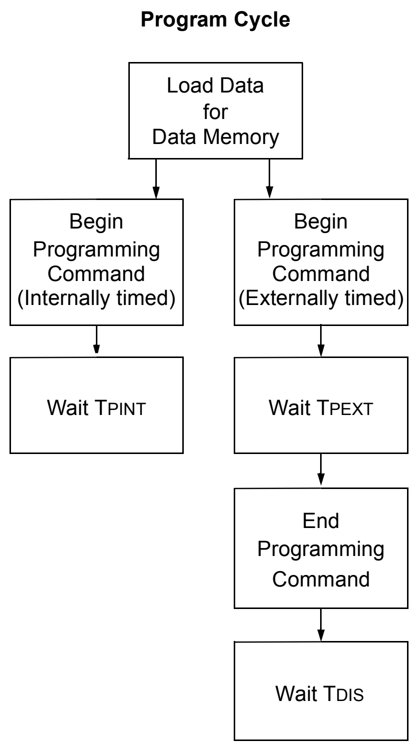
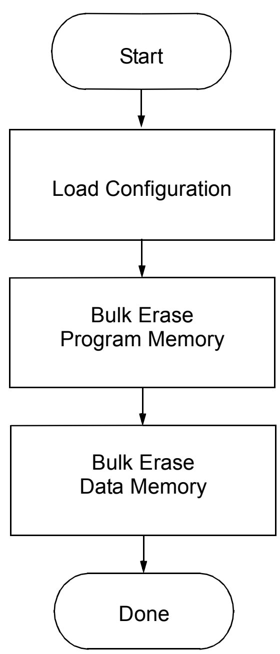


FIGURE 5-8: ERASE FLOWCHART



Note: This sequence does not erase the Calibration Words.

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6.0 CODE PROTECTION

Code protection is controlled using the $\overline{CP}$ bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-7FFFh) read as all '0'. Further programming is disabled for the program memory (0000h-7FFFh).

Data memory is protected with its own code-protect bit ($\overline{CPD}$). When data code protection is enabled ($\overline{CPD}$ = 0), all data memory locations read as '0'. Further programming is disabled for the data memory. Data memory can still be programmed and read during program execution.

The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

6.1 Program Memory

Code protection is enabled by programming the $\overline{CP}$ bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

6.2 Data Memory

Data memory protection is enabled by programming the $\overline{CPD}$ bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

Note:	To ensure system security, if $\overline{CPD}$ bit = 0, the Bulk Erase Program Memory command will also erase data memory.

7.0 HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: Configuration Word 1 is stored at 8007h on the PIC16F/LF1847 and PIC12F/LF1840. In the hex file this will be referenced as 1000Eh-1000Fh).

7.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

7.2 Device ID and Revision

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID (excluding the revision) against the value read from the part. On a mismatch condition the programmer should generate a warning message.

7.3 Data EEPROM

The programmer should be able to read data memory information from a hex file and write data memory contents to a hex file.

The physical address range of the 256 byte data memory is 0000h-00FFh. However, these addresses are logically mapped to address 1E000h-1E1FFh in the hex file. This provides a way of differentiating between the data and program memory locations in this range. The format for data memory storage is one data byte per address location, LSb aligned.

7.4 Checksum Computation

The checksum is calculated by two different methods dependent on the setting of the $\overline{CP}$ Configuration bit.

TABLE 7-1: CONFIGURATION WORD MASK VALUES

Device	Config. Word 1 Mask	Config. Word 2 Mask
PIC12F1840	3FFFh	3713h
PIC12LF1840	3FFFh	3713h
PIC16F1847	3FFFh	3713h
PIC16LF1847	3FFFh	3713h

7.4.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the PIC16F/LF1847 and PIC12F/LF1840 program memory locations and adding up the program memory data starting at address 0000h, up to the maximum user addressable location. Any Carry bit exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

Note:	Data memory does not effect the checksum.

EXAMPLE 7-1: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED PIC12F1840, BLANK DEVICE

```
PIC12F1840   Sum of Memory addresses 0000h-0FFFh           F000h
             Configuration Word 1                          3FFFh
             Configuration Word 1 mask                     3FFFh
             Configuration Word 2                          3FFFh
             Configuration Word 2 mask                     3713h
             Checksum          = F000h + (3FFFh and 3FFFh) + (3FFFh and 3713h)
                               = F000h + 3FFFh + 3713h
                               = 6712h
```

EXAMPLE 7-2: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED PIC12LF1840, 00AAh AT FIRST AND LAST ADDRESS

```
PIC12LF1840  Sum of Memory addresses 0000h-0FFFh           7156h
             Configuration Word 1                          3FFFh
             Configuration Word 1 mask                     3FFFh
             Configuration Word 2                          3FFFh
             Configuration Word 2 mask                     3713h
             Checksum = 7156h + (3FFFh and 3FFFh) + (3FFFh and 3713h)
                               = 7156h + 3FFFh + 3713h
                               = E868h
```

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7.4.2 PROGRAM CODE PROTECTION ENABLED

With the program code protection enabled, the checksum is computed in the following manner: The Least Significant nibble of each user ID is used to create a 16-bit value. The masked value of user ID location 8000h is the Most Significant nibble. This sum of user ID's is summed with the Configuration Words (all unimplemented Configuration bits are masked to '0').

Note:	Data memory does not effect the checksum.

EXAMPLE 7-3: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED PIC12F1840, BLANK DEVICE

```
PIC12F1840   Configuration Word 1                            3F7Fh
             Configuration Word 1 mask                       3FFFh
             Configuration Word 2                            3FFFh
             Configuration Word 2 mask                       3713h
             User ID (8000h)                                 0006h
             User ID (8001h)                                 0007h
             User ID (8002h)                                 0001h
             User ID (8003h)                                 0002h
             Sum of User IDs = (0006h and 000Fh) << 12 + (0007h and 000Fh) << 8 +
                                 (0001h and 000Fh) << 4 + (0002h and 000Fh)
                               = 6000h + 0700h + 0010h + 0002h
                               = 6712h
              Checksum         = (3F7Fh and 3FFFh) + (3FFFh and 3713h) + Sum of User IDs
                               = 3F7Fh +3713h + 6712h
                               = DDA4h
```

EXAMPLE 7-4: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED PIC12LF1840, 00AAh AT FIRST AND LAST ADDRESS

```
PIC12LF1840   Configuration Word 1                           3F7Fh
              Configuration Word 1 mask                      3FFFh
              Configuration Word 2                           3FFFh
              Configuration Word 2 mask                      3713h
              User ID (8000h)                                000Eh
              User ID (8001h)                                0008h
              User ID (8002h)                                0006h
              User ID (8003h)                                0008h
              Sum of User IDs   = (000Eh and 000Fh) << 12 + (0008h and 000Fh) << 8 +
                                    (0006h and 000Fh) << 4 + (0008h and 000Fh)
                                = E000h + 0800h + 0060h + 0008h
                                = E868h
              Checksum          = (3F7Fh and 3FFFh) + (3FFFh and 3713h) + Sum of User IDs
                                = 3F7Fh +3713h + E868h
                                = 5EFAh
```

8.0 ELECTRICAL SPECIFICATIONS

Refer to device specific data sheet for absolute maximum ratings.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +85°C				
Sym.	**Characteristics**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
Supply Voltages and Currents							
VDD	**VDD**						
	Read/Write and Row Erase operations	PIC12F1840 PIC16F1847	2.1	—	5.5	V	
		PIC12LF1840 PIC16LF1847	2.1	—	3.6	V	
	Bulk Erase operations	PIC12F1840 PIC16F1847	2.7	—	5.5	V	
		PIC12LF1840 PIC16LF1847	2.7	—	3.6	V	
IDDI	Current on VDD, Idle		—	—	1.0	mA	
IDDP	Current on VDD, Programming		—	—	3.0	mA	
	VPP						
IPP	Current on $\overline{MCLR}$/VPP		—	—	600	μA	
VIHH	High voltage on $\overline{MCLR}$/VPP for Program/Verify mode entry		8.0	—	9.0	V	
TVHHR	$\overline{MCLR}$ rise time (VIL to VIHH) for Program/Verify mode entry		—	—	1.0	μs	
	I/O pins						
VIH	(ICSPCLK, ICSPDAT, $\overline{MCLR}$/VPP) input high level		0.8 VDD	—	—	V	
VIL	(ICSPCLK, ICSPDAT, $\overline{MCLR}$/VPP) input low level		—	—	0.2 VDD	V	
VOH	ICSPDAT output high level		VDD-0.7 VDD-0.7 VDD-0.7	—	—	V	IOH = 3.5 mA, VDD = 5V IOH = 3 mA, VDD = 3.3V IOH = 2 mA, VDD = 1.8V
VOL	ICSPDAT output low level		—	—	VSS+0.6 VSS+0.6 VSS+0.6	V	IOH = 8 mA, VDD = 5V IOH = 6 mA, VDD = 3.3V IOH = 3 mA, VDD = 1.8V
Programming Mode Entry and Exit							
TENTS	Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before VDD or $\overline{MCLR}$↑		100	—	—	ns	
TENTH	Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after VDD or $\overline{MCLR}$↑		250	—	—	μs	
Serial Program/Verify							
TCKL	Clock Low Pulse Width		100	—	—	ns	
TCKH	Clock High Pulse Width		100	—	—	ns	
TDS	Data in setup time before clock↓		100	—	—	ns	
TDH	Data in hold time after clock↓		100	—	—	ns	
TCO	Clock↑ to data out valid (during a Read Data command)		0	—	80	ns	
TLZD	Clock↓ to data low-impedance (during a Read Data command)		0	—	80	ns	
THZD	Clock↓ to data high-impedance (during a Read Data command)		0	—	80	ns	
TDLY	Data input not driven to next clock input (delay required between command/data or command/command)		1.0	—	—	μs	
TERAB	Bulk Erase cycle time		—	—	5	ms	
TERAR	Row Erase cycle time		—	—	2.5	ms	

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TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY

AC/DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +85°C				
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
TPINT	Internally timed programming operation time	— — —	— — —	2.5 5 5	ms ms ms	Program memory Configuration Words EEPROM
TPEXT	Externally timed programming pulse	1.0	—	2.1	ms	
TDIS	Time delay from program to compare (HV discharge time)	100	—	—	µs	
TEXIT	Time delay when exiting Program/Verify mode	1	—	—	µs	

8.1 AC Timing Diagrams

FIGURE 8-1: PROGRAMMING MODE ENTRY – VDD FIRST

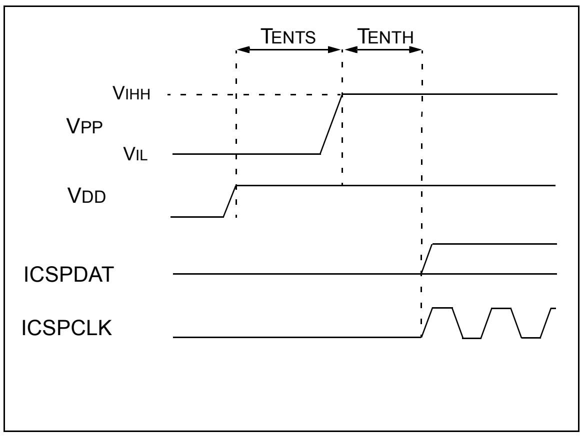

FIGURE 8-2: PROGRAMMING MODE ENTRY – VPP FIRST

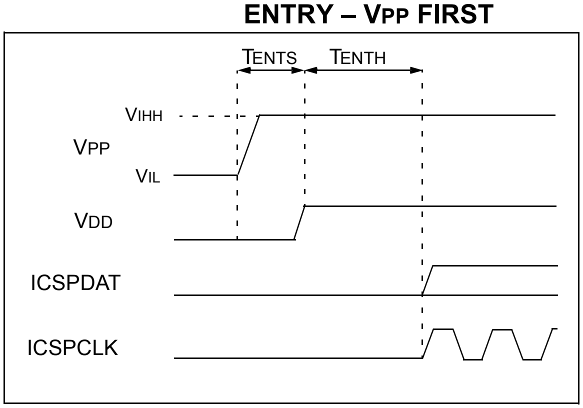

FIGURE 8-3: PROGRAMMING MODE EXIT – VPP LAST

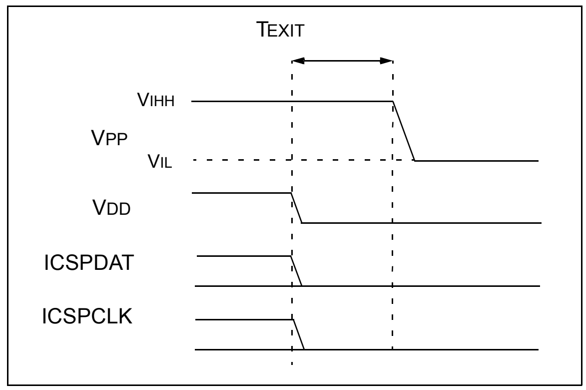

FIGURE 8-4: PROGRAMMING MODE EXIT – VDD LAST

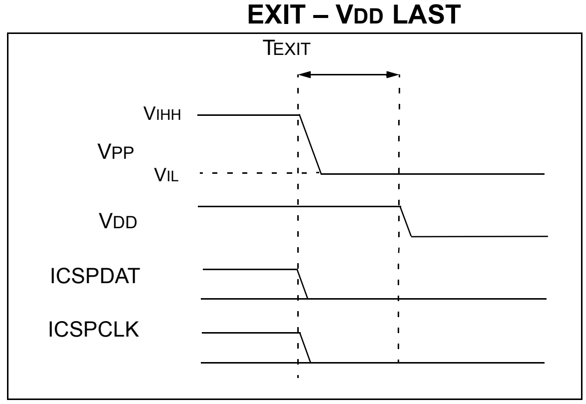

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FIGURE 8-5: CLOCK AND DATA TIMING

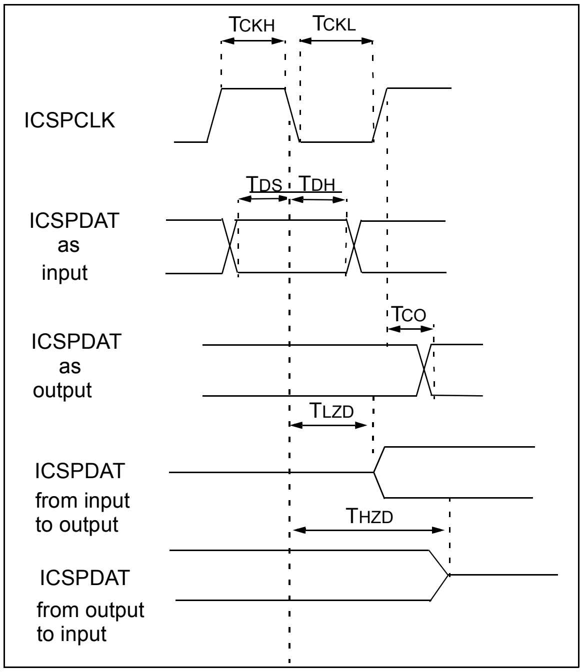

FIGURE 8-6: WRITE COMMAND-PAYLOAD TIMING

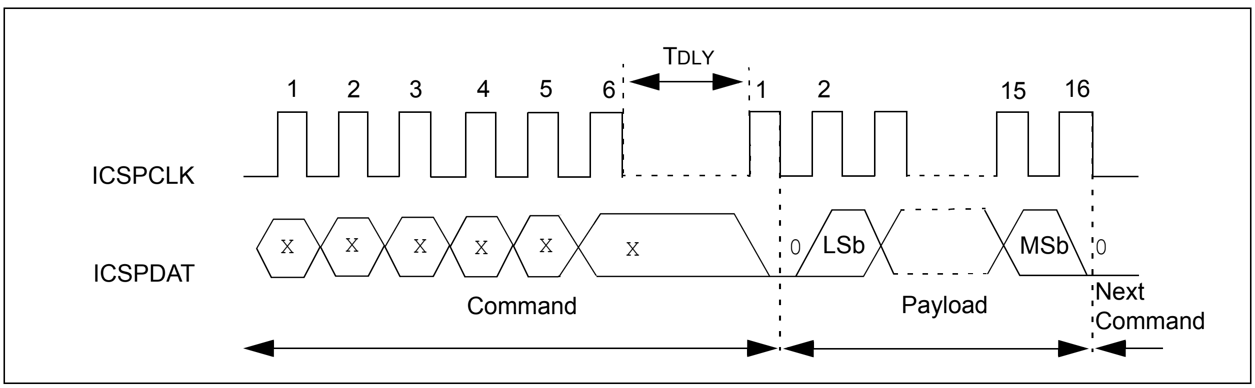

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FIGURE 8-7: READ COMMAND-PAYLOAD TIMING

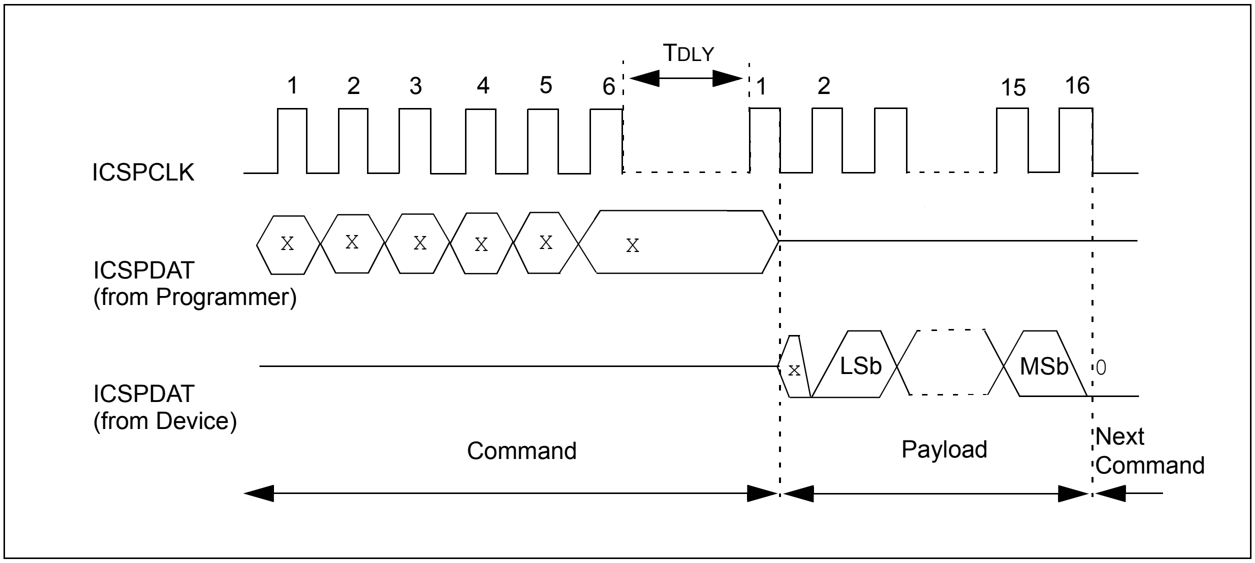


FIGURE 8-8: LVP ENTRY (POWERING UP)

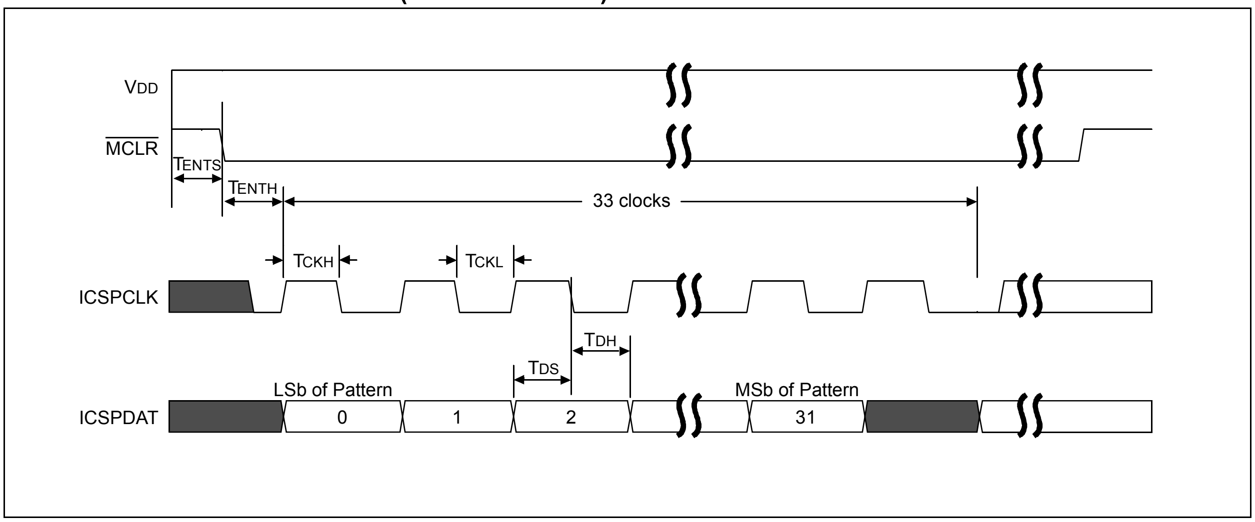
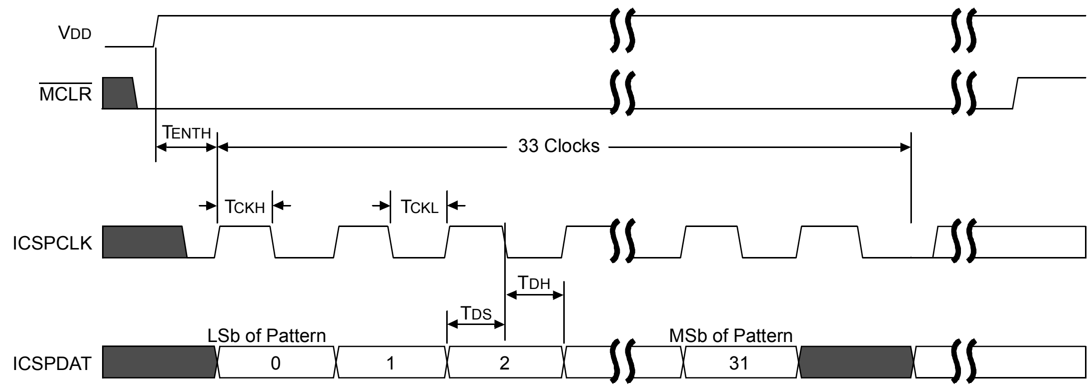


FIGURE 8-9: LVP ENTRY (POWERED)



Note 1: Sequence matching can start with no edge on $\overline{\text{MCLR}}$ first.

APPENDIX A: REVISION HISTORY

Revision A (08/2010)

Original release of this document.

NOTES:

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Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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Printed on recycled paper.

ISBN: 978-1-60932-472-8

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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08/04/10

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