

Some key facts about avalanche

About this document



Scope and purpose

The document aims to provide details about avalanche that are often overlooked, disregarded or simply not commonly known. Theory is examined in order to establish a baseline that is used later on when considering examples. Some relevant comments about common avalanche test methods are also given. The final section of the document covers repetitive avalanche.

Intended audience

Power supply design engineers, applications engineers, students.

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1 Introduction

1 Introduction

Avalanche (and especially repetitive avalanche) do not necessarily belong to the list of common parameters considered by a MOSFET manufacturer when developing a new family. The reason for this is quite simple: avalanche typically occurs when the breakdown voltage ($V_{BR(DSS)}$) of the MOSFET is exceeded, meaning that the part is being used outside its datasheet specification. Consequently, a designer should make all reasonable attempts NOT to operate a MOSFET in avalanche.

In some applications with long operating lifetime, such as telecom (AC-DC rectifiers, DC-DC bricks) or server power supply units, the increasing requirement to comply with standards that impose significant voltage derating (such as IPC9592B-2012) leads designers in the direction of “zero-avalanche-tolerance”. However, IPC9592 and other similar standards do not necessarily stipulate any derating guidelines for abnormal conditions.

Additionally, low voltage drives applications such as forklifts and power tools are rarely subject to voltage derating, due to their short operating lifetime and/or their high loop inductances (L_{loop}) that make them more likely to face high V_{DS} spikes and, therefore, avalanche conditions.

Furthermore, due to challenging efficiency requirements, designers of other high performance applications such as servers -*do not confuse with server power supplies*- would prefer to use repetitive-avalanche-proof MOSFETs to avoid having to move to a higher voltage class.

As a result of the high number of ‘special cases’ within the multitude of applications where MOSFETs are used, ruggedness against avalanche is a key requirement for users that MOSFET manufacturers cannot afford to ignore during any new technology development. Regarding ‘repetitive avalanche’ in particular, the absence of any rating within a datasheet does not necessarily mean that it was not investigated during the design phase of the technology.

In the following sections of this document, we will list key facts about avalanche that any designer should keep in mind when using industrial and standard versions of Infineon’s OptiMOS™ families of MOSFETs. We therefore focus on OptiMOS™ 3 and the subsequent families that are all n-channel enhancement mode trench power MOSFETs. Consequently, other MOSFET families are outside the scope of this document.

For engineers who do not want to devote too much time to the theory behind avalanche, section 2.1.2 provides a simulation circuit that can be used to monitor the temperatures at various locations of the MOSFET during avalanche. Additionally, specific examples are given in sections 3.2.1 and 3.2.2 to allow engineers to assess if a MOSFET is avalanche safe under their own application conditions. Finally, a formula supplied in section 3.3 assists with rapid computation of avalanche energy when the circuit presents a different loop inductance.

2 Single pulse avalanche

2 Single pulse avalanche

2.1 What is single pulse avalanche?

2.1.1 Brief reminder about avalanche

The avalanche mechanism has already been comprehensively explained in other publications, such as [1]. It originates from an operation above the $V_{BR(DSS)}$ of the FET, which then induces electric fields in excess of the critical electric field (E_C). The acceleration applied to the free carriers by these strong electric fields provides them with enough energy to release electron-hole pairs via impact ionization. This phenomenon cannot be controlled, potentially leading to large currents being generated and/or high temperature rise within the silicon. Ultimately, such uncontrolled events can lead to the destruction of the device.

Avalanche manifests itself through a clamping of the V_{DS} spike, as shown in Figure 1, where we can already observe that the MOSFET is clamped higher than the minimum $V_{BR(DSS)}$ rating provided in the datasheet at a junction temperature (T_j) of 25°C ($V_{BR(DSS)(min,25)}$). Further details about the actual clamping voltage will be provided in section 2.1.3

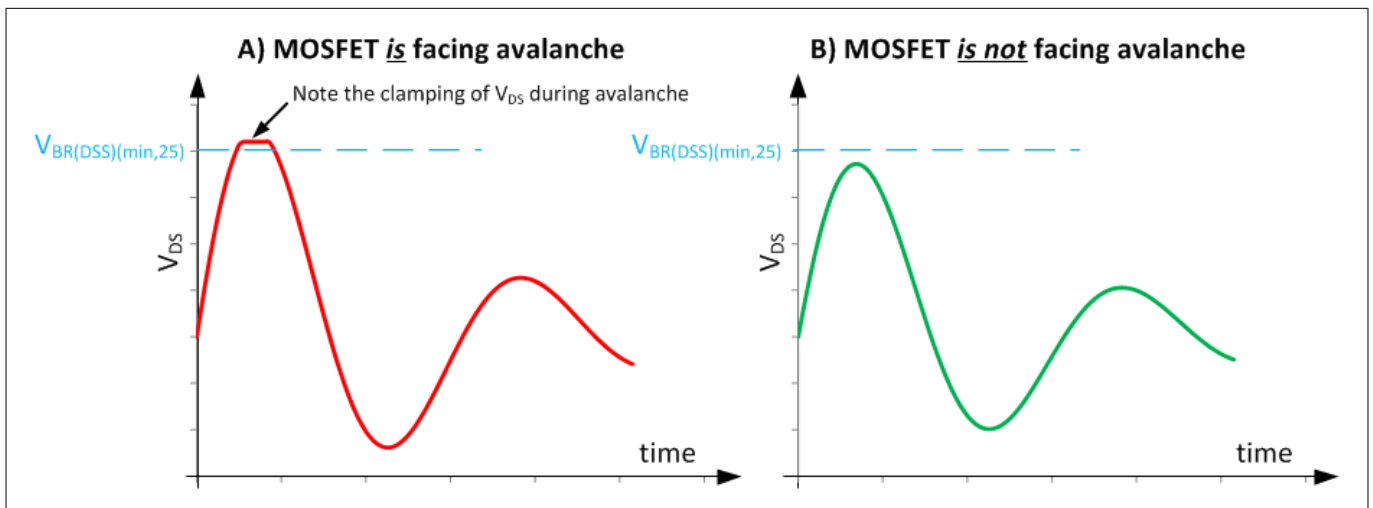


Figure 1 V_{DS} waveforms when MOSFET is in and is not in avalanche

2.1.2 Defining single pulse avalanche

Single pulse avalanche is an isolated event that can potentially (but not necessarily) generate significant avalanche current and/or energy. When the energy and current generated by such an event are low, the impact on the MOSFET is negligible. However, if avalanche induces either high energies or high currents, the MOSFET can be destroyed, as we shall see in section 2.2 when discussing the failure mechanisms.

For that matter, note that energy is not the real issue here, it is current and temperature that cause the failure. You might then wonder: if temperature is so important, why do we provide a single pulse avalanche rating within datasheets without any reference to the thermal properties of the test platform (e.g. R_{thJA})? Simply because avalanche events occur over such short time periods that the heat doesn't have time to be transferred to the PCB. The following statement will validate this.

As a starting point, we realize that the thermal behavior of our MOSFETs is usually represented in our PSpice models with the help of a high order Cauer network including all necessary thermal resistances and capacitances (R_{thi} and C_{thi}). An example for the IPB072N15N3 G is introduced in Figure 2.

2 Single pulse avalanche

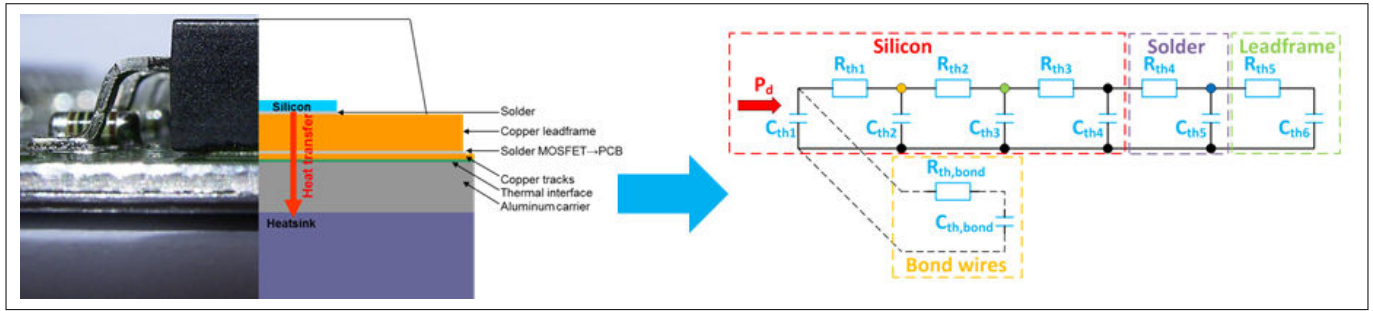


Figure 2 IPB072N15N3 G - from MOSFET to thermal network

The network representation for the MOSFET is used to generate the $Z_{thJC} = f(\text{time})$ graph provided inside our datasheets, as summarized in Figure 3.

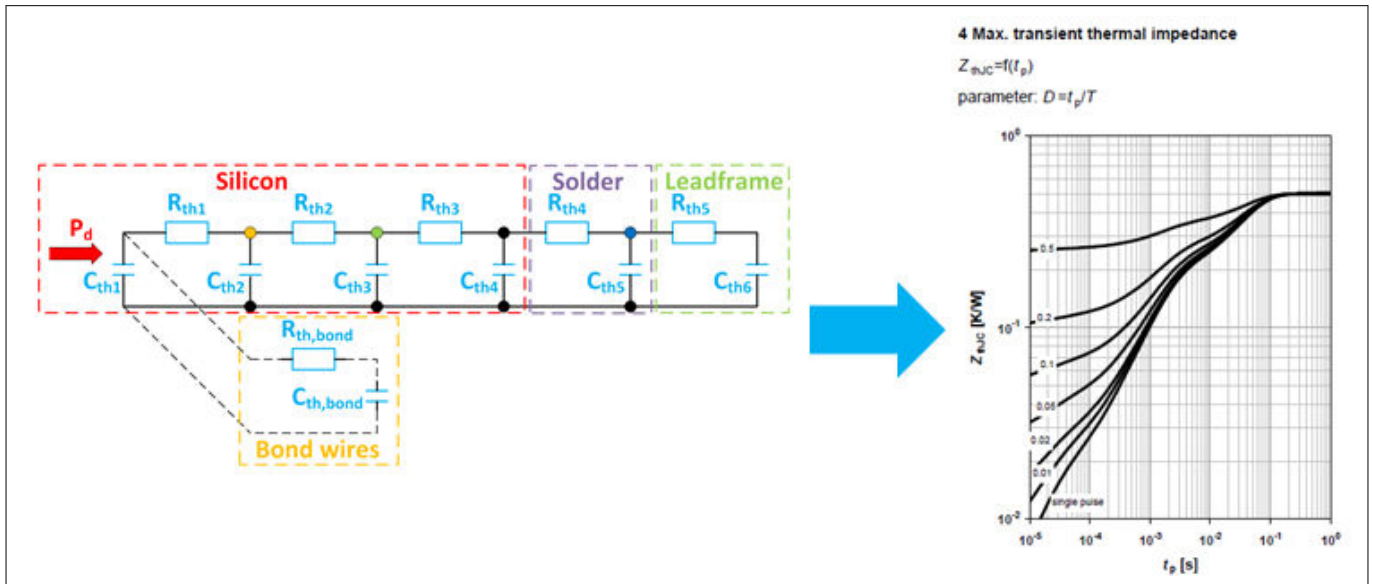


Figure 3 IPB072N15N3 G - from thermal network to Z_{thJC} graph

To make use of the values for these (R_{thi} , C_{thi}) parameters, designers must use the level 3 model from the PSpice files provided by Infineon. In Figure 4, the parametric values for IPB072N15N3 G are shown. For this MOSFET, the thermal impact of the bond wires is negligible, and this is not included within the PSpice level 3 model.

The values for the R_{thi} and C_{thi} parameters are provided in Kelvin per Watt (K/W) and Watt-second per Kelvin ($W \cdot s / K$) respectively. Moreover, if, for example, we refer to the parameters for “Rth1” in Figure 4, “1.44m” and “534.18u” correspond to 1.44 millikelvin per Watt and 534.18 microkelvin per Watt respectively. Similarly, for “Cth6”, “190m” is equivalent to 190 milliwatt-second per Kelvin.

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```
.SUBCKT IPB072N15N3 drain gate source Tj Tcase PARAMS: dvth=0 dRdson=0 dgfs=0 dc=0 Zthtype=0 Ls=1.8n Ld=1n Lg=4n
.PARAM RS=878u Rg=2.3 Rd=50u Rm=340u
.PARAM Inn=100 Unn=10 Rmax=7.2m gmin=65
.PARAM RRF=389m Rrbond=16m Rtb=6.2 g2=758m
.PARAM act=27.28
.FUNC Pb(I,dT,Rb) {Rb/(2*Rtb)*(I-limit(dT/(max(I,1n)*Rb)+RRF*I*g2,0,I))**2}
X1 d1 g s Tj S3_150_n_var PARAMS: a={act} dvth={dvth} dR={dRdson} dgfs={dgfs} Inn={Inn} unn={unn}
+Rmax={Rmax} gmin={gmin} Rs={RS} Rp={Rd} dC={dc} Rm={Rm}
Rg g1 g {Rg}
Lg gate g1 {Lg*if(dgfs==99,0,1)}
GS s1 s VALUE={V(s1,s)/(RS*(1+(limit(V(Tj),-200,999)-25)*4m)-Rm)}
Rsa s1 s 1Meg
Ls source s1 {Ls*if(dgfs==99,0,1)}
Rda d1 d2 {Rd}
Ld drain d2 {Ld*if(dgfs==99,0,1)}
Rsb source s1 10
Rga gate g1 10
Rdb drain d2 10
G_TH 0 Tb VALUE = {Pb(abs(I(Ls)),V(Tj,Tcase),Rrbond*(1+(limit((V(Tb)+V(Tj)))/2,-200,999)-25)*4m)}
Cthb Tb 0 9.36m
Rthb Tb Ti {Rtb}
Rth1 Tj t1 {1.44m+limit(Zthtype,0,1)*534.18u}
Rth2 t1 t2 {13.22m+limit(Zthtype,0,1)*4.9m}
Rth3 t2 t3 {57.09m+limit(Zthtype,0,1)*24.83m}
Rth4 t3 t4 {67.52m+limit(Zthtype,0,1)*44.28m}
Rth5 t4 Tcase {172.84m+limit(Zthtype,0,1)*113.35m}
Cth1 Tj 0 569.697u
Cth2 t1 0 666.158u
Cth3 t2 0 6.372m
Cth4 t3 0 4.637m
Cth5 t4 0 137.136m
Cth6 Tcase 0 190m
.ENDS
*****
```

Figure 4 PSpice level 3 model for IPB072N15N3 G

Using this model, and ensuring that we retain the simulation data for all the sub-circuits, we can observe the temperature behavior at various locations of the chip under the datasheet conditions used to define the rating for avalanche energy, single pulse (E_{AS}). These conditions include $T_j = 25^\circ\text{C}$ and $i_{AS}(0) = 100\text{ A}$, where $i_{AS}(0)$ is the initial current of a single pulse avalanche event. The SIMetrix schematic [2] is shown in Figure 5, where the supply V3 is disconnected from the circuit when the Device Under Test (DUT) faces avalanche. In this case the DUT is U1.

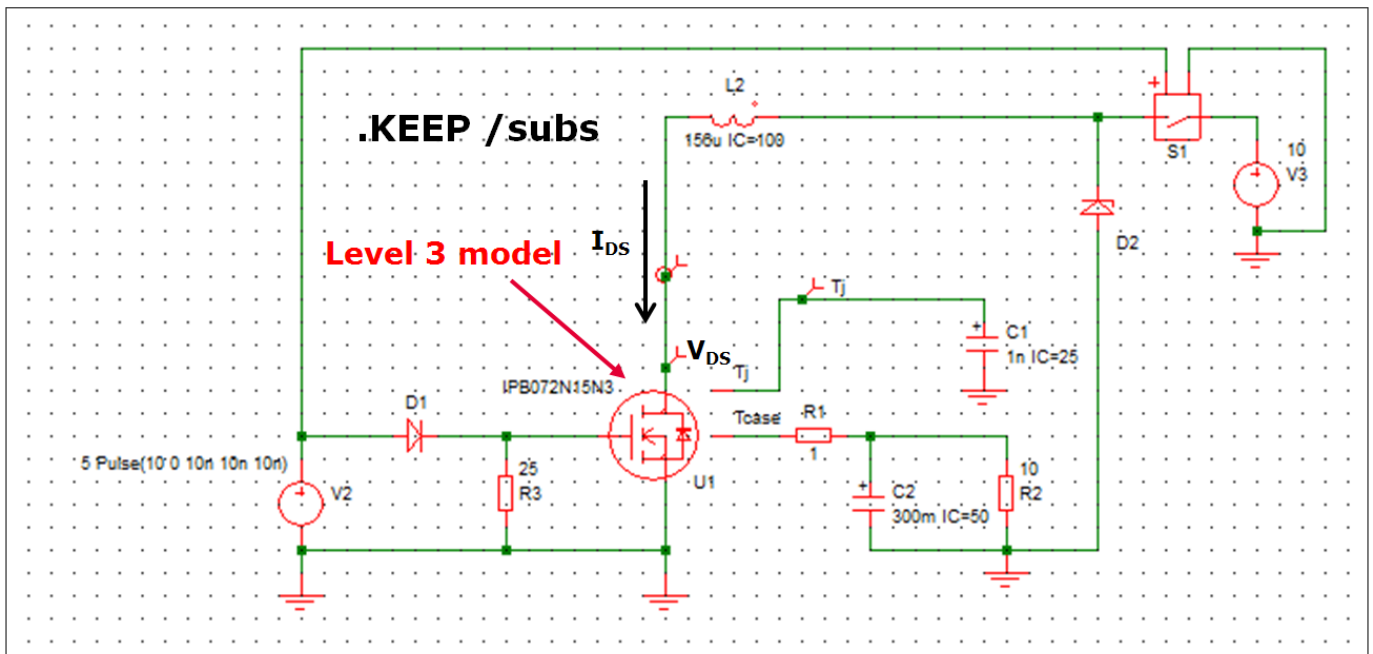


Figure 5 Single pulse avalanche - simulation circuit for heat spreading

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Note: The character “E” is employed here to refer to energy (E_{AS}), whereas it was previously used to refer to an electric field (E_C). It would have been difficult to follow another nomenclature, therefore we kindly ask the reader to keep this fact in mind for the rest of this document.

The results of the simulation are shown in Figure 6, where the equivalent thermal network depicts the location within the model of the junction temperature (T_j), t1, t2 and t4. As can be seen, although T_j peaked above 200°C, the temperature at t4, which is located between the solder joint and lead frame (as shown in **Figure 2**), exhibits minimal increase. This clearly shows that, even under a strong avalanche event lasting for 70 μ s, the heat does not have time to spread anywhere near the PCB. Therefore, the single pulse avalanche rating is independent of the PCB conditions.

Within the simulations, the peak value of T_j is approximately 210°C, which is well above the maximum allowed junction temperature ($T_{j,max}$) of 175°C for IPB072N15N3 G. When defining the E_{AS} datasheet rating, this high T_j is considered acceptable due to the very limited number of occurrences over lifetime (you should only tolerate one event at these energy levels) and the fact that such temperatures remain significantly below the destructive junction temperature ($T_{j,destr}$). $T_{j,destr}$ is the temperature at which OptiMOS™ FETs stop behaving like semiconductors, and will be discussed further in section 2.2.2.

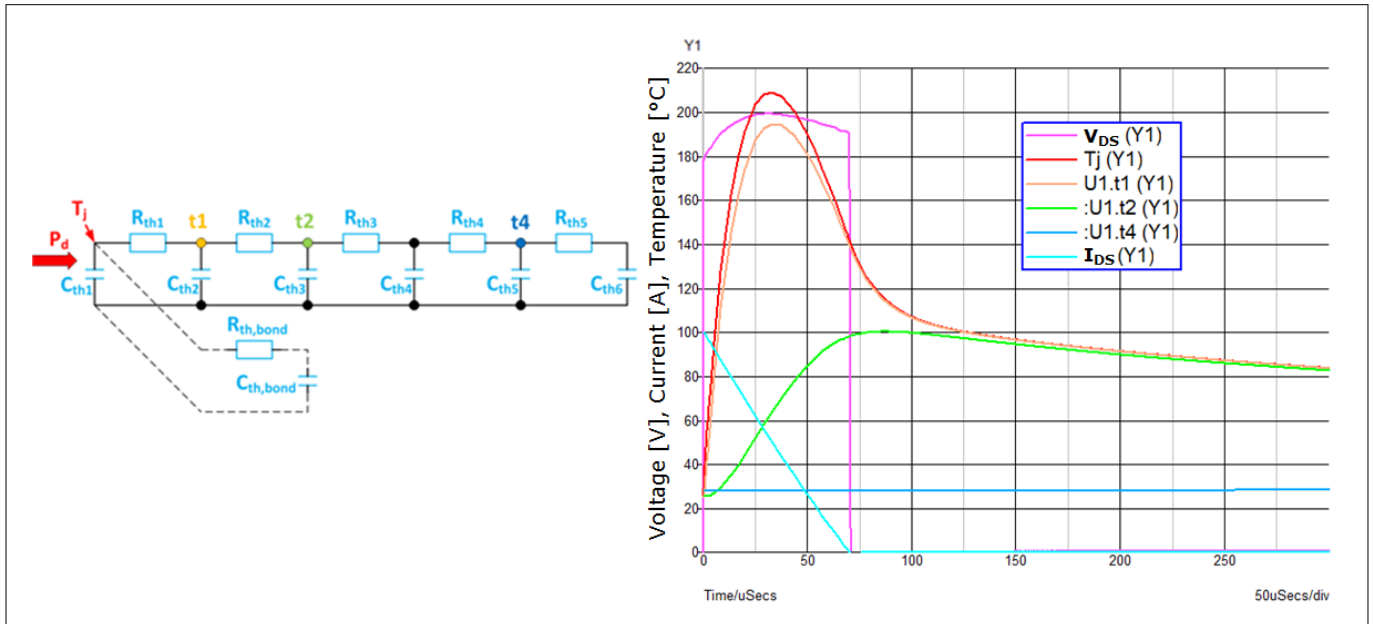


Figure 6 Results of single pulse avalanche simulation with IPB072N15N3 G

2.1.3 Amplitude of V_{DS} spikes in single pulse avalanche

There are two parameters that impact the amplitude of the V_{DS} spikes during avalanche:

- Parameter A: the production distribution of the MOSFET breakdown voltage ($V_{BR(DSS)}$);
- Parameter B: the junction temperature of the MOSFET.

In order to understand this, it is important to remember that avalanche occurs when electric fields begin to exceed the critical electric field (E_c) of the technology, as discussed in section 2.1.1. Figure 7 shows the portion of a basic power MOSFET structure that contributes to the breakdown voltage, as well as the distribution of the electric field over this region when reverse polarized. The green area defines the $V_{BR(DSS)}$ capability of the MOSFET. As a first approximation, the area to the left of the vertical axis can be ignored. From this diagram, it is clear that the actual $V_{BR(DSS)}$ of a MOSFET is proportional to the E_c of its structure. In Figure 7 and throughout the rest of the document, we use the terminology loosely, as all electric fields should actually be represented as absolute values.

2 Single pulse avalanche

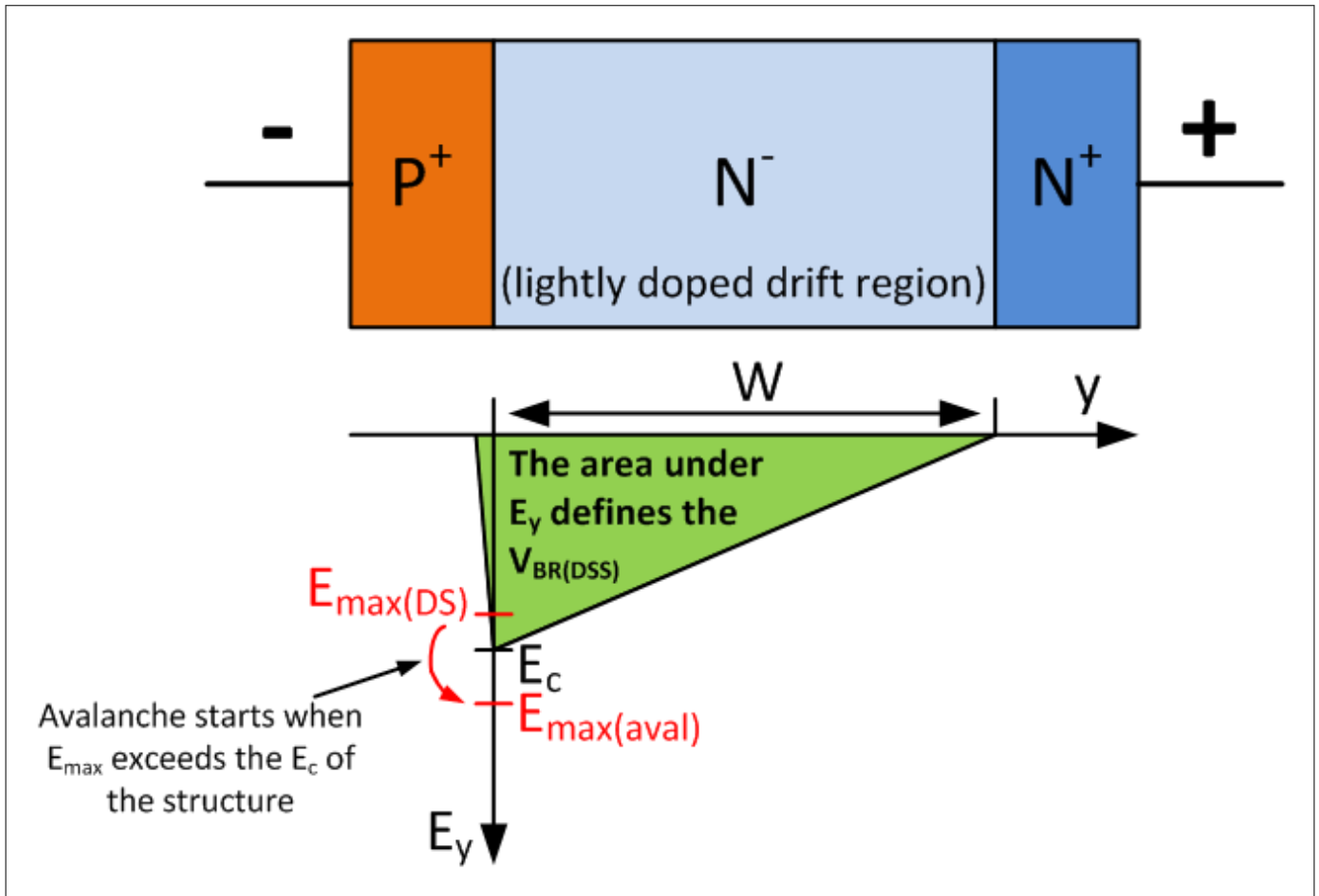


Figure 7 Portion of a reverse polarized power FET, also showing electric field distribution

Let’s focus first on ‘Parameter A’, the production distribution of the MOSFET breakdown voltage ($V_{BR(DSS)}$). When mass-produced in millions of units, the MOSFET $V_{BR(DSS)}$ will exhibit a certain distribution. When developing this technology, the engineer must ensure that the MOSFETs at the bottom of the distribution curve also exhibits a $V_{BR(DSS)}$ above the minimum datasheet value ($V_{BR(DSS)(min,25)}$) (which is 60 V for BSC014N06NS) in order to avoid yield losses. Putting this another way, at $T_j = 25^\circ\text{C}$, the engineer must make sure that the maximum electric field within the structure (E_{max}) can only reach E_c when V_{DS} is already above $V_{BR(DSS)(min,25)}$. That way, at $V_{BR(DSS)(min,25)}$, E_{max} is lower than E_c , and corresponds to the $E_{max(DS)}$ parameter shown in Figure 7.

Avalanche begins when the electric field in a portion of the structure exceeds E_c , as represented by the maximum electric field observed inside the structure during avalanche ($E_{max(aval)}$) in Figure 7. Then, assuming for the time being a constant temperature, the observed V_{DS} spike will exhibit a plateau at the actual $V_{BR(DSS)}$ of the FET. This was drawn in its most basic form in [Figure 1](#).

Figure 8 provides an example of $V_{BR(DSS)}$ distribution for different lots of the same MOSFET. To compute the distribution of each lot, we use at least several hundred parts. Despite obscuring the y-axis scale, it is clear that the MOSFETs all exhibit an actual $V_{BR(DSS)}$ above $V_{BR(DSS)(min,25)}$. However, designers should NOT take advantage of a $V_{BR(DSS)}$ slightly higher than the official rating of the part: if a MOSFET is rated for 60 V at $T_j = 25^\circ\text{C}$, Infineon only recommends using it up to this rating. Any usage above the $V_{BR(DSS)}$ rating of the MOSFET as stated on the datasheet is at the user’s risk. Moreover, as shown in [Figure 11](#), designers must be aware that the variation of $V_{BR(DSS)}$ with temperature will lead to lower $V_{BR(DSS)}$ values for junction temperatures below 25°C .

2 Single pulse avalanche



Figure 8 Example of production distribution for $V_{BR(DSS)}$

Although the original purpose of Figure 8 was to highlight that the actual $V_{BR(DSS)}$ of OptiMOS™ FETs is always higher than $V_{BR(DSS)(min,25)}$, we can derive other information from this figure. Indeed, due to the $V_{BR(DSS)}$ distribution between MOSFETs of the same lot, each MOSFET will exhibit a different clamping voltage when in avalanche, as summarized in Figure 9 for low energy avalanche events (i.e. the impact of temperature, which we will discuss next, is negligible). In the case of OptiMOS™ FETs, due to the tight distribution of $V_{BR(DSS)}$, the difference in clamping voltage between MOSFETs in the same lot is very small.

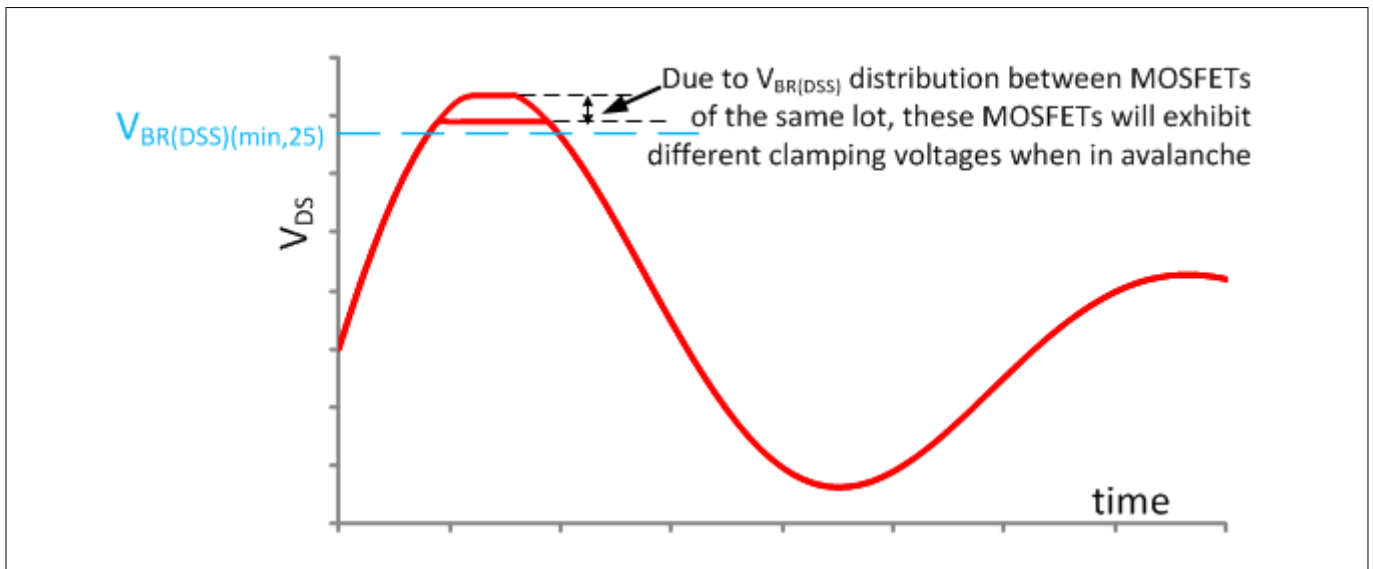


Figure 9 Different $V_{BR(DSS)}$ means different clamping voltages during low energy avalanche event

Regarding the influence of temperature on the amplitude of the V_{DS} spikes during avalanche (previously introduced as ‘Parameter B’), it turns out that E_c monotonously increases with temperature. Therefore, $V_{BR(DSS)}$ does too. During high energy avalanche events, T_j varies over time. As a consequence, the voltage at which the V_{DS} of the MOSFET is clamped during avalanche varies over time, as can be observed in Figure 10, which is simplified to show the most relevant waveforms of Figure 6. Finally, Figure 10 also provides the peak V_{DS} voltage observed during avalanche ($V_{DS,peak}$). Later, even when making calculations for avalanche events of high energy, we shall approximate that the V_{DS} voltage of the MOSFET during an avalanche event is constant and equals $V_{DS,peak}$.

2 Single pulse avalanche

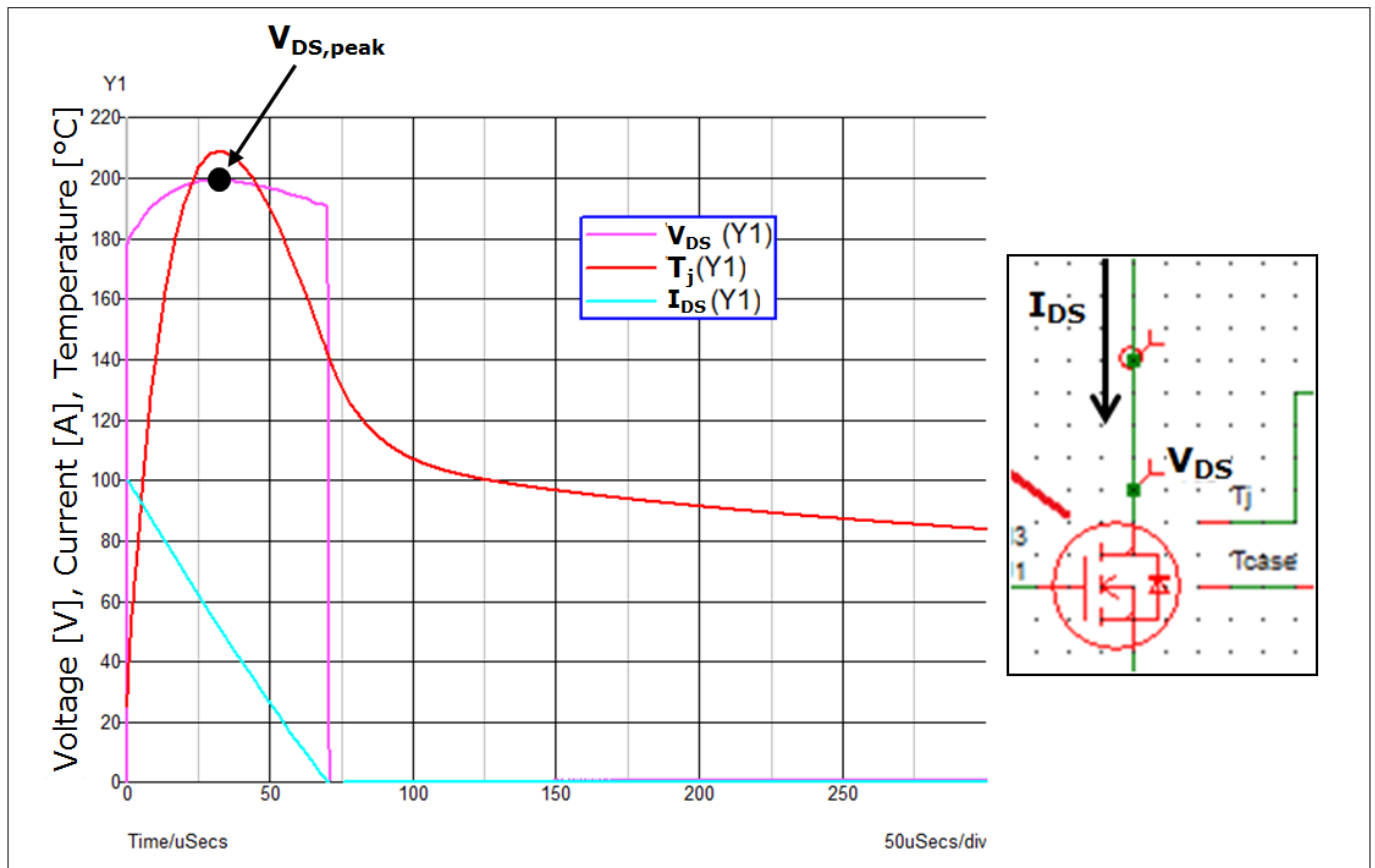


Figure 10 Variation of V_{DS} and temperature during high energy avalanche event

For our OptiMOS™ FETs, the variation of E_c with temperature leads to a $V_{BR(DSS)}$ increase of 5% per 100°C for the latest families, and up to 9% per 100°C for some older families, as can be seen for BSC014N06NS (latest OptiMOS™ 60 V) and IPP110N20N3 G (OptiMOS™ 3 200 V) in Figure 11.

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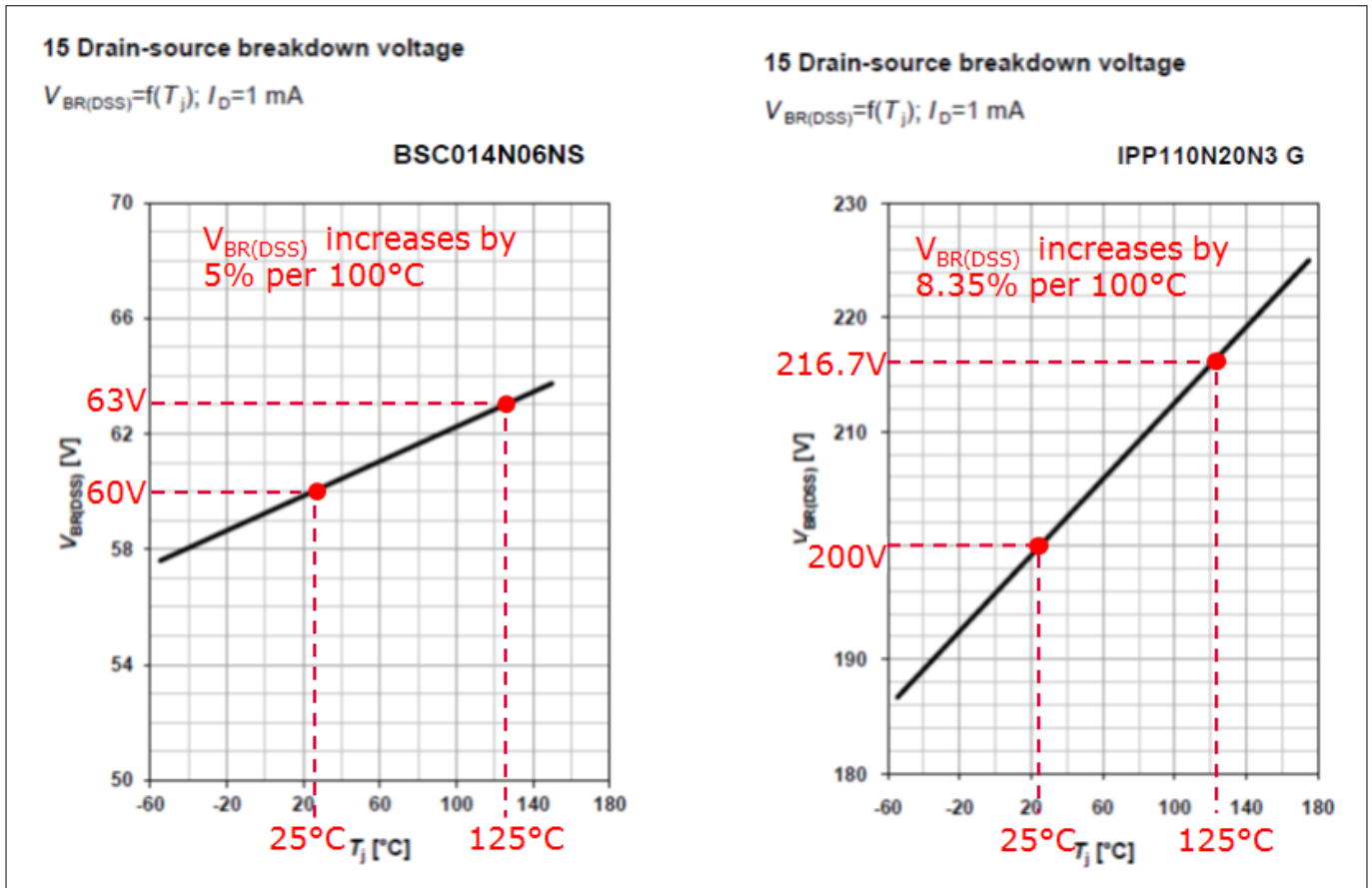


Figure 11 Variation of $V_{BR(DSS)}$ with temperature for two OptiMOS™ MOSFETs

As we saw in section 2.1.2, with the test conditions used to provide the datasheet value for E_{AS} , temperatures as high as 210°C can be reached inside the silicon, which is almost 200°C above the typical T_j of 25°C used to define most parameters within the OptiMOS™ datasheets. This increase of T_j causes a $V_{BR(DSS)}$ increase of up to almost 20% for OptiMOS™ FETs.

Adding a 5 to 10% higher $V_{BR(DSS)}$ due to the production distribution, we obtain the familiar $1.3 \times V_{BR(DSS)(min,25)}$ value often provided in literature for the peak amplitude of V_{DS} spikes during avalanche, previously defined as $V_{DS,peak}$. However, for all the latest OptiMOS™ families, due to the lower variation of $V_{BR(DSS)}$ with temperature, V_{DS} spikes during avalanche should not exceed $1.2 \times V_{BR(DSS)(min,25)}$.

It can also be derived that, for low energy avalanche events, the observed V_{DS} spikes will remain well below $1.2 \sim 1.3 \times V_{BR(DSS)(min,25)}$, as the rise in T_j will be approximately negligible.

This can be demonstrated with the use of a test circuit, the schematic of which is shown in Figure 12. For the DUT, we will use BSC014N06NS, which is part of Infineon’s latest OptiMOS™ 60 V family. For this test platform, V_{DD} is set to 50 V. This voltage amplitude is very high when using a 60 V-rated MOSFET as DUT, because the V_{DS} spikes generated when turning off the DUT will simply be superposed on top of this V_{DD} . In this case, by leaving a small voltage span for the V_{DS} spikes between V_{DD} and $V_{BR(DSS)}$, we can facilitate the occurrence of avalanche.

2 Single pulse avalanche

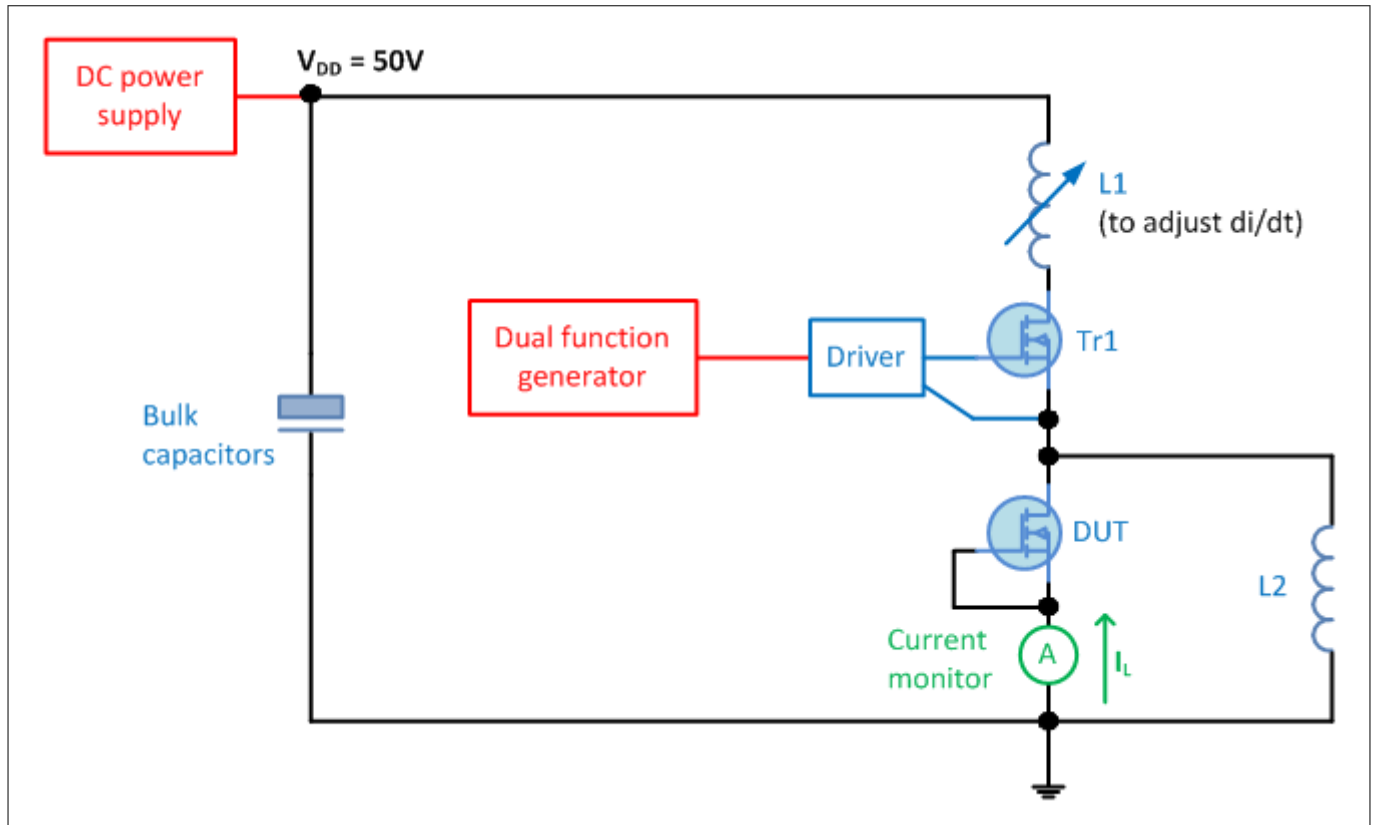


Figure 12 Test circuit to study low energy avalanche events

In Figure 13, just after 1 μ s on the x-axis, we can observe that BSC014N06NS enters avalanche, as indicated by the clamping of V_{DS} for approximately 40 ns. On this occasion, the energy generated during avalanche was insufficient to heat the MOSFET, as indicated by the flatness of the clamping voltage. Consequently, the clamping occurs at approximately 64 V, which corresponds to the actual $V_{BR(DSS)}$ of this sample at an ambient temperature around 25°C.

2 Single pulse avalanche

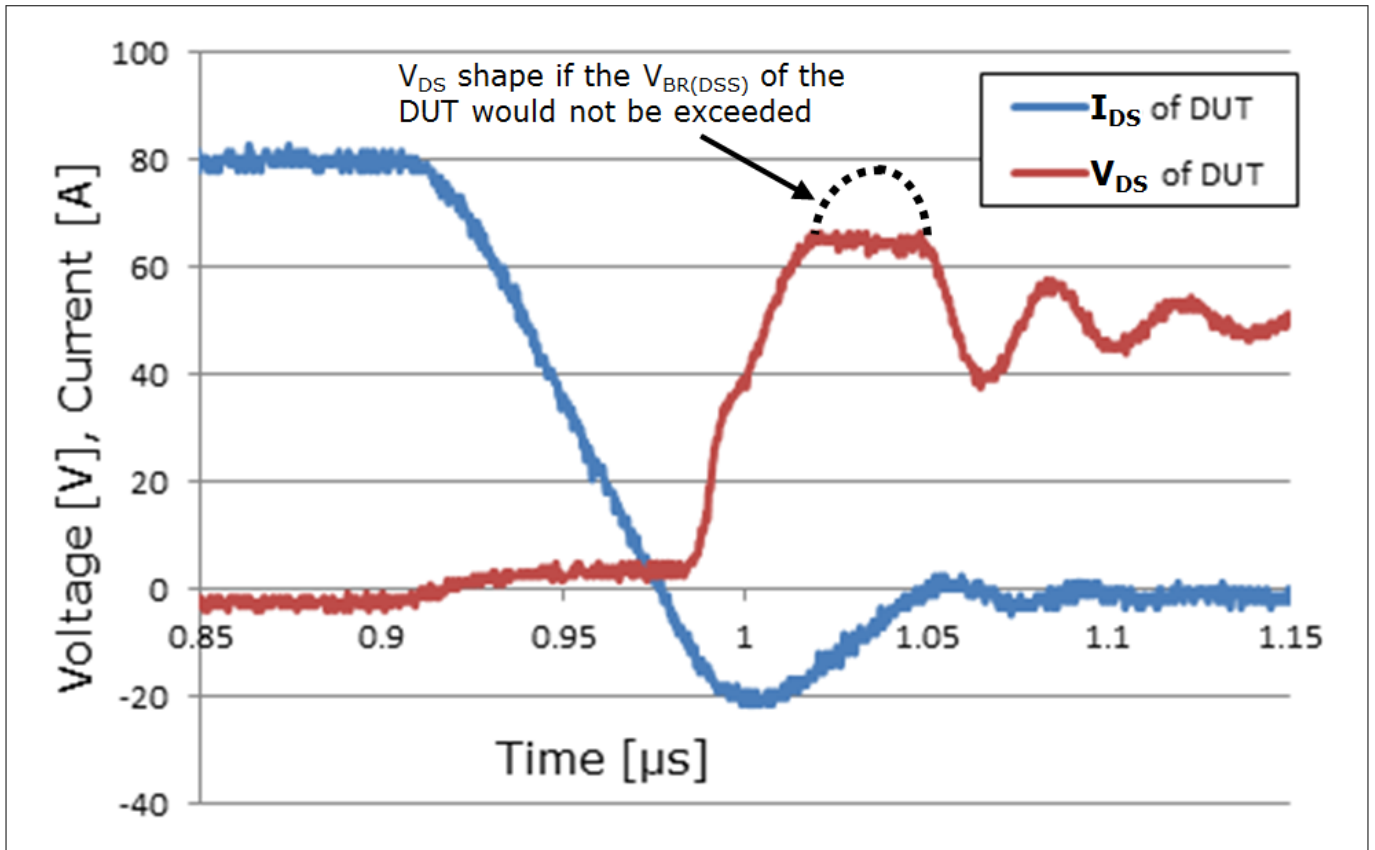


Figure 13 BSC014N06NS waveforms with test circuit

2.2 Failure mechanisms

We will now introduce the two types of failure that can affect OptiMOS™ FETs during avalanche.

2.2.1 Latch-up

The latch-up mechanism is best understood by referring to Figure 14 and [1]. The avalanche event generates a drain current, the amplitude of which will be greater where the electric field has more intensity. If the technology is structured in such a way that the electric field is high in the vicinity of the parasitic NPN bipolar junction transistor (BJT), a significant amount of current will flow through its base resistor, producing a voltage between base and emitter. If this voltage reaches a certain threshold, the bipolar transistor turns on and most of the avalanche current now flows through it, with potentially damaging effects as there is no means of controlling it.

Since the latch-up mechanism is well understood, Infineon strived to mitigate its impact during the development of all OptiMOS™ technologies covered by this document. Hence, in many of these technologies, latch-up can no longer occur. However, due to their specific structures, there are still a few technologies for which the risk of latch-up could only be reduced, but not fully removed.

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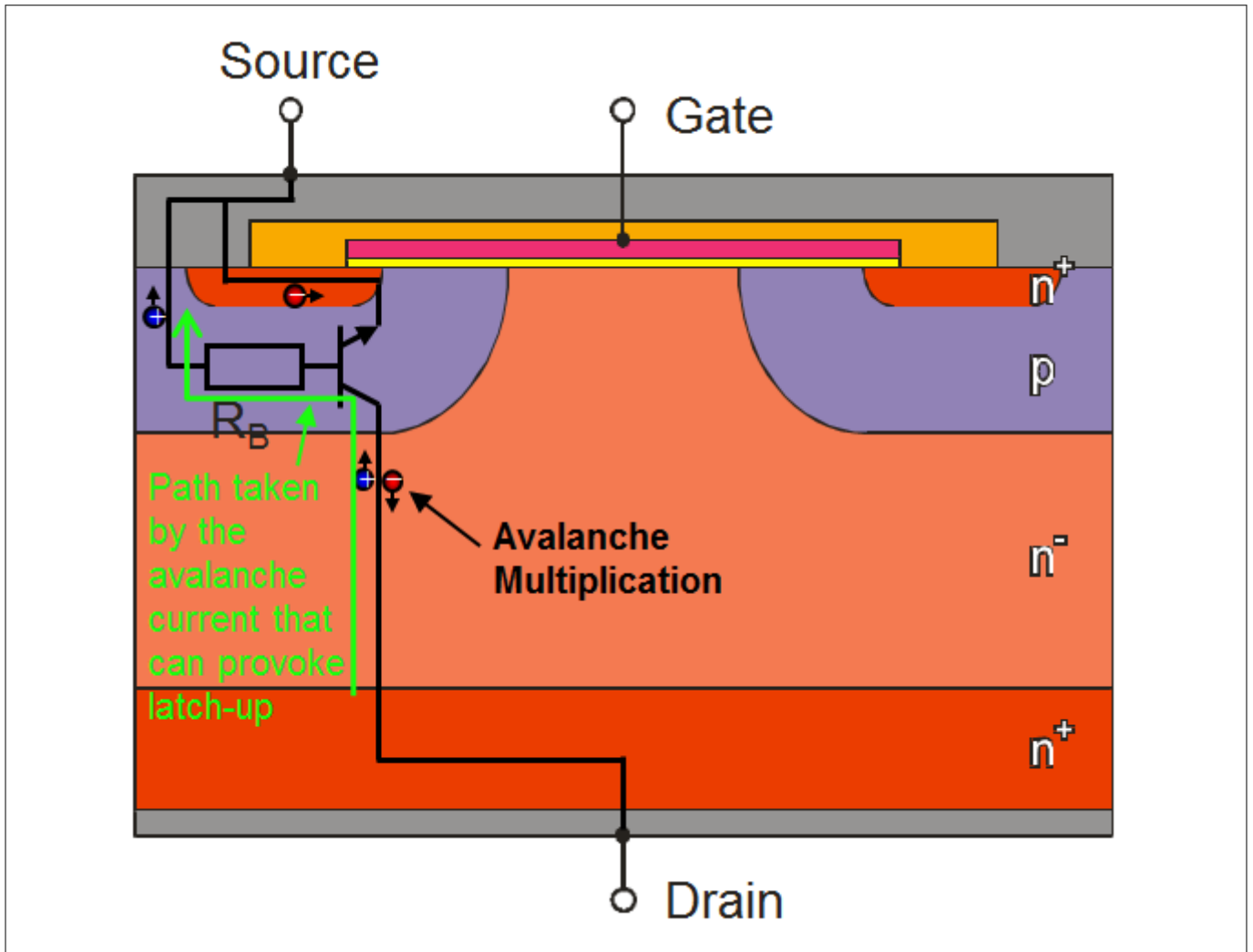


Figure 14 MOSFET cross-section with parasitic BJT

We will now look closer at latch-up, using some equations.

The first equation introduces I_{crit} , the critical current at which the parasitic bipolar transistor is turned on. This typically takes place when its base-to-emitter voltage reaches approximately 0.6 V.

$$V_{BE} = R_B \times I_{crit} \approx 0.6 \text{ V}$$

Equation 1

Since the temperature can vary significantly during avalanche, it is important to observe how the critical current varies. We can re-arrange Equation 1 as shown in Equation 2, where we can see that both numerator and denominator vary with temperature.

$$I_{crit} = I_{crit}(T) = \frac{V_{BE}(T)}{R_B(T)}$$

Equation 2

Regarding the numerator of Equation 2, the V_{BE} of this parasitic BJT decreases linearly with temperature by a few mV/°C.

2 Single pulse avalanche

Then, we can expand the denominator of Equation 2 and obtain the following equation.

$$R_B = R_B(T) \approx R_B(T_0) \times \left[\frac{T}{T_0} \right]^{2.5}$$

Equation 3

As opposed to the numerator of Equation 2, the denominator quickly increases with temperature.

Based on equations 1-3, the variation of the I_{crit} limit during an avalanche event is plotted in magenta in Figure 15. It is clear that I_{crit} initially drops very quickly, before its rate of decrease slows down. At a certain point, I_{crit} starts increasing with time. On the other hand, the avalanche current (dark blue line) is considered to linearly decrease for our applications as it corresponds to the inductor current. On that basis, latch-up can only occur towards the beginning of an avalanche event, while the slope of the diminishing I_{crit} is steep.

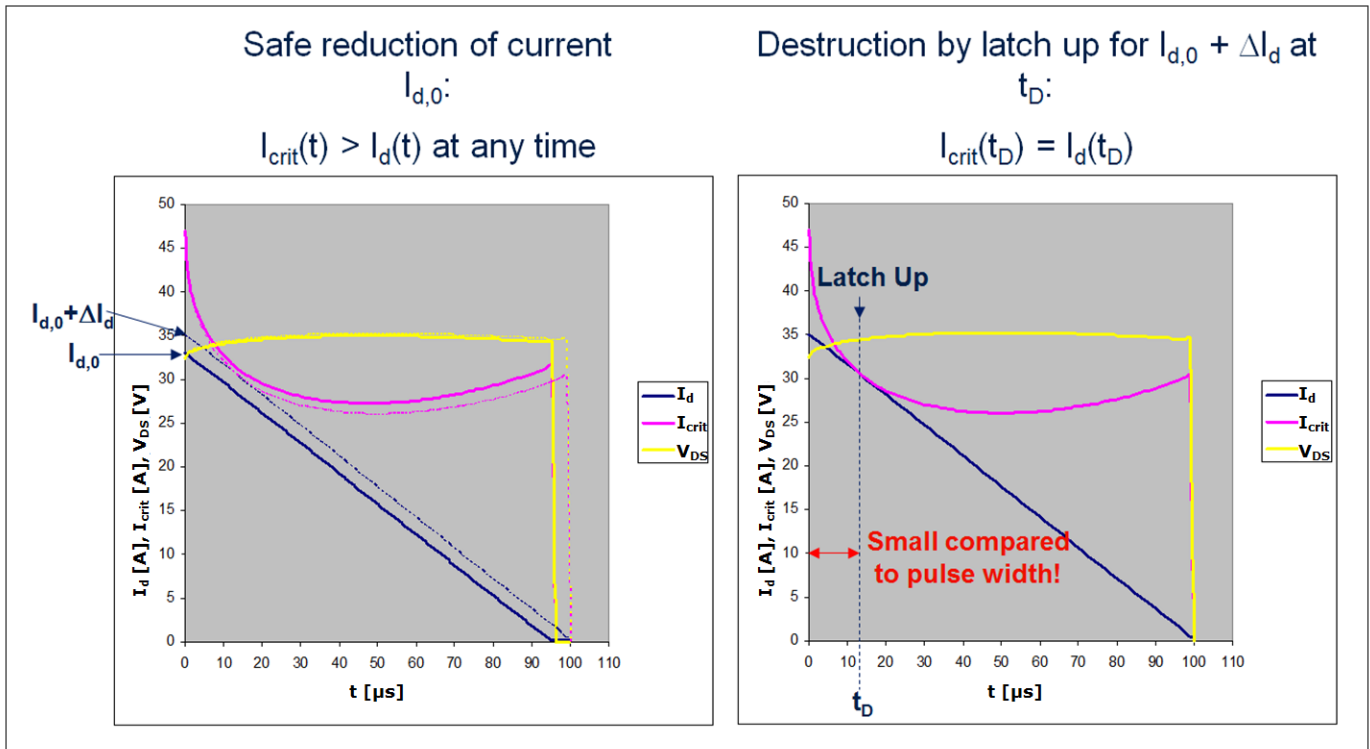


Figure 15 Impact of critical current on latch-up

2.2.2 Thermal destruction

Thermal destruction occurs when the junction temperature of the MOSFET reaches $T_{j,destr}$. Given the precautions taken against latch-up during the technology development of our OptiMOS™ families, thermal destruction is responsible for the majority of failures caused by avalanche. Even for technologies prone to latch-up, such a failure mechanism will only prevail over thermal destruction in applications with a low L_{loop} . This is because the temperature increase during avalanche is caused by energy that is proportional to $L_{loop} \times (i_{AS}(0))^2$. $T_{j,destr}$ is close to the intrinsic temperature of silicon, that is the temperature at which the density of thermally generated carriers equals the background doping. Hence, when such a temperature is reached, our MOSFET will no longer behave like a semiconductor.

There is not much variation in $T_{j,destr}$ for the OptiMOS™ devices being discussed, and the value is usually close to 400°C. Additionally, this value is independent of external conditions (start temperature, pulse duration, pulse shape).

2 Single pulse avalanche

In order to determine the exact $T_{j,destr}$ of an OptiMOS™ family, the avalanche current under which the MOSFET is thermally destroyed is recorded at a fixed L_{loop} with different values for the junction temperature at the start of avalanche ($T_{j(start)}$). These results are then placed on a graph similar to Figure 16, and a line is drawn between all these points. The value on the x-axis corresponding to $y = 0$ represents $T_{j,destr}$. The measurements at different $T_{j(start)}$ values can be repeated for other L_{loop} values in order to confirm the validity of the results, since all lines should cross the x-axis at roughly the same temperature, as is the case for the blue and green lines in Figure 16

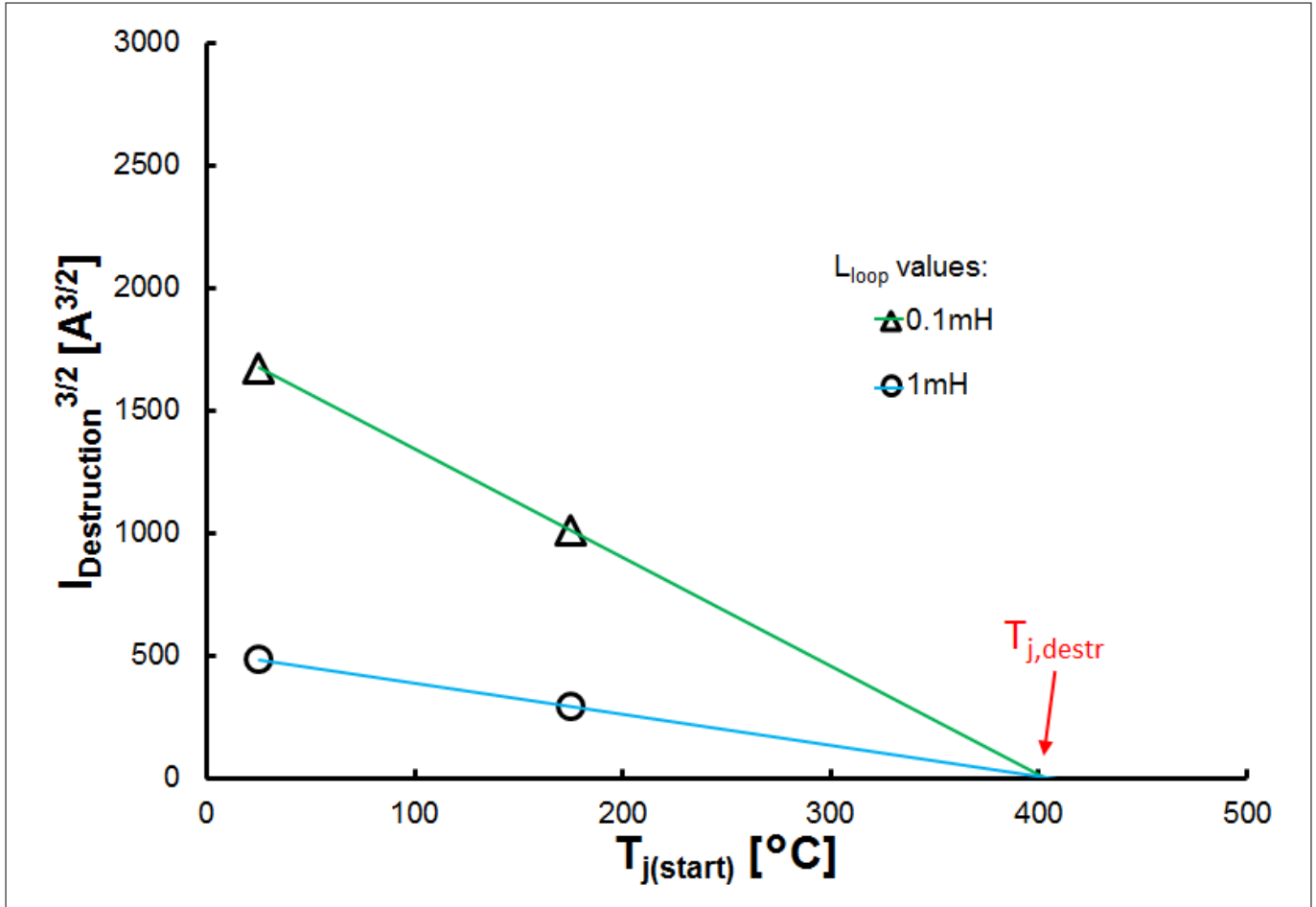


Figure 16 Extraction of $T_{j,destr}$ for a technology

Unfortunately, coping with thermal destruction implies some trade-offs, as it impacts some key drivers of high performance technologies, in particular the product of drain-source on-state resistance by active area, also known as $R_{DS(on)} \times A$. Indeed, whereas a technology reduction of $R_{DS(on)} \times A$ usually leads to smaller chip sizes for a defined $R_{DS(on)}$ value, the device itself requires a bigger chip size in order to mitigate the temperature increase caused by high energy avalanche events. To a great extent, bigger is better to cope with avalanche!

2.3 100% tested in production

Every single one of our OptiMOS™ FETs must pass a production test for single pulse avalanche. The schematic of the test circuit is quite similar to the one used in Figure 5 for our simulations. For clarity, this schematic is re-drawn on Figure 17, where U1 represents the DUT.

2 Single pulse avalanche

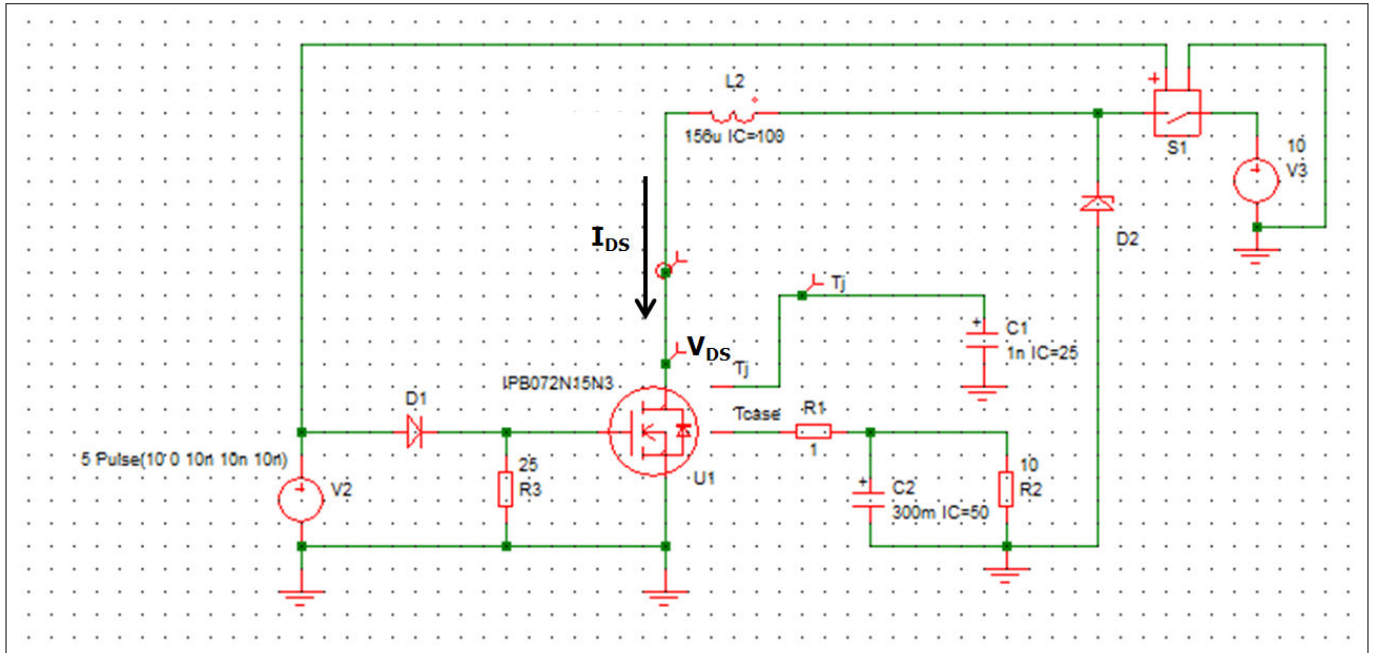


Figure 17 Rough schematic of Infineon’s avalanche production test for OptiMOS™

This production test is commonly known within the semiconductor industry as Unclamped Inductive Switching (UIS), and is very well described on page 5 of [3]. As the DUT is turned off and is therefore exhibiting high impedance, inductance L2 forces its current through this DUT, since there is no alternative path for it. Consequently, the V_{DS} of the DUT quickly exceeds its $V_{BR(DSS)}$ rating, making it operate into avalanche.

While the DUT faces avalanche during an UIS test, its current (which can only be avalanche current since its channel is off) decreases linearly. This triangular current shape is the cornerstone of all avalanche ratings provided within Infineon OptiMOS™ datasheets, therefore other current shapes are not discussed within this document.

As shown in Figure 17, in the case of our OptiMOS™ FETs, the V_{DD} supply (V3) becomes disconnected from the inductor just before the onset of avalanche within the DUT. Therefore, when calculating energies later, the formula used will be $E_{AS} = \frac{1}{2} \times L_{loop} \times (i_{AS}(0))^2$.

The designer should keep this point in mind when comparing datasheets because some suppliers do not disconnect the V_{DD} supply during avalanche, as is the case for the schematic and test procedure shown in Figure 18. This leads to a higher avalanche energy rating, since it is now defined by $E_{AS} = \frac{1}{2} \times L_{loop} \times (i_{AS}(0))^2 \times V_{DS,peak} / (V_{DS,peak} - V_{DD})$.

This can be illustrated by an example with $L_{loop} = 100 \mu H$, $i_{AS}(0) = 50 A$, $V_{DS,peak} = 60 V \times 1.2 = 72 V$ and $V_{DD} = 12 V$. On one hand, when using $E_{AS} = \frac{1}{2} \times L_{loop} \times (i_{AS}(0))^2$, E_{AS1} would be recorded as 125 mJ. On the other hand, when using $E_{AS} = \frac{1}{2} \times L_{loop} \times (i_{AS}(0))^2 \times V_{DS,peak} / (V_{DS,peak} - V_{DD})$, the recorded value of E_{AS2} is 150 mJ, which is 20% higher than E_{AS1} , simply because V_{DD} was not disconnected during avalanche!

Note: As previously stated, when computing single pulse avalanche energies, we shall use as approximation that the V_{DS} voltage of the MOSFET during an avalanche event is constant and equals $V_{DS,peak}$.

2 Single pulse avalanche

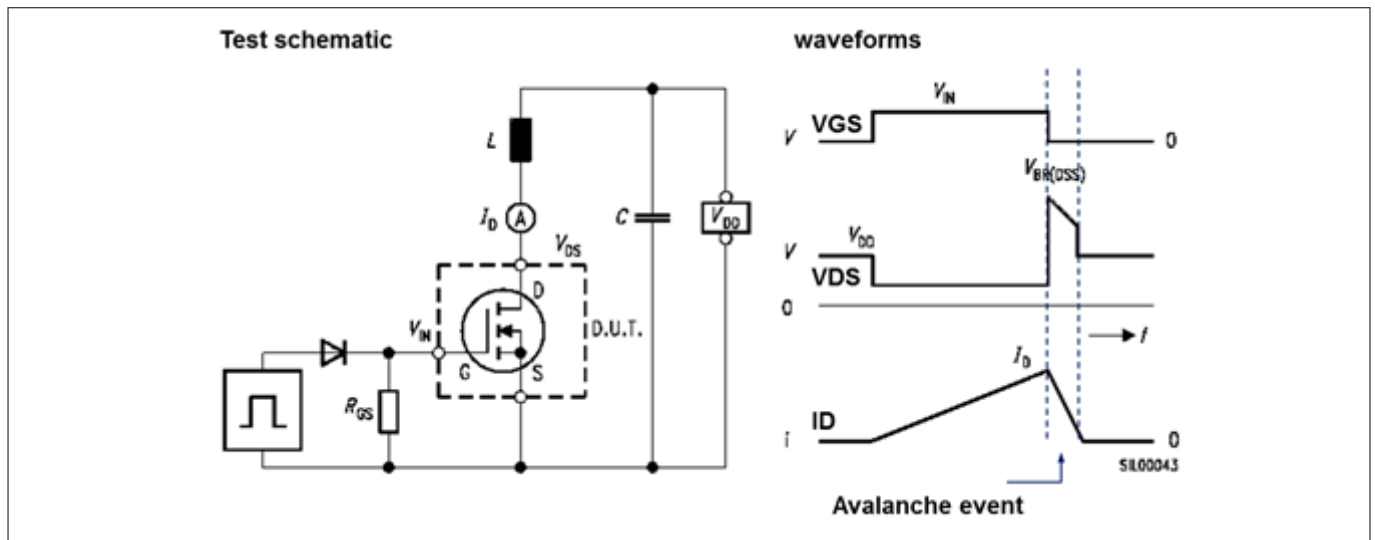


Figure 18 Avalanche tests setup with V_{DD} always connected to circuit

As its name suggests, a single pulse avalanche event should only be allowed to occur once – particularly if the conditions are close to the limits provided on the datasheet diagram entitled “Avalanche characteristics”. This is because those limits correspond to junction temperatures above the $T_{j,max}$ of the MOSFET, and repeating such events would impair the lifetime of the MOSFET. Remember that avalanche is not a condition under which Infineon recommends to use the OptiMOS™ FETs on focus here.

3 Making use of the datasheet

3 Making use of the datasheet

3.1 Existing information

In some cases, the single pulse avalanche capability of an OptiMOS™ FET within an application can be readily assessed by referring to the datasheet, such as the E_{AS} rating and the diagram providing the avalanche characteristics (see Figure 19 and Figure 20 below). Note that I_D (provided as a test condition for E_{AS} inside Table 2) corresponds to the initial avalanche current ($i_{AS}(0)$), which is also called i_{AV} on the y-axis of Figure 20. In the rest of this document, we shall always use $i_{AS}(0)$ to refer to this parameter.

The “Avalanche characteristics” diagram of any datasheet can be interpreted in the following way. For a defined $T_{j(start)}$, if the point of coordinates (t_{AV} , $i_{AS}(0)$) corresponding to the application conditions is below and to the left of the plotted lines, then the device can cope with the avalanche event. As an example, in Figure 20, the area of safe avalanche conditions for $T_{j(start)} = 125^\circ\text{C}$ is covered in green. Given the information provided by this diagram, we shall from now on refer to it as being the SOA_{AS} graph, where SOA_{AS} stands for Safe Operating Area under single pulse avalanche.

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	100 100 30	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ }^\circ\text{C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ }^\circ\text{C}$ $V_{GS}=10\text{ V}$, $T_C=25\text{ }^\circ\text{C}$, $R_{thJA}=50\text{ K/W}^{(1)}$
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	-	-	400	A	$T_C=25\text{ }^\circ\text{C}$
Avalanche energy, single pulse ⁽³⁾	E_{AS}	-	-	580	mJ	$I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$

Figure 19 Various datasheet ratings (including E_{AS}) for BSC014N06NS

3 Making use of the datasheet

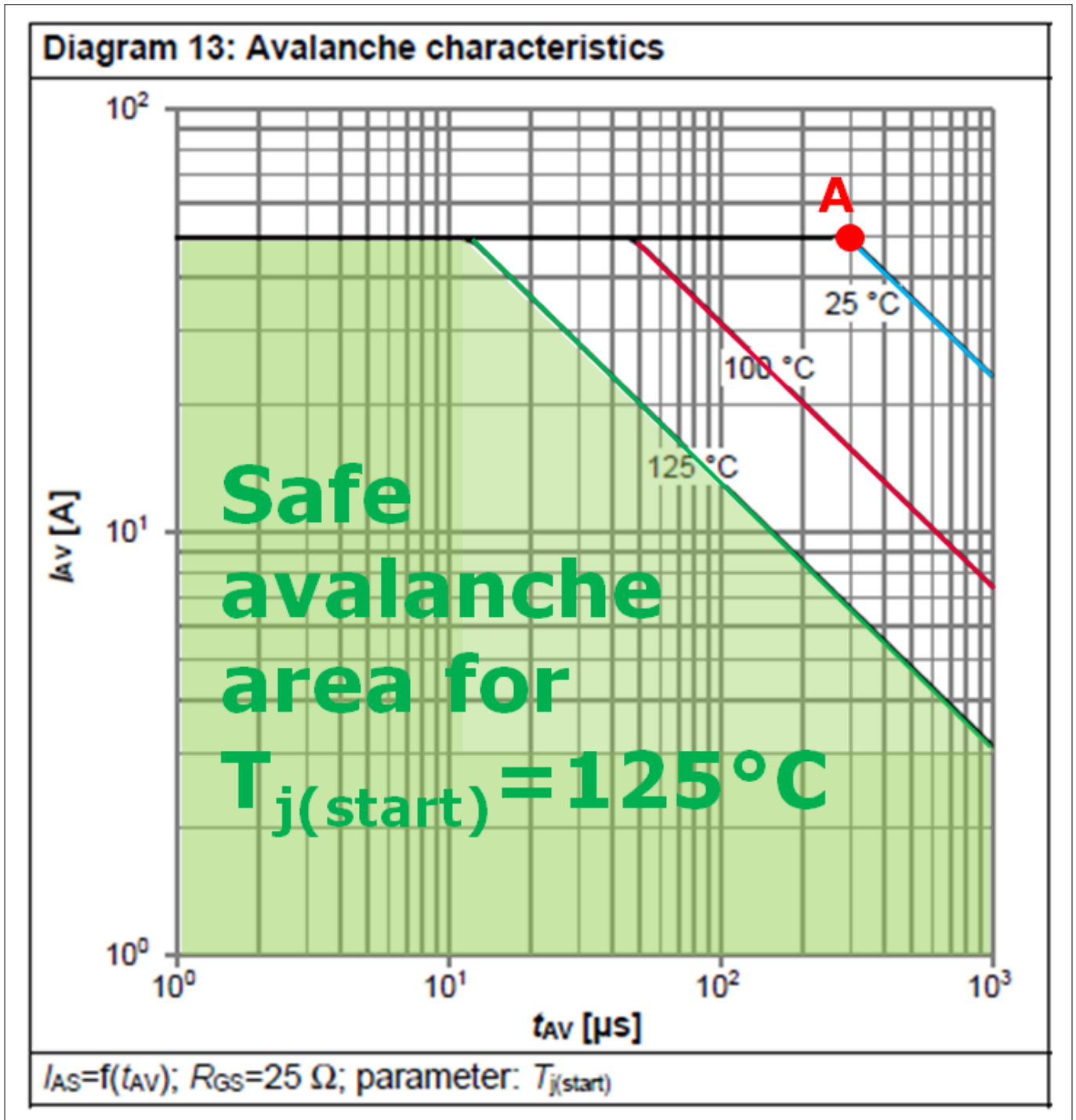


Figure 20 SOA_{AS} graph for BSC014N06NS

Point A in Figure 20 corresponds to the conditions for the E_{AS} value provided in Table 2 of the datasheet (refer to Figure 19). Indeed, at point A, T_{j(start)} = 25 °C, i_{AS(0)} = 50 A, t_{AV} = 300 μs and V_{DS,peak} is approximately 1.3 x V_{BR(DSS)(min,25)}, where V_{BR(DSS)(min,25)} = 60 V for BSC014N06NS.

With E_{AS} = 1/2 x V_{DS,peak} x i_{AS(0)} x t_{AV}, we obtain E_{AS} of approximately 580 mJ.

Note: Based on the information in section 2.1.3, a coefficient of 1.2 would have been more appropriate for BSC014N06NS. At the time this datasheet was released, it was decided to use 1.3 in order to provide some extra derating for the SOA_{AS} graph.

3 Making use of the datasheet

Since we are focusing on avalanche events exhibiting a triangular shape, E_{AS} can alternatively be calculated with $\frac{1}{2} \times L_{loop} \times (i_{AS}(0))^2$, which provides us with the loop inductance (L_{loop}) of the test circuit used to obtain the E_{AS} value in Table 2 of the datasheet. For the BSC014N06NS datasheet, L_{loop} is equal to 464 μ H.

Although the datasheet value for E_{AS} provides the necessary reference for Infineon to validate the avalanche ruggedness of every single MOSFET in production, this rating might prove of limited use for many users, as it is impossible to cover all applications with a single value of loop inductance L_{loop} . In fact, whereas the avalanche energy faced by OptiMOS™ FETs within telecom bricks is due to the combination of low L_{loop} and high current densities, this same avalanche energy results from very high L_{loop} and low current densities within forklift applications. Consequently, it is important to be able to extrapolate the E_{AS} of a MOSFET for any L_{loop} value. For that reason, properly understanding the SOA_{AS} graph allows easy assessment of whether any application (with its different L_{loop}) is safe in terms of single pulse avalanche energy. It is the purpose of the next section.

3.2 Extrapolation for other apps conditions

Before providing extrapolation formulas, we shall start with basic theory, using as a reference the comprehensive work in [4]. Readers that are solely interested in practical examples can skip this section and move to sections 3.2.1 and 3.2.2.

Figure 21 is based on [4] and provides three examples with two different loop inductance values ($L1 < L2$) and two different initial avalanche currents ($i_{AS1}(0) < i_{AS2}(0)$). Since it was shown in section 2.2 that the dominant avalanche failure mode for our OptiMOS™ FETs is caused by an excessive increase in junction temperature, the most critical parameter to monitor is $T_{j,peak}$, the peak junction temperature during avalanche. Figure 21 therefore charts $T_{j,peak}$ for each of the three examples discussed. It is demonstrated in [4] that $T_{j,peak}$ occurs at $\frac{1}{2} \times t_f$, where t_f is the time taken for the avalanche current to reduce to 0.

To begin with, we can see the impact of a different L_{loop} by comparing the examples 1 and 2, whose initial current $i_{AS}(0)$ is identical (see red and blue solid lines). With example 2, the higher L_{loop} , $L2$, slows down the decrease of the avalanche current, which consequently leads to a faster increase of the temperature and, ultimately, a higher peak temperature, as can be observed when comparing the red and blue dotted curves. Assuming that the solid and dotted blue curves refer to datasheet conditions for the E_{AS} rating, it is clear that one cannot use the same $i_{AS}(0)$ if the loop inductance is higher, otherwise the junction temperature peaks far too high. This last remark is self-explanatory when using energies instead of temperatures, because $E_{AS} = \frac{1}{2} \times L_{loop} \times (i_{AS}(0))^2$.

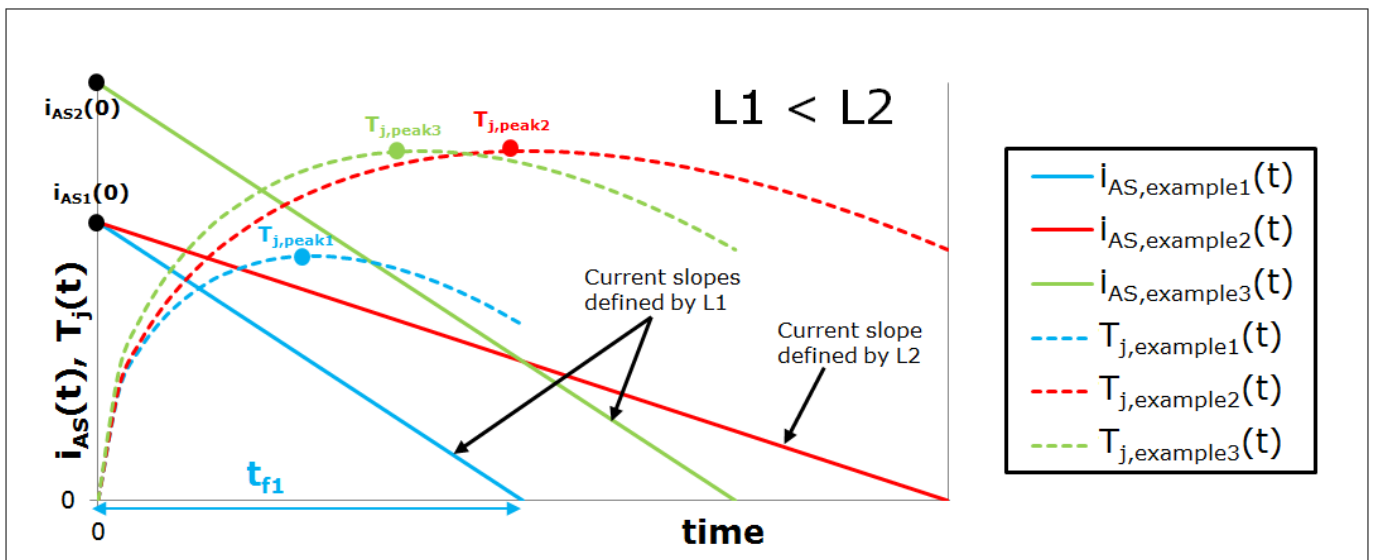


Figure 21 Impact of $i_{AS}(0)$ and L_{loop} on T_j

3 Making use of the datasheet

Under the conditions of a triangular current shape, the maximum temperature delta (ΔT_M) can be defined as follows with the help of reference [4]:

$$\Delta T_M = \frac{\sqrt{2}}{3} \times i_{AS}(0) \times V_{DS,peak} \times F_1 \times \sqrt{t_f}$$

Equation 4

There are a few comments to make about this equation, because it is slightly different to the one found in reference [4].

Firstly, the factor F_1 was denominated as “K” in [4]. We don’t follow this approach in order to avoid any confusion with the symbol for Kelvin. If using the MKS unit system, this factor F_1 is provided in $K/(W \times \sqrt{s})$. F_1 depends on the area of power generation and the thermal properties of silicon. In our examples, since we will keep the same MOSFET part number during our extrapolations and we neglect the production distribution of the MOSFET parameters, F_1 can be considered constant.

Secondly, in a similar way to [4], we assume as a first approximation that the avalanche voltage is constant. In our case, however, we define this constant voltage as being equal to the peak voltage during avalanche ($V_{DS,peak}$). The assumptions made for considering F_1 constant also apply to $V_{DS,peak}$. In addition to them, we also consider as a first approximation that $V_{DS,peak}$ does not change when extrapolating values for different avalanche energies. Following the impact of temperature on $V_{DS,peak}$ introduced in section 2.1.3, we understand that $V_{DS,peak}$ will vary when using different avalanche conditions, but we also know that such variations will remain well below 10% for all latest OptiMOS™ families, especially considering that the extrapolations will usually be for conditions where actual peak temperature values during avalanche ($T_{j,peak}$) (and therefore $V_{DS,peak}$ values) are relatively close.

Thirdly, although all temperature values in the following calculations use °C, their temperature delta ultimately refers to Kelvin.

Finally, we can confirm that the remaining terms of Equation 4 have been previously defined.

It is possible to expand t_f as follows:

$$t_f = \frac{L_{loop} \times i_{AS}(0)}{V_{DS,peak}}$$

Equation 5

By inserting Equation 5 in Equation 4, we obtain an equation that will be more useful for us:

$$\Delta T_M = \frac{\sqrt{2}}{3} \times F_1 \times V_{DS,peak}^{1/2} \times i_{AS}(0)^{3/2} \times L_{loop}^{1/2}$$

Equation 6

Having previously approximated F_1 and $V_{DS,peak}$ as being constant for a defined MOSFET, we can therefore introduce a constant factor F_2 (the unit is $K/\sqrt{I^2 \times V \times s}$) defined as follows:

$$F_2 = \frac{\sqrt{2}}{3} \times F_1 \times V_{DS,peak}^{1/2}$$

Equation 7

Using Equation 7, we can further simplify Equation 6 to obtain:

3 Making use of the datasheet

$$\Delta T_M = F_2 \times i_{AS}(0)^{3/2} \times L_{loop}^{1/2}$$

Equation 8

Within an application, the initial junction temperature ($T_{j(start)}$) and/or L_{loop} and/or $i_{AS}(0)$ will likely differ from the conditions used to define E_{AS} in Infineon datasheets. The following examples will show how designers can assess if their conditions are safe.

3.2.1 Example with $T_{j(start)} = 25^\circ\text{C}$

In this example, an application using BSC014N06NS has an initial avalanche current $i_{AS}(0) = 30\text{ A}$ and $L_{loop3} = 928\ \mu\text{H}$. For simplicity, assume that $T_{j(start)}$ is 25°C . For the E_{AS} defined within the BSC014N06NS datasheet, we had $i_{AS4}(0) = 50\text{ A}$ and $L_{loop4} = 464\ \mu\text{H}$. Note that we have chosen for our example a loop L_{loop3} that equals twice the value of L_{loop4} .

ΔT_M must remain the same for both conditions. Consequently, using Equation 8, the maximum initial avalanche current, $i_{AS3}(0)$, that this application could withstand is defined:

$$i_{AS3}(0)^{3/2} \times L_{loop3}^{1/2} = i_{AS4}(0)^{3/2} \times L_{loop4}^{1/2}$$

Equation 9

$$i_{AS3}(0) = 50\text{ A} \times \sqrt[3]{\frac{464\ \mu\text{H}}{928\ \mu\text{H}}} = 39.7\text{ A}$$

Equation 10

In this application, because $i_{AS}(0)$ is only 30 A , and therefore lower than $i_{AS3}(0)$, BSC014N06NS will safely cope with the single pulse avalanche event.

To confirm that the calculations are correct, we can derive t_{f3} using Equation 5 and obtain:

$$t_{f3} = \frac{928\ \mu\text{H} \times 39.7\text{ A}}{60\text{ V} \times 1.3} = 472\ \mu\text{s}$$

Equation 11

For the slanted curves of the SOA_{AS} graph (highlighted in blue, red and green in Figure 22), t_f corresponds to t_{AV} . In the same figure, the point B with coordinates (t_{f3} , $i_{AS3}(0)$) lies on the blue slanted line with $T_{j(start)} = 25^\circ\text{C}$, which confirms the correctness of our calculations. However, in some cases, the slanted lines plotted on the SOA_{AS} graph of our OptiMOS™ datasheets are derated slightly more than indicated by the formulas previously introduced. Nevertheless, following the method above provides a relatively accurate assessment.

3 Making use of the datasheet

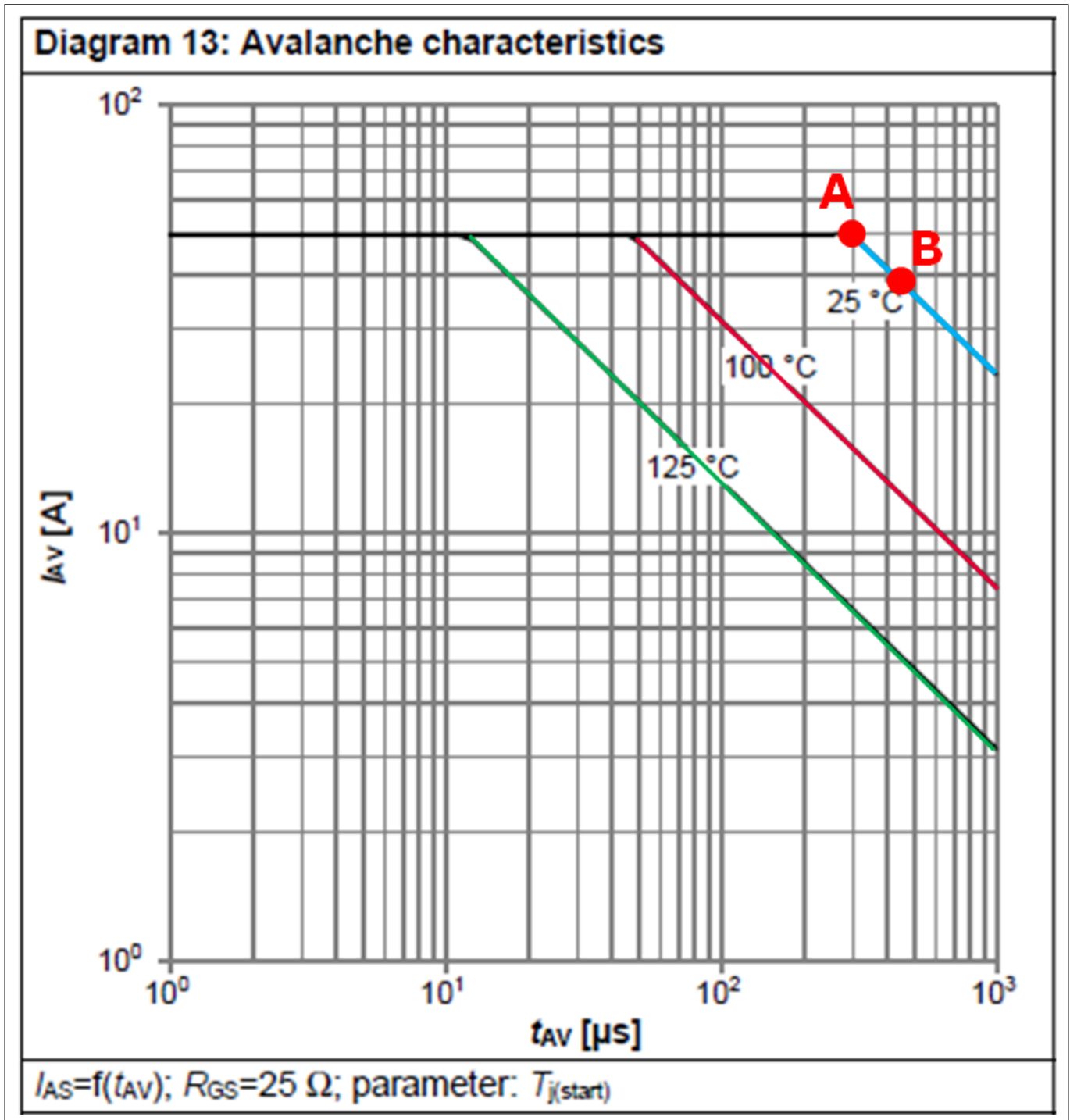


Figure 22 Using SOA_{AS} graph for BSC014N06NS when $T_{j(start)}=25^{\circ}C$

3.2.2 Repeating same procedure with a different $T_{j(start)}$

In applications where $T_{j(start)}$ is not $25^{\circ}C$, before using the formulas introduced in section 3.2, it is necessary to find a reference point for which both the E_{AS} and L_{loop} are known.

As an example, assume a $T_{j(start)}$ of $100^{\circ}C$ when using BSC014N06NS, and determine E_{AS} and L_{loop} corresponding to point C in Figure 23. Since $i_{AS}(0) = 50 A$ and $t_{AV} = 50 \mu s$, use $E_{AS} = \frac{1}{2} \times V_{DS,peak} \times i_{AS}(0) \times t_{AV}$ with $V_{DS,peak} = 1.3 \times V_{BR(DSS)(min,25)} = 78 V$ to obtain $E_{AS} = 97.5 mJ$.

3 Making use of the datasheet

Because $E_{AS} = \frac{1}{2} \times L_{loop} \times (I_{AS}(0))^2$, we can deduct that, for point C, $L_{loop} = 78 \mu H$. It is then straightforward to follow the procedure in 3.2.

If $T_{j(start)}$ does not correspond to any of the three values usually provided on the SOA_{AS} graph in the datasheet, Infineon can plot a chart using another temperature. Simply contact an Infineon representative and request this.

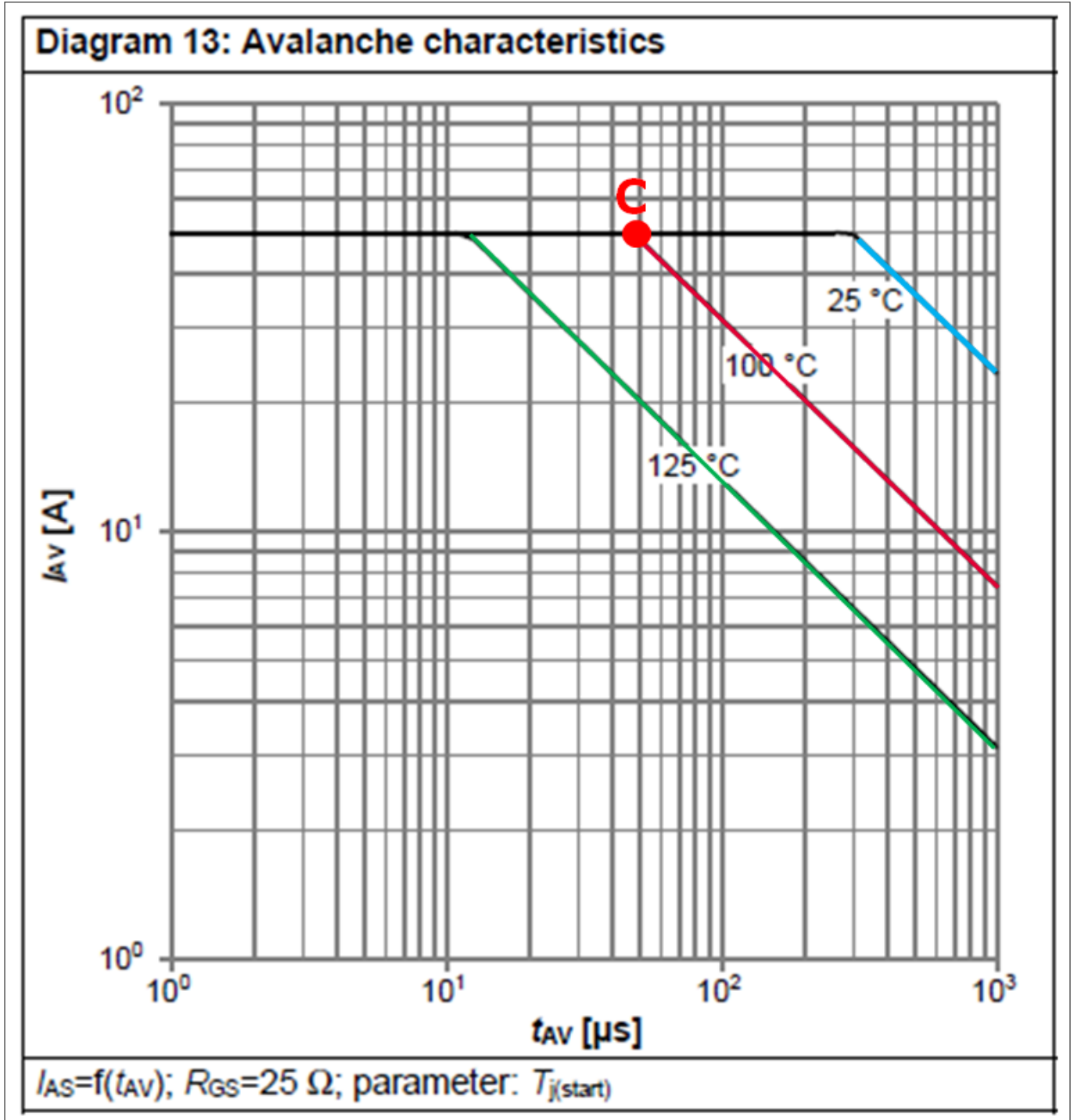


Figure 23 Using SOA_{AS} graph for BSC014N06NS when $T_{j(start)}=100^\circ C$

3 Making use of the datasheet

3.3 Variation of E_{AS} with L_{loop}

It is possible to extract further valuable information from Equation 8. Readers not wanting to follow the detail can move straight to Equation 13.

Referring to Equation 8, the exponents for L_{loop} and $i_{AS}(0)$ differ from those of the formula used for single pulse avalanche energy, namely $E_{AS} = \frac{1}{2} \times L_{loop} \times (i_{AS}(0))^2$. In Equation 8, the exponent for $i_{AS}(0)$ is not two but three times bigger than for L_{loop} . So:

- On one hand, to maintain a constant energy, $L_{loop} \times (i_{AS}(0))^2$ must remain constant;
- On the other hand, to maintain a constant temperature increase (critical to extrapolate single pulse avalanche), $L_{loop} \times (i_{AS}(0))^3$ must remain constant

Assuming that L_{loop} changes by a factor Y , then:

- $i_{AS}(0)$ will have to change by $Y^{(-1/2)}$ to keep the energy constant, and $i_{AS_e}(0) = i_{AS}(0) \times Y^{(-1/2)}$;
- $i_{AS}(0)$ will have to change by $Y^{(-1/3)}$ to maintain the same temperature increase, and $i_{AS_t}(0) = i_{AS}(0) \times Y^{(-1/3)}$.

Therefore, the variation in energy obtained when keeping the same increase in temperature relates to the factor Y of change in L_{loop} by a factor Z equal to $(i_{AS_t}(0)/i_{AS_e}(0))^2$. This gives:

$$Z = \left(\frac{Y^{(-1/3)}}{Y^{(-1/2)}} \right)^2 = Y^{\left(\left(\frac{1}{2} - \frac{1}{3} \right) \times 2 \right)}$$

Equation 12

By simplifying further:

$$Z = Y^{(1/3)}$$

Equation 13

Put another way, varying the loop inductance by a factor Y will cause single pulse avalanche energy to vary by a factor of $Y^{(1/3)}$.

This can be confirmed by reusing the results from section 3.2, which correspond to point B in [Figure 22](#). By doubling the value of L_{loop} , E_{AS} changed from 580 mJ to:

$$E_{AS} = \frac{1}{2} \times 928 \mu H \times 39.7 A^2 = 731 mJ$$

Equation 14

This corresponds to an avalanche energy increase by a factor of 1.26 (= 731 mJ/580 mJ).

Using Equation 13 with $Y = 2$, $Z = 1.26$ is also obtained, confirming the validity of this formula.

There is another point to remember from these findings: based on the above theoretical explanation, the slanted lines of the SOA_{AS} graph for any OptiMOS™ FET are NOT of constant energy!

Finally, please note that the discussion above related to OptiMOS™ FETs for which the following assumptions apply:

- The avalanche current is assumed to take a triangular shape;
- Thermal destruction is the dominant failure mechanism caused by single pulse avalanche.

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3.4 Comparing apples to apples

Previously, we learned that E_{AS} increases with L_{loop} . Therefore, when comparing the E_{AS} from datasheets of different manufacturers, ensure that the values provided are for the same L_{loop} condition! If this is not the case, using Equation 13, it is possible that you need first to re-compute the E_{AS} of each part at the same L_{loop} , preferably the one of your application circuit.

Still regarding the topic of fair comparisons, designers should only compare the avalanche capabilities of MOSFETs with similar values for $R_{DS(on)}$. Unfortunately, as different manufacturers use different technologies, it is probable that MOSFETs with the same $R_{DS(on)}$ will have different chip sizes. But, at least, this comparison makes sense.

Comparing the avalanche capabilities of MOSFETs with significantly dissimilar $R_{DS(on)}$ is not recommended. Recall that, for the same technology, the MOSFET chip size is inversely proportional to its $R_{DS(on)}$ and, as mentioned previously, bigger is usually better when coping with avalanche. Consequently, even if comparing MOSFETs from different manufacturers, it is still likely that the part with the much lower $R_{DS(on)}$ will have a larger chip size.

3.5 Datasheet diagram for thermal impedance

Since avalanche is a dynamic phenomenon, it should be of great use to refer to the variation of the thermal impedance, junction-to-case (Z_{thJC}) with pulse duration and duty cycle, provided in Infineon datasheets. In Figure 24 is an example diagram, extracted from the BSC014N06NS datasheet. As we are concerned with single pulse avalanche, the plot of particular interest is the lower one (single pulse).

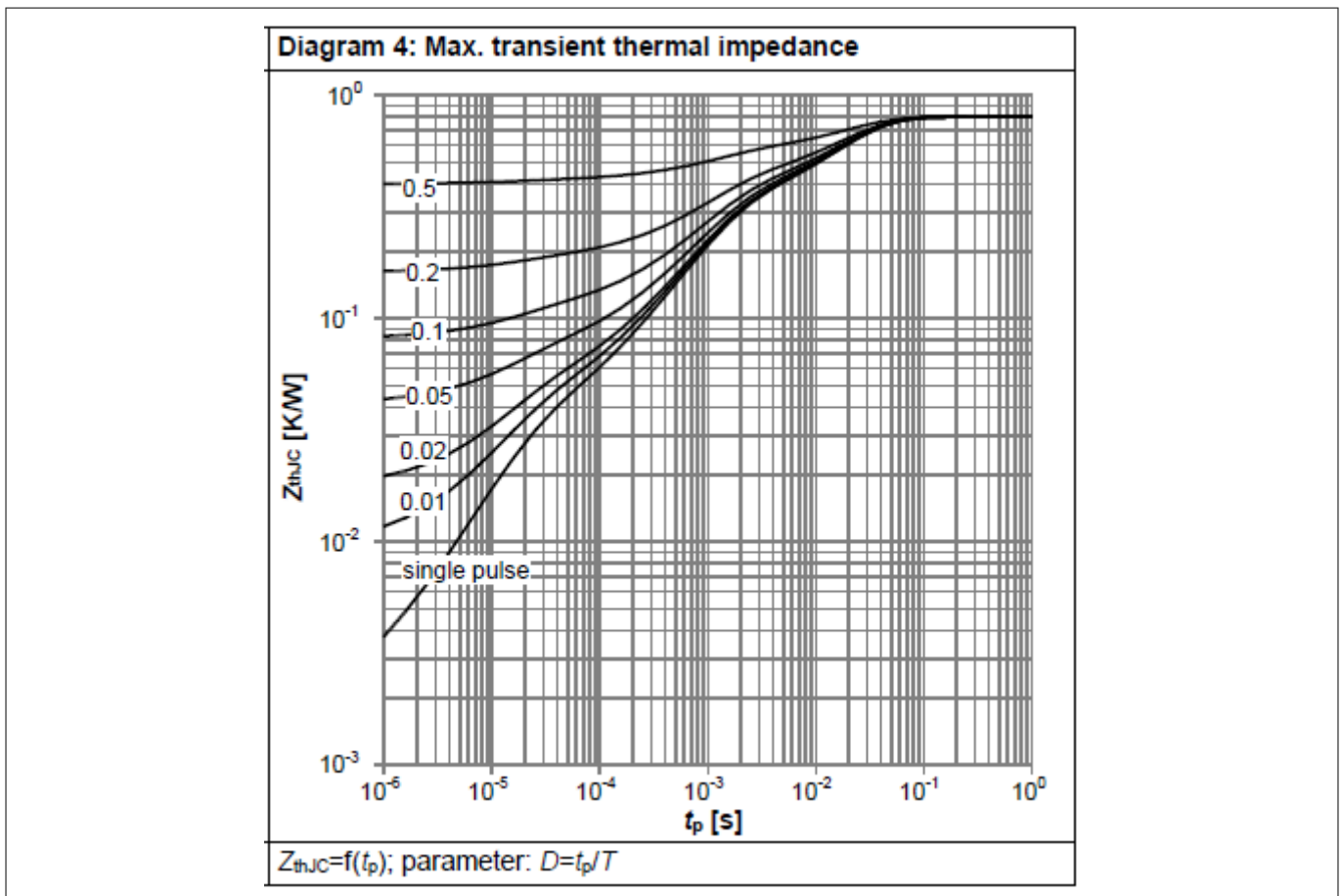


Figure 24 Diagram 4 of BSC014N06NS datasheet

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Unfortunately, as mentioned in [5], this plot tends to underestimate the impact of avalanche on the MOSFET temperature. This mismatch can mainly be attributed to the difference in the shape of the power pulse experienced by the MOSFET, as summarized in Figure 25. For plotting $Z_{thJC} = f(t_p)$ in the datasheet, the power pulse is rectangular. However, during avalanche, the power pulse can be considered to have the same triangular shape as the avalanche current when approximating the avalanche voltage as being constant.

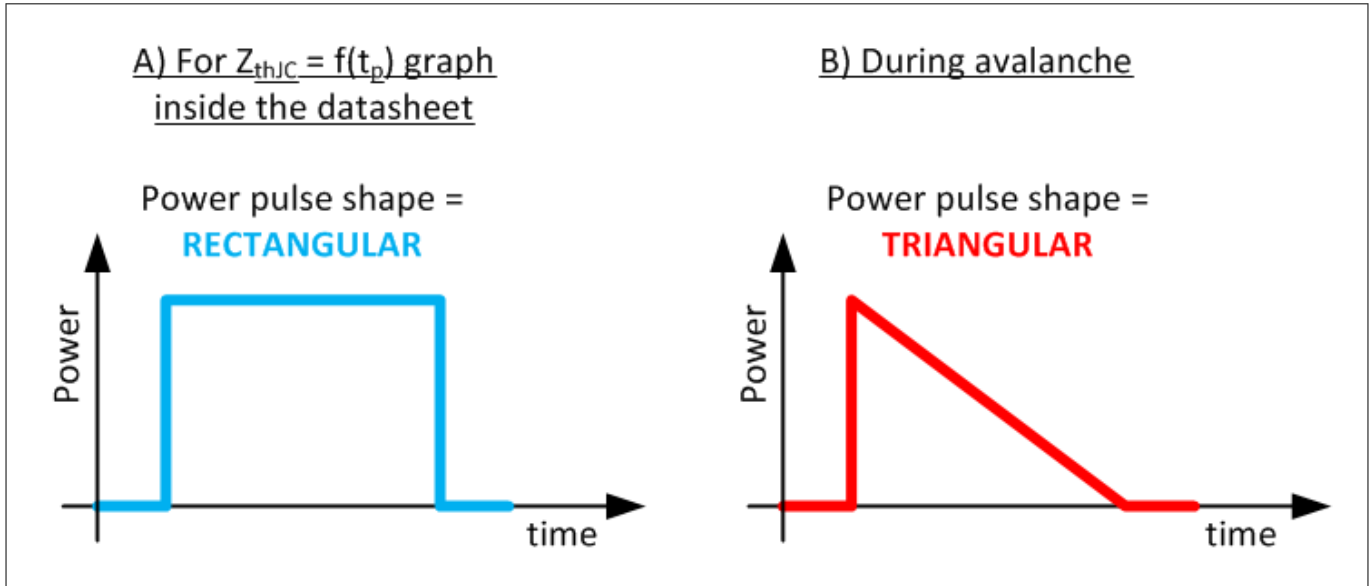


Figure 25 Shape of power pulse faced by MOSFET - $Z_{thJC} = f(t_p)$ graph vs avalanche

The typical temperature behavior of a MOSFET during single pulse avalanche can however take this effect into account relatively well by returning to PSpice simulation and re-using the circuit from [Figure 5](#). But, this time, we will not use the typical values for Z_{thJC} , as set by default for the PSpice level 3 model. Instead, to compensate for the higher impact of avalanche on MOSFET temperature, we can simulate using the maximum value of Z_{thJC} by setting the parameter “Zthtype” to 1, as shown in [Figure 26](#).

Consequently, the junction temperature will peak slightly higher than the 210°C observed in [Figure 6](#). However, this is not of concern because the following still applies:

- This $T_{j,peak}$ remains significantly more than 100°C below the $T_{j,destr}$ of the structure;
- Since only one single pulse avalanche event of such energy is tolerated, the duration above the $T_{j,max}$ of the MOSFET is so short that the lifetime is not impacted.

3 Making use of the datasheet

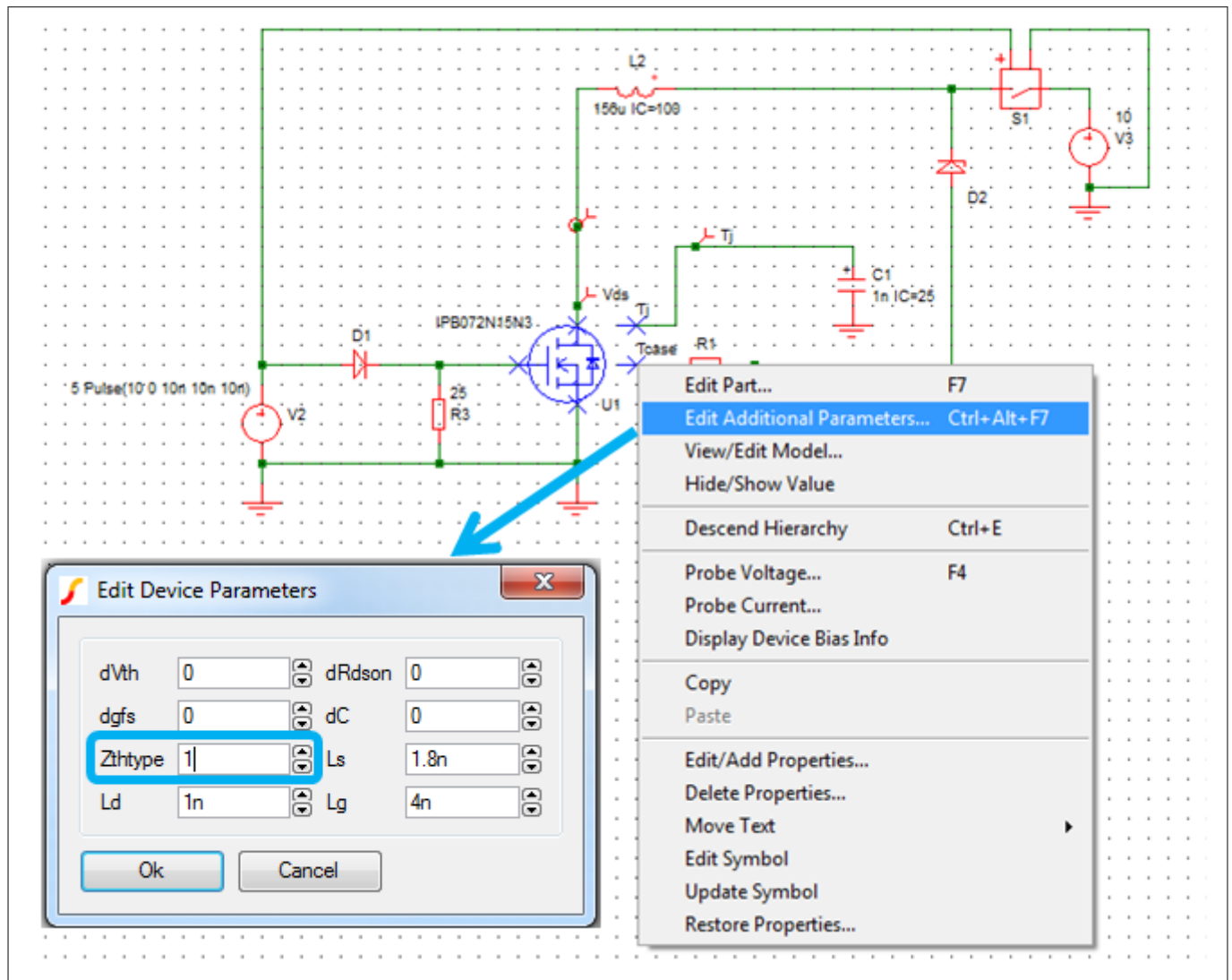


Figure 26 Setting Z_{thJC} to max value for PSpice level 3 model

4 Repetitive avalanche

4 Repetitive avalanche

4.1 What is repetitive avalanche?

In the case of repetitive avalanche, the energy per event is much lower than for single pulse avalanche. As the name implies, its occurrence is characterized by a fast repetition rate, which is typically the same as the switching frequency (f_{sw}) of the application circuit.

The existing repetitive patterns can be categorized into two main types, as shown in Figure 27.

1. In some cases, we could talk about "steady state" repetitive avalanche, because avalanche events happen during every single switching period over the entire product lifetime.
2. In other cases, we are facing some sort of "transient or fault conditions" repetitive avalanche, since avalanche only occurs under specific transient (e.g. start-up) or fault (e.g. short-circuit) conditions, during which 10 to 50 consecutive avalanche events could be observed, after which avalanche would stop until the next start-up or short-circuit causes a re-occurrence of avalanche over many consecutive voltage pulses.

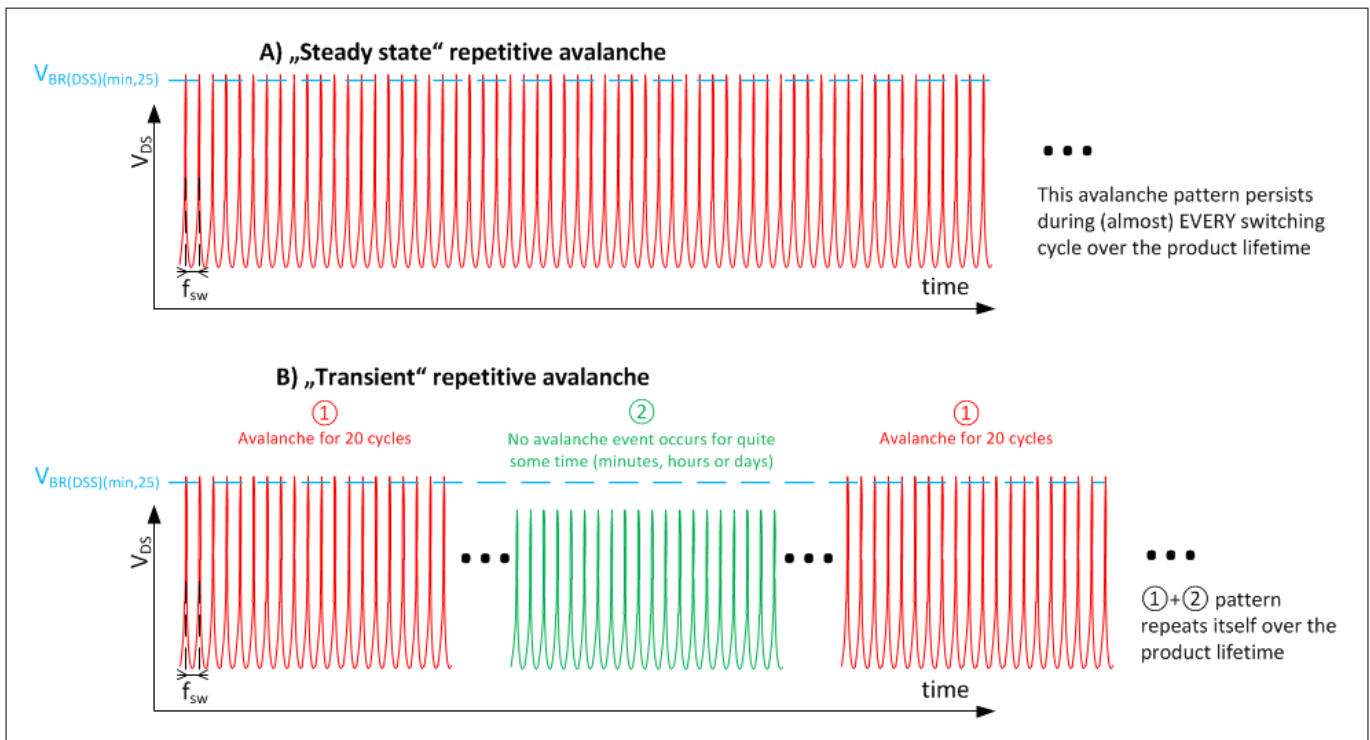


Figure 27 Two types of repetitive avalanche

In most repetitive avalanche cases, due to the low energy of each avalanche event, the silicon temperature hardly rises when compared to the worst-case of single pulse avalanche. Therefore, the observed V_{DS} spikes only slightly exceed the $V_{BR(DSS)(min,25)}$ rating of the MOSFET, as opposed to the $1.2\sim 1.3 \times V_{BR(DSS)(min,25)}$ amplitudes recorded during high-energy single pulse avalanche. This relatively low amplitude of the avalanche spikes was also observed in section 2.1.3 when discussing the topic of low energy avalanche events.

A relevant difference between single pulse and repetitive avalanche ratings relates to the permitted $T_{j,max}$ during such events. Indeed, whereas we showed in section 2.1.2 that the junction temperature is permitted to exceed $T_{j,max}$ during single pulse avalanche, this is not the case for repetitive avalanche. As highlighted on page 9 of [3], if exceeding $T_{j,max}$ during repetitive avalanche, the cumulative effect of such events could impact the reliability of the device over its lifetime, which is not acceptable.

This $T_{j,max}$ can be as low as 150°C for SuperSO8 or S308 devices, which is typically a limitation of the package itself, not of the chip technology. The latter can usually withstand 175°C, as betrayed by the fact that MOSFETs

4 Repetitive avalanche

from the same family as these SuperSO8 MOSFETs, but housed within a different package (e.g. TO-220 and D²PAK) are rated for 175°C.

4.2 Failure mechanisms

We have to distinguish between single pulse and repetitive avalanche because the way they can affect normal MOSFET behavior differs significantly.

As we saw in section 2.2, the two destruction modes for single pulse avalanche are either caused by high current (latch-up) or high energy (thermal destruction). These destruction modes are quite loud and fast.

On the contrary, in the case of repetitive avalanche, the destruction mechanism is far more unassuming and impacts the device very slowly through repeated micro-damages. Indeed, even if it is characterized by low energy, any avalanche event generates some hot carriers, which are charges injected along the trench oxide of the power MOSFET. The repetition of such avalanche events leads to an accumulation of such charges, which slowly but surely influences the normal behavior of the MOSFET, as we shall see in section 4.4.

It might be expected that the “transient or fault conditions” repetitive avalanche has a more moderate impact on the OptiMOS™ FET than the “steady state” repetitive avalanche, because potentially the former gives time for the accumulated charges to recombine between two bursts of avalanche events. In reality, such benefits are very difficult to predict, and it is very hard to build up any kind of correlation.

4.3 Locating where avalanche occurs

As opposed to single pulse avalanche, the lower energies experienced in the case of repetitive avalanche lead to a more localized onset of avalanche. If we refer to the definition provided for avalanche in section 2.1.1 and to the more specific details provided in [6], we can gain some insight into this location.

Given the rapid increase in the number of generated free carriers (and consequently in the current amplitude) as the electric field increases, avalanche is highly likely to originate in the regions of higher electric fields, where the amplitude is most likely to exceed the critical electric field (E_c) when the drain-to-source voltage applied to the device exceeds its $V_{BR(DSS)}$. Please refer to Figure 28 for further details on this.

4 Repetitive avalanche

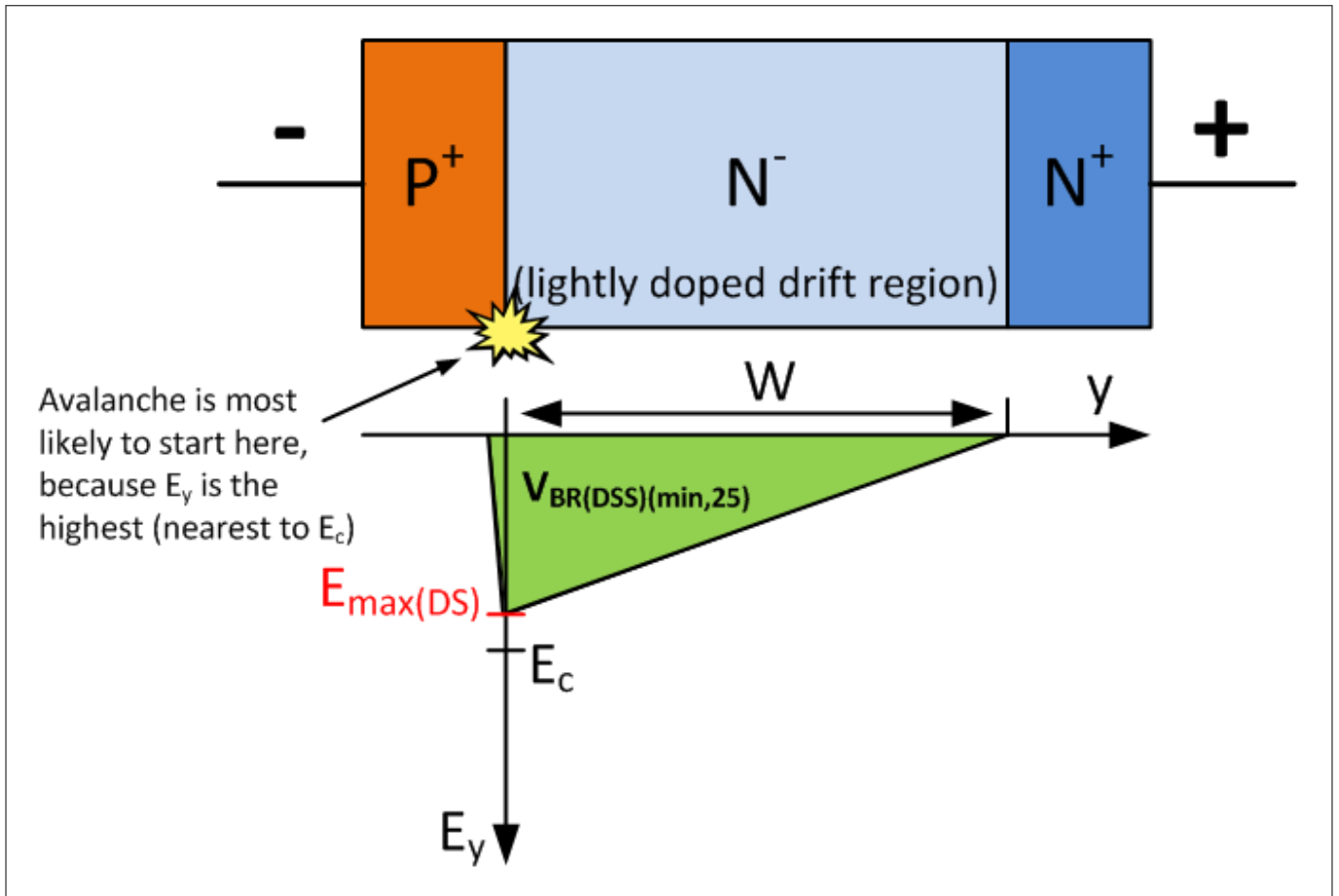


Figure 28 Most likely location for the onset of avalanche

This last statement actually poses a challenge for charge-compensated devices making use of a field plate, such as trench MOSFETs. Indeed, the insertion of a field plate permits a reduction in $R_{DS(on)}$ by enabling a better uniformity of the electric field over the whole trench. As shown in Figure 29, this uniformity ideally materializes in the shape of a rectangular distribution of the electric field along the trench, as opposed to the triangular shape of more conventional approaches (basic trench or planar structures [7]). If referring to the previous paragraph, a very uniformly distributed electric field may have very randomly located position for the onset of avalanche. Unavoidably, some compromise must be found between $R_{DS(on)}$ reduction and robustness against repetitive avalanche.

4 Repetitive avalanche

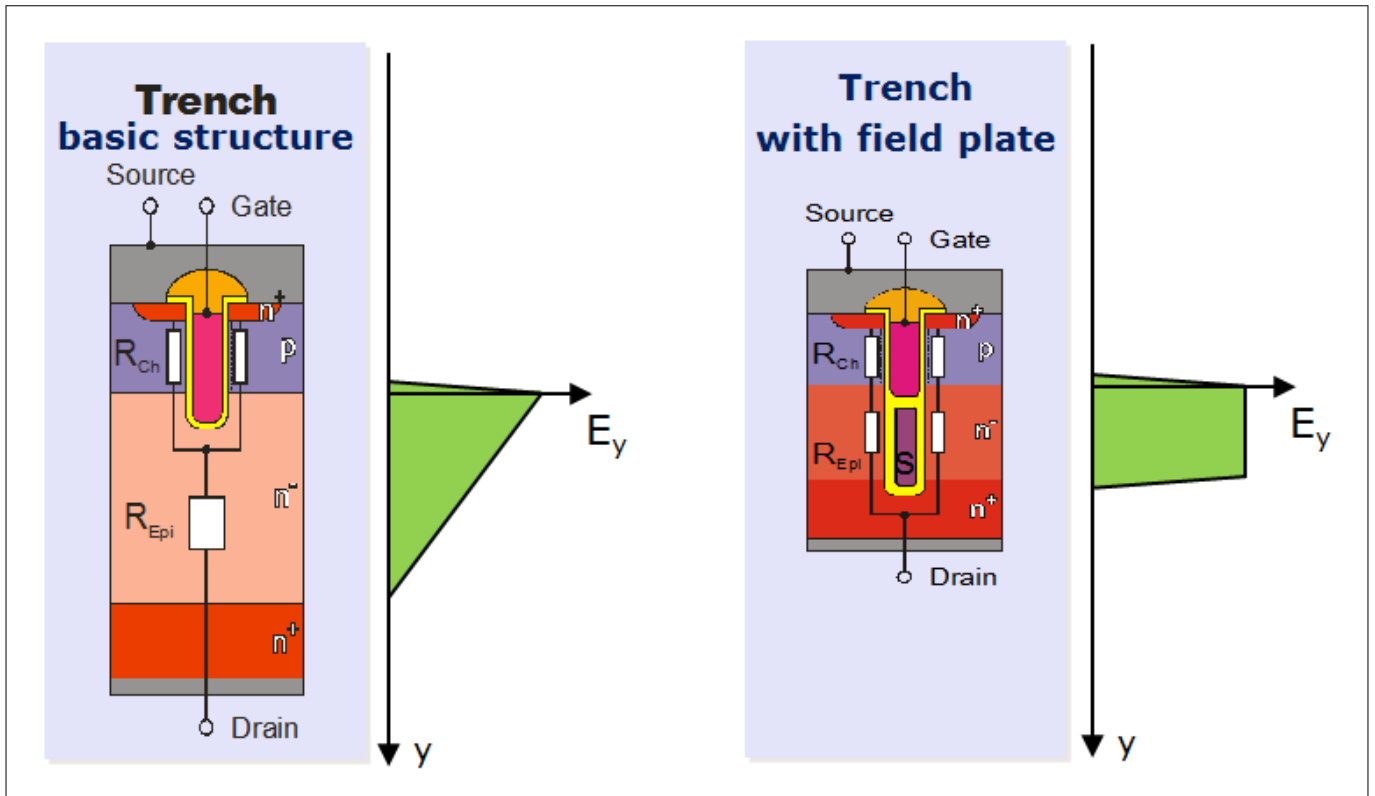


Figure 29 Change in E_y distribution along y-axis for different trench structures

4.4 Rating of OptiMOS™ families under repetitive avalanche

Over the last few years, repetitive avalanche has been considered during the design phase of most of Infineon's OptiMOS™ families. It was observed that some parameters drift over time, with the amount of drift and the actual parameters being dependent on the technology. Figure 30 provides an example of parametric drift for a particular technology. It can clearly be seen that, in the majority of cases, the zero gate voltage drain current (I_{DSS}) and transconductance (g_m) shift closer to the datasheet limits when experiencing repetitive avalanche under the conditions internally defined for this technology. Adding on top of that the natural distribution of the parameters over multiple production lots, there is a clear risk for parameters to move out of specification.

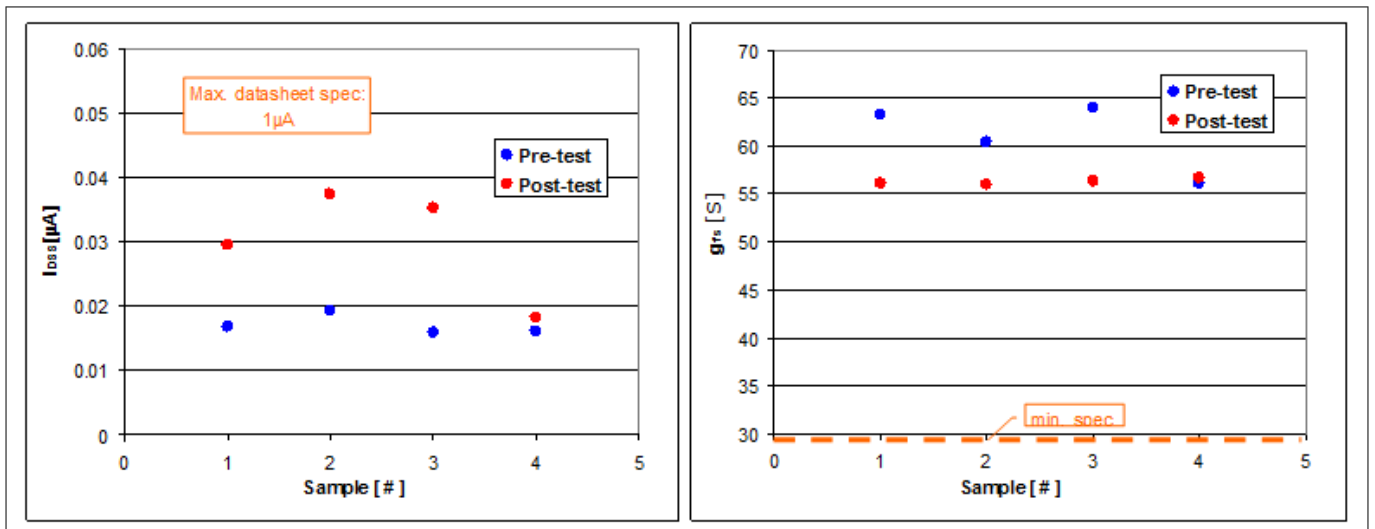


Figure 30 Example of parameters drift during repetitive avalanche

4 Repetitive avalanche

Taking this into account, so as to significantly reduce the impact of repetitive avalanche on technology parameters, Infineon would need to compromise significantly on other figures of merit that are dominant in the vast majority of applications. This would be too high of a price to pay for an event that does not correspond to a normal usage of a MOSFET, and that a designer should strive to avoid by all means. Consequently, Infineon does not insert repetitive avalanche ratings within the OptiMOS™ “Industrial and Standard Grades” datasheets.

5 References

5 References

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6 List of abbreviations

6 List of abbreviations

BJT = Bipolar Junction Transistor

C_{thi} = Thermal capacitance for i^{th} stage of the MOSFET PSpice model

DUT = Device Under Test

E_{AS} = Avalanche energy, single pulse

E_C = Critical electric field

E_{max} = Maximum electric field within the structure

$E_{max(aval)}$ = Maximum electric field within the structure during avalanche

FET = Field Effect Transistor

f_{sw} = Switching frequency

g_{fs} = Transconductance

$i_{AS}(0)$ = Initial current for single pulse avalanche

I_{crit} = Critical current at which the parasitic bipolar transistor is activated

I_{DS} = Drain to source current

I_{DSS} = Zero gate voltage drain current

MOSFET = Metal Oxide Semiconductor Field Effect Transistor

$R_{DS(on)}$ = Drain-source on-state resistance

R_{thi} = Thermal resistance for i^{th} stage of the MOSFET PSpice model

R_{thJA} = Thermal resistance, junction-to-ambient (usually provided with device mounted on a PCB)

SOA_{AS} = Safe Operating Area under single pulse avalanche

t_f = Time taken for avalanche current to reduce to 0

T_j = Junction temperature

$T_{j,destr}$ = Destructive junction temperature

$T_{j,max}$ = Maximum junction temperature

$T_{j,peak}$ = Peak junction temperature during avalanche

$T_{j(start)}$ = Junction temperature at the onset of avalanche

t_p = Pulse duration

UIS = Unclamped Inductive Switching

$V_{BR(DSS)}$ = Drain-source breakdown voltage

$V_{BR(DSS)(min,25)}$ = Datasheet rating for minimum drain-source breakdown voltage @ $T_j=25^\circ\text{C}$

V_{DS} = Drain-source voltage

$V_{DS,peak}$ = Peak V_{DS} voltage during avalanche

Z_{thJC} = Thermal impedance, junction-to-case

ΔT_M = Maximum temperature delta

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Edition 2017-01-9

Published by
Infineon Technologies AG
81726 Munich, Germany

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Document reference
IFX-nac1473154083210

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