LOW NOISE OSCILLATOR SERVICE SHEET

The A18 Low Noise Oscillator board assembly contains two PLLs (Phase locked Loops), and provides the LO (local oscillator signal) to the HP 4195A measurement unit.

CIRCUIT DESCRIPTION:

Figure 1 shows a block diagram of the A18 board assembly. The A18 board consists of a step loop, a sum loop, and a control circuit for these loops.

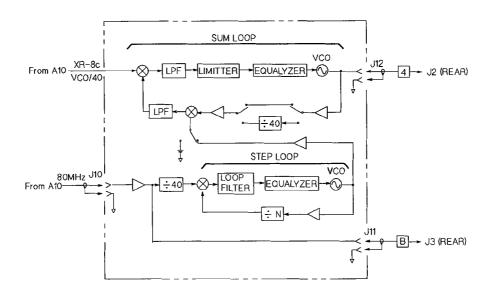


Figure 1. A18 Low Noise Oscillator Block Diagram

The 80 MHz signal from A10 (through A18J10) is amplified and divided to two paths. One signal goes to the rear panel J3 connector (through A18J11). The other signal is divided by 40 (equals to 2 MHz), and is used as the reference frequency for the step loop. The step loop is a PLL circuit which generates 226 MHz to 406 MHz in 2 MHz steps.

The sum loop is a PLL circuit which generates a frequency equal to the sum of the fractional N PLL output frequency (5.833333333 MHz to 10.33333333 MHz, VCO/40 signal) and the step loop output frequency (226 MHz to 406 MHz).

The mixer sums the signals from the sum loop's VCO and the step loop output. The sum frequency of the two signals filtered out by the lowpass filter. The difference frequency of the two signals is passed to the phase detector.

The fractional N PLL output from A10 (VCO/40 signal through A18XR-8c) goes to the phase detector as the reference frequency of the sum loop.

The phase detector outputs the difference frequency component of the lowpass filter output signal and the fractional N PLL output signal (VCO/40 signal).

Then the Sum Loop VCO is controlled so that its output frequency equals the sum of the fractional N PLL output (VCO/40 signal) frequency and the step loop output frequency.

The sum loop operation described above is applicable only when the set SPAN frequency is equal to or narrower than 2.4 MHz.

When the set frequency SPAN is wider than 2.4 MHz, a ÷40 divider is inserted in the sum loop before the mixer, and the step loop output is disabled and a dc voltage is applied to the mixer instead.

The sum loop's VCO output frequency divided by 40 and the fractional N PLL output frequency are compared by the phase detector, so that the VCO output frequency equals to the frequency of the fractional N PLL multiplied by 40.

LOOP FREQUENCIES

```
CASE 1. CENTER < 150 MHz and SPAN \leq 2.4 MHz
```

SUM LOOP (MHz) RF + 246.66666667

STEP LOOP (MHz) 238 (CENTER: 1 mHz to 416.666667 kHz)

240 (CENTER: 416.666667 kHz to 2.416666667 MHz) 242 (CENTER: 2.416666667 MHz to 4.416666667 MHz)

386 (CENTER: 146.416666667 MHz to 148.416666667 MHz) 388 (CENTER: 148.416666667 MHz to 149.999999999 MHz)

VCO/40 (MHz) RF + 246.666666667 - STEP

CASE 2. 150 MHz \leq CENTER < 320 MHz and SPAN \leq 2.4 MHz

SUM LOOP (MHz) RF + 86.66666667

STEP LOOP (MHz) 228 (CENTER: 150 MHz to 150.416666667 MHz)

230 (CENTER: 150.416666667 MHz to 152.416666667 MHz) 232 (CENTER: 152.416666667 MHz to 154.416666667 MHz)

396 (CENTER: 316.416666667 MHz to 318.416666667 MHz)

398 (CENTER: 318.416666667 MHz to 319.999999999 MHz)

VCO/40 (MHz) RF + 86.66666667 - STEP

CASE 3. 320 MHz \leq CENTER and SPAN \leq 2.4 MHz

SUM LOOP (MHz) RF - 86.66666667

STEP LOOP (MHz) 226 (CENTER: 320 MHz to 321.75 MHz)

230 (CENTER: 321.75 MHz to 323.75 MHz) 232 (CENTER: 323.75 MHz to 325.75 MHz)

396 (CENTER: 497.75 MHz to 499.75 MHz)

398 (CENTER: 499.75 MHz to 500 MHz)

VCO/40 (MHz) RF - 86.66666667 - STEP

NOTE

The SUM LOOP output can be monitored at the control unit's rear panel **J2** connector (LOCAL OUT). The **VCO/40** signal comes from A10 through A18XR-8c.

TROUBLESHOOTING GUIDE

1. 80 MHz INPUT CHECK

- 1-1. Disconnect the coaxial cable from A18J10.
- 1-2. Monitor the signal at the disconnected end of the coaxial cable comes from the A10 board, and confirm that its frequency is 80 MHz and its amplitude is -9 dBm ±1 dB. If not, troubleshoot the A10 board.
- 1-3. Reconnect the coaxial cable to A18J10 and reinstall the A18 board.

2. 80 MHz OUTPUT CHECK

2-1. Monitor the signal at **J3** (80M OUT) on the control unit rear panel, and confirm that its frequency is **80 MHz** and its amplitude is **-8 dBm** ±2 dB. If not, replace the A18 board.

3. SUM LOOP OUTPUT CHECK (Single Loop Mode)

3-1. Extend the A18 board. Turn the HP 4195A on. Set up the HP 4195A as follows:

START 320 MHz
STOP 500 MHz
SWEEP TRIGGER MODE MANUAL

MANUAL Frequency 320 MHz (use MARKER knob to control)

- 3-2. Monitor the signal at A18XR-8c using a high impedance (low capacitance) probe, and confirm that its frequency is **5.8333333333 MHz** and its amplitude is **0 dBm** ±2 dB. If is not, troubleshoot the A10 board.
- 3-4. Change the HP 4195A MANUAL Frequency to 500 MHz using the MARKER knob.

- 3-7. Reinstall the A18 board in its normal position.

4. STEP LOOP OPERATION CHECK (Triple Loop Mode)

4-1. Cycle the HP 4195A off and on. Set up the HP 4195A as follows:

CENTER 320 MHz SPAN 0 Hz (zero)

- 4-2. Monitor the signal at connector **J2** (LOCAL OUT) on the control unit rear panel, and confirm that its frequency is **233.333333333 MHz** and its amplitude is **-8 dBm** ±2 dB. If is not, replace the A18 board.
- 4-3. Change the CENTER frequency to 500 MHz.
- 4-4. Monitor the signal at connector J2 (LOCAL OUT) on the control unit rear panel, and confirm that its frequency is 413.333333333 MHz and its amplitude is -8 dBm ±2 dB. If not, replace the A18 board.

PARTS INFORMATION

Table 1. A18 Replaceable Parts

Reference Designator	HP Part Number	Description
A18	04195-66518 04195-69518	LOW NOISE OSC LOW NOISE OSC (RE-BUILT)
1,	04195-00624 04195-00628	CASE SHIELD (Component Side) CASE SHIELD (Circuit Side)
2	04195-00625 04195-00629	CASE SHIELD (Component Side) CASE SHIELD (Circuit Side)
3	04195-00626 04195-00630	CASE SHIELD (Component Side) CASE SHIELD (Circuit Side)
4	04195-00627 04195-00631	CASE SHIELD (Component Side) CASE SHIELD (Circuit Side)

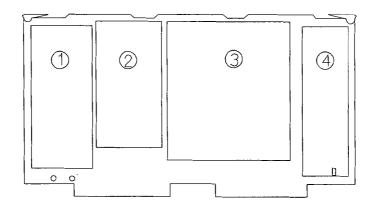


Figure 1. A18 Shield Cases