Migration Guide:
MACRONIX MX25L12805D and MX25L6405D Serial Flash migrating to
MACRONIX MX25L12845E and MX25L6445E Serial Flash

Contents

Migration Guide:
MACRONIX MX25L12805D and MX25L6405D Serial Flash migrating to MACRONIX MX25L12845E and MX25L6445E Serial Flash

1.0 Introduction

This application notes is the migration guide description about how to replace the design from MACRONIX's 128Mb and 64Mb MX25Lxx05D Serial Flash to MACRONIX's MX25Lxx45E. This description is written based on device information available at the time. The MX25Lxx45E datasheet may override this application notes if there is a different description for the same items in the datasheet.

2.0 Major Feature Comparison

The table is a major organization and specification comparison.

	MX25L12805D	MX25L12845E	MX25L6405D	MX25L6445E
Technology	130nm	110nm	130nm	110nm
Packages	300 mil 16-SOP	300 mil 16-SOP 8-WSON(8mmx6mm) (note1)	300 mil 16-SOP 8-WSON(8mmx6mm)	300 mil 16-SOP 200 mil 8-SOP 8-WSON(8mmx6mm)
Temperature Grade	I Grade	I Grade	I Grade	I Grade
Voltage	2.7-3.6V	2.7-3.6V	2.7-3.6V	2.7-3.6V
Interface	x1	x1/x2/x4	x1/x2	x1/x2/x4
Page	256B	256B	256B	256B
Sector	4KB	4KB	4KB	4KB
Block	64KB	32KB & 64KB	64KB	32KB & 64KB
Write Protect	BP0~BP3	BP0~BP3 or individual Block Protect	BP0~BP3	BP0~BP3 or individual Block Protect
OTP	512 bits	4K bits	512bits	4K bits
Parallel mode	x	v	x	x

Notes:
1.MX25L12845EMI-10G 16SOP has PO0~PO7. These pins are for parallel data input and output, which are NC pins defined in MX25L12805DMI-10G.
2.The symbol “x” means no function, ”v” means functional.

Migration Guide:
MACRONIX MX25L12805D and MX25L6405D Serial Flash migrating to
MACRONIX MX25L12845E and MX25L6445E Serial Flash

2-1 DC Characteristic differences

	MX25L12805D	MX25L12845E	MX25L6405D	MX25L6445E
Vcc Standby (ISB1)	20uA (max)	100uA (max)	20uA (max)	10uA (max)
Deep Power-Done (ISB2)	x	40uA (max)	x	30uA (max)
Icc (Read)	15mA @ 33MHz (max) 25mA @ 50MHz (max)	10mA @ 33MHz (max) 15mA @ 66MHz (max) 19mA @ 104MHz (max)	10mA @ 33MHz (max) 20mA @ 66MHz (max) 25mA @ 86MHz (max)	10mA @ 33MHz (max) 15mA @ 66MHz (max) 19mA @ 104MHz (max)
Icc (Write)	20mA (max)	20mA (max)	20mA (max)	20mA (max)

2-2 Read Performance

MX25L12845/6445E fast read performance is enhanced and provides multi IO interface (MXSMIO™ and MXSMIO™ Duplex for Double Transfer Rate, DTR) and backward compatible with MX25L12805/6405D.

	MX25L12805D	MX25L12845E	MX25L6405D	MX25L6445E
Normal Read (1 I/O)	33MHz	50MHz	33MHz	50MHz
Fast Read	50MHz[1 I/O]	104MHz[1 I/O] 140MHz [2 I/O] 280MHz [4 I/O] 100MHz [1 I/O DTR] 200MHz [2 I/O DTR] 400MHz [4 I/O DTR]	86MHz[1 I/O] 100MHz[2 I/O]	104MHz[1 I/O] 140MHz [2 I/O] 280MHz [4 I/O] 100MHz [1 I/O DTR] 200MHz [2 I/O DTR] 400MHz [4 I/O DTR]

2-3 Write Performance

	MX25L12805D	MX25L12845E	MX25L6405D	MX25L6445E
Page Program	1.4ms(Typ.) 5ms(max)	1.4ms(Typ.) 5ms(max)	1.4ms(Typ.) 5ms(max)	1.4ms(Typ) 5ms(max)
Byte Program	9us(Typ) 300us(max)	9us(Typ) 300us(max)	9us(Typ) 300us(max)	9us(Typ) 300us(max)
Sector Erase	60ms(typ) 300ms(max)	60ms(typ) 300ms(max)	60ms(typ) 300ms(max)	60ms(typ) 300ms(max)
Block Erase	0.7s(typ)/2s(max) (64KB)	0.5s(typ)/2s(max) (32KB) 0.7s(typ)/2s(max) (64KB)	0.7s(typ)/2s(max) (64KB)	0.5s(typ)/2s(max) (32KB) 0.7s(typ)/2s(max) (64KB)
Chip Erase	80s(typ)/200s(max)	80s(typ)/200s(max)	50s(typ)/80s(max)	50s(typ)/80s(max)

2-4 Write Protection Comparison

MX25L12845/6445E maintains traditional BP0~BP3 4 protection bits for protect area selection, and also has the flexible uniform block and top/bottom sector lock individually with WPSEL option bit. Under the individual block protection mode (WPSEL=1), hardware protection is performed by driving WP#=0. Once WP#=0 all array blocks/ sectors are protected, it is regardless of the contents of SRAM lock bits.

	MX25L12805/6405D	MX25L12845/6445E
Write Protect	BP0~BP3	BP0~BP3 or individual Block Protect

MX25L12845/6445E BP0~BP3 protection area is different from MX25L12805/6405D, the following table is the comparison for reference.

Status bit				Protection Area			
BP3	BP2	BP1	BP0	MX25L12845E	MX25L12805D	MX25L6445E	MX25L6405D
0	0	0	0	0 (none)	0 (none)	0 (none)	0 (none)
0	0	0	1	1 (2 blocks, 254th-255th)	1 (1 block, 255th)	1 (2 blocks, 126th-127th)	1 (2 blocks, 126th-127th)
0	0	1	0	2 (4 blocks, 252nd-255th)	2 (2 blocks, 254th-255th)	2 (4 blocks, 124th-127th)	2 (4 blocks, 124th-127th)
0	0	1	1	3 (8 blocks, 248th-255th)	3 (4 blocks, 252nd-255th)	3 (8 blocks, 120th-127th)	3 (8 blocks, 120th-127th)
0	1	0	0	4 (16 blocks, 240th-255th)	4 (8 blocks, 248th-255th)	4 (16 blocks, 112nd-127th)	4 (16 blocks, 112nd-127th)
0	1	0	1	5 (32 blocks, 224th-255th)	5 (16 blocks, 240th-255th)	5 (32 blocks, 96th-127th)	5 (32 blocks, 96th-127th)
0	1	1	0	6 (64 blocks, 192nd-255th)	6 (32 blocks, 224th-255th)	6 (64 blocks, 64th-127th)	6 (64 blocks, 64th-127th)
0	1	1	1	7(128 blocks, 128th-255th)	7 (64 blocks, 192th-255th)	7 (128 blocks, all)	7 (128 blocks, all)
1	0	0	0	8 (256 blocks, all)	8(128 blocks, 128th-255th)	8 (128 blocks, all)	8 (128 blocks, all)
1	0	0	1	9 (256 blocks, all)	9 (256 blocks, all)	9 (128 blocks, all)	9 (64 blocks, 0th-63rd)
1	0	1	0	10 (256 blocks, all)	10 (256 blocks, all)	10 (128 blocks, all)	10 (96 blocks, 0th-95th)
1	0	1	1	11 (256 blocks, all)	11 (256 blocks, all)	11 (128 blocks, all)	11 (112 blocks, 0th-111st)
1	1	0	0	12 (256 blocks, all)	12 (256 blocks, all)	12 (128 blocks, all)	12 (120 blocks, 0th-119th)
1	1	0	1	13 (256 blocks, all)	13 (256 blocks, all)	13 (128 blocks, all)	13 (124 blocks, 0th-123rd)
1	1	1	0	14 (256 blocks, all)	14 (256 blocks, all)	14 (128 blocks, all)	14 (126 blocks, 0th-125th)
1	1	1	1	15 (256 blocks, all)	15 (256 blocks, all)	15 (128 blocks, all)	15 (128 blocks, all)

2-5 Status Register

MX25L12845/6445E Quad IO mode needs Status Register QE bit to enable to be effective.

	MX25L12805/6405D	MX25L12845/6445E
bit 0	WIP 1=write operation 0=not in write operation	WIP 1=write operation 0=not in write operation
bit 1	WEL 1=write enable 0=not write enable	WEL 1=write enable 0=not write enable
bit 2	BP0	BP0
bit 3	BP1	BP1
bit 4	BP2	BP2
bit 5	BP3	BP3
bit 6	(Reserved)	QE (Quad Enable) 1=Quad Enable 0=not Quad Enable
bit 7	SRWD Status Register Write Protect	SRWD Status Register Write Protect

2-6 Security Register

MX25L12845/6445E open 4 more Security Register bits for various functions: CP mode bit, WPSEL bit and program/erase fail flag bits for detecting the write progress pass or fail.

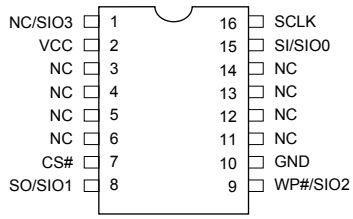
	MX25L12805/6405D	MX25L12845/6445E
bit 0	Secured OTP Indicator Bit 0=non factory lock 1=factory lock	Secured OTP Indicator Bit 0=non factory lock 1=factory lock
bit 1	LDSO (Lock-down status) 0=not Lock-down 1=Lock-down	LDSO (Lock-down status) 0=not Lock-down 1=Lock-down
bit 2	Reserved	Reserved
bit 3	Reserved	Reserved
bit 4	Reserved	Continuously Program Mode 0=normal program mode 1=CP mode
bit 5	Reserved	P_FAIL 0= nornal program succeed 1= program failed
bit 6	Reserved	E_FAIL 0= nornal Erase succeed 1= Erase failed
bit 7	Reserved	WPSEL 0= normal WP mode 1= Individual WP mode

Migration Guide:
MACRONIX MX25L12805D and MX25L6405D Serial Flash migrating to
MACRONIX MX25L12845E and MX25L6445E Serial Flash

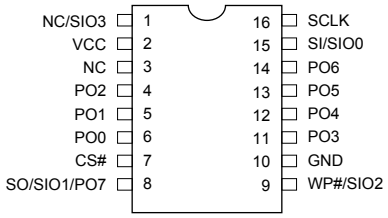
3.0 Hardware Pin 16-PIN SOP Comparison

Only MX25L12845E has PO pin for parallel mode. Moreover, only MX25L12805/6405D have hold# pin. MX25L12845/6445E provide SIO2/SIO3 interface for quad IO read.

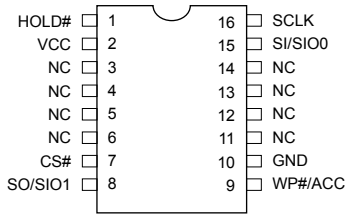
16-PIN SOP (300mil) for MX25L6445E



16-PIN SOP (300mil) for MX25L12845E



16-PIN SOP (300mil) for MX25L12805/6405D



4.0 Conclusion

The MX25L12855/6445E serial flash memory device is function compatible with the MX25L12805D/6405D serial flash memory device on the 110nm technology.

Migration Guide:
MACRONIX MX25L12805D and MX25L6405D Serial Flash migrating to
MACRONIX MX25L12845E and MX25L6445E Serial Flash

Revision History

Revision No.	Description	Page	Date
0.01	1. Added hardware pin comparison.	P8	JUN/02/2009
	2. Added BP0~BP3 protection comparison	P5	
1.0	1. Modified *2.0 Major Feature Comparison* table	P2	JUL/12/2010
	2. Modified *2-1 DC Characteristic differences* table	P3	
	3. Modified *2-4 Write Protection Comparison* table	P5	

Macronix's products are not designed, manufactured, or intended for use for any high risk applications in which the failure of a single component could cause death, personal injury, severe physical damage, or other substantial harm to persons or property, such as life-support systems, high temperature automotive, medical, aircraft and military application. Macronix and its suppliers will not be liable to you and/or any third party for any claims, injuries or damages that may be incurred due to use of Macronix's products in the prohibited applications.

For the contact and order information, please visit Macronix's Web site at: http://www.macronix.com