Migrating from MX25L12836E/45E/35E to MX25L12835F

1. Introduction

This application note compares MX25L12836E, MX25L12845E, MX25L12835E and MX25L12835F Macronix Serial Flash. The document does not provide detailed information on individual devices, but highlights the similarities and differences between them. The comparison covers the general features, performance, command sets, and device identification numbers.

The information provided in this document is based on datasheets listed in Section 8. Newer versions of the datasheets may override the contents of this document.

2. General Features

2-1. Feature Comparison

The MX25L12835F product provides a feature rich solution to cover legacy products which include MX25L12835E, MX25L12836E and MX25L12845E chips.

The MX25L12835F improves the flexibility of device operation with the addition of a new Configuration Register and the Advanced Sector Protection mode.

The Configuration Register sets the number of dummy clock cycles used for fast read operations, the output drive strength, and selects either the top or bottom of memory to be a Block Protect (BP) area.

The MX25L12835E, MX25L12836E, MX25L12845E, and MX25L12835F devices support an individual block protection method as an alternative to the grouped block protection provided by Status Register Block Protection (BP) bits. In addition to single block protection, the MX25L12835F added additional protection features in the Advanced Sector Protection mode that provide higher levels of protection. These higher levels of protection include:

1. Nonvolatile individual sector/block protection.
2. A software locking mechanism to prevent modifications to the nonvolatile protection until after the next Reset or power-up cycle.
3. A password protection option.

These additional protection features can be used to prevent accidental or deliberate data corruption in protected memory areas. Please see the MX25L12835F datasheet for more details.

For additional product differences, please check the descriptions and comparison tables below.

Table 2-1. Feature Comparison

Part no.		MX25L12836E	MX25L12845E	MX25L12835E	MX25L12835F
Technology		110nm	110nm	110nm	75nm
Density		128Mb	128Mb	128Mb	128Mb
VCC		2.7V-3.6V	2.7V-3.6V	2.7V-3.6V	2.7V-3.6V
Structure					
Normal Read		50MHz	50MHz	50MHz	50MHz
Maximum Command Clock Frequency (except READ, 2READ, DREAD, 4READ, QREAD, 4PP)		104MHz	104MHz	104MHz	133MHz (all commands except READ)
Fast Read I/O Support	FAST READ (1-1-1)	Yes	Yes	Yes	Yes
	DREAD (1-1-2)	Yes	Yes	Yes	Yes
	2READ (1-2-2)	-	Yes	Yes	Yes
	QREAD (1-1-4)	Yes	Yes	Yes	Yes
	4READ (1-4-4)	-	Yes	Yes	Yes
	QPI (4-4-4)	-	-	-	Yes
DTR		-	Yes	-	-
Configurable Dummy Cycles		-	-	-	Yes
Sector Size		4KB/32KB/64KB	4KB/32KB/64KB	4KB/32KB/64KB	4KB/32KB/64KB
Program Buffer Size		256Byte	256Byte	256Byte	256Byte
Security OTP		4KBit	4KBit	4KBit	4KBit
BP Protect		Top	Top	Top	Top/Bottom
Software Features					
Read Enhance Mode		Yes	Yes	Yes	Yes
Wrap-around Read Mode		-	-	Yes	Yes
S/W Reset Command		-	-	Yes	Yes
Erase Suspend & Resume		-	-	-	Yes
Program Suspend & Resume		-	-	-	Yes
Adjustable Output Driver Strength		-	-	-	Yes
Fast Boot Mode		-	-	-	Yes
Deep Power Down		Yes	Yes	Yes	Yes
Individual/Volatile Write Protection		Yes	Yes	Yes	Yes
Individual/Nonvolatile Write Protection		-	-	-	Yes
Password Protection		-	-	-	Yes
Hardware Features					
Reset# Pin		-	-	Yes (16SOP only)	Yes
Hold# Pin		-	-	Yes	-
Package Solution	8SOP (209mil)	-	-	-	Yes
	16SOP (300mil)	Yes	Yes	Yes	Yes
	8WSON (8x6mm^2)	Yes	Yes	Yes	Yes
	8WSON (6x5mm^2)	-	-	-	Yes

2-2. Write Protection Comparison

The E (MX25L12835E, MX25L12836E & MX25L12845E) and F (MX25L12835F) version products provide two write protection modes to easily protect sectors from inadvertent changes. The default is Block Protection Mode, utilizing the nonvolatile Block Protection (BP) bits in the Status Register. The BP bits specify which block groups will be protected. The second mode uses an individual block protection method. This method utilizes a volatile SRAM lock bit assigned to each block (or sector) and controls its protection status. The Gang Block Lock (GBLK) and Gang Block Unlock (GBULK) commands set or clear all SRAM lock bits simultaneously and these commands are identical for both E and F versions. The E and F versions use different commands to control individual SRAM lock bits, and this will be discussed in more detail below.

2-2-1 Block Protection (BP) Mode

Both E and F versions use identical Status Register BP bits to specify which group of blocks to protect, but block group sizes are different. The F version has a finer granularity of protection. Furthermore, the F version has the ability to specify whether block protection begins at the top or bottom of memory. This is controlled by the Top/Bottom (TB) bit in the F version's new Configuration Register. The TB default setting is '0' and specifies the top of memory.

Table 2-2 compares the E and F version block protection as specified by all possible BP bit combinations. The E version has no option to begin block protection from the bottom of memory, so the F version's bottom blocks are not shown.

Table 2-2: Block Protection (BP) Comparison (top memory blocks only)

Status Register Bit				Protected Blocks			
BP3	BP2	BP1	BP0	E version		F version	
0	0	0	0	none		none	
0	0	0	1	2 blocks	(#254-255)	1 block	(#255)
0	0	1	0	4 blocks	(#252-255)	2 blocks	(#254-255)
0	0	1	1	8 blocks	(#248-255)	4 blocks	(#252-255)
0	1	0	0	16 blocks	(#240-255)	8 blocks	(#248-255)
0	1	0	1	32 blocks	(#224-255)	16 blocks	(#240-255)
0	1	1	0	64 blocks	(#192-255)	32 blocks	(#224-255)
0	1	1	1	128 blocks	(#128-255)	64 blocks	(#192-255)
1	0	0	0	256 blocks	(all)	128 blocks	(#128-255)
1	0	0	1	256 blocks	(all)	256 blocks	(all)
1	0	1	0	256 blocks	(all)	256 blocks	(all)
1	0	1	1	256 blocks	(all)	256 blocks	(all)
1	1	0	0	256 blocks	(all)	256 blocks	(all)
1	1	0	1	256 blocks	(all)	256 blocks	(all)
1	1	1	0	256 blocks	(all)	256 blocks	(all)
1	1	1	1	256 blocks	(all)	256 blocks	(all)

2-2-2 Individual Block Protection Mode

Individual block protection is only effective after executing the WPSEL command. This one-time-use command permanently disables the block group protection method (Status Register BP bits) and activates individual block protection. The WPSEL command is common to both E and F versions.

E and F version devices implement individual block protection differently and require different commands. The following sections will discuss both implementations.

2-2-3 Individual Block Protection versus Advanced Sector Protection

The ability to quickly unlock individual blocks is convenient when changes are required, but it also makes the protected areas vulnerable to corrupt or malicious software. To enhance the security of the protection feature, the MX25L12835F has added Advanced Sector Protection. Advanced Sector Protection adds nonvolatile protection bits with the ability to lock them until the next reset or power-up cycle. It also adds an optional password mode to further enhance protection. These new features require different commands and the user's application software will need to be modified if the features are desired.

The following sections show the operational differences between E and F version products when using individual sector/block protection.

2-2-4 MX25L12835E/12836E/12845E Individual Block Protection Mode

The Single Block Lock Protection bits are volatile SRAM bits assigned to each protectable sector or block. The bits permit sectors or blocks to be protected individually and independent of any other sector or block. The Single Block Lock Protection bits default to protected mode (set to '1') upon power-up or reset. Table 2-3 illustrates in green, which blocks can be individually protected.

Table 2-3: Individually Protectable Sectors/Blocks

64KB Block #	4KB Sector #	Protectable
255	4095 . . . 4080	16 4KB sectors (lock/unlock)
254	4079 … 4064	254 64KB blocks (lock/unlock)
. . .	. . .	
1	31 . 16	
0	15 . . . 0	16 4KB sectors lock/unlock

Only the sector and block numbers highlighted in green are individually protectable.
The Single Block Lock (SBLK) instruction (36h) enables read only protection for the specified sector

or block of memory. Sector selection is made using address bits A23-A12 and only the top and bottom sixteen 4KB sectors can be individually protected. The remaining sectors are grouped into 64KB blocks. Individual 64KB block selection is made using address bits A23-A16. Use the Single Block Unlock (SBULK) instruction (39h) to cancel the individual sector or block protection state.
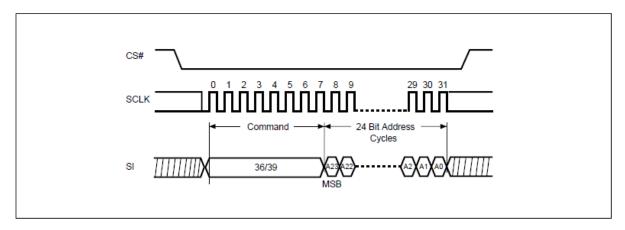
Figure 2-1: Single Block Lock/Unlock Protection (SBLK/SBULK) Sequence

2-2-5 MX25L12835F Individual Block Protection Mode

Dynamic Protection Bits (DPB) are volatile and similar in purpose to the Single Block Lock Protection bits used by the E version devices. Nonvolatile Solid Protection Bits (SPB) is a new feature. Each protectable sector or block (Table 2-3: Individually Protectable Sectors/Blocks) is assigned one DPB and one SPB. This permits sector or block protection to be specified individually and independent of any other sector or block. The DPB default to the protect state (FFh) upon power-up or reset. They work in conjunction with the nonvolatile SPB. Both DPB and SPB states must be cleared to 00h before the associated sector or block can be modified. The SPB are preset to 00h at the factory and there is no need to modify them if you are only migrating from an E version product to the MX25L12835F. Please refer to the MX25L12835F datasheet if you need to use the SPB features.

The SPB protection can also temporary unprotect by solid write protect bit (USPB) feature to temporarily unprotect the sectors protected by SPB.

To modify the DPB status, issue the DPB Program command (WRDPB) including the target sector or block address and set or clear the DPB protection state. All DPB bits can be quickly unlocked by issuing one Gang Block Unlock (GBULK) command (98h). Sector selection is made using address bits A23-A12 and only the top and bottom sixteen 4KB sectors can be individually protected. The remaining sectors are grouped into 64KB blocks. Individual 64KB block selection is made using address bits A23-A16.

DPB Register (DPBR)

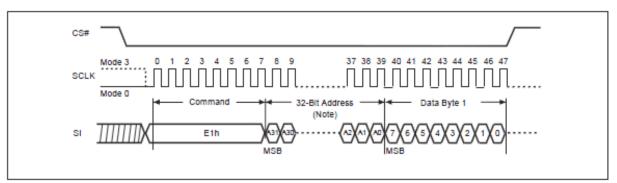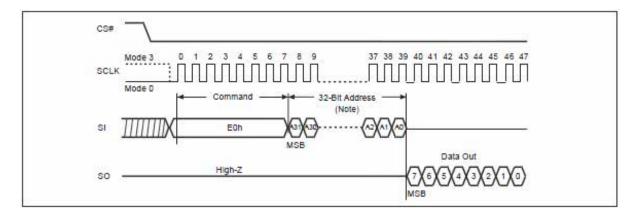| Bit	Description	Bit Status	Default	Type
7 to 0	DPB (Dynamic protected Bit)	00h= DPB for the sector address unprotected FFh=DPB for the sector address protected	FFh	Volatile

2-2-5 MX25L12835F Individual Block Protection Mode - Continued

Figure 2-2: Write DPB Register (WRDPB) Sequence

Figure 2-3: Read DPB Register (RDDPB) Sequence

3. Performance Comparison

The MX25L12835F provides better Fast Read performance, shorter program/erase times, and has lower power consumption than the E version parts.

Table 3-1: Read Performance Comparison

Read Performance	MX25L12836E	MX25L12845E	MX25L12835E	MX25L12835F
VCC	2.7V-3.6V	2.7V-3.6V	2.7V-3.6V	2.7V-3.6V
Normal Read (1-1-1)	50MHz	50MHz	50MHz	50MHz
FASTREAD (1-1-1)	104MHz	104MHz	104MHz	104MHz*
DREAD (1-1-2)	70MHz	-	70MHz	104MHz*
2READ (1-2-2)	-	70MHz	70MHz	84MHz*
QREAD (1-1-4)	70MHz	-	70MHz	104MHz*
4READ (1-4-4)	-	70MHz	70MHz	84MHz*
QPI (4-4-4)	-	-	-	84MHz*
Double Transfer Rate	-	50MHz	-	-
Configurable Dummy Cycles	-	-	-	Yes

*__Note__: All MX25L12835F read modes (except Normal Read Mode) can run at **133MHz** if the number of dummy cycles are increased.

Table 3-2: AC Performance Comparison

AC Performance		Condition	MX25L12836E	MX25L12845E	MX25L12835E	MX25L12835F
Erase	4KB	typ	60ms	60ms	60ms	43ms
		max	300ms	300ms	300ms	200ms
	32KB	typ	0.5s	0.5s	0.5s	0.19s
		max	2s	2s	2s	1s
	64KB	typ	0.7s	0.7s	0.7s	0.34s
		max	2s	2s	2s	2s
	Chip Erase	typ	80s	80s	80s	72s
		max	200s	200s	200s	160s
Program	256Byte	typ	1.4ms	1.4ms	1.4ms	0.6ms
		max	5ms	5ms	5ms	3ms
Clock Low to Output Valid	15pf	max	9.5ns	9.5ns	8ns	6ns
	30pf	max	12ns	12ns	8ns	8ns

Table 3-3: DC Performance Comparison

DC Performance		MX25L12836E	MX25L12845E	MX25L12835E	MX25L12835F
Active Current	Read (4I/O)	22mA	22mA	22mA	20mA
	Erase	25mA	25mA	25mA	25mA
	Program	25mA	25mA	25mA	25mA
VCC Standby Current		100uA	100uA	100uA	30uA(typ)/ 100uA(max)
Deep Power Down Current		40uA	40uA	40uA	5uA(typ)/ 20uA(max)

(**Note**: All of the data shown in Table 3-3 are maximum values unless noted otherwise).

4. Package and Pinout Comparison

Figure 4-1 shows the common packages and the pinout assignments for the E and F version devices. Only the MX25L12835E supports the HOLD# function. It has an internal pull-up and can be left floating if it is not used. It is NC/SIO3 on the other devices. If HOLD# is not used in the application, this difference will not matter.

The MX25L12836E and MX25L12845E support the parallel data input/output mode using pins PO[7:0], whereas the MX25L12835E and MX25L12835F flash do not support this mode. This parallel mode is normally only used by external programmers and should not be a problem for in-circuit applications.

Of the three E version devices shown, only the MX25L12835E supports the hardware RESET# pin and then only in the 16-pin SOP package. The MX25L12835F supports the hardware RESET# function in all available packages. RESET# has an internal pull-up and can be left floating if it is not used.

Figure 4-1: Packages and Pinouts

16-PIN SOP (300mil)										
MX25L12835E	MX25L12836E	MX25L12845E	MX25L12835F			MX25L12835E	MX25L12836E	MX25L12845E	MX25L12835F
HOLD#/SIO3	NC/SIO3	NC/SIO3	HOLD#/SIO3	1	16	SCLK	SCLK	SCLK	SCLK
VCC	VCC	VCC	VCC	2	15	SI/SIO0	SI/SIO0	SI/SIO0	SI/SIO0
RESET#	NC	NC	RESET#	3	14	NC	PO6	PO6	NC
NC	PO2	PO2	NC	4	13	NC	PO5	PO5	NC
NC	PO1	PO1	NC	5	12	NC	PO4	PO4	NC
NC	PO0	PO0	NC	6	11	NC	PO3	PO3	NC
CS#	CS#	CS#	CS#	7	10	GND	GND	GND	GND
SO/SIO1	SO/SIO1/PO7	SO/SIO1/PO7	SO/SIO1	8	9	WP#/SIO2	WP#/SIO2	WP#/SIO2	WP#/SIO2

8-WSON										
MX25L12835E (8x6mm)	MX25L12836E (8x6mm)	MX25L12845E (8x6mm)	MX25L12835F (8x6mm)			MX25L12835E (8x6mm)	MX25L12836E (8x6mm)	MX25L12845E (8x6mm)	MX25L12835F (6x5mm, 8x6mm)
CS#	CS#	CS#	CS#	1	8	VCC	VCC	VCC	VCC
SO/SIO1	SO/SIO1	SO/SIO1	SO/SIO1	2	7	HOLD#/SIO3	NC/SIO3	NC/SIO3	RESET#/SIO3
WP#/SIO2	WP#/SIO2	WP#/SIO2	WP#/SIO2	3	6	SCLK	SCLK	SCLK	SCLK
GND	GND	GND	GND	4	5	SI/SIO0	SI/SIO0	SI/SIO0	SI/SIO0

5. Command Code Comparison

All of the commands are listed in Table 5-1 below. Most commands are common. Differences are due to unsupported or new features.

Table 5-1: Command Code Comparison

Command	Symbol	Description	MX25L12836E	MX25L12845E	MX25L12835E	MX25L12835F
ID Read	RDID	Read Identification	9Fh	9Fh	9Fh	9Fh
	RES	Read Electronic ID	ABh	ABh	ABh	ABh
	REMS	Read Electronic Manufacturer & Device ID	90h	90h	90h	90h
	REMS2	2 x I/O Read ID	EFh	EFh	EFh	-
	REMS4	4 x I/O Read ID	DFh	DFh	DFh	-
	QPIID	QPI ID Read	-	-	-	AFh
Read	READ	Read Data	03h	03h	03h	03h
	FAST READ	Fast Read	0Bh	0Bh	0Bh	0Bh
	2READ	2 x I/O Fast Read	-	BBh	BBh	BBh
	DREAD	1I 2O Fast Read	3Bh	3Bh	3Bh	3Bh
	4READ	4 x I/O Fast Read	-	EBh	EBh	EBh
	QREAD	1I 4O Fast Read	6Bh	6Bh	6Bh	6Bh
	W4READ	4 x I/O Fast Read with 4 dummy clock cycles	-	-	E7h	-
	FASTDTRD	Fast DT Read	-	0Dh	-	-
	2DTRD	Dual I/O DT Read	-	BDh	-	-
	4DTRD	Quad I/O DT Read	-	EDh	-	-
	RDSFDP	-	5Ah	5Ah	5Ah	5Ah
Erase	SE	Sector Erase	20h	20h	20h	20h
	BE (64K)	Block Erase 64KB	D8h	D8h	D8h	D8h
	BE (32K)	Block Erase 32KB	52h	52h	52h	52h
	CE	Chip Erase	60h or C7h	60h or C7h	60h or C7h	60h or C7h
Program	PP	Page Program	02h	02h	02h	02h
	4PP	Quad Page Program	38h	38h	38h	38h
	CP	Continuously Program Mode	ADh	ADh	ADh	-
Mode	WREN	Write Enable	06h	06h	06h	06h
	WRDI	Write Disable	04h	04h	04h	04h
	DP	Deep Power Down	B9h	B9h	B9h	B9h
	RDP	Release from Deep Power Down	ABh	ABh	ABh	ABh
	EQIO	Enable QPI	-	-	-	35h
	RSTQIO	Reset (Exit) QPI	-	-	-	F5h
	SBL	Set Burst Length	-	-	77h	C0h
	WPSEL	Write Protect Selection	68h	68h	68h	68h
	ESRY	Enable SO to Output RY/BY#	70h	70h	70h	-
	DSRY	Disable SO to Output RY/BY#	80h	80h	80h	-
	ENPLM	Enter Parallel Mode	55h	55h	-	-
	EXPLM	Exit Parallel Mode	45h	45h	-	-
	HPM	High Performance Mode Enable	-	A3h	-	-
	ENSO	Enter Secured OTP	B1h	B1h	B1h	B1h
	EXSO	Exit Secured OTP	C1h	C1h	C1h	C1h
	PGM/ERS Suspend	Suspend Program/ Erase	-	-	-	B0h
	PGM/ERS Resume	Resume Program/ Erase	-	-	-	30h

Table 5-1: Command Code Comparison - Continued

Command	Symbol	Description	MX25L12836E	MX25L12845E	MX25L12835E	MX25L12835F
Reset	NOP	No Operation	-	-	00h	00h
	RSTEN	Reset Enable	-	-	66h	66h
	RST	Reset Memory	-	-	99h	99h
	CLSR	Clear SR Fail Flags	30h	30h	30h	Note 1
Register	WRSR	Write Status Register	01h	01h	01h	01h
	RDSR	Read Status Register	05h	05h	05h	05h
	RDSCUR	Read Security Register	2Bh	2Bh	2Bh	2Bh
	WRSCUR	Write Security Register	2Fh	2Fh	2Fh	2Fh
	RDCR	Read Configuration Register	-	-	-	15h
	RDFBR	Read Fast Boot Register	-	-	-	16h
	WRFBR	Write Fast Boot Register	-	-	-	17h
	ESFBR	Erase Fast Boot Register	-	-	-	18h
Protection	SBLK	Single Block Lock	36h	36h	36h	-
	SBULK	Single Block Unlock	39h	39h	39h	-
	RDBLOCK	Block Protect Read	3Ch	3Ch	3Ch	-
	GBLK	Gang Block Lock	7Eh	7Eh	7Eh	7Eh
	GBULK	Gang Block Unlock	98h	98h	98h	98h
	WRLR	Write Lock Register	-	-	-	2Ch
	RDLR	Read Lock Register	-	-	-	2Dh
	RDPASS	Read Password Register	-	-	-	27h
	WRPASS	Write Password Register	-	-	-	28h
	PASSULK	Password Unlock	-	-	-	29h
	RDSPB	Read SPB Status	-	-	-	E2h
	WRSPB	SPB bit Program	-	-	-	E3h
	ESSPB	All SPB bit Erase	-	-	-	E4h
	SPBLK	SPB Lock Set	-	-	-	A6h
	RDSPBLK	Read SPB Lock Register	-	-	-	A7h
	RDDPB	Read DPB Register	-	-	-	E0h
	WRDPB	Write DPB Register	-	-	-	E1h

Note 1: The MX25L12835F does not have a Clear Security Register Fail Flags command to clear the E_FAIL or P_FAIL flags as the E versions do. The MX25L12835F clears these flags automatically upon successful completion of an erase or program operation.

6. Device ID Code Comparison

Table 6-1 shows that the Manufacturer and Device IDs have not changed.

Table 6-1: ID Code Comparison

Electronic Identification		MX25L12836E	MX25L12845E	MX25L12835E	MX25L12835F
RDID	Manufacturer ID	C2h	C2h	C2h	C2h
	Type	20h	20h	20h	20h
	Density	18h	18h	18h	18h
RES	Electronic ID	17h	17h	17h	17h
REMS/REMS2/ REMS4	Manufacturer ID	C2h	C2h	C2h	C2h
	Device ID	17h	17h	17h	17h

7. Summary

The MX25L12835F is backwards compatible with most of the common commands and features of the earlier E versions. Additionally, the supported package types have identical footprints and nearly identical pinout definitions. A more detailed analysis should be done if "special" functions such as: Hold, Continuous Program Mode, Double Transfer Rate Fast Reads (available on MX25L12845E only), or individual sector or block protection is used. If common features are used in standard traditional modes, the replacement will only need minimal software modification.

8. References

Table 8-1 shows the datasheet versions used for comparison in this application note. For the most current Macronix specification, please refer to the Macronix Website at http://www.macronix.com

Table 8-1: Datasheet Version

Datasheet	Location	Date Issued	Versions
MX25L12835F	Macronix Website	Dec. 26, 2012	Rev. 1.1
MX25L12835E	Macronix Website	May 28, 2012	Rev 1.3
MX25L12836E	Macronix Website	Aug. 01, 2012	Rev. 1.7
MX25L12845E	Macronix Website	Feb. 10, 2012	Rev. 1.8

9. Revision History

Table 9-1: Revision History

Revision No.	Description	Page	Date
REV. 1	Initial Release	ALL	SEP. 04, 2012
REV. 2	Optimization of Packages and Pinouts figure	9	MAR. 27, 2013
REV. 3	Add Temporary Unprotect Description of SPB	5	JUN. 25, 2013

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