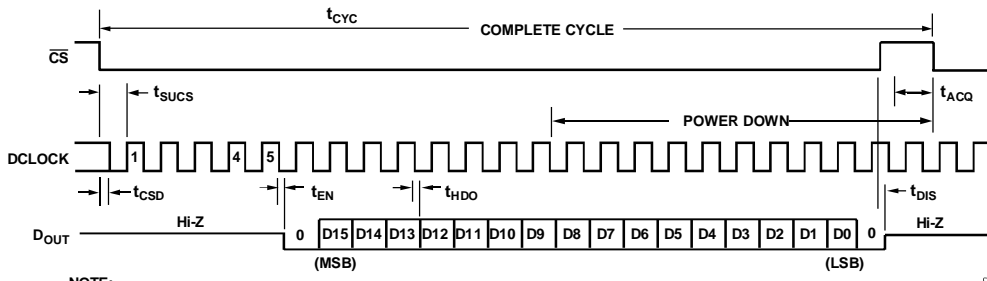


## TIMING SPECIFICATIONS

VDD = 2.7 V to 5.5 V; TA = -40°C to +85°C, unless otherwise noted.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit
Throughput Rate	t <sub>CYC</sub>			100	kHz
$\overline{\text{CS}}$ Falling to DCLOCK Low	t <sub>CSD</sub>			0	μs
$\overline{\text{CS}}$ Falling to DCLOCK Rising	t <sub>SUCS</sub>	20			ns
DCLOCK Falling to Data Remains Valid	t <sub>HDO</sub>	5	16		ns
$\overline{\text{CS}}$ Rising Edge to D <sub>OUT</sub> High Impedance	t <sub>DIS</sub>		14	100	ns
DCLOCK Falling to Data Valid	t <sub>EN</sub>		16	50	ns
Acquisition Time	t <sub>ACQ</sub>	400			ns
D <sub>OUT</sub> Fall Time	t <sub>F</sub>		11	25	ns
D <sub>OUT</sub> Rise Time	t <sub>R</sub>		11	25	ns



NOTE:  
 A MINIMUM OF 22 CLOCK CYCLES ARE REQUIRED FOR 16-BIT CONVERSION. SHOWN ARE 24 CLOCK CYCLES.  
 D<sub>OUT</sub> GOES LOW ON THE DCLOCK FALLING EDGE FOLLOWING THE LSB READING.

04-301-002

Figure 2. Serial Interface Timing