TIMING SPECIFICATIONS

VDD = 2.7 V to 5.5 V; T_A = −40°C to +85°C, unless otherwise noted.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit
Throughput Rate	t_{CYC}			100	kHz
$\overline{CS}$ Falling to DCLOCK Low	t_{CSD}			0	µs
$\overline{CS}$ Falling to DCLOCK Rising	t_{SUCS}	20			ns
DCLOCK Falling to Data Remains Valid	t_{HDO}	5	16		ns
$\overline{CS}$ Rising Edge to D_{OUT} High Impedance	t_{DIS}		14	100	ns
DCLOCK Falling to Data Valid	t_{EN}		16	50	ns
Acquisition Time	t_{ACQ}	400			ns
D_{OUT} Fall Time	t_F		11	25	ns
D_{OUT} Rise Time	t_R		11	25	ns

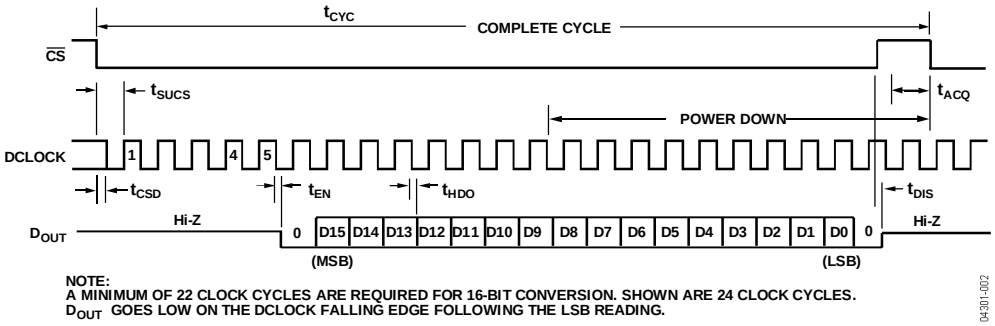

Figure 2. Serial Interface Timing