16-Bit I2C-Bus and SMBus I/O Port with Interrupt

Features

- Operation Power Supply Voltage from 2.3V to 5.5V
- 16-bit I/O pins which can be programmed as Input or Output
- 5V Tolerant I/Os
- Polarity Inversion Register
- Active LOW Interrupt Output
- Low Current Consumption
- 0Hz to 400KHz Clock Frequency
- Noise Filter on SCL/SDA Inputs
- Power-On Reset
- ESD Protection (4KV HBM and 1KV CDM)
- Latch-Up Tested (Exceeds 100mA)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Offered in Two Different Packages: TSSOP-24 and TQFN 4x4-24

Description

The PI4IOE5V9555 is an I²C-bus I/O expander that provides 16-bits of general purpose parallel input/output (GPIO) expansion for I²C-bus/SMBus applications. Its features include a higher driving capability, 5V tolerance, lower power supply, individual I/O configuration, and smaller packaging. It provides a simple solution when an additional I/O is required for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PI4IOE5V9555 consists of two 8-bit configuration registers to configure the I/Os as either inputs or outputs, and two 8-bit polarity registers to change the polarity of the input port register data. The data for each input or output is kept in the corresponding input port or output port register. All registers can be read by the system master.

The PI4IOE5V9555 open-drain interrupt output is activated and indicates to the system when any input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three input pins (A0, A1, A2) can select the I²C-bus address of PI4IOE5V9555 from the eight preset address. It allows up to eight PI4IOE5V9555 to share the same I²C-bus/SMBus and provide maximum 128 I/Os.

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

©Diodes Incorporated

Pin Configuration

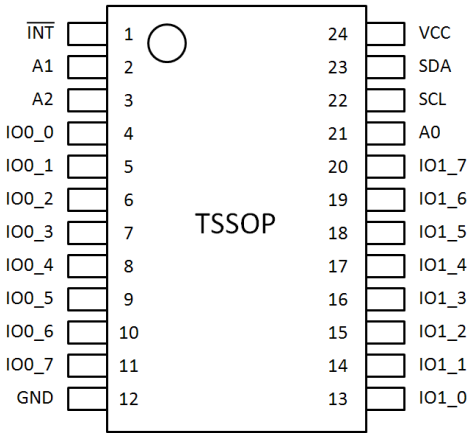


Figure 1. TSSOP-24 (Top View)

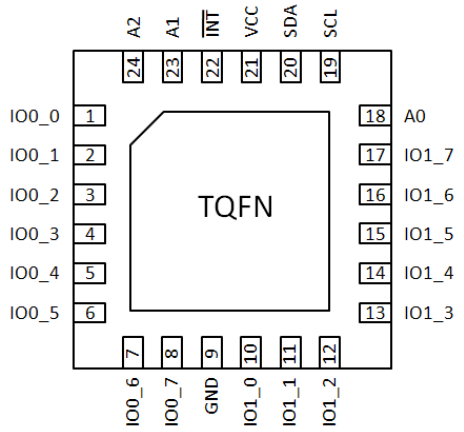


Figure 2. TQFN 4x4-24 (Top View)

Pin Description

Pin		Name	Type	Description
TSSOP24	TQFN24			
1	22	$\overline{INT}$	O	Interrupt Input (Open-Drain)
2	23	A1	I	Address Input 1
3	24	A2	I	Address Input 2
4	1	IO0_0	I/O	Port 0 Input/Output 0
5	2	IO0_1	I/O	Port 0 Input/Output 1
6	3	IO0_2	I/O	Port 0 Input/Output 2
7	4	IO0_3	I/O	Port 0 Input/Output 3
8	5	IO0_4	I/O	Port 0 Input/Output 4
9	6	IO0_5	I/O	Port 0 Input/Output 5
10	7	IO0_6	I/O	Port 0 Input/Output 6
11	8	IO0_7	I/O	Port 0 Input/Output 7
12	9	GND	G	Ground
13	10	IO1_0	I/O	Port 1 Input/Output 0
14	11	IO1_1	I/O	Port 1 Input/Output 1
15	12	IO1_2	I/O	Port 1 Input/Output 2
16	13	IO1_3	I/O	Port 1 Input/Output 3
17	14	IO1_4	I/O	Port 1 Input/Output 4
18	15	IO1_5	I/O	Port 1 Input/Output 5
19	16	IO1_6	I/O	Port 1 Input/Output 6
20	17	IO1_7	I/O	Port 1 Input/Output 7
21	18	A0	I	Address Input 0
22	19	SCL	I	Serial Clock Line Input
23	20	SDA	I	Serial Data Line Open-Drain
24	21	VCC	P	Supply Voltage

* I = Input; O = Output; P = Power; G = Ground

©Diodes Incorporated

Maximum Ratings

Power Supply	-0.5V to +6.0V
Voltage on an I/O pin	GND-0.5V to +6.0V
Input Current	±20mA
Output Current on an I/O pin	±50mA
Supply Current	160mA
Ground Supply Current	200mA
Total Power Dissipation	200mW
Operation Temperature	-40°C ~ 85°C
Storage Temperature	-65°C ~ 150°C
Maximum Junction temperature ,T j(max)	125°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Static Characteristics

VCC = 2.3V to 5.5V; GND = 0V; Tamb= -40°C to +85°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
VCC	Supply Voltage	—	2.3	—	5.5	V
I_{CC}	Supply Current	Operating mode; VCC = 5.5V; no load; fSCL = 100kHz	—	135	200	µA
I_{stb}	Standby Current	Standby mode; VCC = 5.5V; no load; VI = GND; fSCL = 0kHz; I/O = inputs	—	1.1	1.5	mA
		Standby mode; VCC = 5.5V; no load; VI = VCC; fSCL = 0kHz; I/O = inputs	—	0.25	1	µA
V_{POR}	Power-On Reset Voltage(1)	—	—	1.16	1.41	V
Input SCL, Input/Output SDA						
V_{IL}	Low Level Input Voltage	—	-0.5	—	+0.3VCC	V
V_{IH}	High Level Input Voltage	—	0.7VCC	—	5.5	V
I_{OL}	Low Level Output Current	V_{OL}=0.4V	3	—	—	mA
I_L	Leakage Current	V_I = VCC = GND	-1	—	1	µA
C_i	Input Capacitance	V_I = GND	—	6	10	pF

©Diodes Incorporated

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I/Os						
V_{IL}	Low Level Input Voltage	—	-0.5	—	+0.81	V
V_{IH}	High Level Input Voltage	—	+1.8	—	5.5	V
I_{OL}	Low Level Output Current	VCC = 2.3V to 5.5V; V_{OL} = 0.5V(2)	8	20	—	mA
		VCC = 2.3V to 5.5V; V_{OL} = 0.7V(2)	10	24	—	mA
V_{OH}	High Level Output Voltage	I_{OH} = -8mA; VCC = 2.3V[3]	1.8	—	—	V
		I_{OH} = -10mA; VCC = 2.3V[3]	1.7	—	—	V
		I_{OH} = -8mA; VCC = 3.0V[3]	2.6	—	—	V
		I_{OH} = -10mA; VCC = 3.0V[3]	2.5	—	—	V
		I_{OH} = -8mA; VCC = 4.75V[3]	4.1	—	—	V
		I_{OH} = -10mA; VCC = 4.75V[3]	4.0	—	—	V
I_{LIH}	High Level Input Leakage Current	VCC = 5.5V; V_I = VCC	—	—	1	µA
I_{LIL}	Low Level Input Leakage Current	VCC = 5.5V; V_I = GND	—	—	-100	µA
C_i	Input Capacitance	—	—	3.7	10	pF
C_o	Output Capacitance	—	—	3.7	10	pF
Interrupt $\overline{INT}$						
I_{OL}	Low Level Output Current	V_{OL} = 0.4V	3	—	—	mA
Select Inputs A0, A1, A2						
V_{IL}	Low Level Input Voltage	—	-0.5	—	+0.81	V
V_{IH}	High Level Input Voltage	—	+1.8	—	5.5	V
I_L	Input Leakage Current	—	-1	—	1	µA

Note: 1. VCC must be lowered to 0.2V for at least 20µs in order to reset part.
2. Each I/O must be externally limited to a maximum of 25mA and each octal (IO0_0 to IO0_7 and IO1_0 to IO1_7) must be limited to a maximum current of 100mA for a device total of 200mA.
3. The total current sourced by all I/Os must be limited to 160mA.

©Diodes Incorporated

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Standard Mode I^2C		Fast Mode I^2C		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	—	0	100	0	400	kHz
t_{BUF}	Bus Free Time between a STOP and START Condition	—	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold Time (Repeated) START Condition	—	4.0	—	0.6	—	µs
$t_{SU;STA}$	Set-Up Time for a Repeated START Condition	—	4.7	—	0.6	—	µs
$t_{SU;STO}$	Set-Up Time for STOP Condition	—	4.0	—	0.6	—	µs
$t_{VD;ACK}$(1)	Data Valid Acknowledge Time	—	—	3.45	—	0.9	µs
$t_{HD;DAT}$(2)	Data Hold Time	—	0	—	0	—	ns
$t_{VD;DAT}$	Data Valid Time	—	—	3.45		0.9	µs
$t_{SU;DAT}$	Data Set-Up Time	—	250	—	100	—	ns
t_{LOW}	LOW Period of the SCL Clock	—	4.7	—	1.3	—	µs
t_{HIGH}	HIGH Period of the SCL Clock	—	4.0	—	0.6	—	µs
t_f	Fall Time of both SDA and SCL Signals	—	—	300	—	300	ns
t_r	Rise Time of both SDA and SCL Signals	—	—	1000	—	300	ns
t_{SP}	Pulse Width of Spikes that must be Suppressed by the Input Filter	—	—	50	—	50	ns
Port Timing							
$t_{v(Q)}$	Data Output Valid Time(3)	—	—	200	—	200	ns
$t_{su(D)}$	Data Input Set-Up Time	—	150	—	150	—	ns
$T_{h(D)}$	Data Input Hold Time	—	1	—	1	—	µs
Interrupt Timing							
$t_{v(INT)}$	Valid Time on pin $\overline{INT}$	—	—	4	—	4	µs
$T_{rst(INT)}$	Reset Time on pin $\overline{INT}$	—	—	4	—	4	µs

Note: 1. $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.
2. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
3. $t_{v(Q)}$measured from 0.7VCC on SCL to 50% I/O output.

©Diodes Incorporated

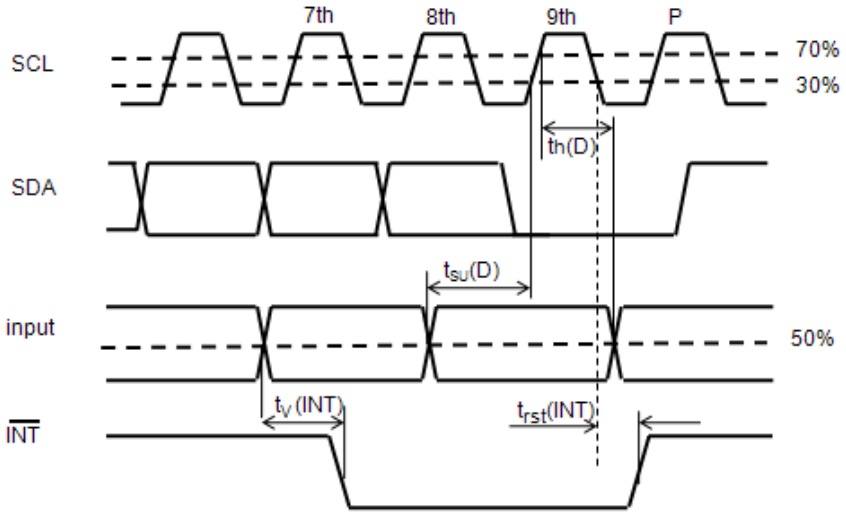
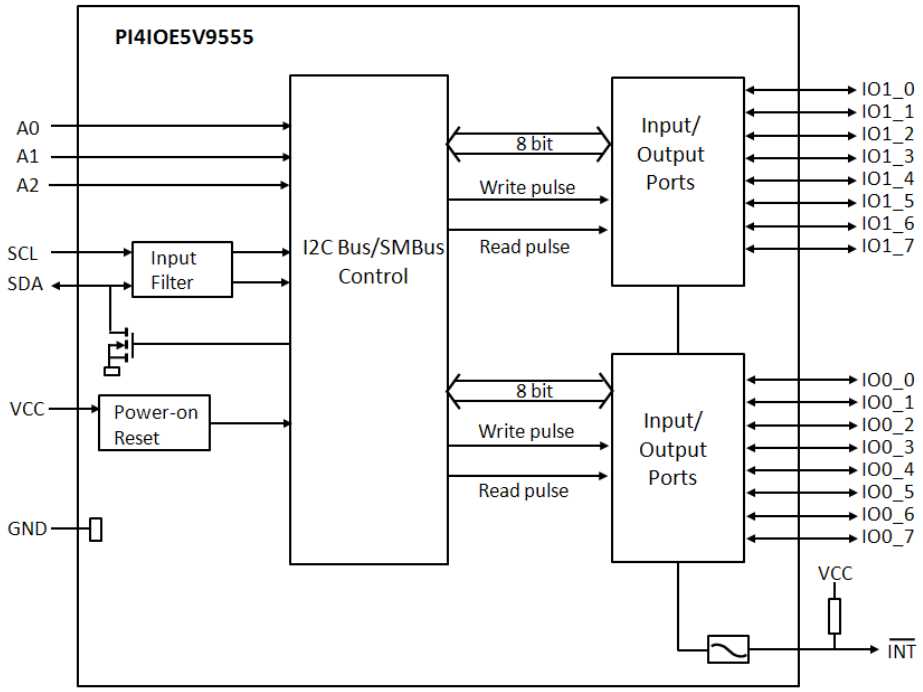


Figure 3. Timing Parameters for INT Signal

PI4IOE5V9555 Block Diagram

Figure 4. Block Diagram



Note: All I/Os are set to inputs at reset.

©Diodes Incorporated

Details Description

a. Device Address

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Address Byte	0	1	0	0	A2	A1	A0	R/W

Note: Read "1", Write "0"

b. Registers

i. Command Byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 1. Command Byte

Command	Register
0	Input Port 0
1	Input Port 1
2	Output Port 0
3	Output Port 1
4	Polarity Inversion Port 0
5	Polarity Inversion Port 1
6	Configuration Port 0
7	Configuration Port 1

ii. Register 0 and 1: Input Port Registers

This register is a read-only port. It reflects the incoming logic levels of the pins regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect. The default value 'X' is determined by the externally applied logic level.

Table 2. Input Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 3. Input Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

iii. Register 2 and 3:Output Port Registers

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by registers 6 and 7. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection—**not** the actual pin value.

Table 4. Output Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

©Diodes Incorporated

Table 5. Output Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

iv. Register 4 and 5: Polarity Inversion Registers

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the input port data polarity is retained.

Table 6. Polarity Inversion Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 7. Polarity Inversion Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

v. Register 6 and 7: Configuration Registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. Note that there is a high value resistor tied to VCC at each pin. At reset, the IOs are configured as inputs with a pull-up to VCC.

Table 7. Configuration Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 8. Configuration Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

c. Power-on Reset

When power is applied to VCC, an internal power-on reset holds the PI4IOE5V9555 in a reset condition until VCC has reached VPOR. At that point, the reset condition releases, the PI4IOE5V9555 registers, and the SMBus state machine initializes to default states. The power-on reset typically completes the reset and enables the part by the time the power supply is above VPOR. However, when it is required to reset the part by lowering the power supply, it is necessary to lower it below 0.2 V.

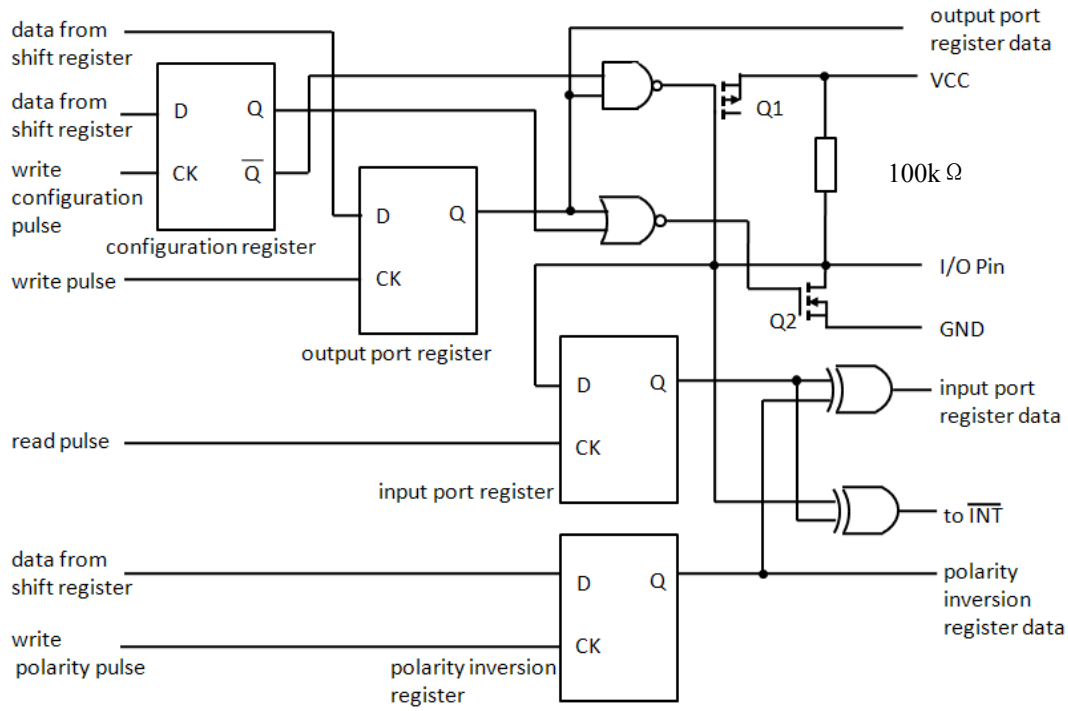
©Diodes Incorporated

d. I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pullup to VCC. The input voltage can be raised above VCC to a maximum of 5.5V.

If the I/O is configured as an output, either Q1 or Q2 is on depending on the state of the output port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either VCC or GND.

Figure 5. Simplified Schematic of I/Os



After power-on reset, all registers return to default values.

e. Bus Transaction

i. Writing to the Port Registers

Data transmits to the PI4IOE5V9555 by sending the device address and setting the least significant bit to a logic 0. The command byte sends after the address and determines which register receives the data following the command byte.

The eight registers within the PI4IOE5V9555 are configured to operate as four register pairs. The four pairs are input ports, output ports, polarity inversion ports, and configuration ports. After sending data to one register, the next data byte is sent to the other register in the pair. For example, if the first byte is sent to Output Port 1 (register 3), the next byte is stored in Output Port 0 (register 2). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register can be updated independently of the other registers.

©Diodes Incorporated

Figure 6. Write to Output Registers

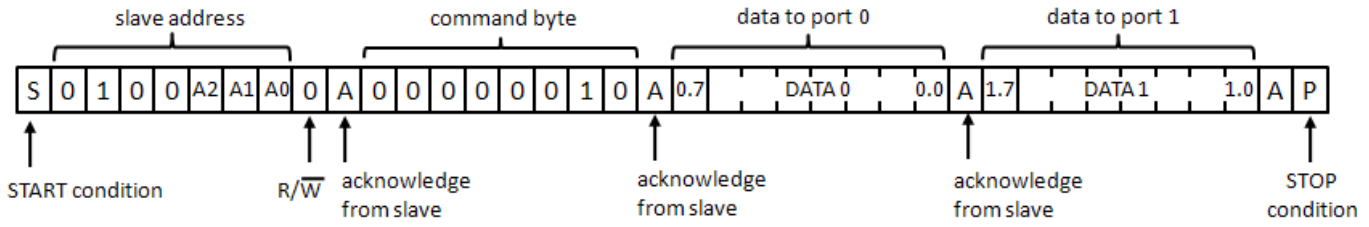
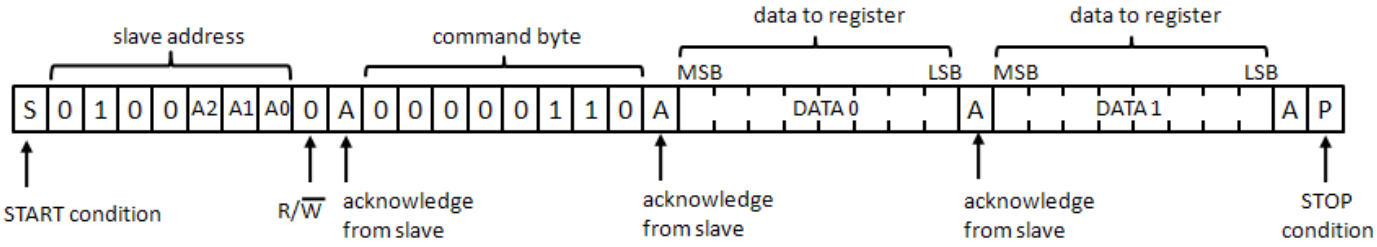


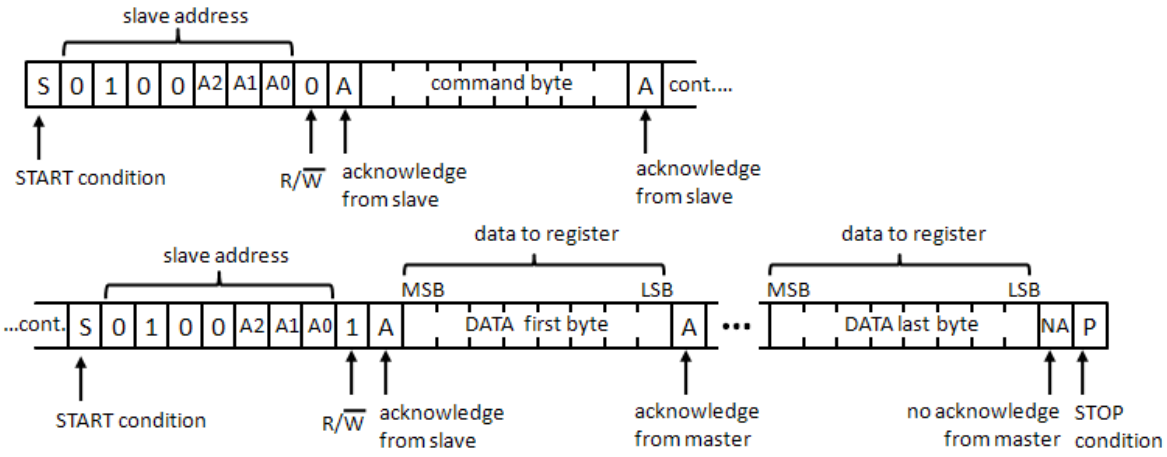
Figure 7. Write to Configuration Registers



ii. Reading the Port Registers

In order to read data from the PI4IOE5V9555, the bus master must first send the PI4IOE5V9555 address with the least significant bit set to a logic 0. The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the PI4IOE5V9555. Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission but the final byte received; the bus master must not acknowledge the data.

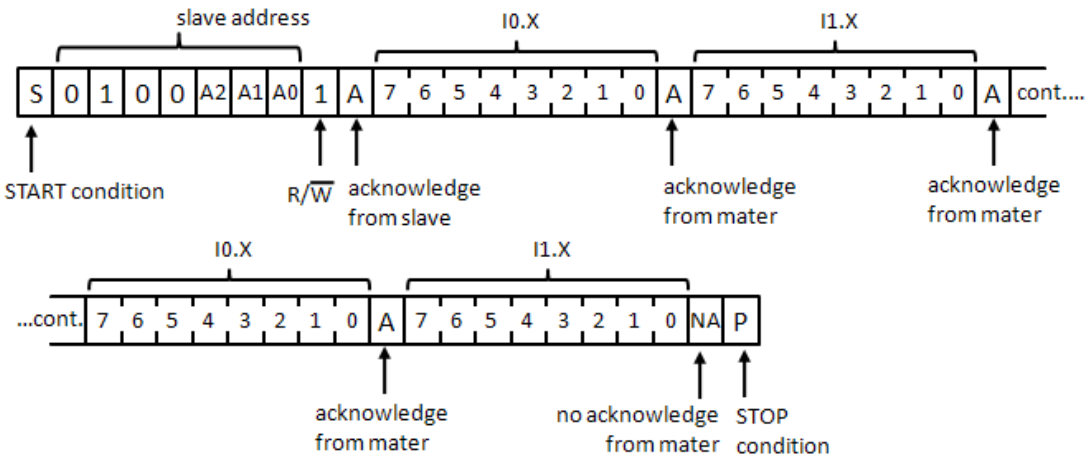
Figure 8. Read from Registers



Note: Transfer can be stopped at any time by a STOP condition.

©Diodes Incorporated

Figure 9. Read Input Port Register



Note: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

iii. Interrupt Output

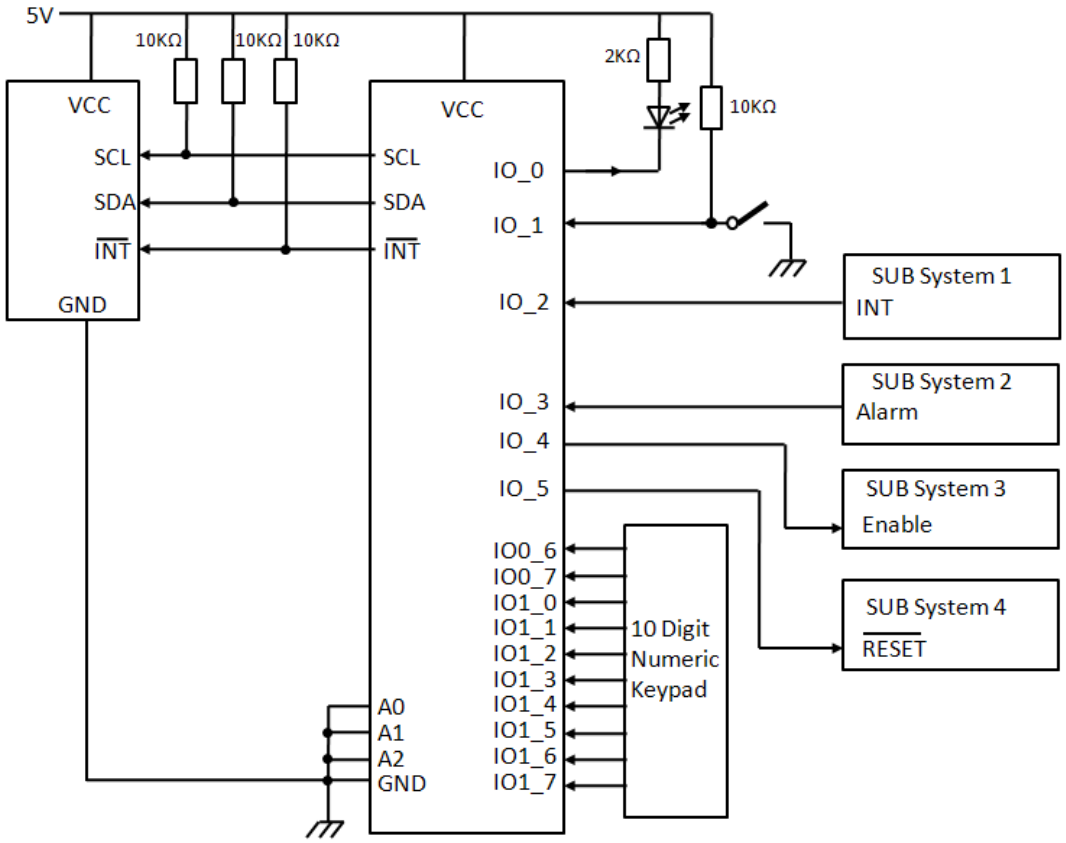
The open-drain interrupt output is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read. A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

Note: Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

©Diodes Incorporated

Application Design-in Information

Figure 10. Typical Application



Device address configured as 0100 000xb for this example.
IO0_0, IO0_4, IO0_5 configured as outputs.
IO0_1, IO0_2, IO0_3 configured as inputs.
IO0_6, IO0_7, and IO1_0 to IO1_7 configured as inputs.

Part Marking

L Package

PI4IOE
5V9555LE
ZYYWWXX̄
○

Z: Die Rev
YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above 2nd "X" means Cu wire

ZD Package

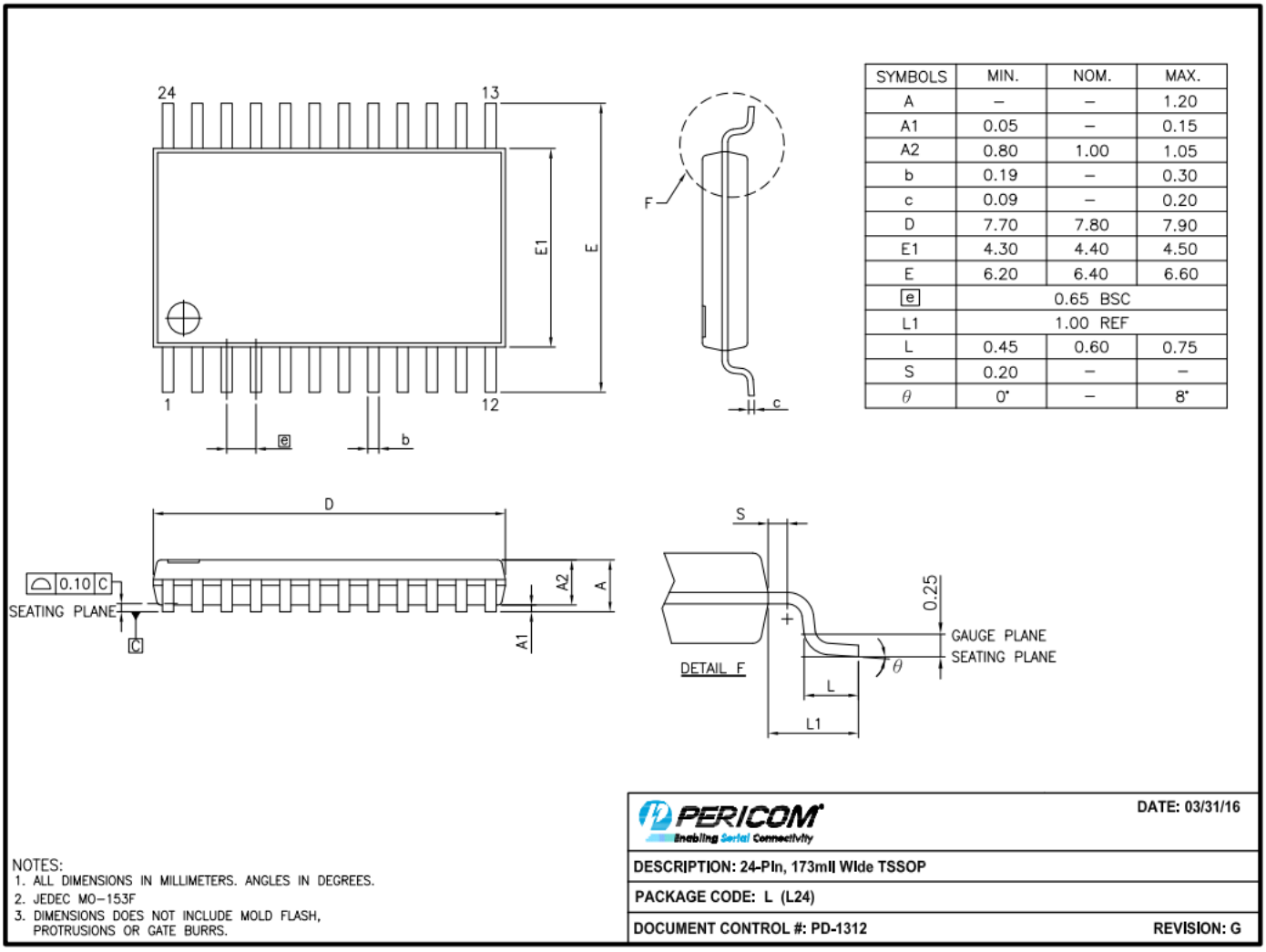
PI4IOE5V
9555ZDE_
ZYYWWXX̄
○

Z: Die Rev
YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above fab code means Cu wire

©Diodes Incorporated

Packaging Mechanical

TSSOP-24(L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e		0.65 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

DATE: 03/31/16

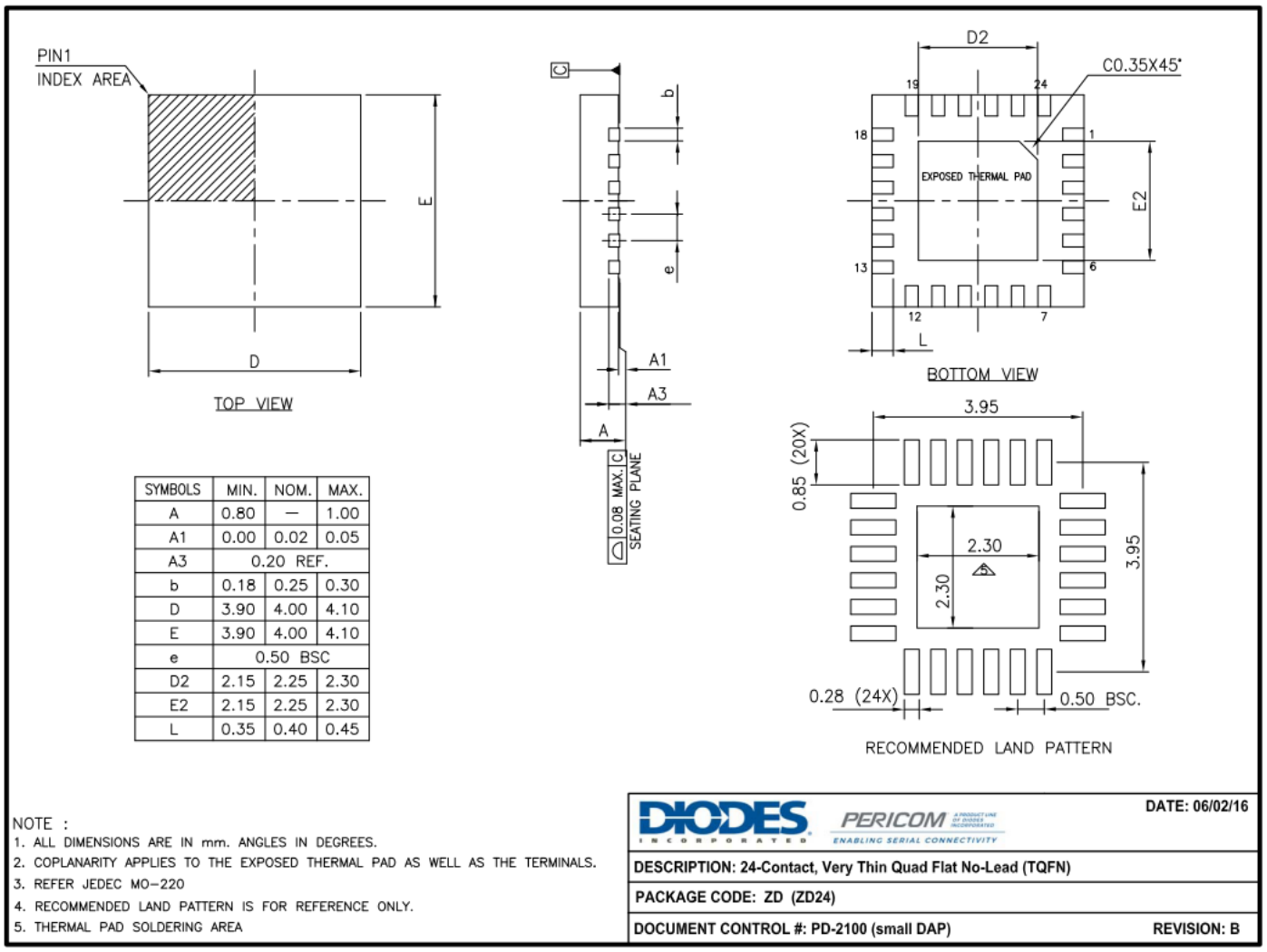
DESCRIPTION: 24-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L24)

DOCUMENT CONTROL #: PD-1312 REVISION: G

©Diodes Incorporated

TQFN-24 (ZD)



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	—	1.00
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.18	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.50 BSC		
D2	2.15	2.25	2.30
E2	2.15	2.25	2.30
L	0.35	0.40	0.45

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA

DATE: 06/02/16
DESCRIPTION: 24-Contact, Very Thin Quad Flat No-Lead (TQFN)
PACKAGE CODE: ZD (ZD24)
DOCUMENT CONTROL #: PD-2100 (small DAP) REVISION: B

For latest package information:
See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Part Numbers	Package Code	Package Description
PI4IOE5V9555LEX	L	24-pin,173mil Wide (TSSOP)
PI4IOE5V9555ZDEX	ZD	24-contact, Very Thin Quad Flat No-Lead (TQFN)
PI4IOE5V9555ZDEX-13R	ZD	24-contact, Very Thin Quad Flat No-Lead (TQFN), Reel pack, 13”

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

©Diodes Incorporated

IMPORTANT NOTICE

1. DIODES INCORPORATED AND ITS SUBSIDIARIES ("DIODES") MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes products. Diodes products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of the Diodes products for their intended applications, (c) ensuring their applications, which incorporate Diodes products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.

5. Diodes products are provided subject to Diodes' Standard Terms and Conditions of Sale (https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

Copyright © 2021 Diodes Incorporated

www.diodes.com