Analysis of LDO oscillation issues

Introduction

Using low noise and stable power supplies is a trend for power application. And LDO is one of the simplest applications. Yet LDO oscillation results in voltage instability. The analysis below tells you how to prevent LDO from oscillation.

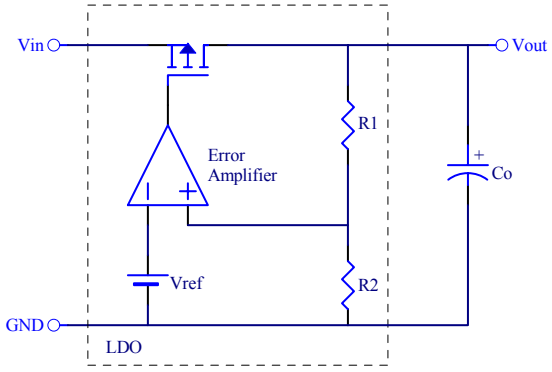


Fig 1.a: LDO basic structure

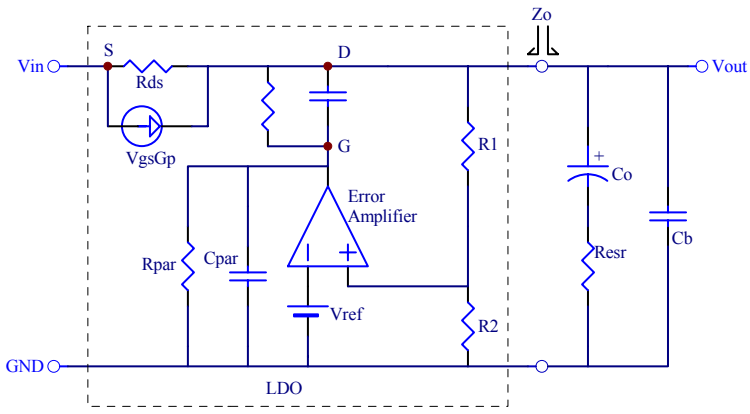


Fig 1.b: LDO ac effective circuit

The LDO in fig. 1.a is composed of four parts - pass element, error amplifier, reference voltage, and feedback resistor. The series pass element, PMOS transistor, is formed into a small signal model. The parasitic parameters, R_{par} and C_{par}, are signified by the output impedance of the error amplifier and the input impedance of PMOS. An ac prototype of LDO

is shown as fig. 1b, which is a combination of an output capacitor Co with R_{ESR} and bypass capacitor Cb.

Why does an LDO regulator oscillate?

The output voltage of LDO regulator varies not only in relation to loading current but also the value of equivalent series resistance (ESR) for external output capacitor.

The variation of LDO output voltage is given by

$$\Delta V_o = \Delta V_{ESR} + \frac{I_O}{C_o}\Delta t \quad \ldots(1)$$

where ΔV_o is the oscillation value of output voltage

Δt is the response time of regulator when a loading adding.

ΔV_{ESR} is the voltage downfall value when ESR applied.

From above equation1, we find that I_O and Δt are proportional to ΔV_o. The increase of C_o improves oscillation. In the following texts, we will explore the stable range of ESR for LDO. [1]

Pole and Zero Analysis

The output impedance Zo in the above ac prototype is given by

$$Zo = \left[R_{ds} \| (R_1 + R_2)\right] \left\| \frac{1}{SCb} \right\| \left(R_{ESR} + \frac{1}{SCo} \right) \ldots(2)$$

And $R_{ds} \| (R_1 + R_2) \approx R_{ds}$, Co >> Cb, R_{ds} >> R_{ESR},

Therefore, Zo can approximate to

$$Z_O \approx R_{ds} \left\| \frac{1}{SCb} \right\| \left(R_{ESR} + \frac{1}{SC_O} \right) = \frac{R_{ds}}{SC_bR_{ds}+1} \left\| \left(R_{ESR} + \frac{1}{SC_O} \right) \right.$$

$$= \frac{\dfrac{R_{ds}\left(R_{ESR} + \dfrac{1}{SC_O} \right)}{SC_bR_{ds}+1}}{\dfrac{R_{ds}}{SC_bR_{ds}+1} + R_{ESR} + \dfrac{1}{SC_O}} = \frac{R_{ds}\left(R_{ESR} + \dfrac{1}{SC_O} \right)}{R_{ds} + (SC_bR_{ds}+1)R_{ESR} + (SC_bR_{ds}+1)\dfrac{1}{SC_O}}$$

$$= \frac{SC_O R_{ds} R_{ESR} + R_{ds}}{SC_O R_{ds} + S^2 C_O C_b R_{ds} R_{ESR} + SC_O R_{ESR} + SC_b R_{ds} + 1}$$

$$\approx \frac{R_{ds}\left(SC_O R_{ESR} + 1\right)}{\left(SC_O R_{ds} + 1\right)\left(SC_b R_{ESR} + 1\right)} \quad \ldots(3)$$

Based on the equation3 above, zero (Z_{ESR}) and poles (Po, Pa, and Pb) can be found as follows.

$$Z_{ESR} = \frac{1}{2\pi R_{ESR} C_O}$$

The first pole is

$$P_O = \frac{1}{2\pi C_O R_{ds}}$$

The second pole depends on the input impedance of the PMOS, R_{par} and Cpar,

$$P_a = \frac{1}{2\pi R_{par} C_{par}}$$

The third pole is

$$P_b = \frac{1}{2\pi R_{ESR} C_b}$$

[2]

Gain-Phase Analysis

Figure2 shows the frequency response of LDO. The solid line and broken line represent the frequency response of LDO with and without external compensation, respectively. Po occurs when a relatively low frequency with low load current applied, thus phase margin reduces. The loop turns unstable when LDO has two poles, resulting from no compensation applied. And phase shift of -180° at UGF(Unity Gain Frequency), as the broken line in fig. 2, causes the linear regulator instability. To maintain a stable regulator, Z_{ESR} must be added so that the

phase margin can go over 0°, as the solid line in figure 2. It is obvious that an LDO requires an output capacitor to stabilize its control loop. Zo, which is produced by ESR of an output capacitor, must be located before UGF so that the phase margin may maintain over 0°. Therefore, the LDO becomes stable. The phase margin at UGF of the control loop should always go over 0° to make sure the stability of the system.

Sufficient phase margin is the necessary condition for the stability of the control loop. However, the ESR should be maintained within a proper range to increase the phase shift of the frequency response. Each LDO has its min/max ESR. When ESR is out of the proper range, the control loop system, even with Zo, could be unstable. And ESR is a major contributing factor of Z_{ESR} and pole P_b. Shift of Z_{ESR} and P_b, only caused by the change of ESR, affects the loop stability. The phase margin at UGF is less than or equal to 0° when ESR is too high or too low respectively. If Z_{ESR} turns too low, UGF increases and makes the phase margin insufficient. With an extremely high Z_{ESR}, gain will be degraded to 0dB after frequency reaches to Zo, and phase shift turns -180°. And that results in system instability.

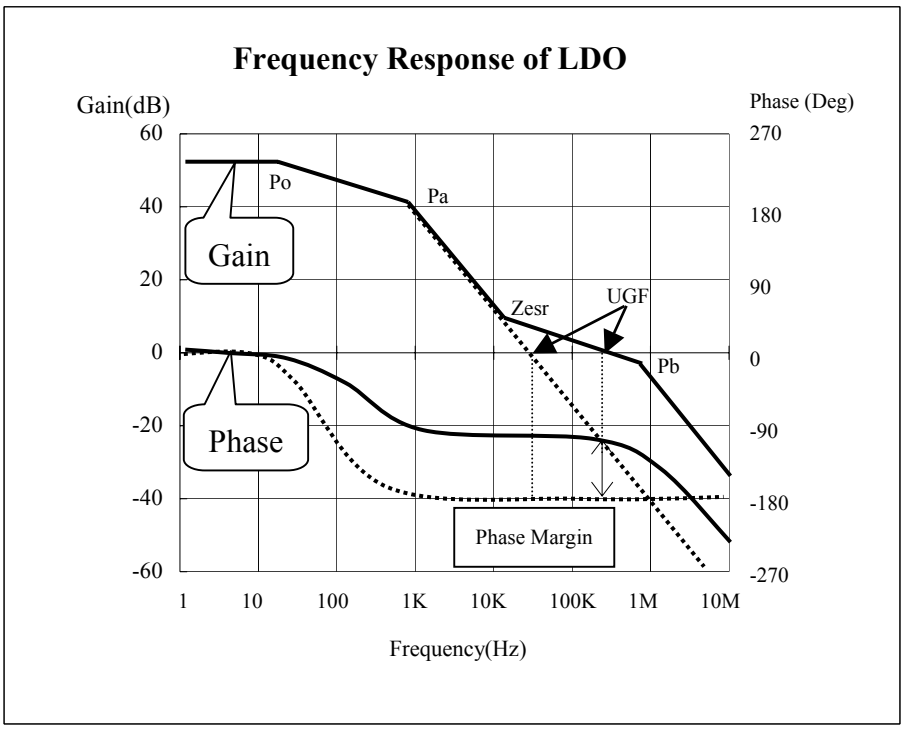
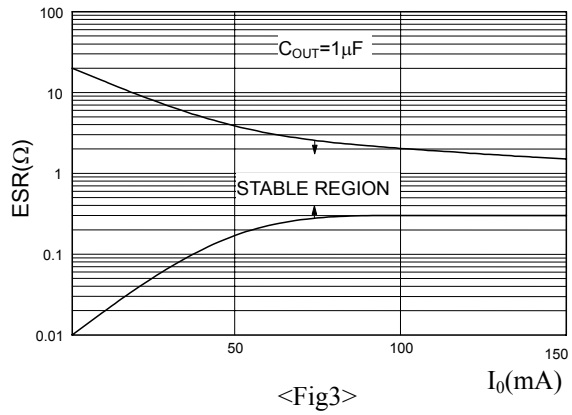


Fig2: Frequency response of LDO

Effect of ESR of capacitor on LDO

Linear regulators require input and output capacitors to maintain stability. LDO does not create ripple noise by itself, unless the input polarity is influenced by external ripple noise. The output capacitor should be selected within the ESR range (shown as figure3 and 4). Without an output capacitor (high ESR), LDO will oscillate as temperature increasing.

Solid tantalum electrolytic, aluminum electrolytic, and multiplayer ceramic capacitors are all suitable, provided they meet the ESR requirements. But capacitors of aluminum and tantalum electrolytic are recommended. Because the ceramic capacitor's ESR is lower and its electrical characteristics vary widely over temperature.



<Fig3>

Fig3: Output Capacitor = 1μF

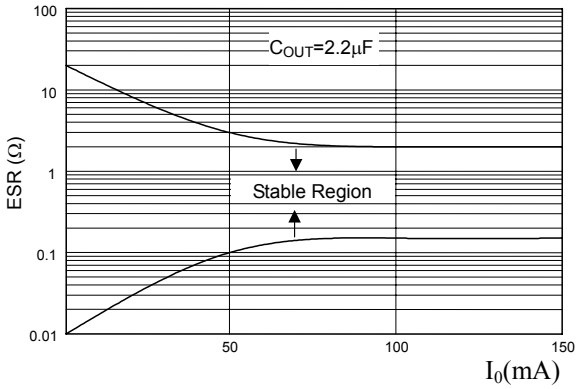


Fig4: Output Capacitor = 2.2μF

In figure5 and 6, AIC1730-33 is applied with 150mA load current. Figure5 shows unusual oscillation with a 1uF ceramic output capacitor (ESR=100mΩ), and output voltage is normal with a 1uF electric capacitor (ESR=500mΩ) which is shown as figure6.

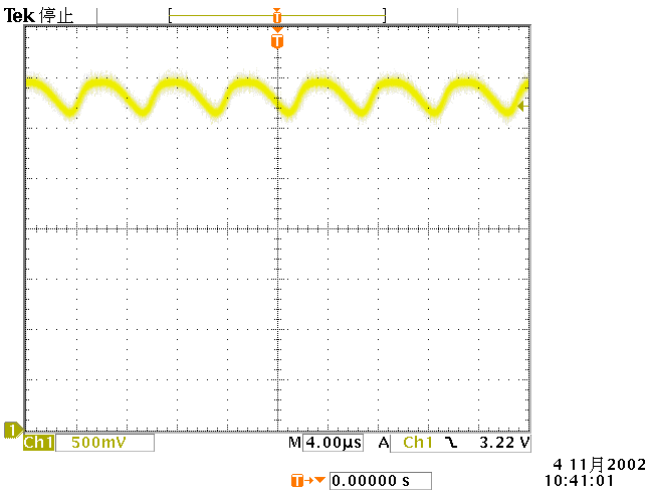


Fig5: AIC1730 abnormal oscillation

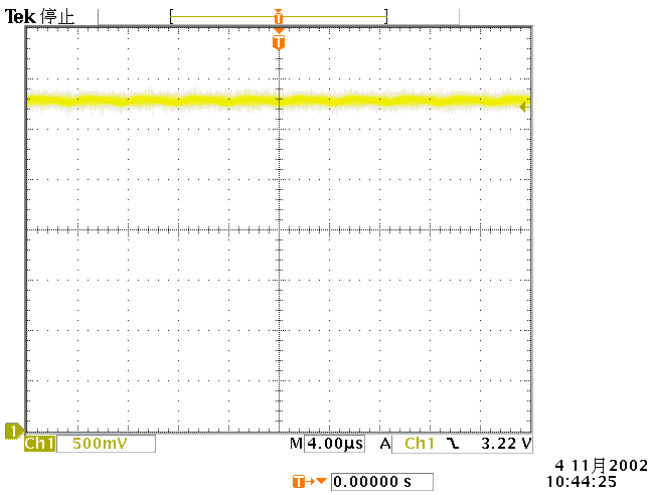


Fig6: AIC1730 normal output voltage

The main concern for LDO oscillation is ESR of output capacitor. It has better transient response with smaller ESR capacitor, but there might not be any effect on compensation. Therefore, choosing a proper ESR to avoid LDO oscillation is an important consideration.

References

[1] Y.S. Hsu and G.C. Wu, "Linear regulator design", July 2001

[2] B.S. Lee, "Understanding the stable range of equivalent series resistor of an LDO regulator", Application Note, Texas Instruments, November 1999

[3] Hawk Chen, "A better approach of dealing with ripple noise of LDO", Application Note, Analog Integrations Corporation