CLA60000 SERIES

CHANNELLESS CMOS GATE ARRAYS

(Supersedes December 1988 Edition)

This advanced family of gate arrays uses many innovative techniques to achieve 110K gates per chip - system clock speeds in excess of 70MHz are achievable. The combination of high speed, high gate complexity and low power operation places Plessey at the forefront of ASIC technology.

GENERAL DESCRIPTION

The CLA60000 gate array family is Plessey's fifth-generation CMOS gate array product. These arrays allow even higher integration densities at enhanced system clock rates as needed for many of today's system applications.

The largest gate array at 110K gates offers a tenfold increase in raw gates than channelled gate arrays. In addition, many new design features have been incorporated such as JTAG/ BIST compliance, analog functionality, slew rate output control, and intermediate I/O buffering for fast data transfer through peripheral cells.

Also, the low-power characteristics of Plessey CMOS processing have been incorporated in these arrays, easing the thermal management problems associated with complex designs of 20,000 gates and above.

FEATURES

- Channelless arrays to 110,000 gates
- 1.4 micron dual layer metal silicon gate CMOS process
- Typical Gate Delays of 700ps (NAND2).
- Comprehensive cell library of microcells, macrocells, and paracells - including DSP functions and JTAG/BIST library.
- Power distribution optimised for maximum noise immunity
- Slew controlled outputs with up to 24mA drivers
- Very high latch-up immunity
- Fully supported by design software (PDS2) and popular workstations

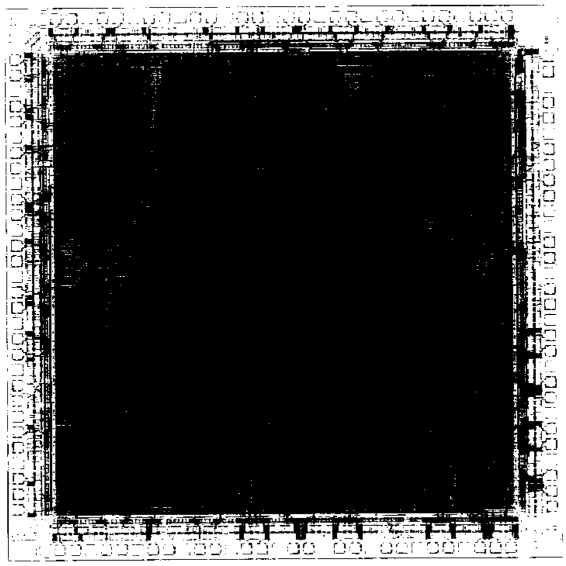

Figure 1: CLA60000 Chip

All CLA60000 arrays have the same architecture. A core of uncommitted transistors is placed for optimum logic connection and surrounded by uncommitted peripheral I/O circuitry. The channelless array architecture is an important feature - the absence of discrete wiring channels increases flexibility and reduces track capacitance, allowing larger transistor sizes for faster logic switching.

The CLA60000 gate array design library has been developed to support basic logic functions, macro functions, and core memory functions (RAM and ROM) with high connectivity. Dual level metallisation for interconnection of cells helps to give compact logic structures and allows a high degree of freedom for the autolayout software.

The overall architecture of these gate arrays exploits many new and emerging developments in CAD tools. Increasing demands are now being made for design tools which are faster, easier to use, and more accurate. The Plessey Design System (PDS2) allows full control over all aspects of design including logic capture, simulation and chip layout.

PRODUCT RANGE

The CLA60000 product range is shown below. Actual gate utilisation can be typically 40-70% of the uncommitted gate count depending on circuit structure.

DEVICE	GATES	PADS (Including Power)
CLA61XXX	2040	40
CLA62XXX	5488	64
CLA63XXX	10608	88
CLA64XXX	19928	120
CLA65XXX	35784	160
CLA66XXX	55616	200
CLA67XXX	80560	240
CLA68XXX	110112	280

CORE CELL ARRANGEMENT

A four transistor group (2 NMOS and 2 PMOS) forms the basic cell of the core array. This array element is repeated in a regular fashion over the complete core area to give a 'Full Field' (sea-of-gates) array. The unique design of the basic four transistor cell gives the Plessey arrays a major advantage over other gate arrays. The silicon layout has been configured so that the basic logic cells, flip-flops and large hierarchical cells can be interconnected easily with through-cell routing channels. It also ensures that an optimum overall data flow and control signal distribution scheme is possible.

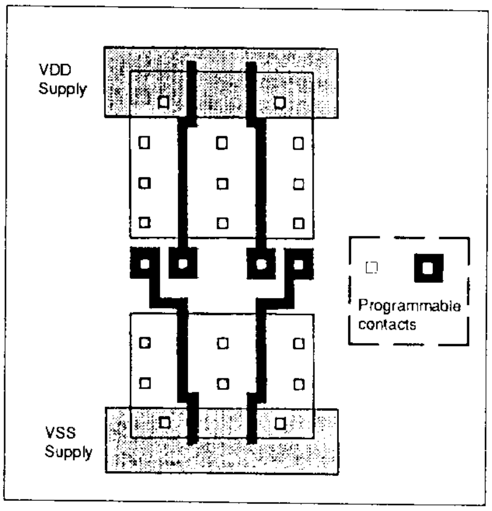

Figure 2: Diagrammatic representation of Array Core Cell

Complete rows of array elements can be used as routing channels to conform to the earlier channelled Plessey arrays or, if desired, compact hierarchical logic blocks and localised routing areas can be defined like a cell based design layout. The array structure has been designed to be totally flexible in architecture with the distribution of logic blocks and routing channels being defined by the designer.

I/O BUFFER ARRANGEMENT

The I/O buffers are the interface to external circuitry and are therefore required to be robust and flexible. The inputs and outputs can withstand electro-static discharges, are not easily susceptible to latch-up (an inherent CMOS problem) and provide the designer with multiple interface options.

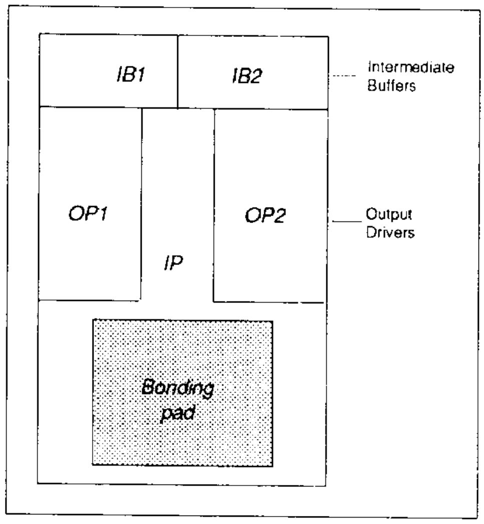

Figure 3: I/O Block

The CLA60000 I/O buffers contain all the components for static protection, input pull-up and pull down resistors, various output drive currents and input interface signals such as CMOS and TTL. In addition, the I/O buffer contains all the components for intermediate buffering stages including Schmitt triggers, TTL threshold detectors, tristate control, signal re-timing flip-flops and slew rate control for the output drivers. Some analog interface cells can also be implemented using the available components. I/O buffer locations can also be configured as supply pads (VDD and VSS).

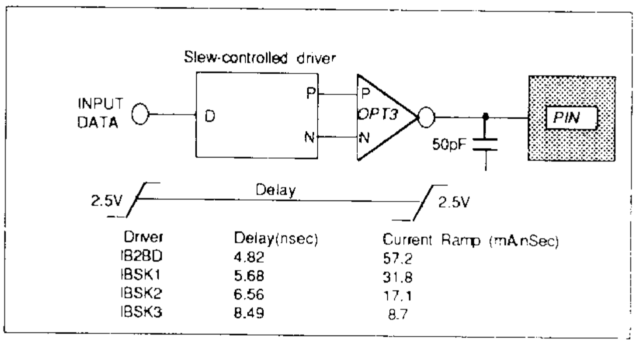

Figure 4: Slew Control

Slew control of output drivers is a useful benefit where outputs are driving large capacitive loads such as busses. Noise transients caused by voltage coupling into peripheral power supplies can give switching problems, resulting in mis-operation. The extent of this voltage disruption is dependent on the number of outputs switching, supply pad locations and the inductance of the chip bond wires/package leads. The CLA60000 family uses proprietary design techniques to reduce this phenomenon by offering output switching control (di/dt) as part of the intermediate buffers.

POWER SUPPLY DISTRIBUTION

The power distribution scheme for the CLA60000 arrays is very flexible (shown in figure 5): three separate power rings are used, one for the internal core logic, one for the large output driver cells and one for the intermediate buffer regions. Each of the separate power rings isolate any noise generated by the low-impedance output drivers from the core logic and intermediate buffers. The power rings can be connected to separate pad locations or combined at a single Input or Ouput pad location. In addition, it is possible to isolate sections of the peripheral supply ring for the implementation of basic analog circuits.

The distribution of the supply rails across the core of the array can be automatically positioned for the interconnect of the base cells and hierarchical blocks. This allows greater design flexibility and provides additional signal routing channels. Supply interconnection is added during autolayout leaving unpopulated areas available for signal routing.

Low core power dissipation is very important for high complexity circuits (see section on Thermal Management).

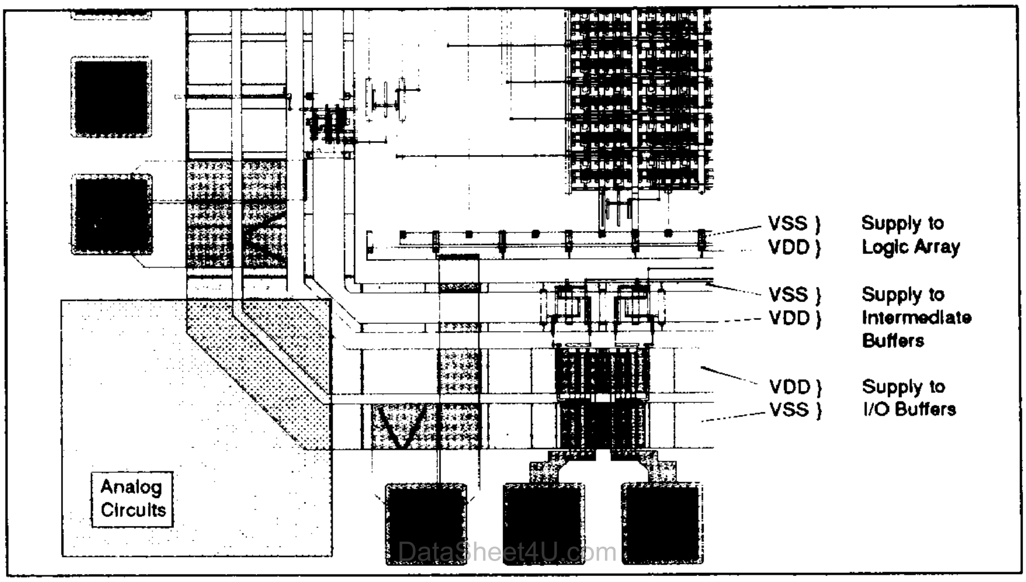

Figure 5 Power Supply Organisation

PDS2 - THE PLESSEY ASIC DESIGN SYSTEM

PDS2 is Plessey's ASIC computer-aided design system. It provides a fully-integrated, technology independent VLSI design system for all Plessey SemiCustom CMOS and ECL products.

PDS2 allows the designer to perform all design activities from schematic entry, circuit debugging, fault grading, through to chip layout and generation of a test program for the production test of the finished ICs.

Logical design of CLA60000 is realised with the same software as is used for the CLA5000 and MVA5000 families of CMOS semicustom products. PDS2 runs on DEC VAX equipment (under VMS)* and comprises schematic entry, logic and fault simulation, extensive result examination facilities and advanced library and configuration management tools. Layout and routing is also supported on PDS2 along with full back annotation. Hierarchical logical design is possible up to 20 levels.

Supplemented by a three day training course for first-time users, PDS2 may be used either at a Plessey Design Centre or under licence at the designer's premises.

DESIGN SUPPORT AND INTERFACES

Plessey Semiconductors offers a variety of design interfaces to customers. For each interface, Plessey requires a given set of information to be forwarded by the designer which is assessed at Design Reviews (1 to 4). At each stage, the design must be deemed to be acceptable by Plessey Project Engineers before commencing the next stage of work. Design Reviews may be held in the designer's premises or at a Plessey Design Centre.

Further information on PDS2 or the interfacing requirements to the Plessey technologies is available from any Plessey Sales Office or Design Centre.

* *DEC, VAX and VMS are trademarks of Digital Equipment Corporation, USA*

DESIGN INTERFACES

	PDS2 USED AT PLESSEY DESIGN CENTRE		PDS2 USED BY CUSTOMER ON OWN PREMISES			PLESSEY COMPLETES DESIGN	
						TURNKEY	WORKSTATION
OPTIONS	**A**	**B**	**C**	**D**	**E**	**F**	**G**
DESIGN REVIEW 1							
LOGICAL DESIGN	CUSTOMER	CUSTOMER	CUSTOMER	CUSTOMER	CUSTOMER	PLESSEY	CUSTOMER
DESIGN REVIEW 2							
PHYSICAL DESIGN	PLESSEY	CUSTOMER	PLESSEY	CUSTOMER	CUSTOMER (AT DESIGN CENTRE)	PLESSEY	PLESSEY
DESIGN REVIEW 3							
PROTOTYPE MANUFACTURING	PLESSEY						
PROTOTYPE EVALUATION	CUSTOMER						
DESIGN REVIEW 4							
PRODUCTION	PLESSEY						

Figure 6: Access Routes to Plessey Semicustom

Plessey operates a design audit procedure with four formal review meetings:

REVIEW 1: Checks that the required specification can be met by the CLA60000 gate array.

LOGICAL DESIGN: Conversion of the logic into hierarchical netlist. Circuit function is simulated for the eventual environmental conditions to be met by the chip, including definition of the test pattern and fault simulation.

REVIEW 2: Checks that logic simulation results are acceptable to both parties, and finalises objectives for physical design (package, pinout, etc).

PHYSICAL DESIGN: Package and pinout are defined. Cells are placed and routed within the array - using Plessey's interactive layout package. A final simulation is performed which takes account of real track loads.

REVIEW 3: Establishes that it is appropriate to proceed with chip manufacture by comparing all PDS2 results with customer's specifications.

PROTO-TYPES: Plessey manufactures four custom masks, develops a test program from the customer's simulation vectors, fabricates wafers and supplies 10 tested, packaged prototypes as standard. Additional prototypes may be supplied at extra cost.

REVIEW 4: Confirms that the customer has fully examined the prototype and approves the chip design for full-scale production.

The schematic entry and logical design work may be done by Plessey, or the customer may licence the PDS2 tools with Plessey providing training to enable the engineer to undertake this phase of development in house. Design rooms and equipment are also available for customer use at any Plessey design centres at attractive rental rates.

For the physical design phase, customers are encouraged to work with Plessey layout engineers to ensure the best possible final performance. This can be completed either at a Plessey design centre or at the customer's premises.

DESIGN THERMAL MANAGEMENT

As gate integration capacity improves with CMOS process geometry reduction, the ability of silicon to exceed the power capabilities of accepted packaging technology is a very real problem. SemiCustom designers now have the ability to design circuits of 50,000 gates and over, and chip power consumption is (or should be) a very important concern.

With complexities approaching 100K gates, the core power at gate level becomes increasingly more dominant. It becomes essential to offer ultra low power core logic to maintain an acceptable overall chip power budget (typically 1 Watt for standard surface mount packaging).

The consequences of higher power consumption are elevated chip temperatures and reductions in product reliability. This means relatively expensive special packaging has to be considered - larger package sizes, heatsinking, and more costly assembly methods.

Plessey CLA60000 arrays offer low power factors. At 5μW per gate per MHz gate power and 2μW per gate load, power is lower than most competitive arrays, with lower operating temperatures and higher inherent long term reliability.

CLA60000 POWER DISSIPATION CALCULATION

CLA60000 series power dissipation for any array can be estimated by following this example (calculated for the CLA68XXX).

Number of available gates	110112
Percent gates used	40%
Number of used gates	44045
Number of gates switching each clock cycle (15%)	6607
Power dissipation/gate/MHz (μW) (gate fanout typically 2 loads)	9
Total core dissipation/MHz (mW)	59.5
Number of available I/O pads	280
Percent of I/O pads used as Outputs	40%
Number of I/O pads used as Outputs	112
Number of output buffers switching each clock cycle (20%)	22
Dissipation/output buffers/MHz/pF (μW)	25
Output loading in pF	50
Power/output buffer/MHz (mW)	1.25
Total output buffer dissipation/MHz (mW)	27.5
Total Power dissipation/MHz (mW)	87
Total Power at 10MHz clock rate (W)	0.87
Total Power at 25MHz clock rate (W)	2.18

1.4 MICRON CMOS PROCESS

The 1.4 micron CMOS process (Plessey process variant VJ) uses the latest manufacturing techniques at Plessey's Class 1, 6-inch fabrication facility at Plymouth, England. The process is a twin well, self aligned Oxide-isolated technology on an epitaxial substrate giving low defect density and high reliability.

Effective channel length is 1.1 micron. Usable gate packing density is 600 gates/sq.mm on two levels of metal. Devices show excellent radiation hardness, ESD, and stable performance characteristics ideal for all commercial, industrial, and military SemiCustom applications.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		MIN	MAX	UNITS
Supply	Voltage	- 0.5	7.0	V
Input	Voltage	- 0.5	Vdd+0.5	V
Output	Voltage	- 0.5	Vdd+0.5	V
Storage	Temperature:			
	Ceramic	- 65	150	Deg.C
	Plastic	- 40	125	Deg.C

Operation above these absolute maximum ratings may permanently damage device characteristics and may affect reliability.

RECOMMENDED OPERATING LIMITS

PARAMETER	MIN	MAX	UNITS
Supply Voltage	3.0	6.0	V
Input Voltage	Vss	Vdd	V
Output Voltage	Vss	Vdd	V
Current per pad		100	mA
Operating Temperature:			
Commercial Grade	0	70	Deg.C
Industrial Grade	-40	85	Deg.C
Military Grade	-55	125	Deg.C

AC CHARACTERISTICS FOR SELECTED CELLS

The CLA60000 technology library contains all the timing information for each cell in the design library. This information is accessible to the simulator, which calculates propagation delays for all signal paths in the circuit design. The PDS2 simulator can automatically derate timings according to the various factors such as:

Supply voltage variation (from nominal 5V)
Chip temperature
Processing tolerance - manufacturing spreads
Gate fanout - logic loading on gate outputs
Interconnection wiring - net loading on gate outputs

For initial assessments of feasibility, worst case estimations of path delays can be done in the following manner - using the Dynamic Characterisics table as a guide to the normal propagation delays at 25 Deg. C and 5V supply.

* For temperature, Plessey Semiconductors has derived a derating multiplier (Kt) of +0.3% per Deg. C
* For supply voltage derating, a factor of (Kv) -25% per volt of VDD change should be used.
* For manufacturing variation (Kp), the tolerance is ± 75%

The *maximum* variation on typical delays over the Commercial grade product will be at 4.5V and 70 Deg. C ambient temperature.

tpd (max) = Kp x Kv x Kt x tpd (typ)
=1.75 x (1+(5.0 - 4.5) 0.25)x (1+(70-25) 0.003) x tpd(typ)
=1.75 x 1.13 x 1.13 x tpd (typ)
=2.23 x tpd (typ)

The *minimum* delay, at 5.5V and 0 Deg. C will be:

tpd (min)
=0.57x (1-(5.5-5.0) x 0.25) x (1-(25-0)0.003) x tpd (typ)
=0.57 x 0.87 x 0.93 x tpd (typ)
=0.46 x tpd (typ)

A similar calculation may be done for any voltage and temperature relevant to the application. An additional "safety factor" of ± 20% is usually applied for conservative design. For worst case military grade characteristics, the performance derating multiplier is 2.57 times (=1.75x1.13x1.30) the commercial typical.

Fanout is in gate load units.

INTERNAL CORE CELLS

				Typical Propagation Delay (nS)	Worst case Propagation Delay (nS)			
					Commercial		Industrial	
					Fanout		Fanout	
Name	Cells	Description	Symbol	Fanout=2	2	4	2	4
INV2	1	INVERTER DUAL DRIVE	tpLH	0.64	1.43	1.65	1.50	1.73
			tpHL	0.39	0.87	1.05	0.91	1.10
NAND2	1	2 - INPUT NAND GATE	tpLH	0.82	1.83	2.28	1.92	2.38
			tpHL	0.67	1.50	1.99	1.57	2.08
NOR 2	1	2 - INPUT NOR GATE	tpLH	1.11	2.48	3.24	2.60	3.40
			tpHL	0.58	1.30	1.66	1.36	1.74
DF	4	MASTER SLAVE D - TYPE FLIP FLOP	tpLH	1.04	2.32	2.76	2.44	2.90
			tpHL	0.93	2.08	2.44	2.18	2.56
DFRS	6	MASTER SLAVE D - TYPE WITH SET AND RESET	tpLH	1.19	2.66	3.11	2.79	3.25
			tpHL	1.12	2.51	3.00	2.62	3.13

INTERMEDIATE BUFFER CELLS

				Typical Propagation Delay (nS)	Worst case Propagation Delay (nS)			
					Commercial		Industrial	
					Fanout		Fanout	
Name	Cells	Description	Symbol	Fanout=2	2	4	2	4
IBGATE	-	LARGE 2 INPUT NAND GATE + 2 INPUT NOR	tpLH	0.73	1.64	1.95	1.71	2.04
			tpHL	0.62	1.39	1.75	1.45	1.83
IBDF	-	MASTER SLAVE D-TYPE FLIP FLOP	tpLH	1.04	2.32	2.77	2.44	2.90
			tpHL	0.93	2.08	2.44	2.18	2.56
IBCMOS1	-	CMOS INPUT BUFFER WITH 2 INPUT NAND GATE	tpLH	1.11	2.48	2.88	2.60	3.02
			tpHL	0.72	1.61	1.83	1.69	1.92

OUTPUT BUFFER CELLS (CMOS)

				Typical Propagation Delay (nS)	Worst case Propagation Delay (nS)			
					Commercial		Industrial	
					Fanout		Fanout	
Name	Cells	Description	Symbol	Fanout=10pF	10pF	50pF	10pF	50pF
OP 3	-	STANDARD OUTPUT BUFFER	tpLH	1.26	2.83	9.99	2.95	10.43
			tpHL	0.92	2.06	5.65	2.16	5.90
OP 6	-	MEDIUM OUTPUT BUFFER	tpLH	0.86	1.93	5.51	2.02	5.76
			tpHL	0.70	1.57	3.36	1.64	3.51
OP 12	-	LARGE OUTPUT BUFFER	tpLH	0.70	1.57	3.36	1.64	3.51
			tpHL	0.56	1.25	2.15	1.31	2.25

Note:
Commercial Worst case is 4.5V, 70 Deg.C operating, Worst Case processing
Industrial Worst case is 4.5V, 85 Deg C operating, Worst Case processing
Military worst case is 4.5V, 125 Deg. C operating, Worst Case processing

DC ELECTRICAL CHARACTERISTICS

All characteristics at Commercial Grade voltage and temperature (Note 1)

CHARACTERISTIC	SYM	VALUE Min	Typ	Max	UNIT	CONDITIONS
LOW LEVEL INPUT VOLTAGE	VIL				V	
TTL Inputs (IBTTL1/IBTTL2)				0.8		
CMOS Inputs (IBCMOS1/IBCMOS2)				1.0		
HIGH LEVEL INPUT VOLTAGE	VIH				V	
TTL Inputs (IBTTL1/IBTTL2)		2.0				
CMOS Inputs (IBCMOS1/IBCMOS2)		VDD - 1.0				
INPUT HYSTERESIS (IBST1) Rising	VT+		2.75		V	VIL to VIH
Falling	VT-		1.92			VIH to VIL
(IBST2) Rising	VT+		2.20			VIL to VIH
Falling	VT-		1.35			VIH to VIL
INPUT CURRENT CMOS / TTL INPUTS	IIN		±5		µA	VIN = VDD or VSS
Inputs with 1Kohm Resistors			±5		mA	VIN = VDD or VSS
Inputs with 2Kohm Resistors			±2.5		mA	VIN = VDD or VSS
Inputs with 4Kohm Resistors			±1.25		mA	VIN = VDD or VSS
Inputs with 100Kohm Resistors			±50		µA	VIN = VDD or VSS
Resistor values nominal - See note 2						
HIGH LEVEL OUTPUT VOLTAGE	VOH				V	
All outputs		VDD - 0.05				IOH = - 1µA
Smallest drive cell OP1 / OPOS1		VDD - 1.0	VDD - 0.5			IOH = - 1mA
Low drive cell OP2 / OPOS2		VDD - 1.0	VDD - 0.5			IOH = - 2mA
Standard drive cell OP3 / OPOS3		VDD - 1.0	VDD - 0.5			IOH = - 3mA
Medium drive cell OP6 / OPOS6		VDD - 1.0	VDD - 0.5			IOH = - 6mA
Large drive cell OP12/OPOS12		VDD - 1.0	VDD - 0.5			IOH = - 12mA
LOW LEVEL OUTPUT VOLTAGE	VOL				V	
All Outputs				VSS + 0.05		IOL = 1µA
Smallest Drive Cell OP1 / OPOD1			0.2	0.4		IOL = 2mA
Low drive cell OP2 / OPOS2			0.2	0.4		IOL = 4mA
Standard drive cell OP3 / OPOS3			0.2	0.4		IOL = 6mA
Medium drive cell OP6 / OPOS6			0.2	0.4		IOL = 12mA
Large drive cell OP12/ OPOS12			0.2	0.4		IOL = 24mA
TRISTATE OUTPUT LEAKAGE CURRENT	IOZ				µA	
All open drain output cells		-10		10		VOH = VSS or VDD
OUTPUT SHORT CIRCUIT CURRENT	IOS				mA	
Standard outputs OP3 / OPT3		36	72	144		VDD = MAX VOUT = VDD
(See Note 3) OPOD3 / OPOS3		18	36	72		VDD = MAX VOUT = 0V
STANDBY SUPPLY CURRENT (per gate)	IDDSB		10		nA	
OPERATING SUPPLY CURRENT (per gate) (See Note 4)	IDDOP		1		µA/MHz	
INPUT CAPACITANCE	CI		5		pF	ANY INPUTS (See Note 5)
OUTPUT CAPACITANCE	COUT		5		pF	ANY OUTPUT (See Note 5)
BIDIRECTIONAL PIN CAPACITANCE	CI/O		7		pF	ANY I/O PIN (See Note 6)

Note 1: Commercial grade is 0 - 70 deg. C, 5V ± 10% power supply voltage.
Note 2: Resistor value spreads (Min - Max):
LOW VALUE (Rtyp 1K) 0.5 - 2Kohm   LOW VALUE (Rtyp 4K) 2K - 8Kohm
LOW VALUE (Rtyp 2K) 1.0 - 4Kohm   HIGH VALUE (Rtyp 100K) 25K - 250Kohm
Note 3: Standard driver output OP3 etc. Short circuit current for other outputs will scale. Not more than one output may be shorted at a time for a maximum duration of one second.
Note 4: Excluding peripheral buffers.
Note 5: Excludes package leadframe capacitance or bidirectional pins.
Note 6: Excludes package.

PACKAGING

Production quantities of the CLA60000 family are available in industry-standard ceramic and plastic packages according to the codes shown below. Prototype samples are normally supplied in ceramic only. Where plastic production packages are requested, ceramic prototypes will be supplied in the nearest equivalent and tested to the final test specification.

		PACKAGE DESCRIPTION -
DC	**DILMON**	Dual in Line, Multilayer ceramic. Brazed leads. Metal sealed lid. Through board.
DG	**CERDIP**	Dual in Line, Ceramic body. Alloy leadframe. Glass sealed. Through board.
DP	**PLASDIP**	Dual in Line, Copper or Alloy leadframe. Plastic moulded. Through board.
AC	**P.G.A.**	Pin Grid Array. Multilayer Ceramic. Metal sealed lid. Through board.
MP	**SMALL OUTLINE**	Dual in Line. 'Gullwing' formed leads. Plastic moulded. Surface mount.
LC	**LCC**	Leadless Chip Carrier. Multilayer ceramic. Metal sealed lid. Surface mount.
HC	**LEADED CHIP CARRIER**	Quad Multilayer ceramic. Brazed 'J' formed leads. Metal sealed lid. Surface mount.
GC	**LEADED CHIP CARRIER**	Quad Multilayer ceramic. Brazed 'Gullwing' leads. Metal sealed lid. Surface mount.
HG	**QUAD CERPAC**	Quad ceramic body. 'J' formed leads. Glass sealed. Surface mount.
GG	**QUAD CERPAC**	Quad ceramic body. 'Gullwing' formed leads. Glass sealed. Surface mount.
HP	**PLCC**	Quad Leaded plastic Chip Carrier. 'J' formed leads. Plastic moulded. Surface mount.
GP	**PQFP**	Quad plastic Flat Pack. 'Gullwing' formed leads. Glass sealed. Surface mount.

PACKAGING OPTIONS

The package style and pin count information is intended only as a guide. Detailed package specifications are available from Plessey Design Centres on request. Available packages are being continuously updated, so if a particular package is not listed, please enquire through your Plessey Sales Representative.

	LEADS	STYLE	CLA61	CLA62	CLA63	CLA64	CLA65	CLA66	CLA67	CLA68
DUAL IN LINE	16	DC	X							
	16	DG	X							
	16	DP	X							
	18	DC	X							
	18	DG								
	18	DP	X							
	20	DC	X							
	20	DG	X							
	20	DP	X							
	22	DC	X	X	X					
	22	DG		X						
	22	DP	X	X						
	24	DC	X	X	X	X				
	24	DG	X	X	X					
	24	DP	X	X	X					
	28	DC	X	X	X	X				
	28	DG	X	X	X	X				
	28	DP	X	X	X					
	40	DC	X	X	X	X	X			
	40	DG		X	X					
	40	DP	X	X	X	X				
	48	DC		X	X	X	X			
	48	DP		X	X	X				
QUAD	16	MP	X							
	18	MP	X	X	X					
	20	MP	X							
	24	MP	X							
	28	MP	X	X						
	28	HP	X	X	X	X				
	28	LC	X	X	X					
	28	HC	X	X	X					
	28	HG	X	X	X					
	44	HP	X	X	X	X	X			
	44	GP	O	O	O					
	44	LC	X	X	X	X				
	44	HC	X	X	X	X				
	44	HG	X	X	X	X				
	48	GP		O	O	O				
	64	GP		O	O	O				
	68	HP		X	X	X	X			
	68	LC		X	X	X	X	X	X	
	68	HC		X	X	X	X			
	68	HG		X	X	X	X	X		
	80	GP			O	O				
	84	HP			X	X	X			
	84	LC			X	X	X	X		
	84	HC			X	X	X	X		
	84	HG		X	X	X	X	X		
	100	GP			O	O				
	100	GG			O	O				
	120	GP				O	O			O
	132	GC					O	O	O	
	160	GP								O
	172	GC						O	O	O
	196	GC						O		
PGA	68	AC		X	X	X	X			
	84	AC			X	X	X	X	X	
	100	AC			X	X	X			
	120	AC				X	X			
	132	AC					X	X		
	144	AC					X	X		
	180	AC					X	X		

X - Approved package O - Under Approval

CELL LIBRARY

A very comprehensive cell library is available in CLA60000, reflecting the considerable amount of influence from a broad base of system designers on earlier array products. This cell library has been designed as a subset of the Cell Design methodology - Plessey Megacell MVA60000 - containing equivalent functions. Design netlists can be transformed from gate array to near full-custom layout without substantial translation effort.

The two micron CMOS array (CLA5000) cell library can be converted to equivalent cells on the CLA60000 arrays to allow system upgrades. In this enhanced library version, 28 new functions have been released, such as RAMs, ROMs, Microprocessor, and DSP Macros. Some macro cells are also available for implementing structured test philosophies. Detailed application notes and user-guides on built-in test for gate arrays (PDS-BIST) are available.

CLA60000 LIBRARY (Version V1R3)

LOGIC ARRAY MICROCELLS:

BUF	Non-Inverting Signal Buffer Cell
DELAY	1.7nS (typical) Delay cell
2INV	Dual Inverter
INV2	Inverter Dual Drive
INV4	Inverter Quad Drive
INV8	Inverter x8 Drive
NAND2	2-Input Nand Gate
ND3	3-Input Nand Gate
NAND3	3-Input Nand Gate + Inverter
2NAND3	Dual 3-Input NAND Gate
NAND4	4-Input NAND Gate
NAND5	5-Input NAND Gate
NAND6	6-Input NAND Gate
NAND8	8-Input NAND Gate
NOR2	2-Input NOR Gate
NR3	3-Input NOR Gate
NOR3	3-Input NOR Gate + Inverter
2NOR3	Dual 3-Input NOR Gate
NOR4	4-Input NOR Gate
NOR5	5-Input NOR Gate
NOR6	6-Input NOR Gate
NOR8	8-Input NOR Gate
A2O2I	2-Input AND to 2-Input NOR Gate + Inverter
O2A2I	2-Input OR to 2-Input NAND Gate + Inverter
2A2O2	Dual 2-Input AND to 2-Input NOR Gate
2O2A2I	Dual 2-Input OR to 2-Input NAND Gate
2ANOR	2-Input ANDs to 2-Input NOR gate
2ONAND	2-Input ORs to 2-Input NAND Gate
A2O3I	2-Input AND to 3-Input NOR Gate
O2A3I	2-Input OR to 3-Input NAND Gate
A3O2I	3-Input AND to 2-Input NOR Gate
O3A2I	3-Input OR to 2-Input NAND Gate
A2O4I	Quad 2-Input ANDs to 4-Input NOR Gate
O2A4I	Quad 2-Input ORs to 4-Input NAND Gate
A4O2I	Dual 4-Input ANDs to 2-Input NOR Gate
O4A2I	Dual 4-Input ORs to 2-Input NAND Gate
3A2O3I	Triple 2-Input ANDs to 3-Input NOR Gate
3O2A3I	Triple 2-Input ORs to 3-Input NAND Gate
A2O2A2I	2-Input AND to 2-Input OR to 2-Input NAND
O2A2O2I	2-Input OR to 2-Input AND to 2-Input NOR
GND	GND Cell
VDD	VDD Cell
EX2	Exclusive OR Gate + Inverter
EXN2	Exclusive NOR Gate + Inverter
EXOR	Exclusive OR Gate + NAND Gate + Inverter
EXNOR	Exclusive NOR Gate + NOR Gate + Inverter
EXOR2	2-Input Exclusive OR Gate
EXNOR2	2-Input Exclusive NOR Gate
EXOR3	3-Input Exclusive OR Gate
EXNOR3	3-Input Exclusive NOR Gate
HADD	Half Adder + Inverter
SUM	Sum Block
CARRY	Carry Block + NOR Gate
FADD	Full Adder + NOR Gate
MUX2TO1	2 To 1 Multiplexor
MUX4TO1	4 to 1 Multiplexor
MUX8TO1	8 to 1 Multiplexor
MUXI2TO1	2 to 1 Inverting Multiplexor
MUXI4TO1	4 to 1 Inverting Multiplexor
MUXI8TO1	8 to 1 Inverting Multiplexor
CLKA	Basic Clock Driver
2CLKA	Dual Basic Clock Driver
CLKAP	Basic Clock Driver + Inverter
CLKAM	Basic Clock Driver + Inverter
CLKB	Large Clock Driver + Inverter
DRV3	Triple Output Internal Driver
DRV6	Hex Output Internal Driver
TM	Buffered Transmission Gate
2TM	Transmission Gate for 2 to 1 Multiplexing
BDR	Bus Driver
DL	Data Latch
DL2	Data Latch
DLRS	Data Latch with Set and Reset
DLARS	Data Latch with Set and Reset
DF	D-Type Flip-Flop
DFRS	D-Type Flip-Flop with Set and Reset
MDF	Multiplexed Master-Slave D-Type Flip-Flop
MDFRS	Multiplexed Master-Slave D-Type Flip-Flop with Set and Reset
M3DF	3 To 1 Multiplexed Master-Slave D-Type Flip-Flop
M3DFRS	3 To 1 Multiplexed Master-Slave D-Type Flip-Flop with Set and Reset
JK	J K Flip Flop
JKRS	J K Flip Flop with Set and Reset
JBARK	JBAR - K Flip Flop
JBARKRS	JBAR - K Flip Flop with Set and Reset
BJBARK	Buffered J-K Flip-Flop
BJBARKRS	Buffered J-K Flip-Flop with Set and Reset
BDL	Buffered Data Latch
BDLRS	Buffered Data Latch with Set and Reset
BDLARS	Buffered Data Latch with Set and Reset
BDF	Buffered Master-Slave D-Type Flip-Flop
BDFRS	Buffered Master-Slave D-Type Flip-Flop with Set and Reset
BMDF	Buffered Multiplexed Master-Slave D-Type Flip-Flop
BMDFRS	Buffered Multiplexed Master-Slave D-Type Flip-Flop with Set and Reset

INTERMEDIATE BUFFERS:

IBST1	Input Buffer with CMOS switching level
IBST2	Input Buffer with 2V switching level
IBSK1	Driver with Lightly Skewed Outputs
IBSK2	Driver with Medium Skewed Outputs
IBSK3	Driver with Heavily Skewed Outputs
IBTRID	Tri-State Driver
IBTRID1	Tri-State Driver with Lightly Skewed Outputs + 2 Inverters
IBTRID2	Tri-State Driver with Medium Skewed Outputs + 2 Inverters
IBTRID3	Tri-State Driver with Heavily Skewed Outputs + 2 Inverters
IBGATE	Large 2-Input NAND Gate + Large 2-Input NOR Gate
IB2BD	Dual High Power Inverters
IBCLKB	Large Clock Driver
IBDF	Master-Slave D-Type Flip-Flop
IBDFA	Master-Slave D-Type Flip-Flop
IBCMOS1	CMOS Input Buffer and Large 2-Input NAND Gate
IBCMOS2	CMOS Input Buffer and Data Latch
IBTTL1	TTL Input Buffer and Large 2-Input NAND Gate
IBTTL2	TTL Input Buffer and Data Latch

INPUT BUFFERS:

IPNR	Input Cell (with no Pullup or Pulldown resistors)
IPR1P	Input Cell with 1K-Ohm Pull-up Resistor
IPR1M	Input Cell with 1K-Ohm Pull-down Resistor
IPR2P	Input Cell with 2K-Ohm Pull-up Resistor
IPR2M	Input Cell with 2K-Ohm Pull-down Resistor
IPR3P	Input Cell with 4K-Ohm Pull-up Resistor
IPR3M	Input Cell with 4K-Ohm Pull-down Resistor
IPR4P	Input Cell with 100K-Ohm Pull-up Resistor
IPR4M	Input Cell with 100K-Ohm Pull-down Resistor

OUTPUT BUFFERS:

OP1	Smallest Drive Output Buffer
OP2	Small Drive Output Buffer
OP3	Standard Drive Output Buffer
OP6	Medium Drive Output Buffer
OP12	Large Drive Output Buffer
OP5B	Standard Drive Non-Inverting Output Buffer
OP11B	Large Drive Non-Inverting Output Buffer
OPT1	Smallest Drive Tri-State Output Buffer
TRID	Tri-State Driver
OPT2	Small Drive Tri-State Output Buffer
OPT3	Standard Drive Tri-State Output Buffer
OPT6	Medium Drive Tri-state Output Buffer
OPT12	Large Drive Tri-State Output Buffer
OPT4B	Standard Drive Non-Inverting Tri-State Output Buffer
OPT10B	Large Drive NonInverting Tri-State Output Buffer
OPOD1	Smallest Drive Open-Drain Output Buffer
OPOD2	Small Drive Open-Drain Output Buffer
OPOD3	Standard Drive Open-Drain Output Buffer
OPOD6	Medium Drive Open-Drain Output Buffer
OPOD12	Large Drive Open-Drain Output Buffer
OPOD5B	Standard Drive Non-Inverting Open Drain Output Buffer
OPOD11B	Large Drive Non-Inverting Open Drain Output Buffer
OPOS1	Smallest Drive Open-Source Output Buffer
OPOS2	Small Drive Open-Source Output Buffer
OPOS3	Standard Drive Open-Source Output Buffer
OPOS6	Medium Drive Open-Source Output Buffer
OPOS12	Large Drive Open-Source Output Buffer
OPOS5B	Standard Drive Non-Inverting Open-Source Output Buffer
OPOS11B	Large Drive Non-Inverting Open-Source Output Buffer

SUPPLY PADS:

OPVP	VDD Power Pad (Outputs)
OPVM	GND Power Pad (Outputs)
OPVPB	VDD Power Pad (Outputs) : Break in VDD
OPVMB	GND Power Pad (Outputs) : Break in GND
OPVPBB	VDD Power Pad (Outputs) : Break in VDD and GND
OPVMBB	GND Power Pad (Outputs) : Break in GND and VDD
IBVP	VDD Power Pad (Buffers)
IBVM	GND Power Pad (Buffers)
IBVPB	VDD Power Pad (Buffers) : Break in VDD
IBVMB	GND Power Pad (Buffers) : Break in GND
IBVPBB	VDD Power Pad (Buffers) : Break in VDD and GND
IBVMBB	GND Power Pad (Buffers) : Break in GND and VDD
LAVP1	Power Pad for Logic Array
LAVP2	Power Pad for Logic Array
LAVP3	Power Pad for Logic Array
LAVP4	Power Pad for Logic Array
LAVP5	Power Pad for Logic Array
LAVM1	Power Pad for Logic Array
LAVM2	Power Pad for Logic Array
LAVM3	Power Pad for Logic Array
LAVM4	Power Pad for Logic Array
LAVM5	Power Pad for Logic Array
LAGND	Power Pad (Vss) for Logic Array
LAVDD	Power Pad (Vdd) for Logic Array

OTHER CELLS:

ANPOR	Power-on Reset
OSC1	Crystal Oscillator Peripheral Cell

Analog

ANIPCMP1	Comparator - Standard
ANIPCMP2	Comparator - Low Power
ANADC4	Four Bit Analogue To Digital Converter
ANDAC4	Four Bit Digital To Analogue Converter
ANVREFGN	Reference Generator/Power On Reset
ANVREFSH	Shunt Regulator/Power On Reset

MEMORY CELLS:

RAM2	2 bit memory
RAM4	4 bit memory
RAM8	8 bit memory
RAM16	6 bit memory
RAM32	32 bit memory
RAM64	64 bit memory

SINGLE PORT DECODERS:

RAD2S	2 words (1-16 bits RAM)
RAD2SL	2 words (17-64 bits RAM)
RAD4S	4 words (1-16 bits RAM)
RAD4SL	4 words (17-64 bits RAM)
RAD8S	8 words (1-16 bits RAM)
RAD8SL	8 words (17-64 bits RAM)
RAD16S	16 words (1-16 bits RAM)
RAD16SL	16 words (17-64 bits RAM)
RAD32S	32 words (1-16 bits RAM)
RAD32SL	32 words (17-64 bits RAM)
RAD64S	64 words (1-16 bits RAM)
RAD64SL	64 words (17-64 bits RAM)

DUAL PORT DECODERS:

RAD2D	2 words (1-16 bits RAM)
RAD2DL	2 words (17-64 bits RAM)
RAD4D	4 words (1-16 bits RAM)
RAD4DL	4 words (17-64 bits RAM)
RAD8D	8 words (1-16 bits RAM)
RAD8DL	8 words (17-64 bits RAM)
RAD16D	16 words (1-16 bits RAM)
RAD16DL	16 words (17-64 bits RAM)
RAD32D	32 words (1-16 bits RAM)
RAD32DL	32 words (17-64 bits RAM)
RAD64D	64 words (1-16 bits RAM)
RAD64DL	64 words (17-64 bits RAM)

PROCESSOR CELLS - CLA6PROC:

MI2901	4 Bit Processor Slice
MI8085	8 Bit Microprocessor

PARACELLS - CLA6PARA:

RBRAM	Random Access Memory
ROROM	Read Only Memory (mask programmed)

JTAG/BIST CELLS - CLA6BIST:

This design library module contains 15 cells to incorporate JTAG/BIST architectures into the gate array. The boundary-scan cells support BIST, and can be configured to provide pseudo-random test vector generators and signature analysers. Further information on these structures and their use is contained in the Plessey application notes on JTAG/BIST.

DSP CELL LIBRARY - CLA6DSP:

The DSP module contains a range of cells for DSP-type applications - Ripple Carry Adders, Subtractors, Left/Right shifters, Logic units, and ALU's. Further information is available in the DSP application note (available October 1989).

MACROCELL LIBRARY - CLA6MAC

Many of the macro functions perform similar logic functions to the standard TTL and CMOS logic families. These macrocells are constructed from the basic microcells and are already placed and routed to give optimum use of silicon area.

Adders

ADA4	4 bit binary full adders with fast carry
ADG4	Look ahead carry generator

Counters

CNA4	BCD counter/4 bit latch BCD decoder/driver
CNB4	4 bit counter latch
CNC4	4 bit synchronous counter
CND4	4 bit synchronous binary up/down counter
CND4A	4 bit synchronous binary up/down counter with reset
CNE4	4 bit decade counter
CNF4	4 bit synchronous binary counter
CNG4	4 bit synchronous binary counter with enable

Decoders

DRA3T8	3 line to 8 line decoder/demultiplexer
DRA4T16	4 line to 16 line decoder/demultiplexer
DRA4T16A	4 line to 16 line decoder/demultiplexer with no enable
DRB3T8	3 line to 8 line decoder/demultiplexer with address registers
DRC3T8	3 line to 8 line decoder/demultiplexer with address latches
DRD2T4	2 line to 4 line decoder/demultiplexer
DRF4T101	4 line to 10 line BCD decoder
DRG4T10	4 line to 10 line Excess 3 to decimal decoder
DRH4T10	4 line to 10 line Excess Gray to decimal decoder
DRI10	BCD to decimal decoder/driver
DRJ7	BCD to 7-Segment decoder/driver
DRK7	BCD to 7-Segment decoder/driver
DRL7	BCD to 7-Segment decoder/driver

Encoders

ENA8T3	8 line to 3 line priority encoder
ENB10T4	10 line to 4 line priority encoder

Flip-flops

FFA8	8 bit bistable latches
FFB6	6 bit D-type flip-flops with clear
FFC4	4 bit D-type flip-flops with clear and complementary outputs
FFD8	Octal D-type flip-flops with clear

ALU/Function generator

FGA4	Arithmetic logic unit/function generator

Magnitude comparator

MCA4	4 bit magnitude comparators

Multipliers

MLA10	Decade rate multiplier
MLB4X4	4 bit binary multiplier with tristate outputs
MLW7	7 bit slice Wallace tree with tristate outputs

Multiplexers

MXA8T1	8 line to 1 line data selector/multiplexer
MXB4T1	4 line to 1 line data selector/multiplexer with tristate outputs
MXB4T1A	4 line to 1 line data selector/multiplexer with inverted tristate outputs
MXC2T1	Quad 2 line to 1 line data selector/multiplexer
MXC2T1A	Quad 2 line to 1 line data selector/multiplexer with inverted outputs
MXD4T1	4 line to 1 line data selector/multiplexer
MXE4T1	Dual 4 line to 1 line data selector/multiplexer
MXF2T1	Quad 2 line to 1 line multiplexer with storage

Parity generators

PGA9	9 bit odd/even parity generator/checker

Monitor

PERF	Performance monitor for CLA60000

Shift registers

SRA2	2 bit parallel out serial shift registers with clear
SRA4	4 bit parallel out serial shift registers with clear
SRA8	8 bit parallel out serial shift registers with clear
SRA8A	8 bit parallel out serial shift registers with no clear
SRB2	2 bit parallel in serial out shift registers with clear
SRB4	4 bit parallel in serial out shift registers with clear
SRB8	8 bit parallel in serial out shift registers with clear
SRB8A	8 bit parallel in serial out shift registers with no clear
SRC8	8 bit parallel in serial out shift registers
SRD4	4 bit serial in parallel out shift registers
SRE4	4 bit parallel in parallel out shift registers with J.KBAR input
SRF8	8 bit shift and store registers with tristate outputs
SRG4	4 bit bidirectional universal shift registers
SRJ4	4 bit parallel access shift register
SRK5	5 bit shift register

QUALITY AND RELIABILITY

At Plessey Semiconductors, quality and reliability are built into the product by rigorous control of all processing operations and by minimising random uncontrolled effects in all manufacturing operations. Process management involves full documentation of procedures, recording of batch-by-batch data, using traceability procedures and the provision of appropriate equipment and facilities to perform sample screens and conformance testing on finished product.

A common information management system is used to monitor the manufacturing of Plessey CMOS and Bipolar processes. All products benefit from the use of an integrated monitoring system throughout all manufacturing operations leading to high quality standards for all technologies.

Further information is contained in the Quality Brochure, available from Plessey Semiconductors Sales Offices.