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APPROVED BY: <i>Messrs Chen</i>		ISSUE : MAY.07,1996
		TOTAL PAGE : 11
		VERSION : 6

CUSTOMER	ACCEPTANCE	SPECIFICATIONS
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MODEL NO. :

EG64I00BCWU

FOR MESSRS :

CUSTOMER'S APPROVAL

DATE :

BY :

EMERGING DISPLAY
TECHNOLOGIES CORPORATION

MODEL NO . EG64I00BCWU	VERSION 6
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RECORDS OF REVISION	DOC . FIRST ISSUE SEP.25,1995
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DATE	REVISED DRAWING NO.	SUMMARY
MAR.12,1996	1,2,3,4,6,7,8,9,10	ALL PAGES ARE REVISED AND ENLARGED
MAR.21,1996	1	2. MECHANICAL SPECIFICATIONS (2)MODULE SIZE:254.0*276.8*19.5Dmm → 254.0*276.8*21.5Dmm
	7	7. OUTLINE DIMENSION : 223.97±2.5 → 223.97±0.25
	8	ALL PAGE REVISED
APR.01,1996	8	ALL PAGE REVISED
APR.29,1996	2	NOTE(4) OPERATING TEMPERATURE FOR CCFL BACKLIGHT IS 0°C ~ - 20°C
MAY.07,1996	3	POWER SUPPLY FOR CCFL : VCCFL=300Vrms → 455Vrms.
	5	RISE , FALL TIME : tr , tf = 30ns → 50ns.MAX.

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1. GENERAL SPECIFICATIONS

1.1 GENERAL SPECIFICATIONS
PLEASE REFER TO :

CUSTOMER ACCEPTANCE STANDARD SPECIFICATIONS :

EU-001A

1.2 THIS INDIVIDUAL SPECIFICATION IS PRIOR TO GENERAL
SPECIFICATIONS .

2. MECHANICAL SPECIFICATIONS

- (1) NUMBER OF DOTS ----- 640W * 480H DOTS
- (2) MODULE SIZE ----- 254.0W * 276.8H * 21.5D mm
- (3) EFFECTIVE AREA ----- 230.0W * 198.0H mm
- (4) ACTIVE AREA ----- 223.97W * 191.97H mm
- (5) DOT SIZE ----- 0.32W * 0.37H mm
- (6) DOT PITCH ----- 0.35W * 0.40H mm
- (7) LCD TYPE ----- STN , BLUE, TRANSMISSIVE , NEGATIVE
- (8) DRIVING METHOD ----- 1 / 240 DUTY MULTIPLEX DRIVE
- (9) VIEWING DIRECTION ----- 12 O'CLOCK
- (10) BACK- LIGHT ----- CCFL
- (11) LCD DOT COLOR ----- DARK BLUE

3. ABSOLUTE MAXIMUM RATINGS

3.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	COMMENT
POWER SUPPLY FOR LOGIC	VDD - VSS	0	6.0	V	
POWER SUPPLY FOR LCD DRIVING	VDD - VO	0	32.0	V	
INPUT VOLTAGE	VI	VSS	VDD	V	
STATIC ELECTRICITY	—	—	100	V	NOTE (1)

NOTE (1) : TEST METHOD AND CONDITIONS :

AFTER CHARGING UP 200 PF CAPACITOR BY STATED VOLTAGE ,
THE CAPACITOR IS CONNECTED WITH INTERFACE PINS OF THE
MODULE .

3.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS.

I T E M	OPERATING		STORAGE		COMMENT
	MIN.	MAX.	MIN.	MAX.	
AMBIENT TEMPERATURE	0 °C	50 °C	-20 °C	60 °C	NOTE (2)(3)(4)
HUMIDITY	—	90 % RH	—	90 % RH	WITHOUT CONDENSATION
VIBRATION	—	2.45 m/s ² (0.25 G)	—	11.76 m/s ² (1.2 G)	10~100 HZ XYZ DIRECTIONS 1 Hr. EACH
SHOCK	—	29.4 m/s ² (3 G)	—	490.0 m/s ² (50 G)	10 mSECONDS XYZ DIRECTIONS 1 TIME EACH
CORROSIVE GAS	NOT ACCEPTABLE		NOT ACCEPTABLE		

NOTE (2) : Ta AT -20°C : 48HR MAX.

60°C : 48HR MAX.

NOTE (3) : BACKGROUND COLOR CHANGES SLIGHTLY DEPENDING ON AMBIENT
TEMPERATURE THIS PHENOMENON IS REVERSIBLE.

NOTE (4) : WITH THE CCFL OPERATING TEMPERATURE OF 0°C ~ -20°C THE
START UP VOLTAGE FOR THE CCFL BACKLIGHT MUST BE V=1100
VAC.ONCE THE CCFL BACKLIGHT IS OPERATIONAL THE DRIVING
VOLTAGE IS REDUCED TO V=455VAC WITH A CURRENT OF 5 mA.

4. ELECTRICAL CHARACTERISTICS

Ta = 25 °C

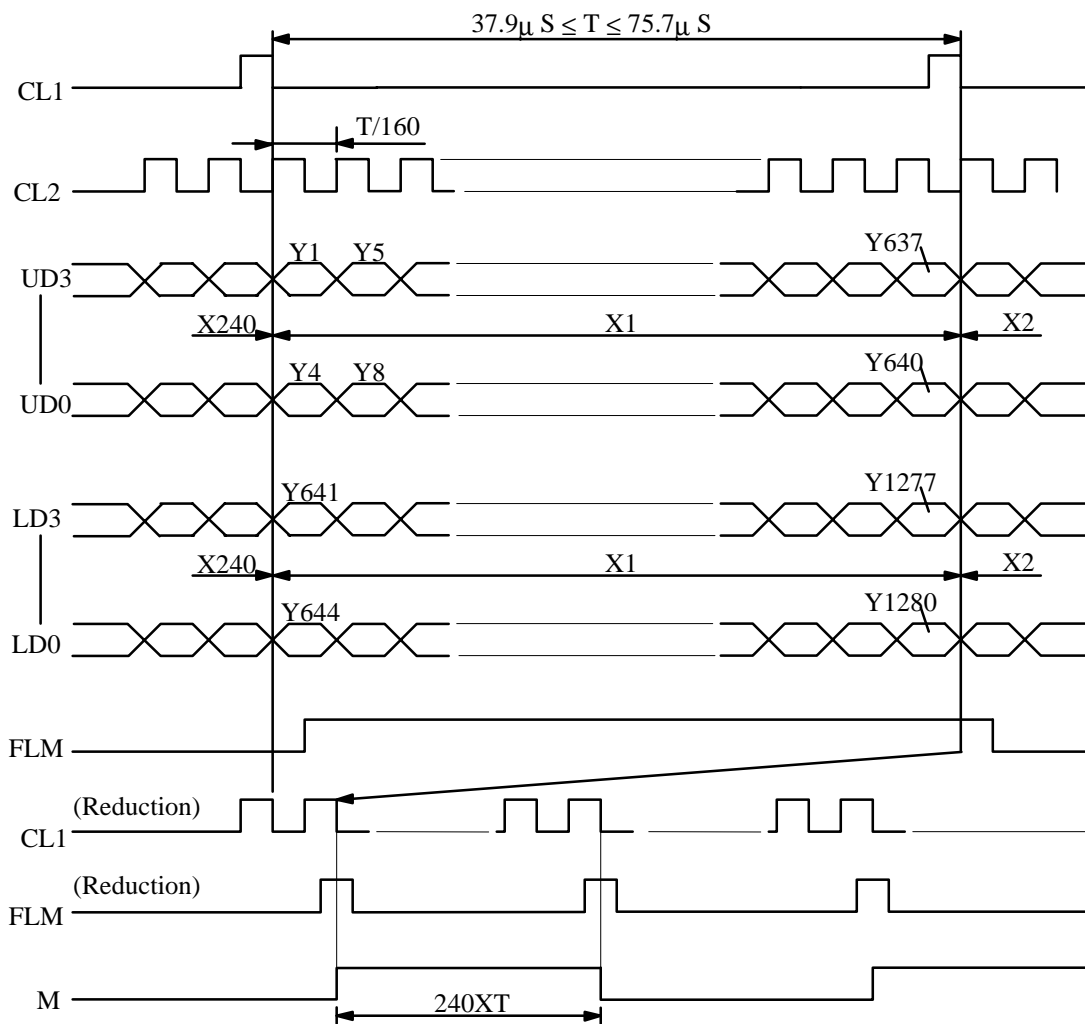
VDD = 5.0 V

PARAMETER	SYMBOL	CONDITION	MIN .	TYP .	MAX .	UNIT
POWER SUPPLY VOLTAGE FOR LOGIC	VDD - VSS	—	4.75	5.0	5.25	V
POWER SUPPLY VOLTAGE FOR LCD DRIVE	VO - VSS	—	- 17.0	- 19.0	- 22.0	V
INPUT VOLTAGE NOTE (1)	VIH	H LEVEL	0.8*VDD	—	—	V
	VIL	L LEVEL	—	—	0.2*VDD	V
POWER SUPPLY CURRENT FOR LOGIC	IDD	VDD-VSS = 5.0 V VO-VSS = -19.0V	—	18	—	mA
POWER SUPPLY CURRENT FOR LCD DRIVE	IO	VDD-VSS = 5.0 V VO-VSS = -19.0V	—	16	—	mA
RECOMMENDED LCD DRIVING VOLTAGE NOTE (2)	VDD - VO ∅ = 10 ° θ = 180 °	Ta = 0 °C	—	25.0	—	V
		Ta = 25 °C	—	24.0	—	V
		Ta = 50 °C	—	22.5	—	V
FLM FREQUENCY	f FLM	—	55	75	110	HZ
POWER SUPPLY FOR CCFL	VOLTAGE	VCCFL	—	—	455	Vrms
	FREQUENCY	f CCFL	—	—	30K	HZ
	CURRENT	IL	—	—	5	mA

NOTE (1) : APPLIED TO TERMINALS M , FLM , CL1 , CL2 , UD0~UD3 .

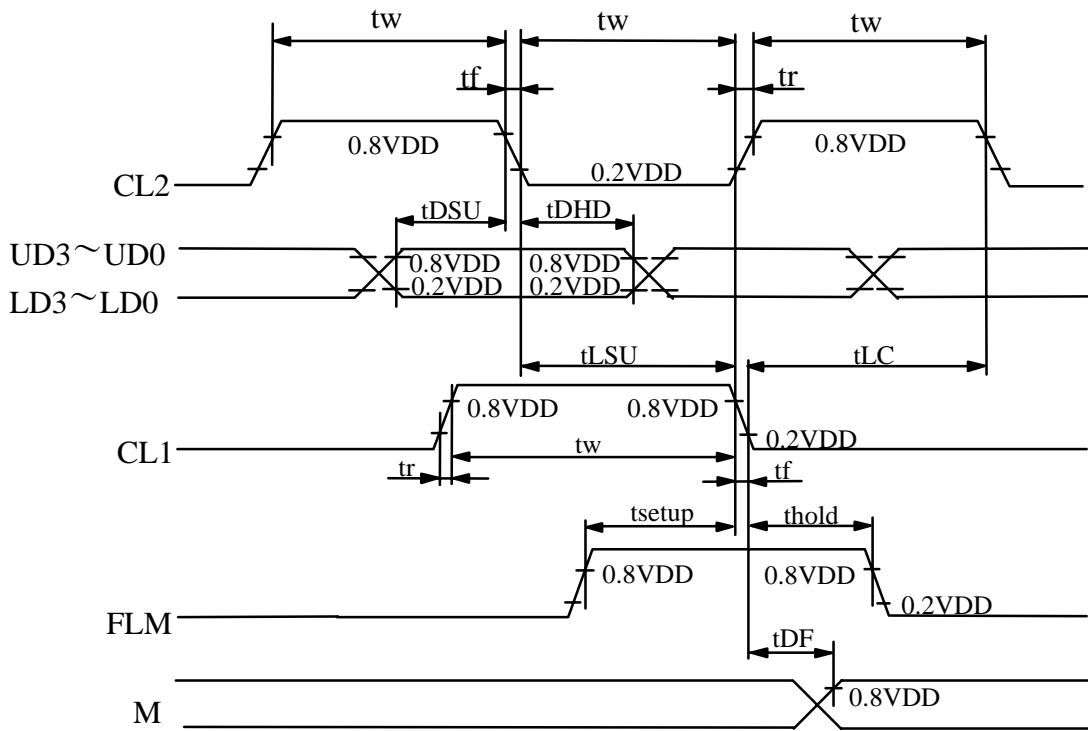
NOTE (2) : RECOMMENDED LCD DRIVING VOLTAGE MAY FLUCTUATE ABOUT ±1.0V BY EACH MODULE .

5. TIMING CHARACTERISTICS
5.1 INTERFACE TIMING



5.2 SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Frequency of maximum clock	fcp	—	—	8	MHZ
CL1, CL2, pulse width	tw	45	—	—	nS
Rise, fall time	tr, tf	—	—	50	nS
Data setup time	tDSU	20	—	—	nS
Data hold time	tDHD	20	—	—	nS
CL1 setup time	tLSU	80	—	—	nS
CL1 → CL2 time	tLC	80	—	—	nS
FLM setup time	tsetup	100	—	—	nS
FLM hold time	thold	100	—	—	nS
M delay time	tDF	—	—	300	nS



6. OPTICAL CHARACTERISTICS

Ta = 25 °C

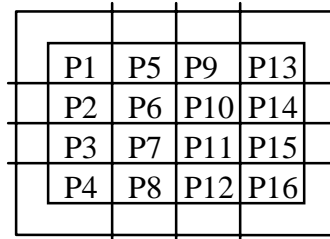
VDD = 5.0 V

VDD - VO = 24.0 V

I T E M	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
VIEWING AREA	∅2 - ∅1	K ≥ 2.0	40	—	—	deg.	1
CONTRAST RATIO	K	∅ = 10° θ = 180°	—	5	—	—	1
RESPONSE TIME	tr(rise)	∅ = 10° θ = 180°	—	250	—	ms	1
	tf(fall)	∅ = 10° θ = 180°	—	350	—	ms	1
BRIGHTNESS OF BACKLIGHT	B	—	64	—	—	cd / m ²	1
RISE TIME OF BACKLIGHT	TC	—	—	3	—	MINUTE	
BRIGHTNESS UNIFORMITY	—	—	—	—	10	%	2,3

NOTE (1) : PLEASE REFER TO :
CUSTOMER ACCEPTANCE STANDARD SPECIFICATIONS. (EU - 001A)

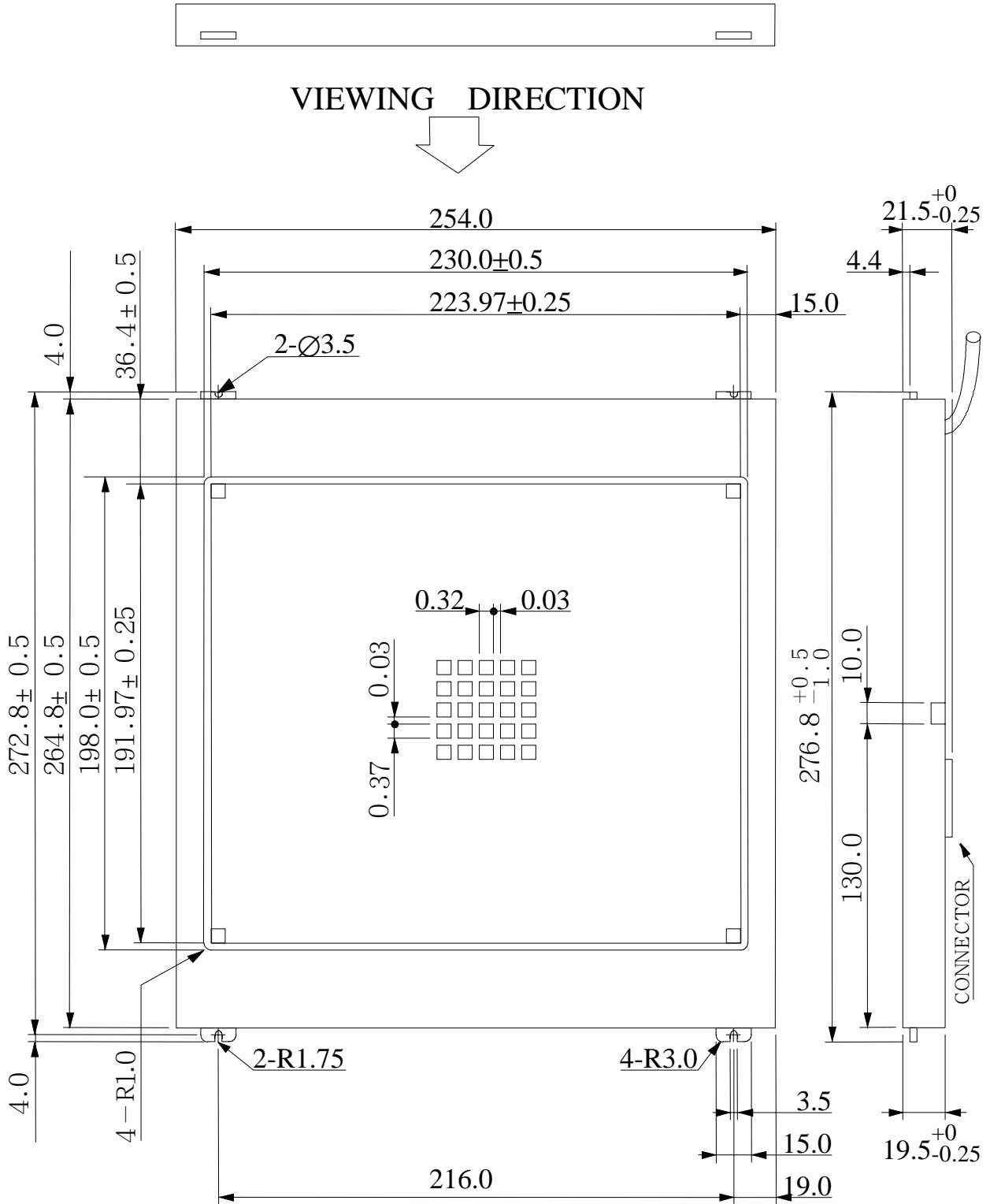
NOTE (2) : MEASUREMENT OF THE FOLLOWING 16 PLACES ON THE DISPLAY .
DEFINITION OF THE BRIGHTNESS UNIFORMITY



NOTE (3) : BRIGHTNESS UNIFORMITY IS DEFINED AS FOLLOWING

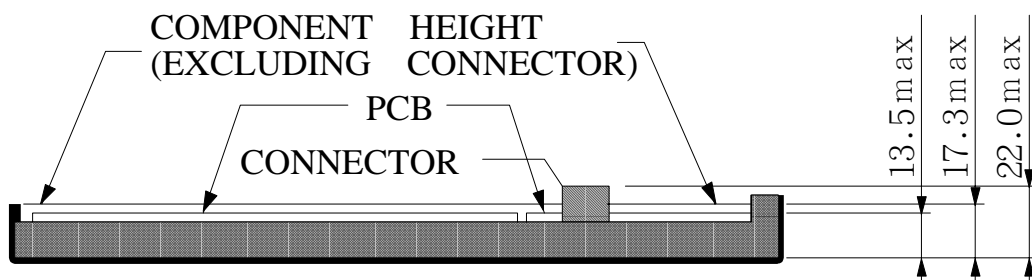
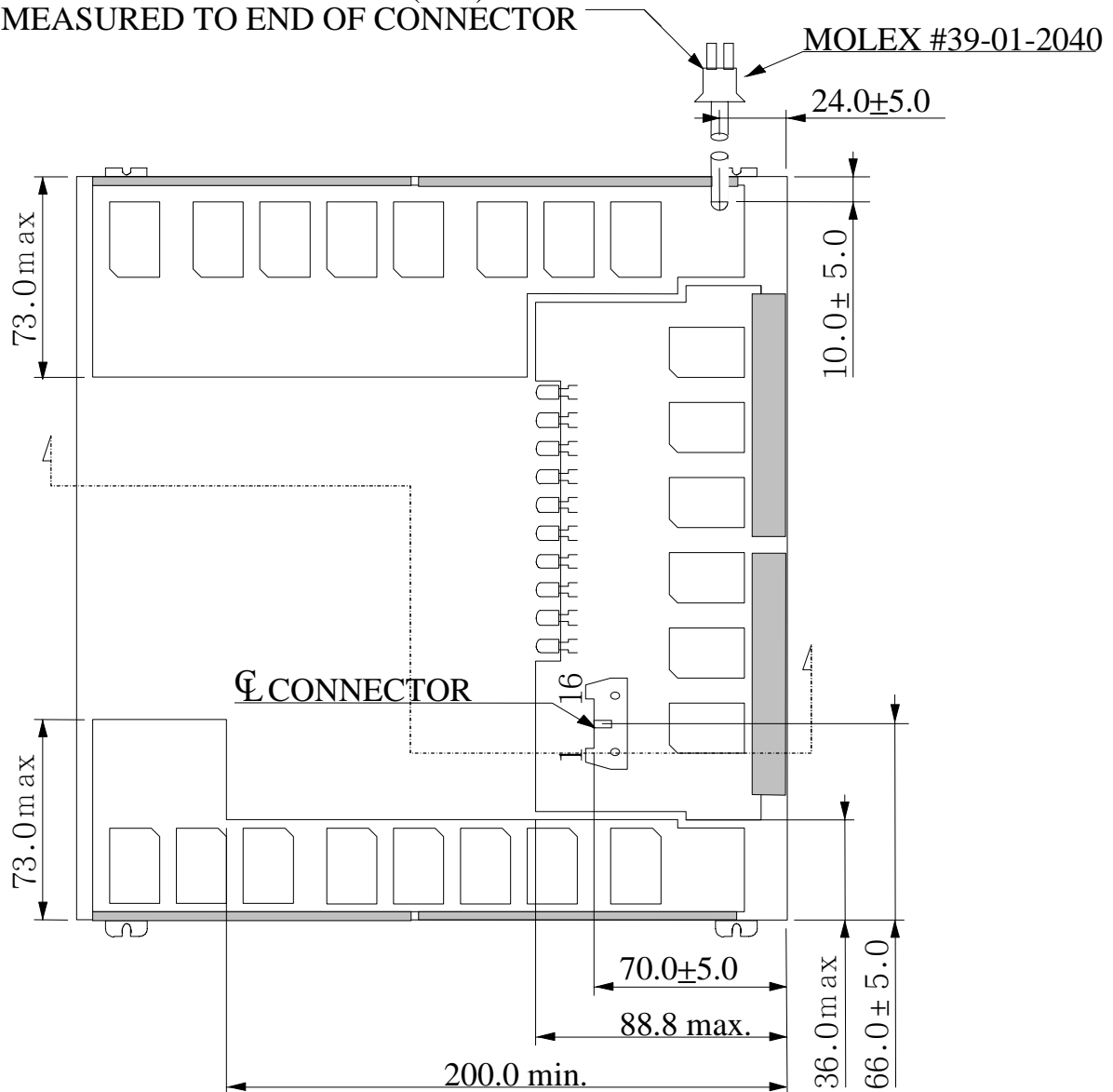
$$\sum_x \left[\frac{|(\text{MAXIMUM BRIGHTNESS OR MINIMUM BRIGHTNESS}) - \text{AVERAGE BRIGHTNESS}|}{\text{AVERAGE BRIGHTNESS}} \right]$$

7. OUTLINE DIMENSION

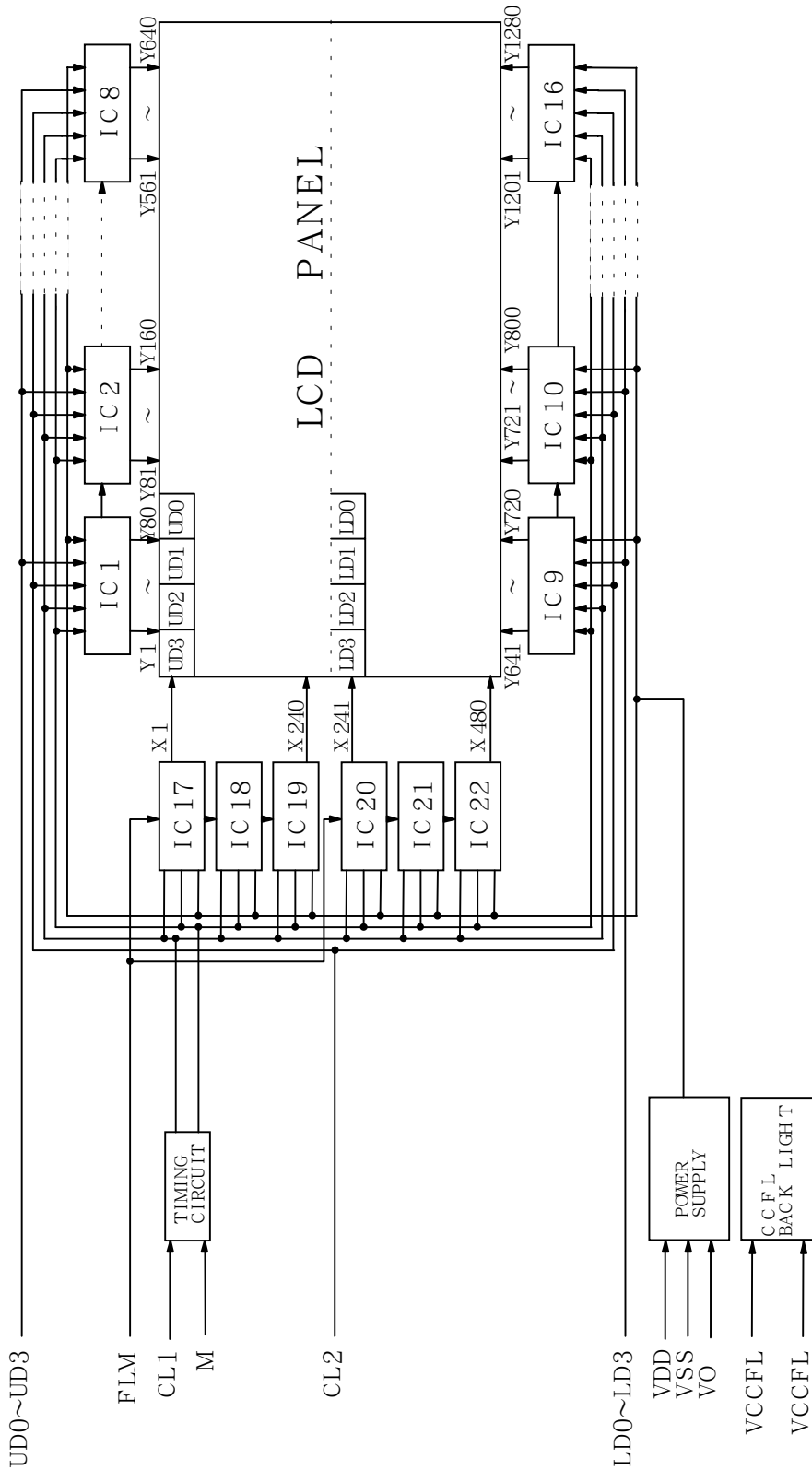


UNIT:mm
SCALE:NTS
NOT SPECIFIED TOLERANCE IS \pm 0.5mm

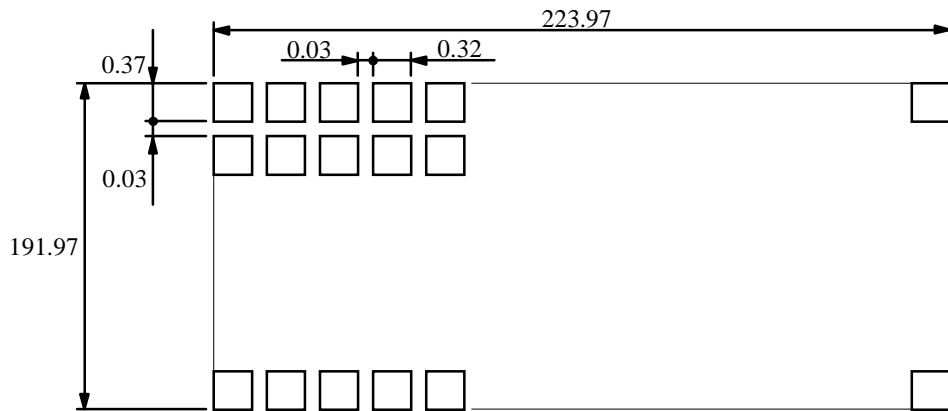
CABLE LENGTH IS 250mm (9.8") ± 20mm
MEASURED TO END OF CONNECTOR



8. BLOCK DIAGRAM



9. DETAIL DRAWING OF DOT MATRIX



UNIT : mm
SCALE : NTS

10. INTERFACE SIGNALS

IF1 :

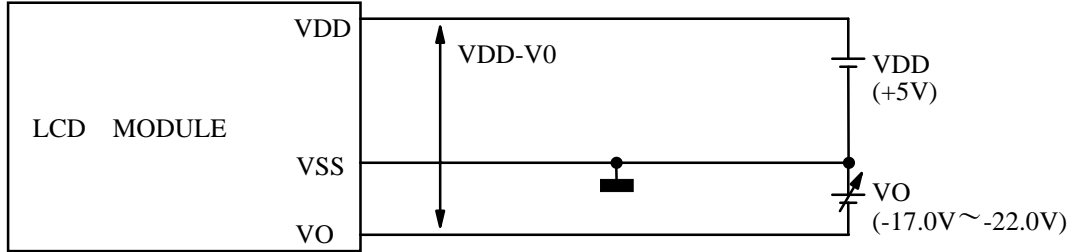
PIN NO	SYMBOL	LEVEL	FUNCTION
1	FLM	H	THE FLM SIGNAL INDICATING THE BEGINNING OF EACH DISPLAY CYCLE
2	CL1	H → L	DISPLAY DATA LATCH
3	CL2	H → L	DISPLAY DATA SHIFT
4	M	H/L	CONTROL SIGNAL FOR AC DRIVING
5	VO	————	OPERATING VOLTAGE FOR LCD DRIVING
6	VDD	————	POWER SUPPLY FOR LOGIC CIRCUIT
7	VSS	————	GROUND
8	NC	————	NOT USE
9	UD0	H/L	DISPLAY DATA
10	UD1	H/L	
11	UD2	H/L	
12	UD3	H/L	
13	LD0	H/L	
14	LD1	H/L	
15	LD2	H/L	
16	LD3	H/L	

IF2 :

INTERFACE	PIN	SINGAL	LEVEL	FUNCTION
CCFL	1	VCCFL	————	POWER SUPPLY FOR CCFL DRIVING (POWER TO BACKLIGHT)
	2,3	NC	————	
	4	VCCFL	————	POWER SUPPLY FOR CCFL DRIVING (POWER RETURN)

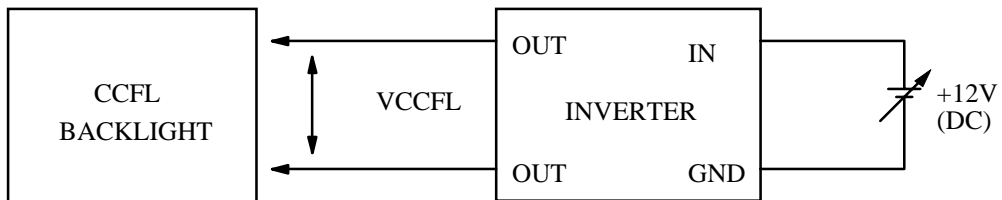
11. POWER SUPPLY

11.1 POWER SUPPLY FOR LCM



VDD-V0 : LCD DRIVING VOLTAGE

11.2 POWER SUPPLY FOR CCFL BACK - LIGHT



RECOMMENDED INVERTER : CXA-M10L(TDK)

11.3 TIMING OF POWER SUPPLY AND INTERFACE SIGNAL

