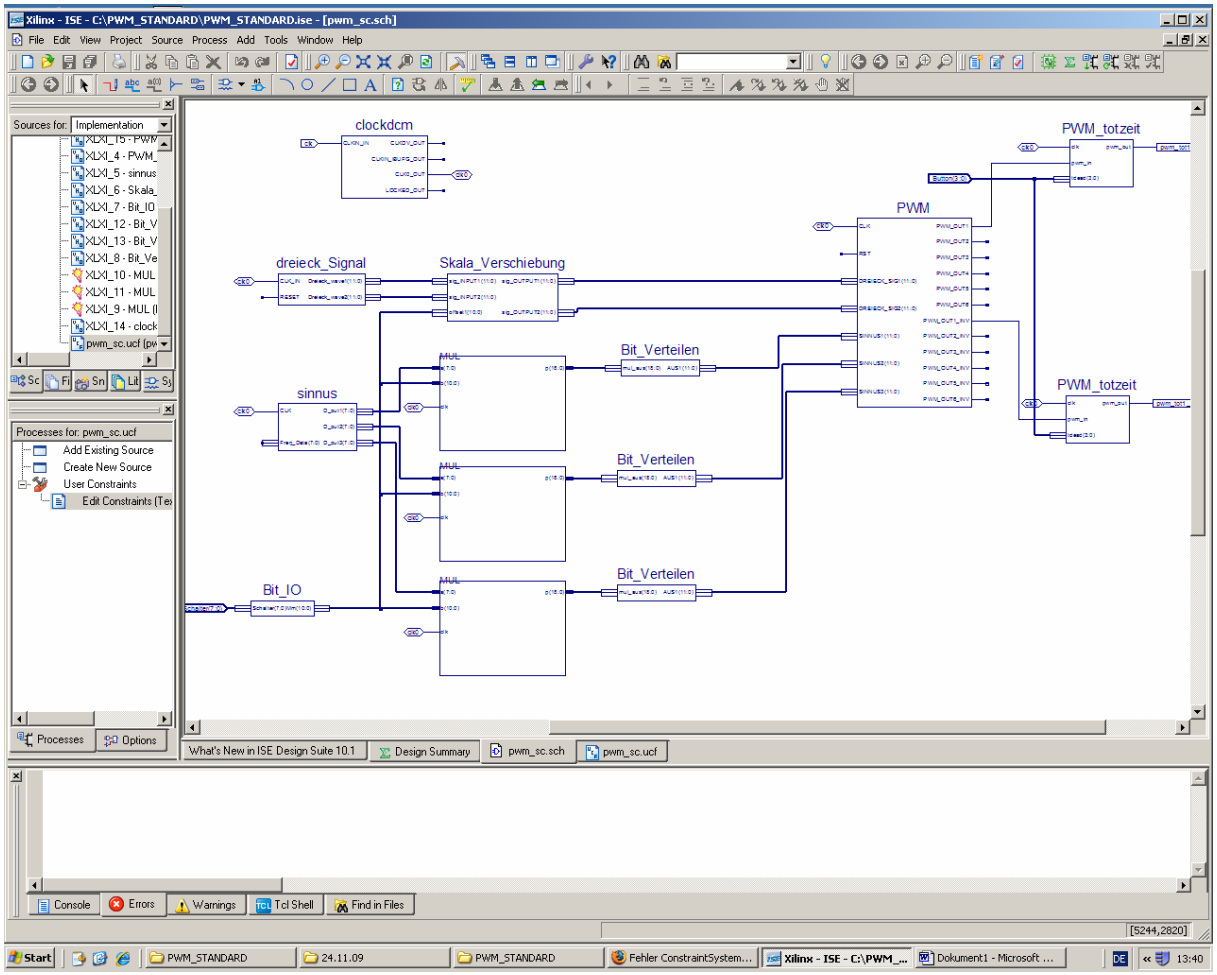
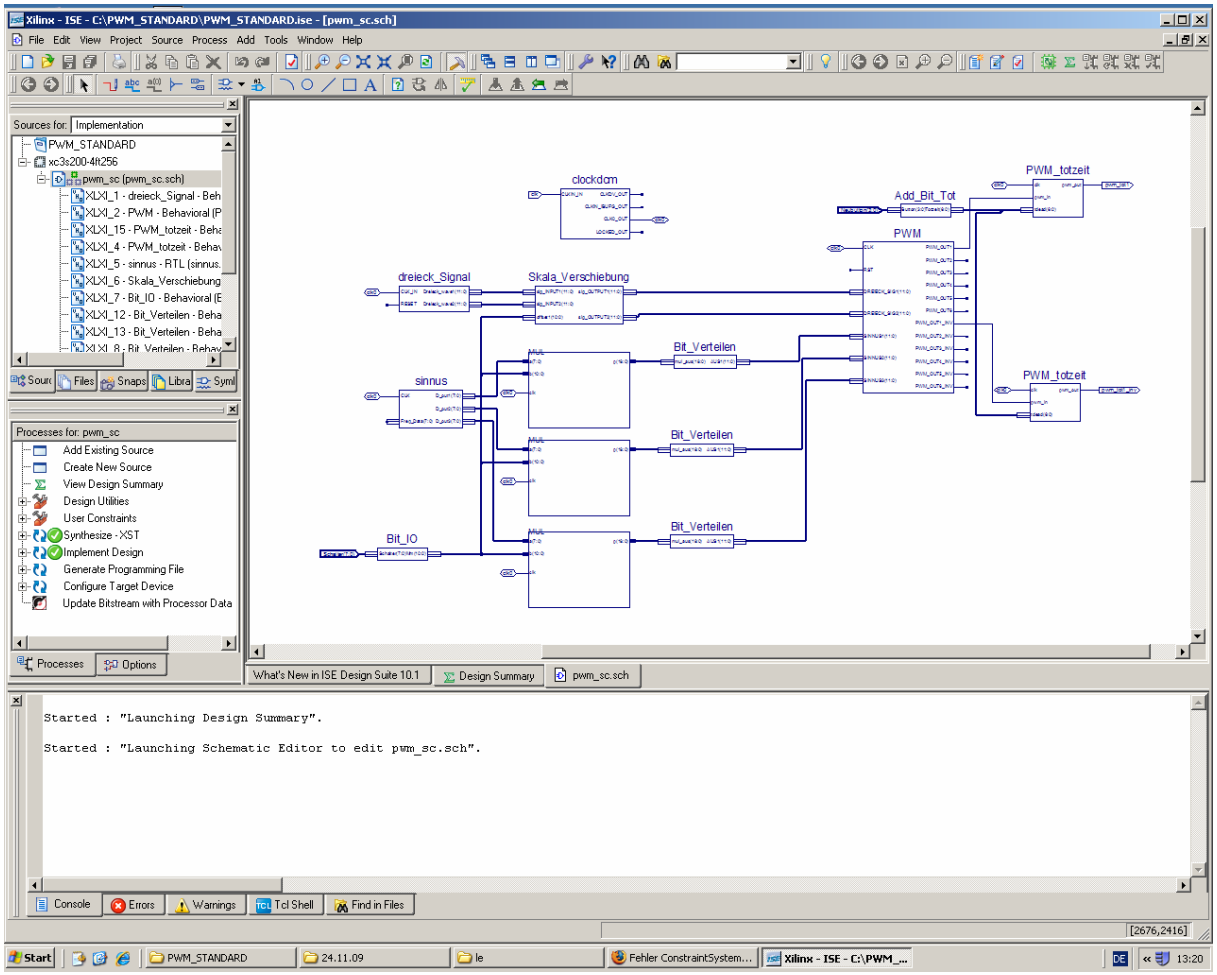

Xilinx - ISE - C:\PWM_STANDARD\PWM_STANDARD.ise - [pwm_sc.sch]
File Edit View Project Source Process Add Tools Window Help
clockdcm
PWM_totzeit
PWM
dreieck_Signal
Skala_Verschiebung
Bit_Verteilen
Bit_Verteilen
Bit_Verteilen
sinnus
Bit_IO
PWM_totzeit
Add Existing Source
Create New Source
User Constraints
Processes
Options
What's New in ISE Design Suite 10.1
Design Summary
pwm_sc.sch
pwm_sc.ucf
Console
Errors
Warnings
Tcl Shell
Find in Files
Start
PWM_STANDARD
24.11.09
PWM_STANDARD
Fehler ConstraintSystem...
Xilinx - ISE - C:\PWM_...
Dokument1 - Microsoft ...
13:40


Xilinx - ISE - C:\PWM_STANDARD\PWM_STANDARD.ise - [pwm_sc.sch]
File Edit View Project Source Process Add Tools Window Help
Sources for: Implementation
PWM_STANDARD
xc3s200-4ft256
pwm_sc (pwm_sc.sch)
Processes for: pwm_sc
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Update Bitstream with Processor Data
clockdom
dreieck_Signal
Skala_Verschiebung
sinnus
Bit_IO
Bit_Verteilen
Bit_Verteilen
Bit_Verteilen
Add_Bit_Tot
PWM
PWM_totzeit
PWM_totzeit
What's New in ISE Design Suite 10.1
Design Summary
pwm_sc.sch
Started : "Launching Design Summary".
Started : "Launching Schematic Editor to edit pwm_sc.sch".
Console
Errors
Warnings
Tcl Shell
Find in Files
[2676,2416]
Start
PWM_STANDARD
24.11.09
le
Fehler ConstraintSystem...
Xilinx - ISE - C:\PWM_...
13:20

pwm_sc.ucf

```
#PACE: Start of Constraints generated by PACE

#PACE: Start of PACE I/O Pin Assignments
NET "clk"  LOC = "T9"  ;
NET "pwm_tot1"  LOC = "D5"  ;
NET "pwm_tot1_inv"  LOC = "D7"  ;
NET "Schalter<0>"  LOC = "F12"  ;
NET "Schalter<1>"  LOC = "G12"  ;
NET "Schalter<2>"  LOC = "H14"  ;
NET "Schalter<3>"  LOC = "H13"  ;
NET "Schalter<4>"  LOC = "J14"  ;
NET "Schalter<5>"  LOC = "J13"  ;
NET "Schalter<6>"  LOC = "K14"  ;
NET "Schalter<7>"  LOC = "K13"  ;
NET "XLXN_37<0>"  LOC = "M13"  ;
NET "XLXN_37<1>"  LOC = "M14"  ;
NET "XLXN_37<2>"  LOC = "L13"  ;
NET "XLXN_37<3>"  LOC = "L14"  ;

#PACE: Start of PACE Area Constraints

#PACE: Start of PACE Prohibit Constraints

#PACE: End of Constraints generated by PACE
```

Nach dem Erlöschen XLXL_37 dann re-implementieren.
Dann funktioniert

pwm_sc.ucf

```
#PACE: Start of Constraints generated by PACE

#PACE: Start of PACE I/O Pin Assignments
NET "Button<0>"  LOC = "M13"  ;
NET "Button<1>"  LOC = "M14"  ;
NET "Button<2>"  LOC = "L13"  ;
NET "Button<3>"  LOC = "L14"  ;
NET "clk"  LOC = "T9"  ;
NET "pwm_tot1"  LOC = "D5"  ;
NET "pwm_tot1_inv"  LOC = "D7"  ;
NET "Schalter<0>"  LOC = "F12"  ;
NET "Schalter<1>"  LOC = "G12"  ;
NET "Schalter<2>"  LOC = "H14"  ;
NET "Schalter<3>"  LOC = "H13"  ;
NET "Schalter<4>"  LOC = "J14"  ;
NET "Schalter<5>"  LOC = "J13"  ;
NET "Schalter<6>"  LOC = "K14"  ;
NET "Schalter<7>"  LOC = "K13"  ;
```

#PACE: Start of PACE Area Constraints

#PACE: Start of PACE Prohibit Constraints

#PACE: End of Constraints generated by PACE

Dritte Mal,wenn es neue Block gibt ,nicht pwm_sc wird erzeugt sondern Add_Bit_Tot wird erzeugt

Ich hab alle NET "Button<0>" LOC = "M13" ;
NET "Button<1>" LOC = "M14" ;
NET "Button<2>" LOC = "L13" ;
NET "Button<3>" LOC = "L14" ; erlöscht
Aber dann nicht funktioniert

pwm_sc.ucf

#PACE: Start of Constraints generated by PACE

#PACE: Start of PACE I/O Pin Assignments

NET "clk" LOC = "T9" ;
NET "pwm_tot1" LOC = "D5" ;
NET "pwm_tot1_inv" LOC = "D7" ;
NET "Schalter<0>" LOC = "F12" ;
NET "Schalter<1>" LOC = "G12" ;
NET "Schalter<2>" LOC = "H14" ;
NET "Schalter<3>" LOC = "H13" ;
NET "Schalter<4>" LOC = "J14" ;
NET "Schalter<5>" LOC = "J13" ;
NET "Schalter<6>" LOC = "K14" ;
NET "Schalter<7>" LOC = "K13" ;

#PACE: Start of PACE Area Constraints

#PACE: Start of PACE Prohibit Constraints

#PACE: End of Constraints generated by PACE

Reading design: Add_Bit_Tot.prj

==========
======

```
*                     HDL Compilation                     *
=========================================================================
======
Compiling vhdl file "C:/PWM_STANDARD/Add_Bit_Tot.vhd" in Library work.
Architecture behavioral of Entity add_bit_tot is up to date.

=========================================================================
======
*                  Design Hierarchy Analysis                  *
=========================================================================
======
Analyzing hierarchy for entity <Add_Bit_Tot> in library <work> (architecture <behavioral>).


=========================================================================
======
*                     HDL Analysis                     *
=========================================================================
======
Analyzing Entity <Add_Bit_Tot> in library <work> (Architecture <behavioral>).
Entity <Add_Bit_Tot> analyzed. Unit <Add_Bit_Tot> generated.


=========================================================================
======
*                     HDL Synthesis                     *
=========================================================================
======

Performing bidirectional port resolution...

Synthesizing Unit <Add_Bit_Tot>.
    Related source file is "C:/PWM_STANDARD/Add_Bit_Tot.vhd".
Unit <Add_Bit_Tot> synthesized.


=========================================================================
======
HDL Synthesis Report

Found no macro
=========================================================================
======

=========================================================================
======
*                  Advanced HDL Synthesis                  *
=========================================================================
======
```

Loading device for application Rf_Device from file '3s200.nph' in environment C:\Xilinx\10.1\ISE.

===
Advanced HDL Synthesis Report

Found no macro
===

===
*   Low Level Synthesis   *
===

Optimizing unit <Add_Bit_Tot> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block Add_Bit_Tot, actual ratio is 0.

Final Macro Processing ...

===
Final Register Report

Found no macro
===

===
*   Partition Report   *
===

Partition Implementation Status

  No Partitions were found in this design.

===
*   Final Report   *
===

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -4

  Minimum period: No path found
  Minimum input arrival time before clock: No path found
  Maximum output required time after clock: No path found
  Maximum combinational path delay: 7.266ns

==========
======

Process "Synthesis" completed successfully

Command Line: C:\Xilinx\10.1\ISE\bin\nt\unwrapped\ngdbuild.exe -ise C:/PWM_STANDARD/PWM_STANDARD.ise -intstyle ise -dd _ngo -nt timestamp -i -p xc3s200-ft256-4 Add_Bit_Tot.ngc Add_Bit_Tot.ngd

Reading NGO file "C:/PWM_STANDARD/Add_Bit_Tot.ngc" ...
Reading in constraint information from 'pwm_sc.ucf'...
Gathering constraint information from source properties...
Done.

Resolving constraint associations...
Checking Constraint Associations...
ERROR:ConstraintSystem:59 - Constraint <NET "clk" LOC = "T9" ;>
  [pwm_sc.ucf(8)]: NET "clk" not found. Please verify that:
  1. The specified design element actually exists in the original design.
  2. The specified object is spelled correctly in the constraint source file.

ERROR:ConstraintSystem:59 - Constraint <NET "pwm_tot1" LOC = "D5" ;>
  [pwm_sc.ucf(9)]: NET "pwm_tot1" not found. Please verify that:
  1. The specified design element actually exists in the original design.
  2. The specified object is spelled correctly in the constraint source file.

ERROR:ConstraintSystem:59 - Constraint <NET "pwm_tot1_inv" LOC = "D7" ;>
  [pwm_sc.ucf(10)]: NET "pwm_tot1_inv" not found. Please verify that:
  1. The specified design element actually exists in the original design.
  2. The specified object is spelled correctly in the constraint source file.

ERROR:ConstraintSystem:59 - Constraint <NET "Schalter<0>" LOC = "F12" ;>
  [pwm_sc.ucf(11)]: NET "Schalter<0>" not found. Please verify that:

1. The specified design element actually exists in the original design.
2. The specified object is spelled correctly in the constraint source file.

ERROR:ConstraintSystem:59 - Constraint <NET "Schalter<1>" LOC = "G12" ;>
[pwm_sc.ucf(12)]: NET "Schalter<1>" not found. Please verify that:
1. The specified design element actually exists in the original design.
2. The specified object is spelled correctly in the constraint source file.

ERROR:ConstraintSystem:59 - Constraint <NET "Schalter<2>" LOC = "H14" ;>
[pwm_sc.ucf(13)]: NET "Schalter<2>" not found. Please verify that:
1. The specified design element actually exists in the original design.
2. The specified object is spelled correctly in the constraint source file.

ERROR:ConstraintSystem:59 - Constraint <NET "Schalter<3>" LOC = "H13" ;>
[pwm_sc.ucf(14)]: NET "Schalter<3>" not found. Please verify that:
1. The specified design element actually exists in the original design.
2. The specified object is spelled correctly in the constraint source file.

ERROR:ConstraintSystem:59 - Constraint <NET "Schalter<4>" LOC = "J14" ;>
[pwm_sc.ucf(15)]: NET "Schalter<4>" not found. Please verify that:
1. The specified design element actually exists in the original design.
2. The specified object is spelled correctly in the constraint source file.

ERROR:ConstraintSystem:59 - Constraint <NET "Schalter<5>" LOC = "J13" ;>
[pwm_sc.ucf(16)]: NET "Schalter<5>" not found. Please verify that:
1. The specified design element actually exists in the original design.
2. The specified object is spelled correctly in the constraint source file.

ERROR:ConstraintSystem:59 - Constraint <NET "Schalter<6>" LOC = "K14" ;>
[pwm_sc.ucf(17)]: NET "Schalter<6>" not found. Please verify that:
1. The specified design element actually exists in the original design.
2. The specified object is spelled correctly in the constraint source file.

ERROR:ConstraintSystem:59 - Constraint <NET "Schalter<7>" LOC = "K13" ;>
[pwm_sc.ucf(18)]: NET "Schalter<7>" not found. Please verify that:
1. The specified design element actually exists in the original design.
2. The specified object is spelled correctly in the constraint source file.

Done...
Checking Partitions ...

Checking expanded design ...

Partition Implementation Status

No Partitions were found in this design.

NGDBUILD Design Results Summary:

Number of errors: 11
Number of warnings: 0

One or more errors were found during NGDBUILD. No NGD file will be written.

Writing NGDBUILD log file "Add_Bit_Tot.bld"...

Process "Translate" failed