Terawins, Inc.

Release
Version 1.05

June 26, 2008

T302B Portable Multimedia Processor

1 Introduction

1.1 Features

n 32-bit RISC CPU up to 120Mhz with MMU
- System control
- Audio/Voice encoding and decoding

n Built-in hardwired JPEG, Motion-JPEG decoder
- Baseline support. YCbCr-444, YcbCr-422, YcbCr-420, Grey-level
- Decoding speed up to 16 M pixels/sec
- Hardwired image rotation
- Frequency domain first-level scaling down

n LCD processor with Scalar, OSD, TCON, DAC, DC/DC and LED/CCFL controller
- Direct TCON interface to analog panel and digital panel (T302BT)
- Luminance Enhancement (BLE, Contrast, Peaking, DLTi and Brightness adjustment)
- Chroma Enhancement (DCTi, Saturation and Hue adjustment)
- Scaler supports 2-D adaptive intra-field de-interlacer and non-linear 16:9 aspect ration.
- Programmable Timing controller
- 256-entry TBL Gamma correction for panel compensation
- Integration TFT-LCD backlight inverter drive unit supports CCFL/LED typed backlight
- 8k-word OSD(Pattern-Filled background) memory and 114+ built-in font
- Graphic OSD memory for designing UI usage and its size depends on customer design request.

n On-chip Video DAC for TV-out display

n On-chip audio DAC for playback

n On-chip SAR

n USB 2.0 high speed OTG controller up to 480 Mb/s

n Memory subsystem

- NOR flash controller – both SPI/PPI support
- NAND flash controller – support on-board NAND for storage
- SDR-SDRAM controller – 16-bit data bus up to size of 256MB

n Flash card interfaces controllers
- SD/MMC
- MS/MS Pro
- xD/SM
- CF (T302BC, T302BI)

n Descriptor-based DMA engine
- Memory to Memory copy
- Memory to IO device, IO device to Memory
- IO device to IO device transfer

n On-chip peripherals
- 2-wired serial bus interface
- EJTAG interface
- UART
- GPIOs
- Interrupt controller, System Timer, Watch-Dog Timer

n System (Power) Management Unit
- Dynamic Clock frequency adjustment to save power consumption
- Operation, Suspend, Shutdown mode

n Built-in Real-Time Clock (RTC) for alarm function with battery

n Package Type and Voltage

- LQFP 144 pin (T302BC, T302BI, T302BT, T302BV)
- LQFP 128 pin (T302BA, T302BZ)
- Voltage : 3.3V/1.8V

1.2 General Description

The T302B is a highly integrated All-in-one Digital Photo Frame Processor that provides major cost saving solution for the Digital Photo Frame applications. T302B has built-in high performance 32bit MCU, JPEG/MJPEG decoder, flash card reader, USB 2.0 OTG, TCON, triple DACs, Memory and TFT-LCD Backlight controller. T302B could direct support most typed of analog and digital panels with refine and adjustable image quality. T302B builds in Terawins high quality video processor engine and is easy to make the JPEG/MJPEG image quality better.

1.3 Applications

1. Digital Photo Frame
2. Multimedia portable application

1.4 System Architecture

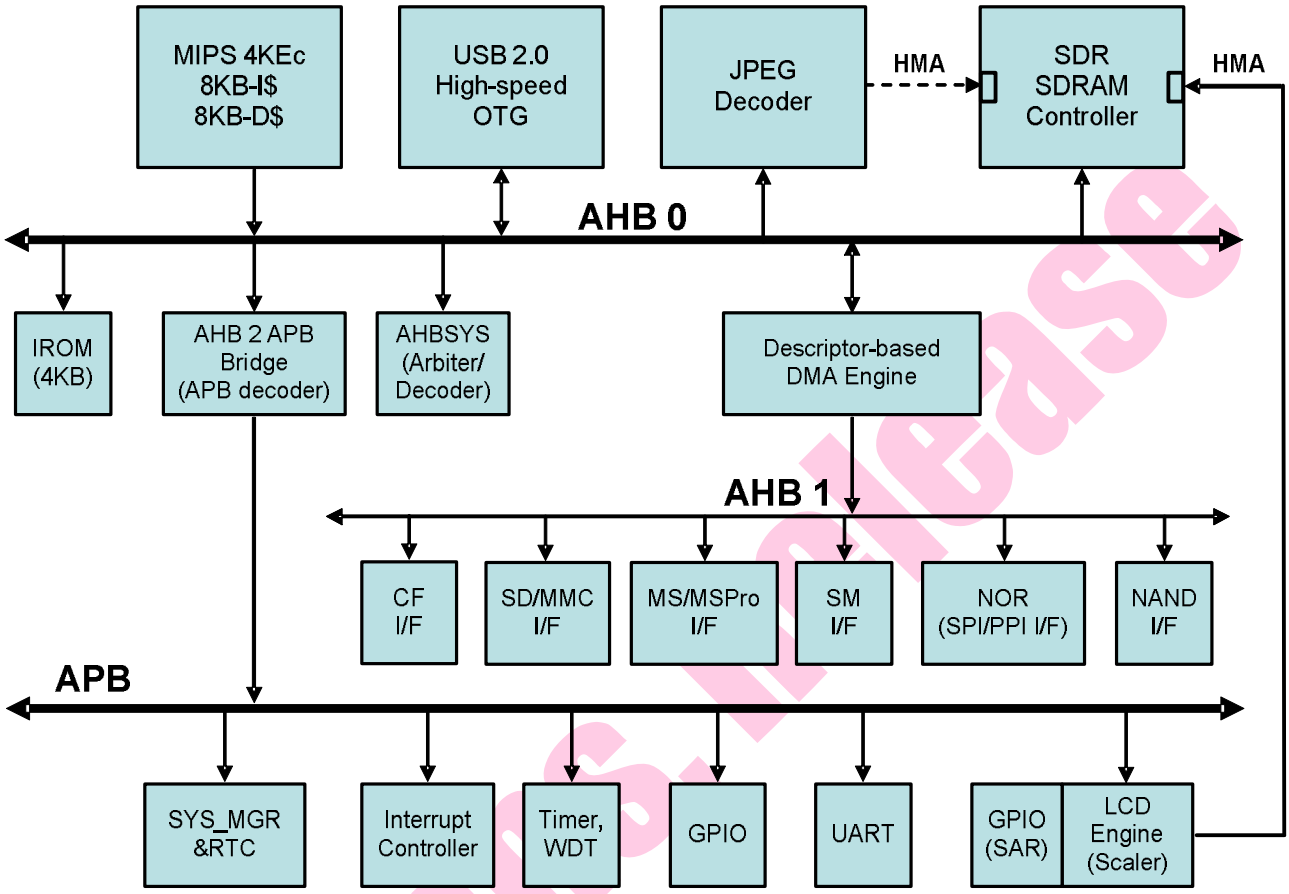


Figure 1-1 System Architecture

1.5 System Configurations

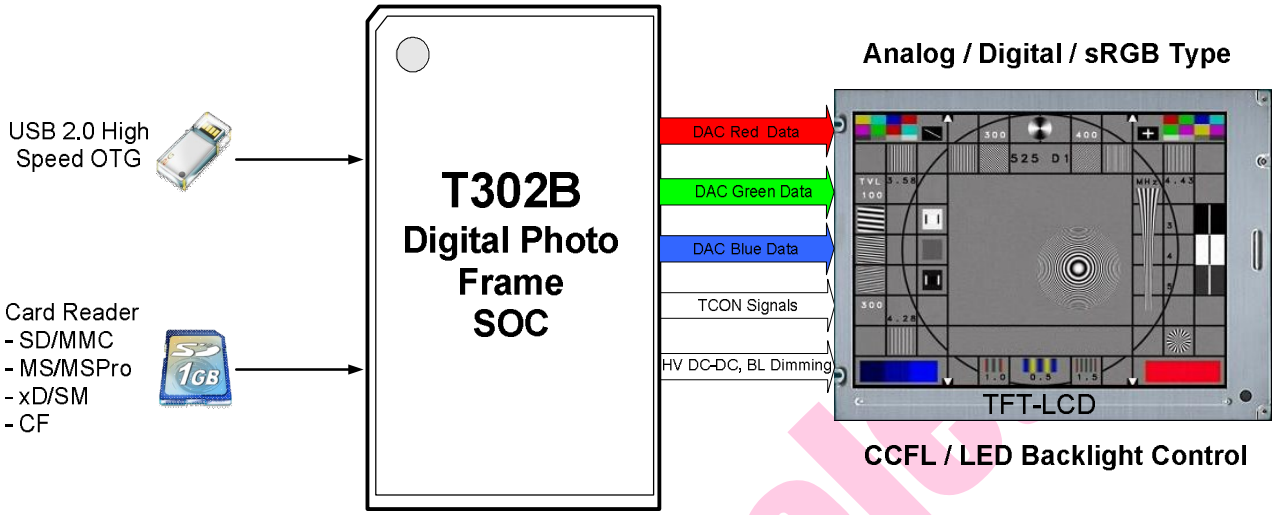


Figure 1-2 System Configuration

1.6 Pinout vs. features

Table 1-1 Pinout vs. Features

T302B	144 pin					128 pin	
	T302BC	T302BI	T302BD	T302BT	T302BV	T302BA	T302BZ
JPEG/MJPEG decode	V	V	V	V	V	V	V
MP3 decode	V	V	V	V	V	V	V
Panel type support	Analog	Analog/ sRGB	Analog/ sRGB	**Digital**	**Digital**	Analog	Analog
Backlight control	CCFL/LED	CCFL/LED	CCFL/LED	CCFL/LED	CCFL/LED	LED	LED
SD/MMC/xD/SM/MS/MSPro	V	V	V	V	V	V	V
CF	V	V	V				
USB 2.0 OTG	V	V	V	V	V	V	V
NAND/NOR(PPI/SPI) Boot	V	V	V	V	V	V	V
SDRAM (8/16MB)	V	V	V	V	V	V	V
Internal Audio DAC	V			V		V	
Audio I^2S I/F		V	V		V		V

1.7 Pinout Diagram – T302BC (144pin Analog panel, CF, CCFL/LED backlight support with internal audio DAC)

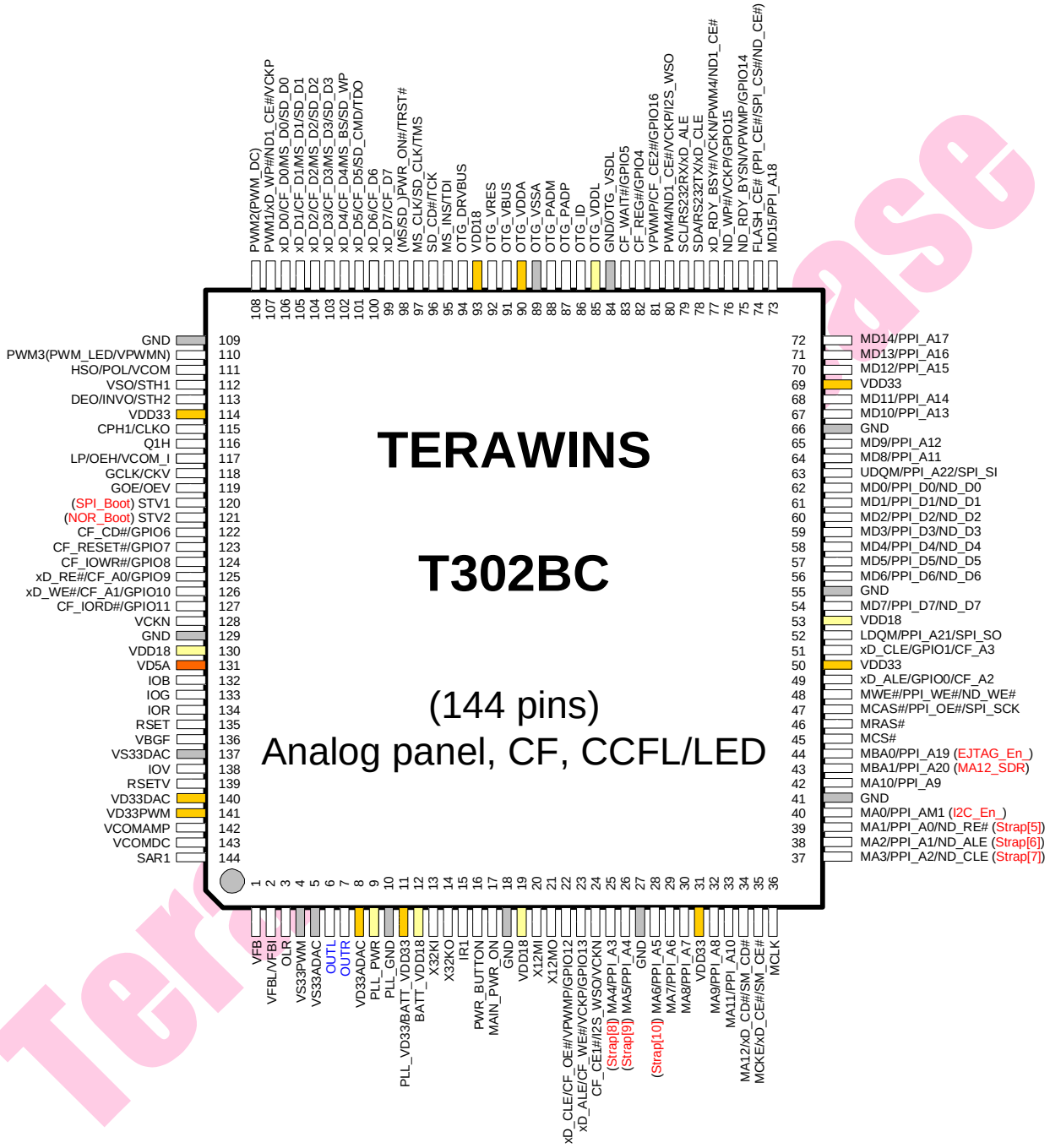


Figure 1-3 Pinout Diagram

T302B for Analog Panel, CF, CCFL/LED backlight 144pin Version

1.8 Pin Description – T302BC (144pin)

Table 1-2 Pin Description

Pin Name	Type	Functionality Description (T302BC)	Pin #
System Management Interface			
X32KI	I	32.768KHz crystal input	13
X32KO	O	32.768KHz crystal output	14
IR1	I	IR input	15
PWR_BUTTON	I	Power Up button pressed sensing signal	16
MAIN_PWR_ON	O	Signal to turn on main power	17
USB 2.0 OTG Interface			
OTG_ID	I	ID pin	86
OTG_PADP	IO	D+	87
OTG_PADM	IO	D-	88
OTG_VBUS	O	VBUS	91
OTG_VRES	I	Connect to Resistor with 8.2Kohm	92
OTG_DRVBUS	O	Signal to turn-on Vbus to provide power USB device (used in Host mode)	94
SDRAM Memory Interface			
MCLK	O	SDRAM clock	36
MCS#	O	SDRAM CS#	45
MRAS#	O	SDRAM RAS#	46
MCAS#/PPI_OE#/SPI_SCK	O	SDRAM CAS#	47
MWE#/PPI_WE#/ND_WE#	O	SDRAM WE#	48
MBA1/PPI_A20 (MA12_SDR)	IO	SDRAM BA1	43
MBA0/PPI_A19 (EJTAG_En_)	IO	SDRAM BA0	44
MA11/PPI_A10	O	SDRAM MA11	33
MA10/PPI_A9	O	SDRAM MA10	42
MA9/PPI_A8	O	SDRAM MA9	32
MA8/PPI_A7	O	SDRAM MA8	30
MA7/PPI_A6	O	SDRAM MA7	29
MA6/PPI_A5	O	SDRAM MA6	28
MA5/PPI_A4	O	SDRAM MA5	26
MA4/PPI_A3	O	SDRAM MA4	25
MA3/PPI_A2/ND_CLE (Strap[7])	IO	SDRAM MA3	37
MA2/PPI_A1/ND_ALE (Strap[6])	IO	SDRAM MA2	38
MA1/PPI_A0/ND_RE# (Strap[5])	IO	SDRAM MA1	39
MA0/PPI_AM1 (I2C_En_)	IO	SDRAM MA0	40
UDQM/PPI_A22/SPI_SI	O	SDRAM DQM for D15~D8	63
MD15/PPI_A18	IO	SDRAM D15	73
MD14/PPI_A17	IO	SDRAM D14	72
MD13/PPI_A16	IO	SDRAM D13	71
MD12/PPI_A15	IO	SDRAM D12	70
MD11/PPI_A14	IO	SDRAM D11	68
MD10/PPI_A13	IO	SDRAM D10	67
MD9/PPI_A12	IO	SDRAM D9	65
MD8/PPI_A11	IO	SDRAM D8	64
LDQM/PPI_A21/SPI_SO	O	SDRAM DQM for D7~D0	52
MD7/PPI_D7/ND_D7	IO	SDRAM D7	54

Pin Name	Type	Functionality Description (T302BC)	Pin #
MD6/PPI_D6/ND_D6	IO	SDRAM D6	56
MD5/PPI_D5/ND_D5	IO	SDRAM D5	57
MD4/PPI_D4/ND_D4	IO	SDRAM D4	58
MD3/PPI_D3/ND_D3	IO	SDRAM D3	59
MD2/PPI_D2/ND_D2	IO	SDRAM D2	60
MD1/PPI_D1/ND_D1	IO	SDRAM D1	61
MD0/PPI_D0/ND_D0	IO	SDRAM D0	62
SPI NOR Flash Interface (Note: SPI, PPI NOR and NAND are mutually exclusive on oard)			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	SPI NOR Chip Enable	74
MCAS#/PPI_OE#/SPI_SCK	O	SPI NOR Clock	47
LDQM/PPI_A21/SPI_SO	O	SPI Serial Data Output (to input of the flash)	52
UDQM/PPI_A22/SPI_SI	I	SPI Serial Data Input (from output of the flash)	63
PPI NOR Flash Interface			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	PPI NOR Chip Enable	74
MCAS#/PPI_OE#/SPI_SCK	O	PPI NOR OE#	47
MWE#/PPI_WE#/ND_WE#	O	PPI NOR WE#	48
UDQM/PPI_A22/SPI_SI	O	PPI NOR A22	63
LDQM/PPI_A21/SPI_SO	O	PPI NOR A21	52
MBA1/PPI_A20 (MA12_SDR)	IO	PPI NOR A20	43
MBA0/PPI_A19 (EJTAG_En_)	IO	PPI NOR A19	44
MD15/PPI_A18	IO	PPI NOR A18	73
MD14/PPI_A17	IO	PPI NOR A17	72
MD13/PPI_A16	IO	PPI NOR A16	71
MD12/PPI_A15	IO	PPI NOR A15	70
MD11/PPI_A14	IO	PPI NOR A14	68
MD10/PPI_A13	IO	PPI NOR A13	67
MD9/PPI_A12	IO	PPI NOR A12	65
MD8/PPI_A11	IO	PPI NOR A11	64
MA11/PPI_A10	O	PPI NOR A10	33
MA10/PPI_A9	O	PPI NOR A9	42
MA9/PPI_A8	O	PPI NOR A8	32
MA8/PPI_A7	O	PPI NOR A7	30
MA7/PPI_A6	O	PPI NOR A6	29
MA6/PPI_A5	O	PPI NOR A5	28
MA5/PPI_A4	O	PPI NOR A4	26
MA4/PPI_A3	O	PPI NOR A3	25
MA3/PPI_A2/ND_CLE (Strap[7])	IO	PPI NOR A2	37
MA2/PPI_A1/ND_ALE (Strap[6])	IO	PPI NOR A1	38
MA1/PPI_A0/ND_RE# (Strap[5])	IO	PPI NOR A0	39
MA0/PPI_AM1 (I2C_En_)	IO	PPI NOR A-1	40
MD7/PPI_D7/ND_D7	IO	PPI NOR D7	54
MD6/PPI_D6/ND_D6	IO	PPI NOR D6	56
MD5/PPI_D5/ND_D5	IO	PPI NOR D5	57
MD4/PPI_D4/ND_D4	IO	PPI NOR D4	58
MD3/PPI_D3/ND_D3	IO	PPI NOR D3	59
MD2/PPI_D2/ND_D2	IO	PPI NOR D2	60
MD1/PPI_D1/ND_D1	IO	PPI NOR D1	61
MD0/PPI_D0/ND_D0	IO	PPI NOR D0	62
NAND Flash Interface			

Pin Name	Type	Functionality Description (T302BC)	Pin #
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	NAND Chip Enable	74
MA3/PPI_A2/ND_CLE (Strap[7])	IO	NAND_CLE	37
MA2/PPI_A1/ND_ALE (Strap[6])	IO	NAND_ALE	38
MA1/PPI_A0/ND_RE# (Strap[5])	IO	NAND_RE#	39
MWE#/PPI_WE#/ND_WE#	O	NAND_WE#	48
ND_RDY_BYSN/VPWMP/GPIO14/xD_RE#	I	NAND_RDY_BSY#	75
ND_WP#/VCKP/GPIO15/xD_WE#	O	NAND_WP#	76
MD7/PPI_D7/ND_D7	IO	NAND_D7	54
MD6/PPI_D6/ND_D6	IO	NAND_D6	56
MD5/PPI_D5/ND_D5	IO	NAND_D5	57
MD4/PPI_D4/ND_D4	IO	NAND_D4	58
MD3/PPI_D3/ND_D3	IO	NAND_D3	59
MD2/PPI_D2/ND_D2	IO	NAND_D2	60
MD1/PPI_D1/ND_D1	IO	NAND_D1	61
MD0/PPI_D0/ND_D0	IO	NAND_D0	62
UART Interface			
SDA/RS232TX/xD_CLE	O	UART_TX	78
SCL/RS232RX/xD_ALE	I	UART_RX	79
ETJAG Interface			
SD_CD#/TCK	I	EJTAG_TCK	96
MS_CLK/SD_D1/CF_RESET_/TMS	I	EJTAG_TMS	97
MS_INS/TDI	I	EJTAG_TDI	95
(MS/SD/CF_)PWR_ON#/TRST#	I	EJTAG_TRST#	98
xD_D5/CF_D5/SD_CMD/TDO	O	EJTAG_TDO	101
Flash Card Power Interface			
(MS/SD/CF_)PWR_ON#/TRST#	O	Power On/Off for Flash card. (0: ON, 1: Off)	98
SD/MMC Card Interface			
SD_CD#/TCK	I	SD Card Detect	96
MS_CLK/SD_CLK/TMS	O	SD CLK	97
xD_D5/CF_D5/SD_CMD/TDO	IO	SD CMD	101
xD_D3/CF_D3/MS_D3/SD_D3	IO	SD D3	103
xD_D2/CF_D2/MS_D2/SD_D2	IO	SD D2	104
xD_D1/CF_D1/MS_D1/SD_D1	IO	SD D1	105
xD_D0/CF_D0/MS_D0/SD_D0	IO	SD D0	106
xD_D4/CF_D4/MS_BS/SD_WP	I	SD WP	102
MS/MS Pro Card Interface			
MS_INS/TDI	I	MS Card Insert	95
MS_CLK/SD_CLK/TMS	O	MS CLK	97
xD_D4/CF_D4/MS_BS/SD_WP	O	MS BS	102
xD_D3/CF_D3/MS_D3/SD_D3	IO	MS D3	103
xD_D2/CF_D2/MS_D2/SD_D2	IO	MS D2	104
xD_D1/CF_D1/MS_D1/SD_D1	IO	MS D1	105
xD_D0/CF_D0/MS_D0/SD_D0	IO	MS D0	106
XD/SM Card Interface			
MA12/xD_CD#/SM_CD#	I	XD/SM Card Detect	34
MCKE/xD_CE#/SM_CE#	O	XD/SM Chip Enable	35
xD_RDY_BSY#/CF_RDY_BSY#/ VCKN/PWM4/ND1_CE#	I	XD/SM RDY_BSY#	77

Pin Name	Type	Functionality Description (T302BC)	Pin #
xD_ALE/GPIO0/CF_A2	O	XD/SM ALE	49
xD_CLE/GPIO1/CF_A3	O	XD/SM CLE	51
PWM1/xD_WP#/ND1_CE#/VCKP	O	XD/SM WP#	107
xD_RE#/CF_A0/GPIO9	O	XD/SM RE#	125
xD_WE#/CF_A1/GPIO10	O	XD/SM WE#	126
xD_D7/CF_D7	IO	XD/SM D7	99
xD_D6/CF_D6	IO	XD/SM D6	100
xD_D5/CF_D5/SD_CMD/TDO	IO	XD/SM D5	101
xD_D4/CF_D4/MS_BS/SD_WP	IO	XD/SM D4	102
xD_D3/CF_D3/MS_D3/SD_D3	IO	XD/SM D3	103
xD_D2/CF_D2/MS_D2/SD_D2	IO	XD/SM D2	104
xD_D1/CF_D1/MS_D1/SD_D1	IO	XD/SM D1	105
xD_D0/CF_D0/MS_D0/SD_D0	IO	XD/SM D0	106
CF Card Interface			
CF_CD#/GPIO6	I	CF Card Detect	122
CF_RESET#/GPIO7	O	CF Reset	123
CF_CE1#/I2S_WSO/VCKN	O	CF CE1	24
VPWMP/CF_CE2#/GPIO16	O	CF CE2	102
xD_ALE/CF_WE#/VCKP/GPIO13	O	CF WE#	23
xD_CLE/CF_OE#/VPWMP/GPIO12	O	CF OE#	22
CF_REG#/GPIO4	O	CF REG#	82
CF_IOWR#/GPIO8	O	CF IOWR#	124
CF_IORD#/GPIO11	O	CF IORD#	127
CF_WAIT#/GPIO5	IO	CF WAIT#	83
xD_RDY_BSY#/VCKN/PWM4/ND1_CE#	I	CF RDY_BSY#	77
xD_CLE/GPIO1/CF_A3	O	CF A3	51
xD_ALE/GPIO0/CF_A2	O	CF A2	49
xD_WE#/CF_A1/GPIO10	O	CF A1	126
xD_RE#/CF_A0/GPIO9	O	CF A0	125
xD_D7/CF_D7	IO	CF D7	99
xD_D6/CF_D6	IO	CF D6	100
xD_D5/CF_D5/SD_CMD/TDO	IO	CF D5	101
xD_D4/CF_D4/MS_BS/SD_WP	IO	CF D4	102
xD_D3/CF_D3/MS_D3/SD_D3	IO	CF D3	103
xD_D2/CF_D2/MS_D2/SD_D2	IO	CF D2	104
xD_D1/CF_D1/MS_D1/SD_D1	IO	CF D1	105
xD_D0/CF_D0/MS_D0/SD_D0	IO	CF D0	106
I2C Interface			
SDA/RS232TX/xD_CLE	IO	I2C_SDA	78
SCL/RS232RX/xD_ALE	IO	I2C_SCL	79
LCD TCON			
HSO/POL/VCOM	O	Hsync to panel, or Horizontal Polarity output or VCOM	111
VSO/STH1	O	Vsync to panel or Horizontal Start Pulse 1 Signal	112
DEO/INVO/STH2	O	Horizontal Output Data enable, or INVO or Horizontal Start Pulse 2 Signal	113
CPH1/CLKO	O	Clocks to panel	115
Q1H	O	Panel polarity control	116
LP/OEH/VCOM_I	O	Latch pulse for column driver	117

Pin Name	Type	Functionality Description (T302BC)	Pin #
GCLK/CKV	O	Gate driver clock	118
GOE/OEV	O	Gate driver output enable	119
STV1 (SPI_Boot)	O	Gate driver start pulse 1	120
STV2 (NOR_Boot)	O	Gate driver start pulse 2	121
LCD Analog Output and Panel Backlight control			
IOB	O	B-channel analog output	132
IOG	O	G-channel analog output	133
IOR	O	R-channel analog output	134
RSET	I	DAC reference current adjust	135
VBGF	I	DAC voltage reference output	136
IOV	O	Composite Video Encoder output	138
RSETV	I	DAC reference current adjust for TV out	139
VCOMAMP	O	VCOM Amplify	142
VCOMDC	O	VCOM DC	143
VFB	I	Feedback of Lamp current (DC2DC)	1
VFBI	I	Feedback of Lamp current (LED or CCFL)	2
OLR	I	Open Lamp protection (CCFL)	3
PWM2 (PWM_DC)	O	PWM output for DC2DC	108
PWM3 (PWM_LED or VPWMN)	O	PWM output for LED or VPWMN for CCFL	110
Misc.			
X12MI	I	12 MHz crystal input	20
X12MO	O	12 MHz crystal output	21
SAR1	I	SARADC for keypads sense	144
PWM4/ND1_CE#/VCKP/I2S_WSO	O	PWM4 output	80
DR5/VCKN	O	Digital PWM output: VCKN for CCFL, this VCKN works with PWM3(VPWMN) become a half bridge	128
OUTL/OUTR	O	Audio DAC output (Left/Right channel)	6,7
Analog Power			
VD33ADAC	P33A	Audio DAC power 3.3V	8
PLL_PWR	P18A	PLL power 1.8 V	9
OTG_VDDA	P33A	OTG power 3.3V	90
VD5A	P50A	Video DAC power 5.0V	131
VD33DAC	P33A	Video DAC power 3.3V	140
VD33PWM	P33A	PWM power 3.3V	141
Digital Power			
VDD33	P33	Digital IO power 3.3 V	31, 50, 69, 114
VDD18	P18	Core power 1.8V	19, 53, 93, 130
OTG_VDDL	P18	OTG VDDU 1.8V	85
Battery Power (3.3V)			
VDD33	P33	Battery Power for RTC IO, 3.3 V	11
Battery Power (1.8V)			
VDD18	P18	Battery Power for RTC core, 1.8V	12
GND (Analog)			
VS33PWM	GNDA	PWM Ground	4
VS33ADAC	GNDA	Audio DAC Ground	5

Pin Name	Type	Functionality Description (T302BC)	Pin #
PLL_GND	GNDA	PLL Ground	10
OTG_VSSA	GNDA	OTG VS33	89
VS33DAC	GNDA	Video DAC Ground	137
GND (Digital)			
GND	GND	Digital Ground	18, 27, 41, 55, 66, 84, 109, 129

Hardware Trapping Pins of T302BC

Pin #	Pin Symbol	Trapping Name	0 (pull-down) Determines :	1 (pull-up) Determines :
121	STV2/sD7 (NOR_Boot)	NOR_Boot	Boot from NAND	Boot from NOR
120	STV1/sD6 (SPI_Boot)	SPI_Boot	Boot from PPI NOR	Boot from SPI NOR
44	MBA0/PPI_A19 (EJTAG_En_)	EJTAG_En_	EJTAG Enable (no Flash Card allowed)	SD present
43	MBA1/PPI_A20 (MA12_SDR)	MA12_SDR	Pin-34/35 as xD/SM	Pin-34/35 as MA12/MCKE
40	MA0/PPI_AM1 (I2C_En_)	I2C_En_	Pin-78/79 as I2C func.	Pin-78/79 as UART func.
39	MA1/PPI_A0/ND_RE# (Strap[5])	Trap_5	Reserved	Reserved
38	MA2/PPI_A1/ND_ALE (Strap[6])	Trap_6	Reserved	Reserved
37	MA3/PPI_A2/ND_CLE (Strap[7])	Trap_7	Reserved	Reserved
25	MA4/PPI_A3 (Strap[8])	Trap_8		
26	MA5/PPI_A4 (Strap[9])	Trap_9	Trap[9:8] = 00: ND_CE0# (or the primary ND_CE0#) from FLASH_CE# (pin # 74) 01: Reserved 10: xD_RDY_BSY# (pin # 77) --- Reserved 11: PWM4 (pin # 80)	
28	MA6/PPI_A5 (Strap[10])	Trap_10	ND_CE1# at non-FLASH_CE# pin, and configured though firmware	ND_CE1# at FLASH_CE# pin

1.9 Pinout Diagram – T302BI (144pin Analog panel, CF, CCFL/LED backlight support with audio I²S I/F)

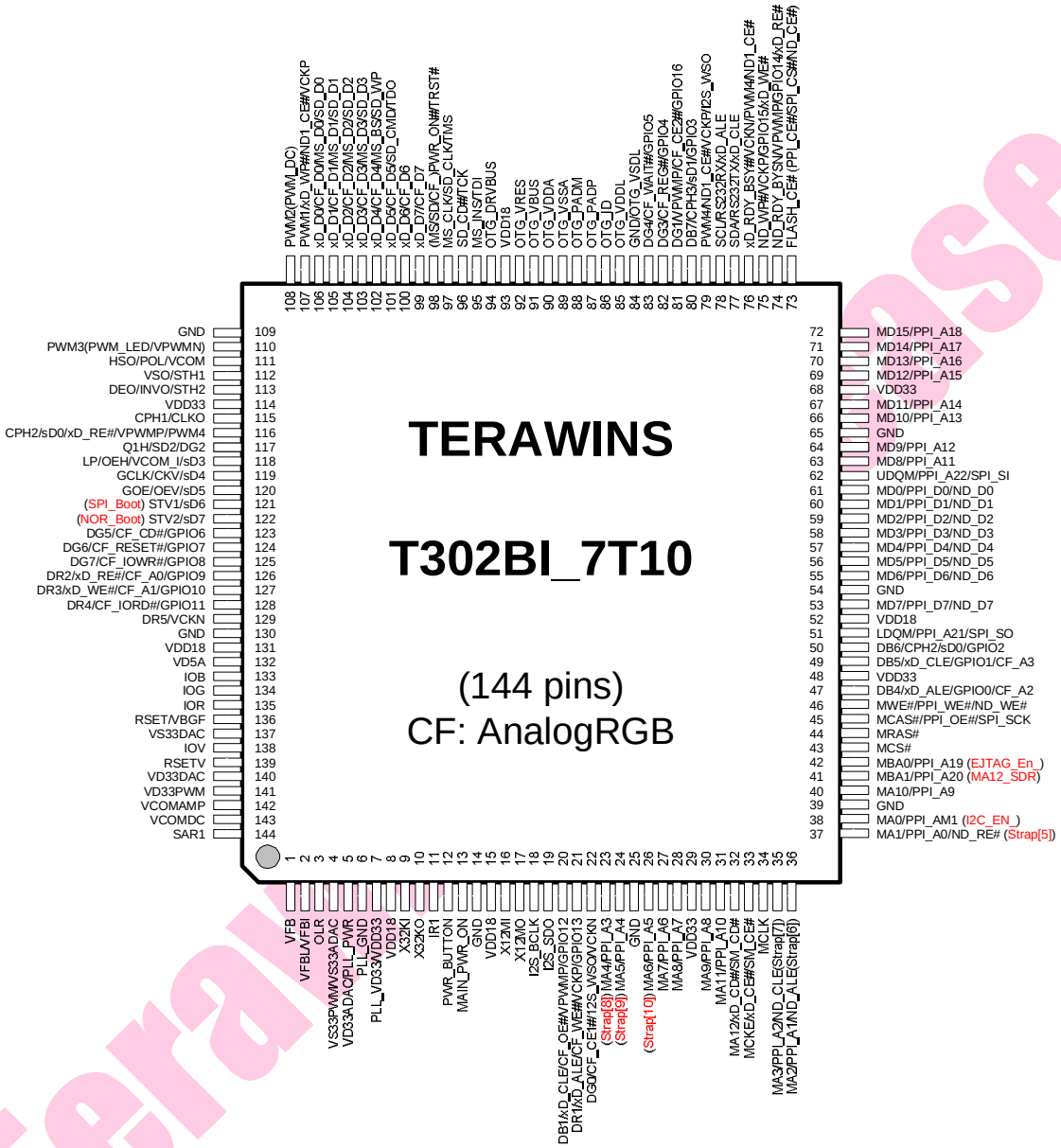


Figure 1-4 Pinout Diagram

T302BI for Analog Panel, CF, CCFL/LED backlight 144pin Version

1.10 Pin Description – T302BI (144pin)

Table 1-3 Pin Description

Pin Name	Type	Functionality Description (T302BI)	Pin #
System Management Interface			
X32KI	I	32.768KHz crystal input	9
X32KO	O	32.768KHz crystal output	10
IR1	I	IR input	11
PWR_BUTTON	I	Power Up button pressed sensing signal	12
MAIN_PWR_ON	O	Signal to turn on main power	13
USB 2.0 OTG Interface			
OTG_ID	I	ID pin	86
OTG_PADP	IO	D+	87
OTG_PADM	IO	D-	88
OTG_VBUS	O	VBUS	91
OTG_VRES	I	Connect to Resistor with 8.2Kohm	92
OTG_DRVBUS	O	Signal to turn-on Vbus to provide power USB device (used in Host mode)	94
SDRAM Memory Interface			
MCLK	O	SDRAM clock	34
MCS#	O	SDRAM CS#	43
MRAS#	O	SDRAM RAS#	44
MCAS#/PPI_OE#/SPI_SCK	O	SDRAM CAS#	45
MWE#/PPI_WE#/ND_WE#	O	SDRAM WE#	46
MBA1/PPI_A20 (MA12_SDR)	IO	SDRAM BA1	41
MBA0/PPI_A19 (EJTAG_En_)	IO	SDRAM BA0	42
MA11/PPI_A10	O	SDRAM MA11	31
MA10/PPI_A9	O	SDRAM MA10	40
MA9/PPI_A8	O	SDRAM MA9	30
MA8/PPI_A7	O	SDRAM MA8	28
MA7/PPI_A6	O	SDRAM MA7	27
MA6/PPI_A5	O	SDRAM MA6	26
MA5/PPI_A4	O	SDRAM MA5	24
MA4/PPI_A3	O	SDRAM MA4	23
MA3/PPI_A2/ND_CLE (Strap[7])	IO	SDRAM MA3	35
MA2/PPI_A1/ND_ALE (Strap[6])	IO	SDRAM MA2	36
MA1/PPI_A0/ND_RE# (Strap[5])	IO	SDRAM MA1	37
MA0/PPI_AM1 (I2C_En_)	IO	SDRAM MA0	38
UDQM/PPI_A22/SPI_SI	O	SDRAM DQM for D15~D8	62
MD15/PPI_A18	IO	SDRAM D15	72
MD14/PPI_A17	IO	SDRAM D14	71
MD13/PPI_A16	IO	SDRAM D13	70
MD12/PPI_A15	IO	SDRAM D12	69
MD11/PPI_A14	IO	SDRAM D11	67
MD10/PPI_A13	IO	SDRAM D10	66
MD9/PPI_A12	IO	SDRAM D9	64
MD8/PPI_A11	IO	SDRAM D8	63
LDQM/PPI_A21/SPI_SO	O	SDRAM DQM for D7~D0	51
MD7/PPI_D7/ND_D7	IO	SDRAM D7	53

Pin Name	Type	Functionality Description (T302BI)	Pin #
MD6/PPI_D6/ND_D6	IO	SDRAM D6	55
MD5/PPI_D5/ND_D5	IO	SDRAM D5	56
MD4/PPI_D4/ND_D4	IO	SDRAM D4	57
MD3/PPI_D3/ND_D3	IO	SDRAM D3	58
MD2/PPI_D2/ND_D2	IO	SDRAM D2	59
MD1/PPI_D1/ND_D1	IO	SDRAM D1	60
MD0/PPI_D0/ND_D0	IO	SDRAM D0	61
SPI NOR Flash Interface (Note: SPI, PPI NOR and NAND are mutually exclusive on oard)			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	SPI NOR Chip Enable	73
MCAS#/PPI_OE#/SPI_SCK	O	SPI NOR Clock	45
LDQM/PPI_A21/SPI_SO	O	SPI Serial Data Output (to input of the flash)	51
UDQM/PPI_A22/SPI_SI	I	SPI Serial Data Input (from output of the flash)	62
PPI NOR Flash Interface			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	PPI NOR Chip Enable	73
MCAS#/PPI_OE#/SPI_SCK	O	PPI NOR OE#	45
MWE#/PPI_WE#/ND_WE#	O	PPI NOR WE#	46
UDQM/PPI_A22/SPI_SI	O	PPI NOR A22	62
LDQM/PPI_A21/SPI_SO	O	PPI NOR A21	51
MBA1/PPI_A20 (MA12_SDR)	IO	PPI NOR A20	41
MBA0/PPI_A19 (EJTAG_En_)	IO	PPI NOR A19	42
MD15/PPI_A18	IO	PPI NOR A18	72
MD14/PPI_A17	IO	PPI NOR A17	71
MD13/PPI_A16	IO	PPI NOR A16	70
MD12/PPI_A15	IO	PPI NOR A15	69
MD11/PPI_A14	IO	PPI NOR A14	67
MD10/PPI_A13	IO	PPI NOR A13	66
MD9/PPI_A12	IO	PPI NOR A12	64
MD8/PPI_A11	IO	PPI NOR A11	63
MA11/PPI_A10	O	PPI NOR A10	31
MA10/PPI_A9	O	PPI NOR A9	40
MA9/PPI_A8	O	PPI NOR A8	30
MA8/PPI_A7	O	PPI NOR A7	28
MA7/PPI_A6	O	PPI NOR A6	27
MA6/PPI_A5	O	PPI NOR A5	26
MA5/PPI_A4	O	PPI NOR A4	24
MA4/PPI_A3	O	PPI NOR A3	23
MA3/PPI_A2/ND_CLE (Strap[7])	IO	PPI NOR A2	35
MA2/PPI_A1/ND_ALE (Strap[6])	IO	PPI NOR A1	36
MA1/PPI_A0/ND_RE# (Strap[5])	IO	PPI NOR A0	37
MA0/PPI_AM1 (I2C_En_)	IO	PPI NOR A-1	38
MD7/PPI_D7/ND_D7	IO	PPI NOR D7	53
MD6/PPI_D6/ND_D6	IO	PPI NOR D6	55
MD5/PPI_D5/ND_D5	IO	PPI NOR D5	56
MD4/PPI_D4/ND_D4	IO	PPI NOR D4	57
MD3/PPI_D3/ND_D3	IO	PPI NOR D3	58
MD2/PPI_D2/ND_D2	IO	PPI NOR D2	59
MD1/PPI_D1/ND_D1	IO	PPI NOR D1	60
MD0/PPI_D0/ND_D0	IO	PPI NOR D0	61
NAND Flash Interface			

Pin Name	Type	Functionality Description (T302BI)	Pin #
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	NAND Chip Enable	73
MA3/PPI_A2/ND_CLE (Strap[7])	IO	NAND_CLE	35
MA2/PPI_A1/ND_ALE (Strap[6])	IO	NAND_ALE	36
MA1/PPI_A0/ND_RE# (Strap[5])	IO	NAND_RE#	37
MWE#/PPI_WE#/ND_WE#	O	NAND_WE#	46
ND_RDY_BYSN/VPWMP/GPIO14/xD_RE#	I	NAND_RDY_BSY#	74
ND_WP#/VCKP/GPIO15/xD_WE#	O	NAND_WP#	75
MD7/PPI_D7/ND_D7	IO	NAND_D7	53
MD6/PPI_D6/ND_D6	IO	NAND_D6	55
MD5/PPI_D5/ND_D5	IO	NAND_D5	56
MD4/PPI_D4/ND_D4	IO	NAND_D4	57
MD3/PPI_D3/ND_D3	IO	NAND_D3	58
MD2/PPI_D2/ND_D2	IO	NAND_D2	59
MD1/PPI_D1/ND_D1	IO	NAND_D1	60
MD0/PPI_D0/ND_D0	IO	NAND_D0	61
UART Interface			
SDA/RS232TX/xD_CLE	O	UART_TX	77
SCL/RS232RX/xD_ALE	I	UART_RX	78
ETJAG Interface			
SD_CD#/TCK	I	EJTAG_TCK	96
MS_CLK/SD_D1/CF_RESET_/TMS	I	EJTAG_TMS	97
MS_INS/TDI	I	EJTAG_TDI	95
(MS/SD/CF_)PWR_ON#/TRST#	I	EJTAG_TRST#	98
xD_D5/CF_D5/SD_CMD/TDO	O	EJTAG_TDO	101
Flash Card Power Interface			
(MS/SD/CF_)PWR_ON#/TRST#	O	Power On/Off for Flash card. (0: ON, 1: Off)	98
SD/MMC Card Interface			
SD_CD#/TCK	I	SD Card Detect	96
MS_CLK/SD_CLK/TMS	O	SD CLK	97
xD_D5/CF_D5/SD_CMD/TDO	IO	SD CMD	101
xD_D3/CF_D3/MS_D3/SD_D3	IO	SD D3	103
xD_D2/CF_D2/MS_D2/SD_D2	IO	SD D2	104
xD_D1/CF_D1/MS_D1/SD_D1	IO	SD D1	105
xD_D0/CF_D0/MS_D0/SD_D0	IO	SD D0	106
xD_D4/CF_D4/MS_BS/SD_WP	I	SD WP	102
MS/MS Pro Card Interface			
MS_INS/TDI	I	MS Card Insert	95
MS_CLK/SD_CLK/TMS	O	MS CLK	97
xD_D4/CF_D4/MS_BS/SD_WP	O	MS BS	102
xD_D3/CF_D3/MS_D3/SD_D3	IO	MS D3	103
xD_D2/CF_D2/MS_D2/SD_D2	IO	MS D2	104
xD_D1/CF_D1/MS_D1/SD_D1	IO	MS D1	105
xD_D0/CF_D0/MS_D0/SD_D0	IO	MS D0	106
XD/SM Card Interface			
MA12/xD_CD#/SM_CD#	I	XD/SM Card Detect	32
MCKE/xD_CE#/SM_CE#	O	XD/SM Chip Enable	33
xD_RDY_BSY#/CF_RDY_BSY#/ VCKN/PWM4/ND1_CE#	I	XD/SM RDY_BSY#	76

Pin Name	Type	Functionality Description (T302BI)	Pin #
xD_ALE/GPIO0/CF_A2	O	XD/SM ALE	47
xD_CLE/GPIO1/CF_A3	O	XD/SM CLE	49
PWM1/xD_WP#/ND1_CE#/VCKP	O	XD/SM WP#	107
xD_RE#/CF_A0/GPIO9	O	XD/SM RE#	126
xD_WE#/CF_A1/GPIO10	O	XD/SM WE#	127
xD_D7/CF_D7	IO	XD/SM D7	99
xD_D6/CF_D6	IO	XD/SM D6	100
xD_D5/CF_D5/SD_CMD/TDO	IO	XD/SM D5	101
xD_D4/CF_D4/MS_BS/SD_WP	IO	XD/SM D4	102
xD_D3/CF_D3/MS_D3/SD_D3	IO	XD/SM D3	103
xD_D2/CF_D2/MS_D2/SD_D2	IO	XD/SM D2	104
xD_D1/CF_D1/MS_D1/SD_D1	IO	XD/SM D1	105
xD_D0/CF_D0/MS_D0/SD_D0	IO	XD/SM D0	106
CF Card Interface			
CF_CD#/GPIO6	I	CF Card Detect	123
CF_RESET#/GPIO7	O	CF Reset	124
CF_CE1#/I2S_WSO/VCKN	O	CF CE1	22
VPWMP/CF_CE2#/GPIO16	O	CF CE2	102
xD_ALE/CF_WE#/VCKP/GPIO13	O	CF WE#	21
xD_CLE/CF_OE#/VPWMP/GPIO12	O	CF OE#	20
CF_REG#/GPIO4	O	CF REG#	82
CF_IOWR#/GPIO8	O	CF IOWR#	125
CF_IORD#/GPIO11	O	CF IORD#	128
CF_WAIT#/GPIO5	IO	CF WAIT#	83
xD_RDY_BSY#/VCKN/PWM4/ND1_CE#	I	CF RDY_BSY#	76
xD_CLE/GPIO1/CF_A3	O	CF A3	49
xD_ALE/GPIO0/CF_A2	O	CF A2	47
xD_WE#/CF_A1/GPIO10	O	CF A1	127
xD_RE#/CF_A0/GPIO9	O	CF A0	126
xD_D7/CF_D7	IO	CF D7	99
xD_D6/CF_D6	IO	CF D6	100
xD_D5/CF_D5/SD_CMD/TDO	IO	CF D5	101
xD_D4/CF_D4/MS_BS/SD_WP	IO	CF D4	102
xD_D3/CF_D3/MS_D3/SD_D3	IO	CF D3	103
xD_D2/CF_D2/MS_D2/SD_D2	IO	CF D2	104
xD_D1/CF_D1/MS_D1/SD_D1	IO	CF D1	105
xD_D0/CF_D0/MS_D0/SD_D0	IO	CF D0	106
I2C Interface			
SDA/RS232TX/xD_CLE	IO	I2C_SDA	77
SCL/RS232RX/xD_ALE	IO	I2C_SCL	78
LCD TCON			
HSO/POL/VCOM	O	Hsync to panel, or Horizontal Polarity output or VCOM	111
VSO/STH1	O	Vsync to panel or Horizontal Start Pulse 1 Signal	112
DEO/INVO/STH2	O	Horizontal Output Data enable, or INVO or Horizontal Start Pulse 2 Signal	113
CPH1/CLKO	O	Clocks to panel	115
Q1H	O	Panel polarity control	117
LP/OEH/VCOM_I	O	Latch pulse for column driver	118

Pin Name	Type	Functionality Description (T302BI)	Pin #
GCLK/CKV	O	Gate driver clock	119
GOE/OEV	O	Gate driver output enable	120
STV1 (SPI_Boot)	O	Gate driver start pulse 1	121
STV2 (NOR_Boot)	O	Gate driver start pulse 2	122
LCD Analog Output and Panel Backlight control			
IOB	O	B-channel analog output	133
IOG	O	G-channel analog output	134
IOR	O	R-channel analog output	135
VBGF	I	DAC voltage reference output	136
IOV	O	Composite Video Encoder output	138
RSETV	I	DAC reference current adjust for TV out	139
VCOMAMP	O	VCOM Amplify	142
VCOMDC	O	VCOM DC	143
VFB	I	Feedback of Lamp current (DC2DC)	1
VFBI	I	Feedback of Lamp current (LED or CCFL)	2
OLR	I	Open Lamp protection (CCFL)	3
PWM2 (PWM_DC)	O	PWM output for DC2DC	108
PWM3 (PWM_LED or VPWMN)	O	PWM output for LED or VPWMN for CCFL	110
Audio I^2S Interface			
I2S_BCLK	O	Audio I^2S Bit clock output	
I2S_SDO	O	Audio I^2S Serial data output	
Misc.			
X12MI	I	12 MHz crystal input	16
X12MO	O	12 MHz crystal output	17
SAR1	I	SARADC for keypads sense	144
PWM4/ND1_CE#/VCKP/I2S_WSO	O	PWM4 output	79
DR5/VCKN	O	Digital PWM output: VCKN for CCFL, this VCKN works with PWM3(VPWMN) become a half bridge	129
Analog Power			
VD33ADAC	P33A	Audio DAC power 3.3V	5
OTG_VDDA	P33A	OTG power 3.3V	90
VD5A	P50A	Video DAC power 5.0V	132
VD33DAC	P33A	Video DAC power 3.3V	140
VD33PWM	P33A	PWM power 3.3V	141
Digital Power			
VDD33	P33	Digital IO power 3.3 V	29, 48, 68, 114
VDD18	P18	Core power 1.8V	15, 52, 93, 131
OTG_VDDL	P18	OTG VDDU 1.8V	85
Battery Power (3.3V)			
VDD33	P33	Battery Power for RTC IO, 3.3 V	7
Battery Power (1.8V)			
VDD18	P18	Battery Power for RTC core, 1.8V	8
GND (Analog)			
VS33ADAC	GNDA	Audio DAC Ground	4

Pin Name	Type	Functionality Description (T302BI)	Pin #
PLL_GND	GNDA	PLL Ground	6
OTG_VSSA	GNDA	OTG VS33	89
VS33DAC	GNDA	Video DAC Ground	137
GND (Digital)			
GND	GND	Digital Ground	14, 25, 39, 54, 65, 84, 109, 130

Hardware Trapping Pins of T302BI

Pin #	Pin Symbol	Trapping Name	0 (pull-down) Determines :	1 (pull-up) Determines :
122	STV2/sD7 (NOR_Boot)	NOR_Boot	Boot from NAND	Boot from NOR
121	STV1/sD6 (SPI_Boot)	SPI_Boot	Boot from PPI NOR	Boot from SPI NOR
42	MBA0/PPI_A19 (EJTAG_En_)	EJTAG_En_	EJTAG Enable (no Flash Card allowed)	SD present
41	MBA1/PPI_A20 (MA12_SDR)	MA12_SDR	Pin-32/33 as xD/SM	Pin-32/33 as MA12/MCKE
38	MA0/PPI_AM1 (I2C_En_)	I2C_En_	Pin-77/78 as I2C func.	Pin-77/78 as UART func.
37	MA1/PPI_A0/ND_RE# (Strap[5])	Trap_5	Reserved	Reserved
36	MA2/PPI_A1/ND_ALE (Strap[6])	Trap_6	Reserved	Reserved
35	MA3/PPI_A2/ND_CLE (Strap[7])	Trap_7	Reserved	Reserved
23	MA4/PPI_A3 (Strap[8])	Trap_8		
24	MA5/PPI_A4 (Strap[9])	Trap_9	Trap[9:8] / ND_CE0# (or the primary ND_CE0#) from 00 / FLASH_CE# (pin # 73) 01 / Reserved 10 / xD_RDY_BSY# (pin # 76) --- Reserved 11 / PWM4 (pin # 79)	
26	MA6/PPI_A5 (Strap[10])	Trap_10	ND_CE1# at non-FLASH_CE# pin, and configured though firmware	ND_CE1# at FLASH_CE# pin

1.11 Pinout Diagram – T302BD(144pin Analog panel, CF, CCFL/LED backlight support with audio I²S I/F)

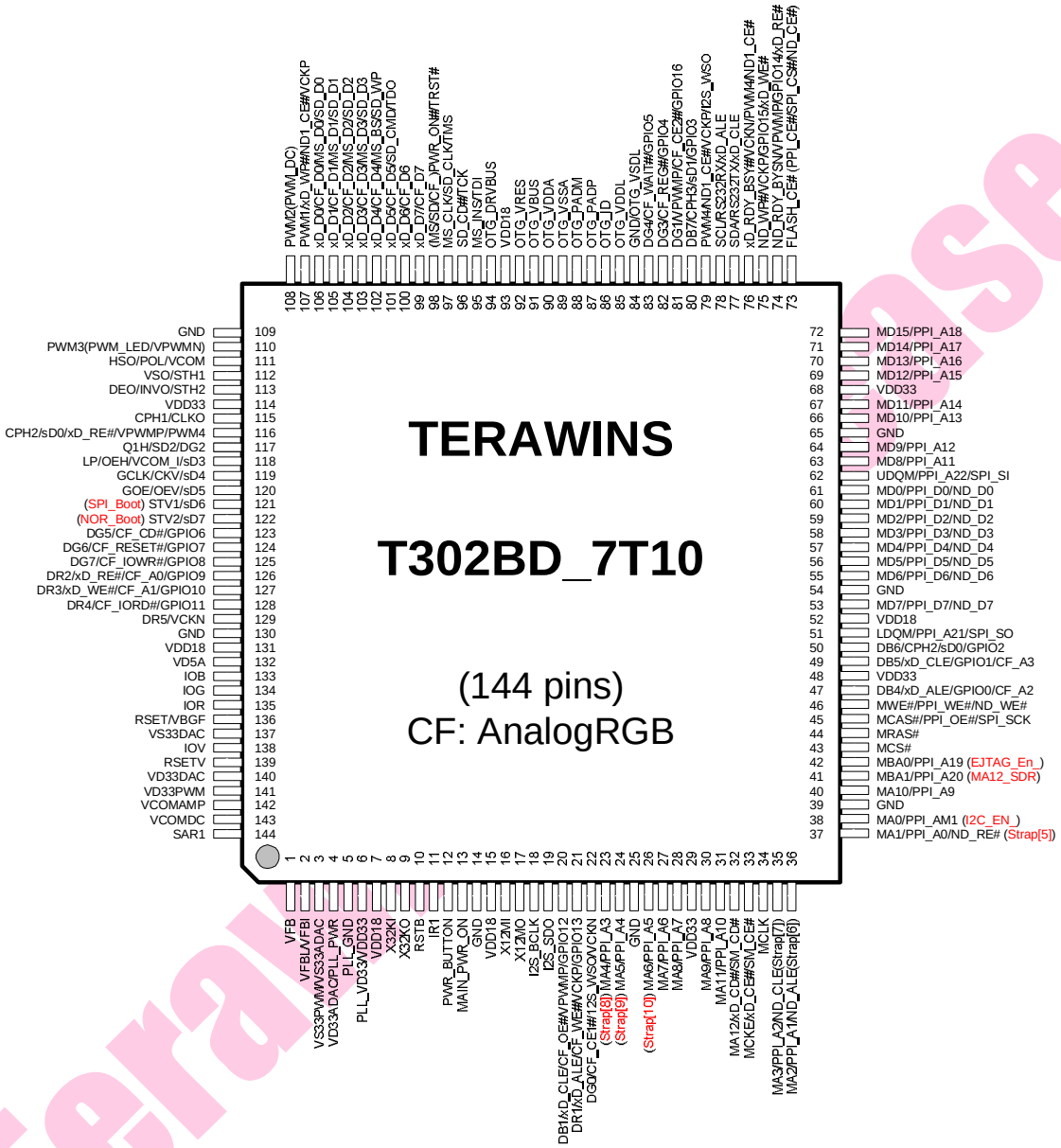


Figure 1-4 Pinout Diagram

T302BD for Analog Panel, CF, CCFL/LED backlight 144pin Version

1.12 Pin Description – T302BD (144pin)

Table 1-3 Pin Description

Pin Name	Type	Functionality Description (T302BD)	Pin #
System Management Interface			
X32KI	I	32.768KHz crystal input	8
X32KO	O	32.768KHz crystal output	9
RSTB	I	Whole chip reset	10
IR1	I	IR input	11
PWR_BUTTON	I	Power Up button pressed sensing signal	12
MAIN_PWR_ON	O	Signal to turn on main power	13
USB 2.0 OTG Interface			
OTG_ID	I	ID pin	86
OTG_PADP	IO	D+	87
OTG_PADM	IO	D-	88
OTG_VBUS	O	VBUS	91
OTG_VRES	I	Connect to Resistor with 8.2Kohm	92
OTG_DRVBUS	O	Signal to turn-on Vbus to provide power USB device (used in Host mode)	94
SDRAM Memory Interface			
MCLK	O	SDRAM clock	34
MCS#	O	SDRAM CS#	43
MRAS#	O	SDRAM RAS#	44
MCAS#/PPI_OE#/SPI_SCK	O	SDRAM CAS#	45
MWE#/PPI_WE#/ND_WE#	O	SDRAM WE#	46
MBA1/PPI_A20 (MA12_SDR)	IO	SDRAM BA1	41
MBA0/PPI_A19 (EJTAG_En_)	IO	SDRAM BA0	42
MA11/PPI_A10	O	SDRAM MA11	31
MA10/PPI_A9	O	SDRAM MA10	40
MA9/PPI_A8	O	SDRAM MA9	30
MA8/PPI_A7	O	SDRAM MA8	28
MA7/PPI_A6	O	SDRAM MA7	27
MA6/PPI_A5	O	SDRAM MA6	26
MA5/PPI_A4	O	SDRAM MA5	24
MA4/PPI_A3	O	SDRAM MA4	23
MA3/PPI_A2/ND_CLE (Strap[7])	IO	SDRAM MA3	35
MA2/PPI_A1/ND_ALE (Strap[6])	IO	SDRAM MA2	36
MA1/PPI_A0/ND_RE# (Strap[5])	IO	SDRAM MA1	37
MA0/PPI_AM1 (I2C_En_)	IO	SDRAM MA0	38
UDQM/PPI_A22/SPI_SI	O	SDRAM DQM for D15~D8	62
MD15/PPI_A18	IO	SDRAM D15	72
MD14/PPI_A17	IO	SDRAM D14	71
MD13/PPI_A16	IO	SDRAM D13	70
MD12/PPI_A15	IO	SDRAM D12	69
MD11/PPI_A14	IO	SDRAM D11	67
MD10/PPI_A13	IO	SDRAM D10	66
MD9/PPI_A12	IO	SDRAM D9	64
MD8/PPI_A11	IO	SDRAM D8	63
LDQM/PPI_A21/SPI_SO	O	SDRAM DQM for D7~D0	51

Pin Name	Type	Functionality Description (T302BD)	Pin #
MD7/PPI_D7/ND_D7	IO	SDRAM D7	53
MD6/PPI_D6/ND_D6	IO	SDRAM D6	55
MD5/PPI_D5/ND_D5	IO	SDRAM D5	56
MD4/PPI_D4/ND_D4	IO	SDRAM D4	57
MD3/PPI_D3/ND_D3	IO	SDRAM D3	58
MD2/PPI_D2/ND_D2	IO	SDRAM D2	59
MD1/PPI_D1/ND_D1	IO	SDRAM D1	60
MD0/PPI_D0/ND_D0	IO	SDRAM D0	61
SPI NOR Flash Interface (Note: SPI, PPI NOR and NAND are mutually exclusive on oard)			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	SPI NOR Chip Enable	73
MCAS#/PPI_OE#/SPI_SCK	O	SPI NOR Clock	45
LDQM/PPI_A21/SPI_SO	O	SPI Serial Data Output (to input of the flash)	51
UDQM/PPI_A22/SPI_SI	I	SPI Serial Data Input (from output of the flash)	62
PPI NOR Flash Interface			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	PPI NOR Chip Enable	73
MCAS#/PPI_OE#/SPI_SCK	O	PPI NOR OE#	45
MWE#/PPI_WE#/ND_WE#	O	PPI NOR WE#	46
UDQM/PPI_A22/SPI_SI	O	PPI NOR A22	62
LDQM/PPI_A21/SPI_SO	O	PPI NOR A21	51
MBA1/PPI_A20 (MA12_SDR)	IO	PPI NOR A20	41
MBA0/PPI_A19 (EJTAG_En_)	IO	PPI NOR A19	42
MD15/PPI_A18	IO	PPI NOR A18	72
MD14/PPI_A17	IO	PPI NOR A17	71
MD13/PPI_A16	IO	PPI NOR A16	70
MD12/PPI_A15	IO	PPI NOR A15	69
MD11/PPI_A14	IO	PPI NOR A14	67
MD10/PPI_A13	IO	PPI NOR A13	66
MD9/PPI_A12	IO	PPI NOR A12	64
MD8/PPI_A11	IO	PPI NOR A11	63
MA11/PPI_A10	O	PPI NOR A10	31
MA10/PPI_A9	O	PPI NOR A9	40
MA9/PPI_A8	O	PPI NOR A8	30
MA8/PPI_A7	O	PPI NOR A7	28
MA7/PPI_A6	O	PPI NOR A6	27
MA6/PPI_A5	O	PPI NOR A5	26
MA5/PPI_A4	O	PPI NOR A4	24
MA4/PPI_A3	O	PPI NOR A3	23
MA3/PPI_A2/ND_CLE (Strap[7])	IO	PPI NOR A2	35
MA2/PPI_A1/ND_ALE (Strap[6])	IO	PPI NOR A1	36
MA1/PPI_A0/ND_RE# (Strap[5])	IO	PPI NOR A0	37
MA0/PPI_AM1 (I2C_En_)	IO	PPI NOR A-1	38
MD7/PPI_D7/ND_D7	IO	PPI NOR D7	53
MD6/PPI_D6/ND_D6	IO	PPI NOR D6	55
MD5/PPI_D5/ND_D5	IO	PPI NOR D5	56
MD4/PPI_D4/ND_D4	IO	PPI NOR D4	57
MD3/PPI_D3/ND_D3	IO	PPI NOR D3	58
MD2/PPI_D2/ND_D2	IO	PPI NOR D2	59
MD1/PPI_D1/ND_D1	IO	PPI NOR D1	60
MD0/PPI_D0/ND_D0	IO	PPI NOR D0	61

Pin Name	Type	Functionality Description (T302BD)	Pin #
NAND Flash Interface			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	NAND Chip Enable	73
MA3/PPI_A2/ND_CLE (Strap[7])	IO	NAND_CLE	35
MA2/PPI_A1/ND_ALE (Strap[6])	IO	NAND_ALE	36
MA1/PPI_A0/ND_RE# (Strap[5])	IO	NAND_RE#	37
MWE#/PPI_WE#/ND_WE#	O	NAND_WE#	46
ND_RDY_BYSN/VPWMP/GPIO14/xD_RE#	I	NAND_RDY_BSY#	74
ND_WP#/VCKP/GPIO15/xD_WE#	O	NAND_WP#	75
MD7/PPI_D7/ND_D7	IO	NAND_D7	53
MD6/PPI_D6/ND_D6	IO	NAND_D6	55
MD5/PPI_D5/ND_D5	IO	NAND_D5	56
MD4/PPI_D4/ND_D4	IO	NAND_D4	57
MD3/PPI_D3/ND_D3	IO	NAND_D3	58
MD2/PPI_D2/ND_D2	IO	NAND_D2	59
MD1/PPI_D1/ND_D1	IO	NAND_D1	60
MD0/PPI_D0/ND_D0	IO	NAND_D0	61
UART Interface			
SDA/RS232TX/xD_CLE	O	UART_TX	77
SCL/RS232RX/xD_ALE	I	UART_RX	78
ETJAG Interface			
SD_CD#/TCK	I	EJTAG_TCK	96
MS_CLK/SD_D1/CF_RESET_/TMS	I	EJTAG_TMS	97
MS_INS/TDI	I	EJTAG_TDI	95
(MS/SD/CF_)PWR_ON#/TRST#	I	EJTAG_TRST#	98
xD_D5/CF_D5/SD_CMD/TDO	O	EJTAG_TDO	101
Flash Card Power Interface			
(MS/SD/CF_)PWR_ON#/TRST#	O	Power On/Off for Flash card. (0: ON, 1: Off)	98
SD/MMC Card Interface			
SD_CD#/TCK	I	SD Card Detect	96
MS_CLK/SD_CLK/TMS	O	SD CLK	97
xD_D5/CF_D5/SD_CMD/TDO	IO	SD CMD	101
xD_D3/CF_D3/MS_D3/SD_D3	IO	SD D3	103
xD_D2/CF_D2/MS_D2/SD_D2	IO	SD D2	104
xD_D1/CF_D1/MS_D1/SD_D1	IO	SD D1	105
xD_D0/CF_D0/MS_D0/SD_D0	IO	SD D0	106
xD_D4/CF_D4/MS_BS/SD_WP	I	SD WP	102
MS/MS Pro Card Interface			
MS_INS/TDI	I	MS Card Insert	95
MS_CLK/SD_CLK/TMS	O	MS CLK	97
xD_D4/CF_D4/MS_BS/SD_WP	O	MS BS	102
xD_D3/CF_D3/MS_D3/SD_D3	IO	MS D3	103
xD_D2/CF_D2/MS_D2/SD_D2	IO	MS D2	104
xD_D1/CF_D1/MS_D1/SD_D1	IO	MS D1	105
xD_D0/CF_D0/MS_D0/SD_D0	IO	MS D0	106
XD/SM Card Interface			
MA12/xD_CD#/SM_CD#	I	XD/SM Card Detect	32
MCKE/xD_CE#/SM_CE#	O	XD/SM Chip Enable	33

Pin Name	Type	Functionality Description (T302BD)	Pin #
xD_RDY_BSY#/CF_RDY_BSY#/ VCKN/PWM4/ND1_CE#	I	XD/SM RDY_BSY#	76
DB4/xD_ALE/GPIO0/CF_A2	O	XD/SM ALE	47
DB5/xD_CLE/GPIO1/CF_A3	O	XD/SM CLE	49
PWM1/xD_WP#/ND1_CE#/VCKP	O	XD/SM WP#	107
DR2/xD_RE#/CF_A0/GPIO9	O	XD/SM RE#	126
DR3/xD_WE#/CF_A1/GPIO10	O	XD/SM WE#	127
xD_D7/CF_D7	IO	XD/SM D7	99
xD_D6/CF_D6	IO	XD/SM D6	100
xD_D5/CF_D5/SD_CMD/TDO	IO	XD/SM D5	101
xD_D4/CF_D4/MS_BS/SD_WP	IO	XD/SM D4	102
xD_D3/CF_D3/MS_D3/SD_D3	IO	XD/SM D3	103
xD_D2/CF_D2/MS_D2/SD_D2	IO	XD/SM D2	104
xD_D1/CF_D1/MS_D1/SD_D1	IO	XD/SM D1	105
xD_D0/CF_D0/MS_D0/SD_D0	IO	XD/SM D0	106
CF Card Interface			
DG5/CF_CD#/GPIO6	I	CF Card Detect	123
DG6/CF_RESET#/GPIO7	O	CF Reset	124
DG0/CF_CE1#/I2S_WSO/VCKN	O	CF CE1	22
DG1/VPWMP/CF_CE2#/GPIO16	O	CF CE2	81
xD_ALE/CF_WE#/VCKP/GPIO13	O	CF WE#	21
xD_CLE/CF_OE#/VPWMP/GPIO12	O	CF OE#	20
DG3/CF_REG#/GPIO4	O	CF REG#	82
DG7/CF_IOWR#/GPIO8	O	CF IOWR#	125
DR4/CF_IORD#/GPIO11	O	CF IORD#	128
DG4/CF_WAIT#/GPIO5	IO	CF WAIT#	83
xD_RDY_BSY#/VCKN/PWM4/ND1_CE#	I	CF RDY_BSY#	76
DB5/xD_CLE/GPIO1/CF_A3	O	CF A3	49
DB4/xD_ALE/GPIO0/CF_A2	O	CF A2	47
DR3/xD_WE#/CF_A1/GPIO10	O	CF A1	127
DR2/xD_RE#/CF_A0/GPIO9	O	CF A0	126
xD_D7/CF_D7	IO	CF D7	99
xD_D6/CF_D6	IO	CF D6	100
xD_D5/CF_D5/SD_CMD/TDO	IO	CF D5	101
xD_D4/CF_D4/MS_BS/SD_WP	IO	CF D4	102
xD_D3/CF_D3/MS_D3/SD_D3	IO	CF D3	103
xD_D2/CF_D2/MS_D2/SD_D2	IO	CF D2	104
xD_D1/CF_D1/MS_D1/SD_D1	IO	CF D1	105
xD_D0/CF_D0/MS_D0/SD_D0	IO	CF D0	106
I2C Interface			
SDA/RS232TX/xD_CLE	IO	I2C_SDA	77
SCL/RS232RX/xD_ALE	IO	I2C_SCL	78
LCD TCON			
HSO/POL/VCOM	O	Hsync to panel, or Horizontal Polarity output or VCOM	111
VSO/STH1	O	Vsync to panel or Horizontal Start Pulse 1 Signal	112
DEO/INVO/STH2	O	Horizontal Output Data enable, or INVO or Horizontal Start Pulse 2 Signal	113
CPH1/CLKO	O	Clocks to panel	115

Pin Name	Type	Functionality Description (T302BD)	Pin #
Q1H	O	Panel polarity control	117
LP/OEH/VCOM_I	O	Latch pulse for column driver	118
GCLK/CKV	O	Gate driver clock	119
GOE/OEV	O	Gate driver output enable	120
STV1 (SPI_Boot)	O	Gate driver start pulse 1	121
STV2 (NOR_Boot)	O	Gate driver start pulse 2	122
LCD Analog Output and Panel Backlight control			
IOB	O	B-channel analog output	133
IOG	O	G-channel analog output	134
IOR	O	R-channel analog output	135
VBGF	I	DAC voltage reference output	136
IOV	O	Composite Video Encoder output	138
RSETV	I	DAC reference current adjust for TV out	139
VCOMAMP	O	VCOM Amplify	142
VCOMDC	O	VCOM DC	143
VFB	I	Feedback of Lamp current (DC2DC)	1
VFBL/VFBI	I	Feedback of Lamp current (LED or CCFL)	2
OLR	I	Open Lamp protection (CCFL)	
PWM2 (PWM_DC)	O	PWM output for DC2DC	108
PWM3 (PWM_LED or VPWMN)	O	PWM output for LED or VPWMN for CCFL	110
Audio I^2S Interface			
I2S_BCLK	O	Audio I^2S Bit clock output	18
I2S_SDO	O	Audio I^2S Serial data output	19
Misc.			
X12MI	I	12 MHz crystal input	16
X12MO	O	12 MHz crystal output	17
SAR1	I	SARADC for keypads sense	144
PWM4/ND1_CE#/VCKP/I2S_WSO	O	PWM4 output	79
DR5/VCKN	O	Digital PWM output: VCKN for CCFL, this VCKN works with PWM3(VPWMN) become a half bridge	129
Analog Power			
VD33ADAC	P33A	Audio DAC power 3.3V	4
OTG_VDDA	P33A	OTG power 3.3V	90
VD5A	P50A	Video DAC power 5.0V	132
VD33DAC	P33A	Video DAC power 3.3V	140
VD33PWM	P33A	PWM power 3.3V	141
Digital Power			
VDD33	P33	Digital IO power 3.3 V	29, 48, 68, 114
VDD18	P18	Core power 1.8V	15, 52, 93, 131
OTG_VDDL	P18	OTG VDDU 1.8V	85
Battery Power (3.3V)			
VDD33	P33	Battery Power for RTC IO, 3.3 V	6
Battery Power (1.8V)			
VDD18	P18	Battery Power for RTC core, 1.8V	7

Pin Name	Type	Functionality Description (T302BD)	Pin #
GND (Analog)			
VS33ADAC	GNDA	Audio DAC Ground	3
PLL_GND	GNDA	PLL Ground	5
OTG_VSSA	GNDA	OTG VS33	89
VS33DAC	GNDA	Video DAC Ground	137
GND (Digital)			
GND	GND	Digital Ground	14, 25, 39, 54, 65, 84, 109, 130

Hardware Trapping Pins of T302BD

Pin #	Pin Symbol	Trapping Name	0 (pull-down) Determines :	1 (pull-up) Determines :
122	STV2/sD7 (NOR_Boot)	NOR_Boot	Boot from NAND	Boot from NOR
121	STV1/sD6 (SPI_Boot)	SPI_Boot	Boot from PPI NOR	Boot from SPI NOR
42	MBA0/PPI_A19 (EJTAG_En_)	EJTAG_En_	EJTAG Enable (no Flash Card allowed)	SD present
41	MBA1/PPI_A20 (MA12_SDR)	MA12_SDR	Pin-32/33 as xD/SM	Pin-32/33 as MA12/MCKE
38	MA0/PPI_AM1 (I2C_En_)	I2C_En_	Pin-77/78 as I2C func.	Pin-77/78 as UART func.
37	MA1/PPI_A0/ND_RE# (Strap[5])	Trap_5	Reserved	Reserved
36	MA2/PPI_A1/ND_ALE (Strap[6])	Trap_6	Reserved	Reserved
35	MA3/PPI_A2/ND_CLE (Strap[7])	Trap_7	Reserved	Reserved
23	MA4/PPI_A3 (Strap[8])	Trap_8		
24	MA5/PPI_A4 (Strap[9])	Trap_9		
26	MA6/PPI_A5 (Strap[10])	Trap_10	ND_CE1# at non-FLASH_CE# pin, and configured though firmware	ND_CE1# at FLASH_CE# pin

Trap[9:8]	ND_CE0# (or the primary ND_CE0#) from
00	FLASH_CE# (pin # 73)
01	Reserved
10	xD_RDY_BSY# (pin # 76) --- Reserved
11	PWM4 (pin # 79)

1.13 Pinout Diagram – T302BT (144pin Digital panel, CCFL/LED backlight support with internal audio DAC)

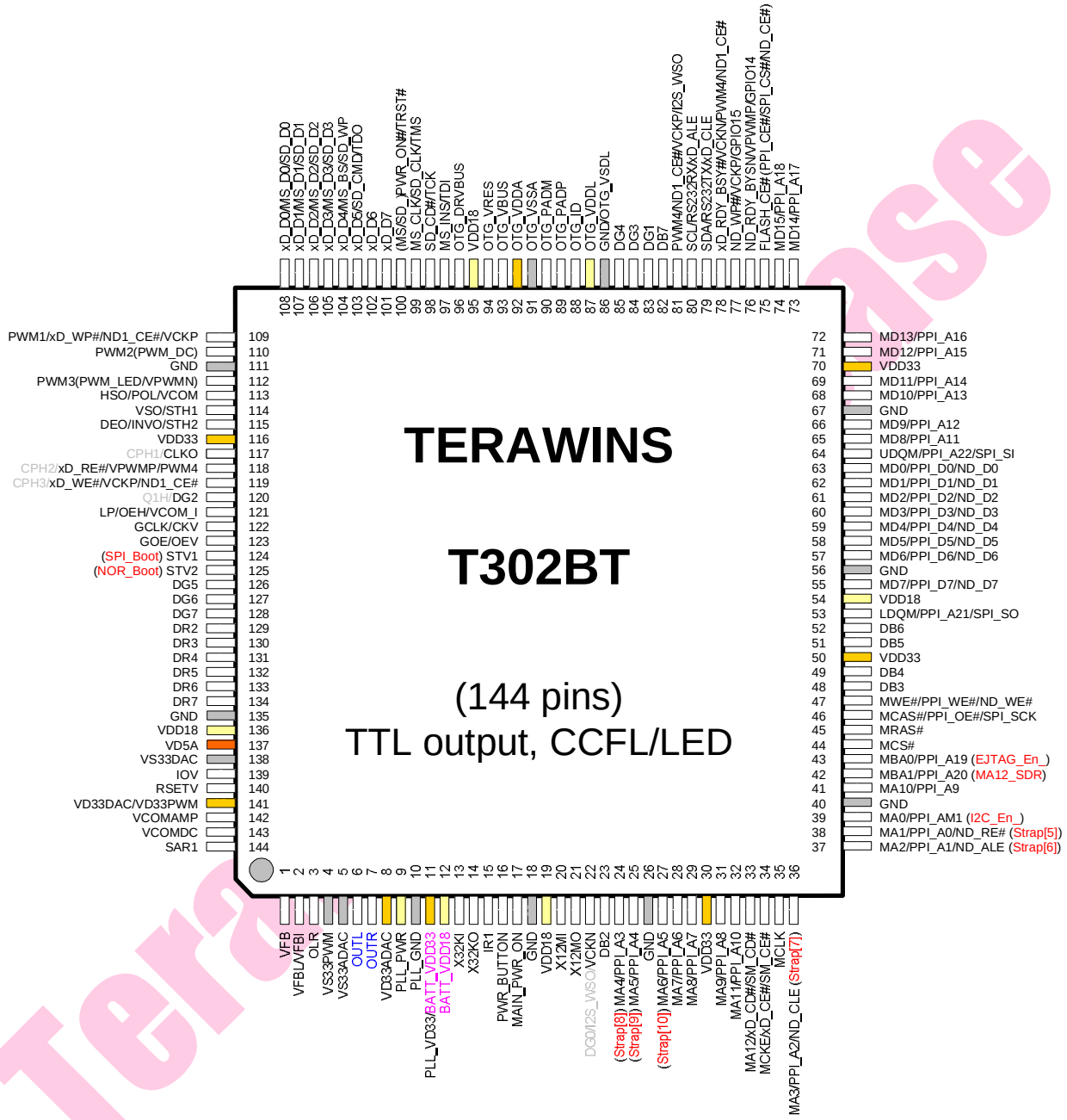


Figure 1-5 Pinout Diagram

T302BT for Digital Panel, CCFL/LED backlight 144pin Version

1.14 Pin Description – T302BT (144pin)

Table 1-4 Pin Description

Pin Name	Type	Functionality Description (T302BT)	Pin #
System Management Interface			
X32KI	I	32.768KHz crystal input	13
X32KO	O	32.768KHz crystal output	14
IR1	I	IR input	15
PWR_BUTTON	I	Power Up button pressed sensing signal	16
MAIN_PWR_ON	O	Signal to turn on main power	17
USB 2.0 OTG Interface			
OTG_ID	I	ID pin	88
OTG_PADP	IO	D+	89
OTG_PADM	IO	D-	90
OTG_VBUS	O	VBUS	93
OTG_VRES	I	Connect to Resistor with 8.2Kohm	94
OTG_DRVBUS	O	Signal to turn-on Vbus to provide power USB device (used in Host mode)	96
SDRAM Memory Interface			
MCLK	O	SDRAM clock	35
MCS#	O	SDRAM CS#	44
MRAS#	O	SDRAM RAS#	45
MCAS#/PPI_OE#/SPI_SCK	O	SDRAM CAS#	46
MWE#/PPI_WE#/ND_WE#	O	SDRAM WE#	47
MBA1/PPI_A20 (MA12_SDR)	IO	SDRAM BA1	42
MBA0/PPI_A19 (EJTAG_En_)	IO	SDRAM BA0	43
MA11/PPI_A10	O	SDRAM MA11	32
MA10/PPI_A9	O	SDRAM MA10	41
MA9/PPI_A8	O	SDRAM MA9	31
MA8/PPI_A7	O	SDRAM MA8	29
MA7/PPI_A6	O	SDRAM MA7	28
MA6/PPI_A5	O	SDRAM MA6	27
MA5/PPI_A4	O	SDRAM MA5	25
MA4/PPI_A3	O	SDRAM MA4	24
MA3/PPI_A2/ND_CLE (Strap[7])	IO	SDRAM MA3	36
MA2/PPI_A1/ND_ALE (Strap[6])	IO	SDRAM MA2	37
MA1/PPI_A0/ND_RE# (Strap[5])	IO	SDRAM MA1	38
MA0/PPI_AM1 (I2C_En_)	IO	SDRAM MA0	39
UDQM/PPI_A22/SPI_SI	O	SDRAM DQM for D15~D8	64
MD15/PPI_A18	IO	SDRAM D15	74
MD14/PPI_A17	IO	SDRAM D14	73
MD13/PPI_A16	IO	SDRAM D13	72
MD12/PPI_A15	IO	SDRAM D12	71
MD11/PPI_A14	IO	SDRAM D11	69
MD10/PPI_A13	IO	SDRAM D10	68
MD9/PPI_A12	IO	SDRAM D9	66
MD8/PPI_A11	IO	SDRAM D8	65
LDQM/PPI_A21/SPI_SO	O	SDRAM DQM for D7~D0	53
MD7/PPI_D7/ND_D7	IO	SDRAM D7	55

Pin Name	Type	Functionality Description (T302BT)	Pin #
MD6/PPI_D6/ND_D6	IO	SDRAM D6	57
MD5/PPI_D5/ND_D5	IO	SDRAM D5	58
MD4/PPI_D4/ND_D4	IO	SDRAM D4	59
MD3/PPI_D3/ND_D3	IO	SDRAM D3	60
MD2/PPI_D2/ND_D2	IO	SDRAM D2	61
MD1/PPI_D1/ND_D1	IO	SDRAM D1	62
MD0/PPI_D0/ND_D0	IO	SDRAM D0	63
SPI NOR Flash Interface (Note: SPI, PPI NOR and NAND are mutually exclusive on oard)			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	SPI NOR Chip Enable	75
MCAS#/PPI_OE#/SPI_SCK	O	SPI NOR Clock	46
LDQM/PPI_A21/SPI_SO	O	SPI Serial Data Output (to input of the flash)	53
UDQM/PPI_A22/SPI_SI	I	SPI Serial Data Input (from output of the flash)	64
PPI NOR Flash Interface			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	PPI NOR Chip Enable	75
MCAS#/PPI_OE#/SPI_SCK	O	PPI NOR OE#	46
MWE#/PPI_WE#/ND_WE#	O	PPI NOR WE#	47
UDQM/PPI_A22/SPI_SI	O	PPI NOR A22	64
LDQM/PPI_A21/SPI_SO	O	PPI NOR A21	53
MBA1/PPI_A20 (MA12_SDR)	IO	PPI NOR A20	42
MBA0/PPI_A19 (EJTAG_En_)	IO	PPI NOR A19	43
MD15/PPI_A18	IO	PPI NOR A18	74
MD14/PPI_A17	IO	PPI NOR A17	73
MD13/PPI_A16	IO	PPI NOR A16	72
MD12/PPI_A15	IO	PPI NOR A15	71
MD11/PPI_A14	IO	PPI NOR A14	69
MD10/PPI_A13	IO	PPI NOR A13	68
MD9/PPI_A12	IO	PPI NOR A12	66
MD8/PPI_A11	IO	PPI NOR A11	65
MA11/PPI_A10	O	PPI NOR A10	32
MA10/PPI_A9	O	PPI NOR A9	41
MA9/PPI_A8	O	PPI NOR A8	31
MA8/PPI_A7	O	PPI NOR A7	29
MA7/PPI_A6	O	PPI NOR A6	28
MA6/PPI_A5	O	PPI NOR A5	27
MA5/PPI_A4	O	PPI NOR A4	25
MA4/PPI_A3	O	PPI NOR A3	24
MA3/PPI_A2/ND_CLE (Strap[7])	IO	PPI NOR A2	36
MA2/PPI_A1/ND_ALE (Strap[6])	IO	PPI NOR A1	37
MA1/PPI_A0/ND_RE# (Strap[5])	IO	PPI NOR A0	38
MA0/PPI_AM1 (I2C_En_)	IO	PPI NOR A-1	39
MD7/PPI_D7/ND_D7	IO	PPI NOR D7	55
MD6/PPI_D6/ND_D6	IO	PPI NOR D6	57
MD5/PPI_D5/ND_D5	IO	PPI NOR D5	58
MD4/PPI_D4/ND_D4	IO	PPI NOR D4	59
MD3/PPI_D3/ND_D3	IO	PPI NOR D3	60
MD2/PPI_D2/ND_D2	IO	PPI NOR D2	61
MD1/PPI_D1/ND_D1	IO	PPI NOR D1	62
MD0/PPI_D0/ND_D0	IO	PPI NOR D0	63
NAND Flash Interface			

Pin Name	Type	Functionality Description (T302BT)	Pin #
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	NAND Chip Enable	75
MA3/PPI_A2/ND_CLE (Strap[7])	IO	NAND_CLE	36
MA2/PPI_A1/ND_ALE (Strap[6])	IO	NAND_ALE	37
MA1/PPI_A0/ND_RE# (Strap[5])	IO	NAND_RE#	38
MWE#/PPI_WE#/ND_WE#	O	NAND_WE#	47
ND_RDY_BYSN/VPWMP/GPIO14/xD_RE#	I	NAND_RDY_BSY#	76
ND_WP#/VCKP/GPIO15/xD_WE#	O	NAND_WP#	77
MD7/PPI_D7/ND_D7	IO	NAND_D7	55
MD6/PPI_D6/ND_D6	IO	NAND_D6	57
MD5/PPI_D5/ND_D5	IO	NAND_D5	58
MD4/PPI_D4/ND_D4	IO	NAND_D4	59
MD3/PPI_D3/ND_D3	IO	NAND_D3	60
MD2/PPI_D2/ND_D2	IO	NAND_D2	61
MD1/PPI_D1/ND_D1	IO	NAND_D1	62
MD0/PPI_D0/ND_D0	IO	NAND_D0	63
UART Interface			
SDA/RS232TX/xD_CLE	O	UART_TX	79
SCL/RS232RX/xD_ALE	I	UART_RX	80
ETJAG Interface			
SD_CD#/TCK	I	EJTAG_TCK	98
MS_CLK/SD_D1/TMS	I	EJTAG_TMS	99
MS_INS/TDI	I	EJTAG_TDI	97
(MS/SD_)PWR_ON#/TRST#	I	EJTAG_TRST#	100
xD_D5/SD_CMD/TDO	O	EJTAG_TDO	103
Flash Card Power Interface			
(MS/SD_)PWR_ON#/TRST#	O	Power On/Off for Flash card. (0: ON, 1: Off)	100
SD/MMC Card Interface			
SD_CD#/TCK	I	SD Card Detect	98
MS_CLK/SD_CLK/TMS	O	SD CLK	99
xD_D5/SD_CMD/TDO	IO	SD CMD	103
xD_D3/MS_D3/SD_D3	IO	SD D3	105
xD_D2/MS_D2/SD_D2	IO	SD D2	106
xD_D1/MS_D1/SD_D1	IO	SD D1	107
xD_D0/MS_D0/SD_D0	IO	SD D0	108
xD_D4/MS_BS/SD_WP	I	SD WP	104
MS/MS Pro Card Interface			
MS_INS/TDI	I	MS Card Insert	97
MS_CLK/SD_CLK/TMS	O	MS CLK	99
xD_D4/MS_BS/SD_WP	O	MS BS	104
xD_D3/MS_D3/SD_D3	IO	MS D3	105
xD_D2/MS_D2/SD_D2	IO	MS D2	106
xD_D1/MS_D1/SD_D1	IO	MS D1	107
xD_D0/MS_D0/SD_D0	IO	MS D0	108
XD/SM Card Interface			
MA12/xD_CD#/SM_CD#	I	XD/SM Card Detect	33
MCKE/xD_CE#/SM_CE#	O	XD/SM Chip Enable	34
xD_RDY_BSY#/VCKN/PWM4/ND1_CE#	I	XD/SM RDY_BSY#	78
SCL/RS232RX/xD_ALE	O	XD/SM ALE	80

Pin Name	Type	Functionality Description (T302BT)	Pin #
SDA/RS232TX/xD_CLE	O	XD/SM CLE	79
PWM1/xD_WP#/ND1_CE#/VCKP	O	XD/SM WP#	109
CPH2/sD0/xD_RE#/VPWMP/PWM4	O	XD/SM RE#	118
CPH3/sD1/xD_WE#/VCKP/ND1_CE#	O	XD/SM WE#	119
xD_D7	IO	XD/SM D7	101
xD_D6	IO	XD/SM D6	102
xD_D5/SD_CMD/TDO	IO	XD/SM D5	103
xD_D4/MS_BS/SD_WP	IO	XD/SM D4	104
xD_D3/MS_D3/SD_D3	IO	XD/SM D3	105
xD_D2/MS_D2/SD_D2	IO	XD/SM D2	106
xD_D1/MS_D1/SD_D1	IO	XD/SM D1	107
xD_D0/MS_D0/SD_D0	IO	XD/SM D0	108
I2C Interface			
SDA/RS232TX/xD_CLE	IO	I2C_SDA	79
SCL/RS232RX/xD_ALE	IO	I2C_SCL	80
LCD TCON			
HSO/POL/VCOM	O	Hsync to panel, or Horizontal Polarity output or VCOM	113
VSO/STH1	O	Vsync to panel or Horizontal Start Pulse 1 Signal	114
DEO/INVO/STH2	O	Horizontal Output Data enable, or INVO or Horizontal Start Pulse 2 Signal	115
CPH1/CLKO	O	Clocks to panel	117
Q1H	O	Panel polarity control	120
LP/OEH/VCOM_I	O	Latch pulse for column driver	121
GCLK/CKV	O	Gate driver clock	122
GOE/OEV	O	Gate driver output enable	123
STV1 (SPI_Boot)	O	Gate driver start pulse 1	124
STV2 (NOR_Boot)	O	Gate driver start pulse 2	125
TTL Panel Output			
DR7	O	R-channel Data 7 output	134
DR6	O	R-channel Data 6 output	133
DR5	O	R-channel Data 5 output	132
DR4	O	R-channel Data 4 output	131
DR3	O	R-channel Data 3 output	130
DR2	O	R-channel Data 2 output	129
DG7	O	G-channel Data 7 output	128
DG6	O	G-channel Data 6 output	127
DG5	O	G-channel Data 5 output	126
DG4	O	G-channel Data 4 output	85
DG3	O	G-channel Data 3 output	84
DG2	O	G-channel Data 2 output	120
DG1/VPWMP	O	G-channel Data 1 output (optional)	83
DB7	O	B-channel Data 7 output	82
DB6	O	B-channel Data 6 output	52
DB5	O	B-channel Data 5 output	51
DB4	O	B-channel Data 4 output	49
DB3	O	B-channel Data 3 output	48
DB2	O	B-channel Data 2 output	23

Pin Name	Type	Functionality Description (T302BT)	Pin #
LCD Analog Output and Panel Backlight control			
IOV	O	Composite Video Encoder output	139
RSETV	I	DAC reference current adjust for TV out	140
VCOMAMP	O	VCOM Amplify	142
VCOMDC	O	VCOM DC	143
VFB	I	Feedback of Lamp current (DC2DC)	1
VFBI/VFBL	I	Feedback of Lamp current (LED or CCFL)	2
OLR	I	Open Lamp protection (CCFL)	3
PWM2 (PWM_DC)	O	PWM output for DC2DC	110
PWM3 (PWM_LED or VPWMN)	O	PWM output for LED or VPWMN for CCFL	112
Misc.			
X12MI	I	12 MHz crystal input	20
X12MO	O	12 MHz crystal output	21
SAR1	I	SARADC for keypads sense	144
PWM4/ND1_CE#/VCKP/I2S_WSO	O	PWM4 output	81
DG0/I2S_WSO/VCKN	O	Digital PWM output: VCKN for CCFL, this VCKN works with PWM3(VPWMN) become a half bridge	22
OUTL/OUTR	O	Audio DAC output (Left/Right channel)	6,7
Analog Power			
VD33ADAC	P33A	Audio DAC power 3.3V	8
PLL_PWR	P18A	PLL power 1.8 V	9
OTG_VDDA	P33A	OTG power 3.3V	92
VD5A	P50A	Video DAC power 5.0V	137
VD33DAC/ VD33PWM	P33A	Video DAC power and PWM power 3.3V	141
Digital Power			
VDD33	P33	Digital IO power 3.3 V	30, 50, 70, 116
VDD18	P18	Core power 1.8V	19, 54, 95, 136
OTG_VSDL	P18	OTG VDDU 1.8V	86
Battery Power (3.3V)			
VDD33	P33	Battery Power for RTC IO, 3.3 V	11
Battery Power (1.8V)			
VDD18	P18	Battery Power for RTC core, 1.8V	12
GND (Analog)			
VS33PWM	GNDA	PWM Ground	4
VS33ADAC	GNDA	Audio DAC Ground	5
PLL_GND	GNDA	PLL Ground	10
OTG_VSSA	GNDA	OTG VS33	91
VS33DAC	GNDA	Video DAC Ground	138
GND (Digital)			
GND	GND	Digital Ground	18, 26, 40, 56, 67, 87, 111, 135

Hardware Trapping Pins of T302BT

<table>
<tr><th>Pin #</th><th>Pin Symbol</th><th>Trapping Name</th><th>0 (pull-down) Determines :</th><th>1 (pull-up) Determines :</th></tr>
<tr><td>125</td><td>STV2/sD7 (NOR_Boot)</td><td>NOR_Boot</td><td>Boot from NAND</td><td>Boot from NOR</td></tr>
<tr><td>124</td><td>STV1/sD6 (SPI_Boot)</td><td>SPI_Boot</td><td>Boot from PPI NOR</td><td>Boot from SPI NOR</td></tr>
<tr><td>43</td><td>MBA0/PPI_A19 (EJTAG_En_)</td><td>EJTAG_En_</td><td>EJTAG Enable
(no Flash Card allowed)</td><td>SD present</td></tr>
<tr><td>42</td><td>MBA1/PPI_A20 (MA12_SDR)</td><td>MA12_SDR</td><td>Pin-33/34 as xD/SM</td><td>Pin-33/34 as MA12/MCKE</td></tr>
<tr><td>39</td><td>MA0/PPI_AM1 (I2C_En_)</td><td>I2C_En_</td><td>Pin-79/80 as I2C func.</td><td>Pin-79/80 as UART func.</td></tr>
<tr><td>38</td><td>MA1/PPI_A0/ND_RE# (Strap[5])</td><td>Trap_5</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>37</td><td>MA2/PPI_A1/ND_ALE (Strap[6])</td><td>Trap_6</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>36</td><td>MA3/PPI_A2/ND_CLE (Strap[7])</td><td>Trap_7</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>24</td><td>MA4/PPI_A3 (Strap[8])</td><td>Trap_8</td><td colspan="2" rowspan="2"></td></tr>
<tr><td>25</td><td>MA5/PPI_A4 (Strap[9])</td><td>Trap_9</td></tr>
<tr><td>27</td><td>MA6/PPI_A5 (Strap[10])</td><td>Trap_10</td><td>ND_CE1# at non-FLASH_CE# pin, and configured though firmware</td><td>ND_CE1# at FLASH_CE# pin</td></tr>
</table>

Trap[9:8]	ND_CE0# (or the primary ND_CE0#) from
00	FLASH_CE# (pin # 75)
01	CPH3 (pin # 119) --- Reserved
10	xD_RDY_BSY# (pin # 78) --- Reserved
11	PWM4 (pin # 81)

1.15 Pinout Diagram – T302BV (144pin Digital panel, CCFL/LED backlight support with audio I²S I/F)

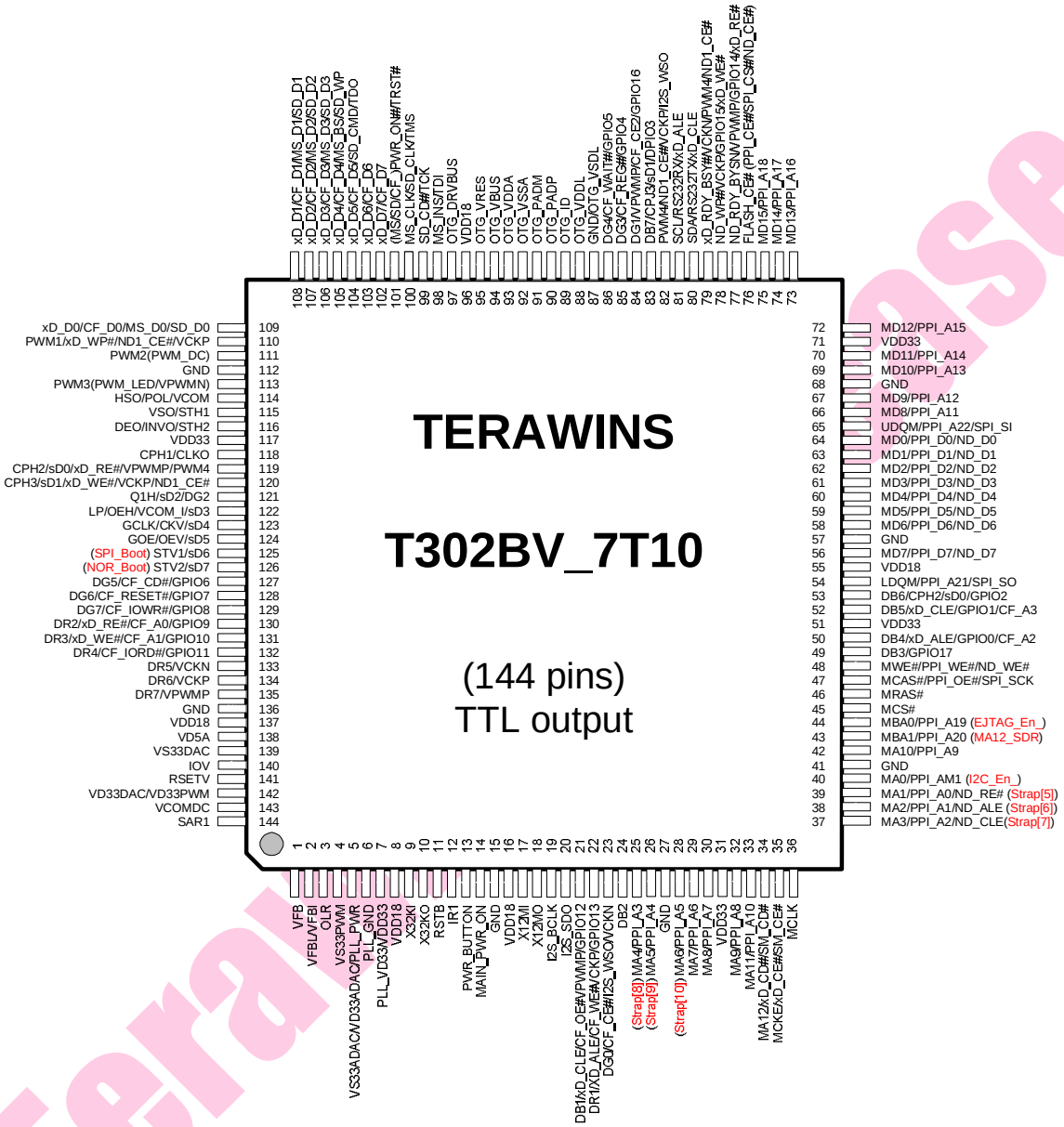


Figure 1-6 Pinout Diagram

T302BV for Digital Panel, CCFL/LED backlight 144pin Version

1.16 Pin Description – T302BV (144pin)

Table 1-5 Pin Description

Pin Name	Type	Functionality Description (T302BV)	Pin #
System Management Interface			
X32KI	I	32.768KHz crystal input	9
X32KO	O	32.768KHz crystal output	10
RSTB	I	Whole chip reset	11
IR1	I	IR input	12
PWR_BUTTON	I	Power Up button pressed sensing signal	13
MAIN_PWR_ON	O	Signal to turn on main power	14
USB 2.0 OTG Interface			
OTG_ID	I	ID pin	89
OTG_PADP	IO	D+	90
OTG_PADM	IO	D-	91
OTG_VBUS	O	VBUS	94
OTG_VRES	I	Connect to Resistor with 8.2Kohm	95
OTG_DRVBUS	O	Signal to turn-on Vbus to provide power USB device (used in Host mode)	97
SDRAM Memory Interface			
MCLK	O	SDRAM clock	36
MCS#	O	SDRAM CS#	45
MRAS#	O	SDRAM RAS#	46
MCAS#/PPI_OE#/SPI_SCK	O	SDRAM CAS#	47
MWE#/PPI_WE#/ND_WE#	O	SDRAM WE#	48
MBA1/PPI_A20 (MA12_SDR)	IO	SDRAM BA1	43
MBA0/PPI_A19 (EJTAG_En_)	IO	SDRAM BA0	44
MA11/PPI_A10	O	SDRAM MA11	33
MA10/PPI_A9	O	SDRAM MA10	42
MA9/PPI_A8	O	SDRAM MA9	32
MA8/PPI_A7	O	SDRAM MA8	30
MA7/PPI_A6	O	SDRAM MA7	29
MA6/PPI_A5	O	SDRAM MA6	28
MA5/PPI_A4	O	SDRAM MA5	26
MA4/PPI_A3	O	SDRAM MA4	25
MA3/PPI_A2/ND_CLE (Strap[7])	IO	SDRAM MA3	37
MA2/PPI_A1/ND_ALE (Strap[6])	IO	SDRAM MA2	38
MA1/PPI_A0/ND_RE# (Strap[5])	IO	SDRAM MA1	39
MA0/PPI_AM1 (I2C_En_)	IO	SDRAM MA0	40
UDQM/PPI_A22/SPI_SI	O	SDRAM DQM for D15~D8	65
MD15/PPI_A18	IO	SDRAM D15	75
MD14/PPI_A17	IO	SDRAM D14	74
MD13/PPI_A16	IO	SDRAM D13	73
MD12/PPI_A15	IO	SDRAM D12	72
MD11/PPI_A14	IO	SDRAM D11	70
MD10/PPI_A13	IO	SDRAM D10	69
MD9/PPI_A12	IO	SDRAM D9	67
MD8/PPI_A11	IO	SDRAM D8	66
LDQM/PPI_A21/SPI_SO	O	SDRAM DQM for D7~D0	54

Pin Name	Type	Functionality Description (T302BV)	Pin #
MD7/PPI_D7/ND_D7	IO	SDRAM D7	56
MD6/PPI_D6/ND_D6	IO	SDRAM D6	58
MD5/PPI_D5/ND_D5	IO	SDRAM D5	59
MD4/PPI_D4/ND_D4	IO	SDRAM D4	60
MD3/PPI_D3/ND_D3	IO	SDRAM D3	61
MD2/PPI_D2/ND_D2	IO	SDRAM D2	62
MD1/PPI_D1/ND_D1	IO	SDRAM D1	63
MD0/PPI_D0/ND_D0	IO	SDRAM D0	64
SPI NOR Flash Interface (Note: SPI, PPI NOR and NAND are mutually exclusive on oard)			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	SPI NOR Chip Enable	76
MCAS#/PPI_OE#/SPI_SCK	O	SPI NOR Clock	47
LDQM/PPI_A21/SPI_SO	O	SPI Serial Data Output (to input of the flash)	54
UDQM/PPI_A22/SPI_SI	I	SPI Serial Data Input (from output of the flash)	65
PPI NOR Flash Interface			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	PPI NOR Chip Enable	76
MCAS#/PPI_OE#/SPI_SCK	O	PPI NOR OE#	47
MWE#/PPI_WE#/ND_WE#	O	PPI NOR WE#	48
UDQM/PPI_A22/SPI_SI	O	PPI NOR A22	65
LDQM/PPI_A21/SPI_SO	O	PPI NOR A21	54
MBA1/PPI_A20 (MA12_SDR)	IO	PPI NOR A20	43
MBA0/PPI_A19 (EJTAG_En_)	IO	PPI NOR A19	44
MD15/PPI_A18	IO	PPI NOR A18	75
MD14/PPI_A17	IO	PPI NOR A17	74
MD13/PPI_A16	IO	PPI NOR A16	73
MD12/PPI_A15	IO	PPI NOR A15	72
MD11/PPI_A14	IO	PPI NOR A14	70
MD10/PPI_A13	IO	PPI NOR A13	69
MD9/PPI_A12	IO	PPI NOR A12	67
MD8/PPI_A11	IO	PPI NOR A11	66
MA11/PPI_A10	O	PPI NOR A10	33
MA10/PPI_A9	O	PPI NOR A9	42
MA9/PPI_A8	O	PPI NOR A8	32
MA8/PPI_A7	O	PPI NOR A7	30
MA7/PPI_A6	O	PPI NOR A6	29
MA6/PPI_A5	O	PPI NOR A5	28
MA5/PPI_A4	O	PPI NOR A4	26
MA4/PPI_A3	O	PPI NOR A3	25
MA3/PPI_A2/ND_CLE (Strap[7])	IO	PPI NOR A2	37
MA2/PPI_A1/ND_ALE (Strap[6])	IO	PPI NOR A1	38
MA1/PPI_A0/ND_RE# (Strap[5])	IO	PPI NOR A0	39
MA0/PPI_AM1 (I2C_En_)	IO	PPI NOR A-1	40
MD7/PPI_D7/ND_D7	IO	PPI NOR D7	56
MD6/PPI_D6/ND_D6	IO	PPI NOR D6	58
MD5/PPI_D5/ND_D5	IO	PPI NOR D5	59
MD4/PPI_D4/ND_D4	IO	PPI NOR D4	60
MD3/PPI_D3/ND_D3	IO	PPI NOR D3	61
MD2/PPI_D2/ND_D2	IO	PPI NOR D2	62
MD1/PPI_D1/ND_D1	IO	PPI NOR D1	63
MD0/PPI_D0/ND_D0	IO	PPI NOR D0	64

Pin Name	Type	Functionality Description (T302BV)	Pin #
NAND Flash Interface			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	NAND Chip Enable	76
MA3/PPI_A2/ND_CLE (Strap[7])	IO	NAND_CLE	37
MA2/PPI_A1/ND_ALE (Strap[6])	IO	NAND_ALE	38
MA1/PPI_A0/ND_RE# (Strap[5])	IO	NAND_RE#	39
MWE#/PPI_WE#/ND_WE#	O	NAND_WE#	48
ND_RDY_BYSN/VPWMP/GPIO14/xD_RE#	I	NAND_RDY_BSY#	77
ND_WP#/VCKP/GPIO15/xD_WE#	O	NAND_WP#	78
MD7/PPI_D7/ND_D7	IO	NAND_D7	56
MD6/PPI_D6/ND_D6	IO	NAND_D6	58
MD5/PPI_D5/ND_D5	IO	NAND_D5	59
MD4/PPI_D4/ND_D4	IO	NAND_D4	60
MD3/PPI_D3/ND_D3	IO	NAND_D3	61
MD2/PPI_D2/ND_D2	IO	NAND_D2	62
MD1/PPI_D1/ND_D1	IO	NAND_D1	63
MD0/PPI_D0/ND_D0	IO	NAND_D0	64
UART Interface			
SDA/RS232TX/xD_CLE	O	UART_TX	80
SCL/RS232RX/xD_ALE	I	UART_RX	81
ETJAG Interface			
SD_CD#/TCK	I	EJTAG_TCK	99
MS_CLK/SD_D1/TMS	I	EJTAG_TMS	100
MS_INS/TDI	I	EJTAG_TDI	98
(MS/SD_)PWR_ON#/TRST#	I	EJTAG_TRST#	101
xD_D5/SD_CMD/TDO	O	EJTAG_TDO	104
Flash Card Power Interface			
(MS/SD_)PWR_ON#/TRST#	O	Power On/Off for Flash card. (0: ON, 1: Off)	101
SD/MMC Card Interface			
SD_CD#/TCK	I	SD Card Detect	99
MS_CLK/SD_CLK/TMS	O	SD CLK	100
xD_D5/SD_CMD/TDO	IO	SD CMD	104
xD_D3/MS_D3/SD_D3	IO	SD D3	106
xD_D2/MS_D2/SD_D2	IO	SD D2	107
xD_D1/MS_D1/SD_D1	IO	SD D1	108
xD_D0/MS_D0/SD_D0	IO	SD D0	109
xD_D4/MS_BS/SD_WP	I	SD WP	105
MS/MS Pro Card Interface			
MS_INS/TDI	I	MS Card Insert	98
MS_CLK/SD_CLK/TMS	O	MS CLK	100
xD_D4/MS_BS/SD_WP	O	MS BS	105
xD_D3/MS_D3/SD_D3	IO	MS D3	106
xD_D2/MS_D2/SD_D2	IO	MS D2	107
xD_D1/MS_D1/SD_D1	IO	MS D1	108
xD_D0/MS_D0/SD_D0	IO	MS D0	109
XD/SM Card Interface			
MA12/xD_CD#/SM_CD#	I	XD/SM Card Detect	34
MCKE/xD_CE#/SM_CE#	O	XD/SM Chip Enable	35

Pin Name	Type	Functionality Description (T302BV)	Pin #
xD_RDY_BSY#/VCKN/PWM4/ND1_CE#	I	XD/SM RDY_BSY#	79
SCL/RS232RX/xD_ALE	O	XD/SM ALE	81
SDA/RS232TX/xD_CLE	O	XD/SM CLE	80
PWM1/xD_WP#/ND1_CE#/VCKP	O	XD/SM WP#	110
CPH2/sD0/xD_RE#/VPWMP/PWM4	O	XD/SM RE#	119
CPH3/sD1/xD_WE#/VCKP/ND1_CE#	O	XD/SM WE#	120
xD_D7	IO	XD/SM D7	102
xD_D6	IO	XD/SM D6	103
xD_D5/SD_CMD/TDO	IO	XD/SM D5	104
xD_D4/MS_BS/SD_WP	IO	XD/SM D4	105
xD_D3/MS_D3/SD_D3	IO	XD/SM D3	106
xD_D2/MS_D2/SD_D2	IO	XD/SM D2	107
xD_D1/MS_D1/SD_D1	IO	XD/SM D1	108
xD_D0/MS_D0/SD_D0	IO	XD/SM D0	109
I2C Interface			
SDA/RS232TX/xD_CLE	IO	I2C_SDA	80
SCL/RS232RX/xD_ALE	IO	I2C_SCL	81
LCD TCON			
HSO/POL/VCOM	O	Hsync to panel, or Horizontal Polarity output or VCOM	114
VSO/STH1	O	Vsync to panel or Horizontal Start Pulse 1 Signal	115
DEO/INVO/STH2	O	Horizontal Output Data enable, or INVO or Horizontal Start Pulse 2 Signal	116
CPH1/CLKO	O	Clocks to panel	118
Q1H	O	Panel polarity control	121
LP/OEH/VCOM_I	O	Latch pulse for column driver	122
GCLK/CKV	O	Gate driver clock	123
GOE/OEV	O	Gate driver output enable	124
STV1 (SPI_Boot)	O	Gate driver start pulse 1	125
STV2 (NOR_Boot)	O	Gate driver start pulse 2	126
TTL Panel Output			
DR7	O	R-channel Data 7 output	135
DR6	O	R-channel Data 6 output	134
DR5	O	R-channel Data 5 output	133
DR4	O	R-channel Data 4 output	132
DR3	O	R-channel Data 3 output	131
DR2	O	R-channel Data 2 output	130
DR1	O	R-channel Data 1 output	22
DG7	O	G-channel Data 7 output	129
DG6	O	G-channel Data 6 output	128
DG5	O	G-channel Data 5 output	127
DG4	O	G-channel Data 4 output	86
DG3	O	G-channel Data 3 output	85
DG2	O	G-channel Data 2 output	121
DG1/VPWMP	O	G-channel Data 1 output (optional)	84
DB7	O	B-channel Data 7 output	83
DB6	O	B-channel Data 6 output	53
DB5	O	B-channel Data 5 output	52
DB4	O	B-channel Data 4 output	50

Pin Name	Type	Functionality Description (T302BV)	Pin #
DB3	O	B-channel Data 3 output	49
DB2	O	B-channel Data 2 output	24
DB1	O	B-channel Data 1 output	21
LCD Analog Output and Panel Backlight control			
IOV	O	Composite Video Encoder output	140
RSETV	I	DAC reference current adjust for TV out	141
VCOMDC	O	VCOM DC	143
VFB	I	Feedback of Lamp current (DC2DC)	1
VFBI/VFBL	I	Feedback of Lamp current (LED or CCFL)	2
OLR	I	Open Lamp protection (CCFL)	3
PWM2 (PWM_DC)	O	PWM output for DC2DC	111
PWM3 (PWM_LED or VPWMN)	O	PWM output for LED or VPWMN for CCFL	113
Audio I^2S Interface			
I2S_BCLK	O	Audio I^2S Bit clock output	19
I2S_SDO	O	Audio I^2S Serial data output	20
Misc.			
X12MI	I	12 MHz crystal input	17
X12MO	O	12 MHz crystal output	18
SAR1	I	SARADC for keypads sense	144
PWM4/ND1_CE#/VCKP/I2S_WSO	O	PWM4 output	82
DG0/I2S_WSO/VCKN	O	Digital PWM output: VCKN for CCFL, this VCKN works with PWM3(VPWMN) become a half bridge	23
Analog Power			
VD33ADAC	P33A	Audio DAC power 3.3V	5
OTG_VDDA	P33A	OTG power 3.3V	93
VD5A	P50A	Video DAC power 5.0V	138
VD33DAC/ VD33PWM	P33A	Video DAC power and PWM power 3.3V	142
Digital Power			
VDD33	P33	Digital IO power 3.3 V	31, 51, 71, 117
VDD18	P18	Core power 1.8V	16, 55, 96, 137
OTG_VSDL	P18	OTG VDDU 1.8V	87
Battery Power (3.3V)			
VDD33	P33	Battery Power for RTC IO, 3.3 V	7
Battery Power (1.8V)			
VDD18	P18	Battery Power for RTC core, 1.8V	8
GND (Analog)			
VS33ADAC	GNDA	Audio DAC Ground	4
PLL_GND	GNDA	PLL Ground	6
OTG_VSSA	GNDA	OTG VS33	92
VS33DAC	GNDA	Video DAC Ground	139
GND (Digital)			
GND	GND	Digital Ground	15, 27, 41, 57, 68, 88, 112, 136

Hardware Trapping Pins of T302BV

<table>
<tr><th>Pin #</th><th>Pin Symbol</th><th>Trapping Name</th><th>0 (pull-down) Determines :</th><th>1 (pull-up) Determines :</th></tr>
<tr><td>126</td><td>STV2/sD7 (NOR_Boot)</td><td>NOR_Boot</td><td>Boot from NAND</td><td>Boot from NOR</td></tr>
<tr><td>125</td><td>STV1/sD6 (SPI_Boot)</td><td>SPI_Boot</td><td>Boot from PPI NOR</td><td>Boot from SPI NOR</td></tr>
<tr><td>44</td><td>MBA0/PPI_A19 (EJTAG_En_)</td><td>EJTAG_En_</td><td>EJTAG Enable
(no Flash Card allowed)</td><td>SD present</td></tr>
<tr><td>43</td><td>MBA1/PPI_A20 (MA12_SDR)</td><td>MA12_SDR</td><td>Pin-34/35 as xD/SM</td><td>Pin-34/35 as MA12/MCKE</td></tr>
<tr><td>40</td><td>MA0/PPI_AM1 (I2C_En_)</td><td>I2C_En_</td><td>Pin-80/81 as I2C func.</td><td>Pin-80/81 as UART func.</td></tr>
<tr><td>39</td><td>MA1/PPI_A0/ND_RE# (Strap[5])</td><td>Trap_5</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>38</td><td>MA2/PPI_A1/ND_ALE (Strap[6])</td><td>Trap_6</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>37</td><td>MA3/PPI_A2/ND_CLE (Strap[7])</td><td>Trap_7</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>25</td><td>MA4/PPI_A3 (Strap[8])</td><td>Trap_8</td><td colspan="2" rowspan="2"></td></tr>
<tr><td>26</td><td>MA5/PPI_A4 (Strap[9])</td><td>Trap_9</td></tr>
<tr><td>28</td><td>MA6/PPI_A5 (Strap[10])</td><td>Trap_10</td><td>ND_CE1# at non-FLASH_CE# pin, and configured though firmware</td><td>ND_CE1# at FLASH_CE# pin</td></tr>
</table>

Trap[9:8]	ND_CE0# (or the primary ND_CE0#) from
00	FLASH_CE# (pin # 76)
01	CPH3 (pin # 120) --- Reserved
10	xD_RDY_BSY# (pin # 79) --- Reserved
11	PWM4 (pin # 82)

1.17 Pinout Diagram – T302BA (128pin Analog panel, LED backlight support with internal audio DAC)

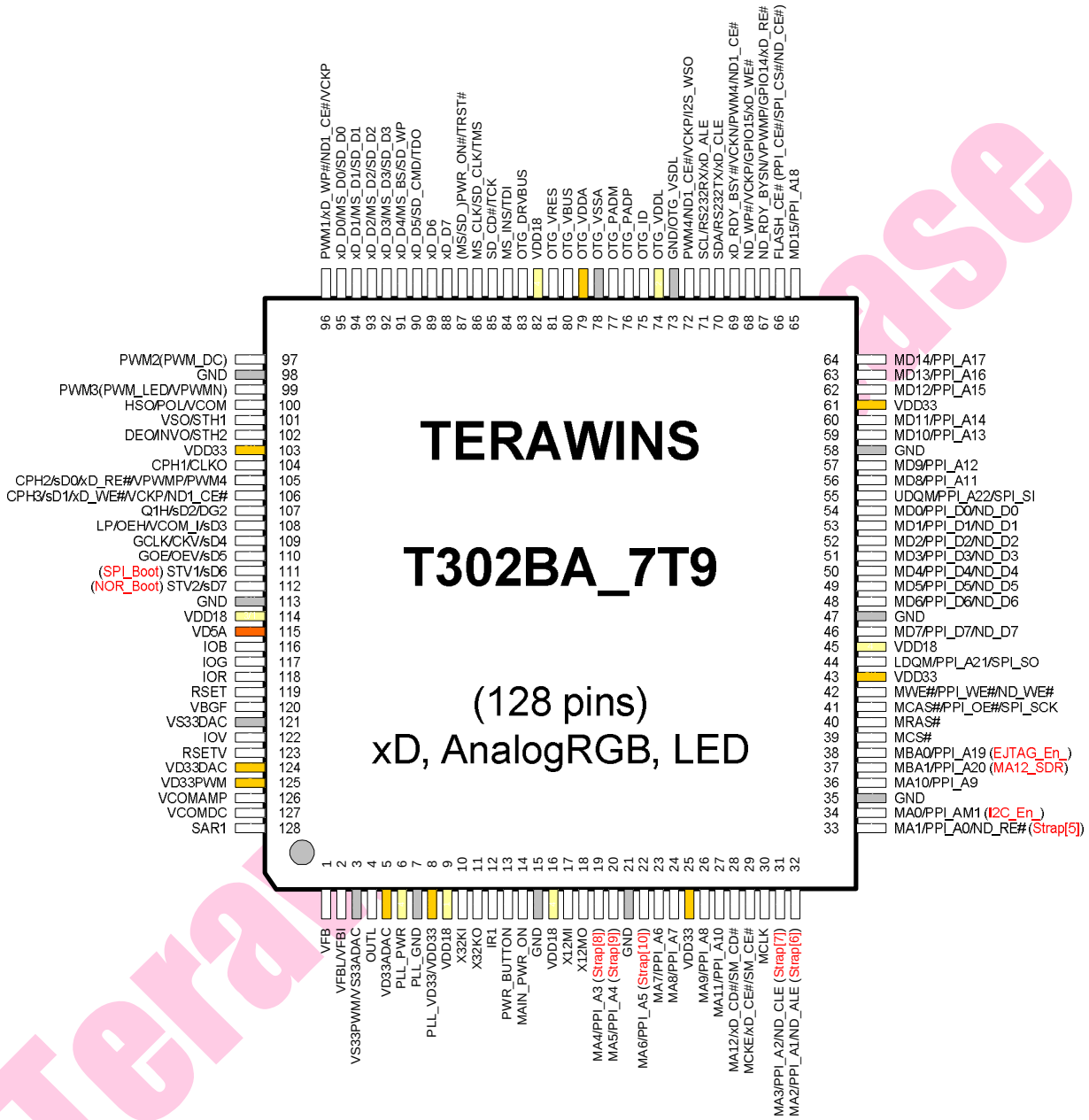


Figure 1-7 Pinout Diagram

T302BZ for Analog Panel, LED backlight 128pin Version

1.18 Pin Description – T302BA (128pin)

Table 1-6 Pin Description

Pin Name	Type	Functionality Description (T302BA)	Pin #
System Management Interface			
X32KI	I	32.768KHz crystal input	11
X32KO	O	32.768KHz crystal output	12
IR1	I	IR input	13
PWR_BUTTON	I	Power Up button pressed sensing signal	14
MAIN_PWR_ON	O	Signal to turn on main power	15
USB 2.0 OTG Interface			
OTG_ID	I	ID pin	76
OTG_PADP	IO	D+	77
OTG_PADM	IO	D-	78
OTG_VBUS	O	VBUS	81
OTG_VRES	I	Connect to Resistor with 8.2Kohm	82
OTG_DRVBUS	O	Signal to turn-on Vbus to provide power USB device (used in Host mode)	84
SDRAM Memory Interface			
MCLK	O	SDRAM clock	31
MCS#	O	SDRAM CS#	40
MRAS#	O	SDRAM RAS#	41
MCAS#/PPI_OE#/SPI_SCK	O	SDRAM CAS#	42
MWE#/PPI_WE#/ND_WE#	O	SDRAM WE#	43
MBA1/PPI_A20 (MA12_SDR)	IO	SDRAM BA1	38
MBA0/PPI_A19 (EJTAG_En_)	IO	SDRAM BA0	39
MA11/PPI_A10	O	SDRAM MA11	28
MA10/PPI_A9	O	SDRAM MA10	37
MA9/PPI_A8	O	SDRAM MA9	27
MA8/PPI_A7	O	SDRAM MA8	25
MA7/PPI_A6	O	SDRAM MA7	24
MA6/PPI_A5	O	SDRAM MA6	23
MA5/PPI_A4	O	SDRAM MA5	21
MA4/PPI_A3	O	SDRAM MA4	20
MA3/PPI_A2/ND_CLE (Strap[7])	IO	SDRAM MA3	32
MA2/PPI_A1/ND_ALE (Strap[6])	IO	SDRAM MA2	33
MA1/PPI_A0/ND_RE# (Strap[5])	IO	SDRAM MA1	34
MA0/PPI_AM1 (I2C_En_)	IO	SDRAM MA0	35
UDQM/PPI_A22/SPI_SI	O	SDRAM DQM for D15~D8	56
MD15/PPI_A18	IO	SDRAM D15	66
MD14/PPI_A17	IO	SDRAM D14	65
MD13/PPI_A16	IO	SDRAM D13	64
MD12/PPI_A15	IO	SDRAM D12	63
MD11/PPI_A14	IO	SDRAM D11	61
MD10/PPI_A13	IO	SDRAM D10	60
MD9/PPI_A12	IO	SDRAM D9	58
MD8/PPI_A11	IO	SDRAM D8	57
LDQM/PPI_A21/SPI_SO	O	SDRAM DQM for D7~D0	45
MD7/PPI_D7/ND_D7	IO	SDRAM D7	47

Pin Name	Type	Functionality Description (T302BA)	Pin #
MD6/PPI_D6/ND_D6	IO	SDRAM D6	49
MD5/PPI_D5/ND_D5	IO	SDRAM D5	50
MD4/PPI_D4/ND_D4	IO	SDRAM D4	51
MD3/PPI_D3/ND_D3	IO	SDRAM D3	52
MD2/PPI_D2/ND_D2	IO	SDRAM D2	53
MD1/PPI_D1/ND_D1	IO	SDRAM D1	54
MD0/PPI_D0/ND_D0	IO	SDRAM D0	55
SPI NOR Flash Interface (Note: SPI, PPI NOR and NAND are mutually exclusive on oard)			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	SPI NOR Chip Enable	67
MCAS#/PPI_OE#/SPI_SCK	O	SPI NOR Clock	42
LDQM/PPI_A21/SPI_SO	O	SPI Serial Data Output (to input of the flash)	45
UDQM/PPI_A22/SPI_SI	I	SPI Serial Data Input (from output of the flash)	56
PPI NOR Flash Interface			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	PPI NOR Chip Enable	67
MCAS#/PPI_OE#/SPI_SCK	O	PPI NOR OE#	42
MWE#/PPI_WE#/ND_WE#	O	PPI NOR WE#	43
UDQM/PPI_A22/SPI_SI	O	PPI NOR A22	56
LDQM/PPI_A21/SPI_SO	O	PPI NOR A21	45
MBA1/PPI_A20 (MA12_SDR)	IO	PPI NOR A20	38
MBA0/PPI_A19 (EJTAG_En_)	IO	PPI NOR A19	39
MD15/PPI_A18	IO	PPI NOR A18	66
MD14/PPI_A17	IO	PPI NOR A17	65
MD13/PPI_A16	IO	PPI NOR A16	64
MD12/PPI_A15	IO	PPI NOR A15	63
MD11/PPI_A14	IO	PPI NOR A14	61
MD10/PPI_A13	IO	PPI NOR A13	60
MD9/PPI_A12	IO	PPI NOR A12	58
MD8/PPI_A11	IO	PPI NOR A11	57
MA11/PPI_A10	O	PPI NOR A10	28
MA10/PPI_A9	O	PPI NOR A9	37
MA9/PPI_A8	O	PPI NOR A8	27
MA8/PPI_A7	O	PPI NOR A7	25
MA7/PPI_A6	O	PPI NOR A6	24
MA6/PPI_A5	O	PPI NOR A5	23
MA5/PPI_A4	O	PPI NOR A4	21
MA4/PPI_A3	O	PPI NOR A3	20
MA3/PPI_A2/ND_CLE (Strap[7])	IO	PPI NOR A2	32
MA2/PPI_A1/ND_ALE (Strap[6])	IO	PPI NOR A1	33
MA1/PPI_A0/ND_RE# (Strap[5])	IO	PPI NOR A0	34
MA0/PPI_AM1 (I2C_En_)	IO	PPI NOR A-1	35
MD7/PPI_D7/ND_D7	IO	PPI NOR D7	47
MD6/PPI_D6/ND_D6	IO	PPI NOR D6	49
MD5/PPI_D5/ND_D5	IO	PPI NOR D5	50
MD4/PPI_D4/ND_D4	IO	PPI NOR D4	51
MD3/PPI_D3/ND_D3	IO	PPI NOR D3	52
MD2/PPI_D2/ND_D2	IO	PPI NOR D2	53
MD1/PPI_D1/ND_D1	IO	PPI NOR D1	54
MD0/PPI_D0/ND_D0	IO	PPI NOR D0	55
NAND Flash Interface			

Pin Name	Type	Functionality Description (T302BA)	Pin #
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	NAND Chip Enable	67
MA3/PPI_A2/ND_CLE (Strap[7])	IO	NAND_CLE	32
MA2/PPI_A1/ND_ALE (Strap[6])	IO	NAND_ALE	33
MA1/PPI_A0/ND_RE# (Strap[5])	IO	NAND_RE#	34
MWE#/PPI_WE#/ND_WE#	O	NAND_WE#	43
ND_RDY_BYSN/VPWMP/GPIO14/xD_RE#	I	NAND_RDY_BSY#	68
ND_WP#/VCKP/GPIO15/xD_WE#	O	NAND_WP#	69
MD7/PPI_D7/ND_D7	IO	NAND_D7	47
MD6/PPI_D6/ND_D6	IO	NAND_D6	49
MD5/PPI_D5/ND_D5	IO	NAND_D5	50
MD4/PPI_D4/ND_D4	IO	NAND_D4	51
MD3/PPI_D3/ND_D3	IO	NAND_D3	52
MD2/PPI_D2/ND_D2	IO	NAND_D2	53
MD1/PPI_D1/ND_D1	IO	NAND_D1	54
MD0/PPI_D0/ND_D0	IO	NAND_D0	55
UART Interface			
SDA/RS232TX/xD_CLE	O	UART_TX	71
SCL/RS232RX/xD_ALE	I	UART_RX	72
ETJAG Interface			
SD_CD#/TCK	I	EJTAG_TCK	86
MS_CLK/SD_D1/CF_RESET_/TMS	I	EJTAG_TMS	87
MS_INS/TDI	I	EJTAG_TDI	85
(MS/SD/CF_)PWR_ON#/TRST#	I	EJTAG_TRST#	88
xD_D5/CF_D5/SD_CMD/TDO	O	EJTAG_TDO	91
Flash Card Power Interface			
(MS/SD/CF_)PWR_ON#/TRST#	O	Power On/Off for Flash card. (0: ON, 1: Off)	88
SD/MMC Card Interface			
SD_CD#/TCK	I	SD Card Detect	86
MS_CLK/SD_CLK/TMS	O	SD CLK	87
xD_D5/CF_D5/SD_CMD/TDO	IO	SD CMD	91
xD_D3/CF_D3/MS_D3/SD_D3	IO	SD D3	93
xD_D2/CF_D2/MS_D2/SD_D2	IO	SD D2	94
xD_D1/CF_D1/MS_D1/SD_D1	IO	SD D1	95
xD_D0/CF_D0/MS_D0/SD_D0	IO	SD D0	96
xD_D4/CF_D4/MS_BS/SD_WP	I	SD WP	92
MS/MS Pro Card Interface			
MS_INS/TDI	I	MS Card Insert	85
MS_CLK/SD_CLK/TMS	O	MS CLK	87
xD_D4/CF_D4/MS_BS/SD_WP	O	MS BS	92
xD_D3/CF_D3/MS_D3/SD_D3	IO	MS D3	93
xD_D2/CF_D2/MS_D2/SD_D2	IO	MS D2	94
xD_D1/CF_D1/MS_D1/SD_D1	IO	MS D1	95
xD_D0/CF_D0/MS_D0/SD_D0	IO	MS D0	96
XD/SM Card Interface			
MA12/xD_CD#/SM_CD#	I	XD/SM Card Detect	29
MCKE/xD_CE#/SM_CE#	O	XD/SM Chip Enable	30
xD_RDY_BSY#/CF_RDY_BSY#/ VCKN/PWM4/ND1_CE#	I	XD/SM RDY_BSY#	70

Pin Name	Type	Functionality Description (T302BA)	Pin #
SCL/RS232RX/xD_ALE	O	XD/SM ALE	72
SDA/RS232TX/xD_CLE	O	XD/SM CLE	71
PWM1/xD_WP#/ND1_CE#/VCKP	O	XD/SM WP#	97
CPH2/sD0/xD_RE#/VPWMP/PWM4	O	XD/SM RE#	106
CPH3/sD1/xD_WE#/VCKP/ND1_CE#	O	XD/SM WE#	107
xD_D7/CF_D7	IO	XD/SM D7	89
xD_D6/CF_D6	IO	XD/SM D6	90
xD_D5/CF_D5/SD_CMD/TDO	IO	XD/SM D5	91
xD_D4/CF_D4/MS_BS/SD_WP	IO	XD/SM D4	92
xD_D3/CF_D3/MS_D3/SD_D3	IO	XD/SM D3	93
xD_D2/CF_D2/MS_D2/SD_D2	IO	XD/SM D2	94
xD_D1/CF_D1/MS_D1/SD_D1	IO	XD/SM D1	95
xD_D0/CF_D0/MS_D0/SD_D0	IO	XD/SM D0	96
I2C Interface			
SDA/RS232TX/xD_CLE	IO	I2C_SDA	71
SCL/RS232RX/xD_ALE	IO	I2C_SCL	72
LCD TCON			
HSO/POL/VCOM	O	Hsync to panel, or Horizontal Polarity output or VCOM	101
VSO/STH1	O	Vsync to panel or Horizontal Start Pulse 1 Signal	102
DEO/INVO/STH2	O	Horizontal Output Data enable, or INVO or Horizontal Start Pulse 2 Signal	103
CPH1/CLKO	O	Clocks to panel	105
Q1H	O	Panel polarity control	108
LP/OEH/VCOM_I	O	Latch pulse for column driver	109
GCLK/CKV	O	Gate driver clock	110
GOE/OEV	O	Gate driver output enable	111
STV1 (SPI_Boot)	O	Gate driver start pulse 1	112
STV2 (NOR_Boot)	O	Gate driver start pulse 2	113
LCD Analog Output and Panel Backlight control			
IOB	O	B-channel analog output	117
IOG	O	G-channel analog output	118
IOR	O	R-channel analog output	119
VBGF	I	DAC voltage reference output	120
IOV	O	Composite Video Encoder output	122
RSETV	I	DAC reference current adjust for TV out	123
VCOMAMP	O	VCOM Amplify	126
VCOMDC	O	VCOM DC	127
VFB	I	Feedback of Lamp current (DC2DC)	1
VFBI	I	Feedback of Lamp current (LED or CCFL)	2
PWM2 (PWM_DC)	O	PWM output for DC2DC	98
PWM3 (PWM_LED or VPWMN)	O	PWM output for LED or VPWMN for CCFL	100
Audio I^2S Interface			
I2S_BCLK	O	Audio I^2S Bit clock output	
I2S_SDO	O	Audio I^2S Serial data output	
Misc.			
X12MI	I	12 MHz crystal input	18
X12MO	O	12 MHz crystal output	19

Pin Name	Type	Functionality Description (T302BA)	Pin #
SAR1	I	SARADC for keypads sense	128
PWM4/ND1_CE#/VCKP/I2S_WSO	O	PWM4 output	73
OUTL/OUTR	O	Audio DAC output (Left/Right channel)	4,5
Analog Power			
VD33ADAC	P33A	Audio DAC power 3.3V	6
OTG_VDDA	P33A	OTG power 3.3V	80
VD5A	P50A	Video DAC power 5.0V	116
VD33DAC	P33A	Video DAC power 3.3V	124
VD33PWM	P33A	PWM power 3.3V	125
Digital Power			
VDD33	P33	Digital IO power 3.3 V	26, 44, 62, 104
VDD18	P18	Core power 1.8V	17, 46, 83, 115
OTG_VDDL	P18	OTG VDDU 1.8V	75
Battery Power (3.3V)			
VDD33	P33	Battery Power for RTC IO, 3.3 V	9
Battery Power (1.8V)			
VDD18	P18	Battery Power for RTC core, 1.8V	10
GND (Analog)			
VS33ADAC	GNDA	Audio DAC Ground	3
PLL_GND	GNDA	PLL Ground	8
OTG_VSSA	GNDA	OTG VS33	79
VS33DAC	GNDA	Video DAC Ground	121
GND (Digital)			
GND	GND	Digital Ground	16, 22, 36, 48, 59, 74, 99, 114

Hardware Trapping Pins of T302BA

Pin #	Pin Symbol	Trapping Name	0 (pull-down) Determines :	1 (pull-up) Determines :
113	STV2/sD7 (NOR_Boot)	NOR_Boot	Boot from NAND	Boot from NOR
112	STV1/sD6 (SPI_Boot)	SPI_Boot	Boot from PPI NOR	Boot from SPI NOR
39	MBA0/PPI_A19 (EJTAG_En_)	EJTAG_En_	EJTAG Enable (no Flash Card allowed)	SD present
38	MBA1/PPI_A20 (MA12_SDR)	MA12_SDR	Pin-33/34 as MA12/MCKE	
35	MA0/PPI_AM1 (I2C_En_)	I2C_En_	Pin-70/71 as I2C func.	Pin-70/71 as UART func.
34	MA1/PPI_A0/ND_RE# (Strap[5])	Trap_5	Reserved	Reserved
33	MA2/PPI_A1/ND_ALE (Strap[6])	Trap_6	Reserved	Reserved
32	MA3/PPI_A2/ND_CLE (Strap[7])	Trap_7	Reserved	Reserved
20	MA4/PPI_A3 (Strap[8])	Trap_8		
21	MA5/PPI_A4 (Strap[9])	Trap_9	Trap[9:8] = 00: ND_CE0# (or the primary ND_CE0#) from FLASH_CE# (pin # 75) 01: CPH3 (pin # 119) --- Reserved 10: xD_RDY_BSY# (pin # 78) --- Reserved 11: PWM4 (pin # 81)	
23	MA6/PPI_A5 (Strap[10])	Trap_10	ND_CE1# at non-FLASH_CE# pin, and configured though firmware	ND_CE1# at FLASH_CE# pin

1.19 Pinout Diagram – T302BZ (128pin Analog panel, LED backlight support with audio I²S I/F)

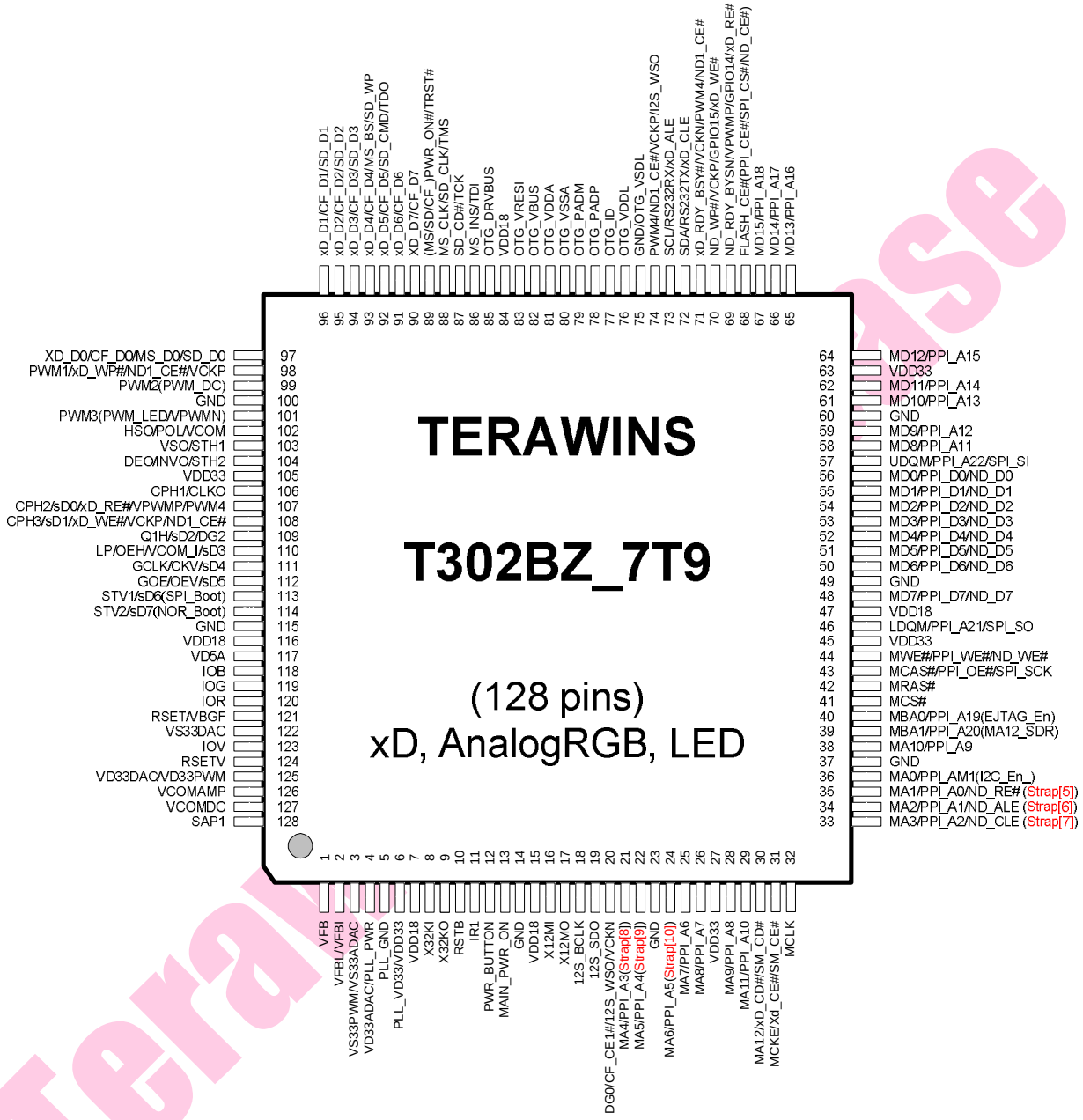


Figure 1-7 Pinout Diagram

T302BZ for Analog Panel, LED backlight 128pin Version

1.20 Pin Description – T302BZ (128pin)

Table 1-6 Pin Description

Pin Name	Type	Functionality Description (T302BZ)	Pin #
System Management Interface			
X32KI	I	32.768KHz crystal input	8
X32KO	O	32.768KHz crystal output	9
IR1	I	IR input	11
PWR_BUTTON	I	Power Up button pressed sensing signal	12
MAIN_PWR_ON	O	Signal to turn on main power	13
USB 2.0 OTG Interface			
OTG_ID	I	ID pin	77
OTG_PADP	IO	D+	78
OTG_PADM	IO	D-	79
OTG_VBUS	O	VBUS	82
OTG_VRES	I	Connect to Resistor with 8.2Kohm	83
OTG_DRVBUS	O	Signal to turn-on Vbus to provide power USB device (used in Host mode)	85
SDRAM Memory Interface			
MCLK	O	SDRAM clock	32
MCS#	O	SDRAM CS#	41
MRAS#	O	SDRAM RAS#	42
MCAS#/PPI_OE#/SPI_SCK	O	SDRAM CAS#	43
MWE#/PPI_WE#/ND_WE#	O	SDRAM WE#	44
MBA1/PPI_A20 (MA12_SDR)	IO	SDRAM BA1	39
MBA0/PPI_A19 (EJTAG_En_)	IO	SDRAM BA0	40
MA11/PPI_A10	O	SDRAM MA11	29
MA10/PPI_A9	O	SDRAM MA10	38
MA9/PPI_A8	O	SDRAM MA9	28
MA8/PPI_A7	O	SDRAM MA8	26
MA7/PPI_A6	O	SDRAM MA7	25
MA6/PPI_A5	O	SDRAM MA6	24
MA5/PPI_A4	O	SDRAM MA5	22
MA4/PPI_A3	O	SDRAM MA4	21
MA3/PPI_A2/ND_CLE (Strap[7])	IO	SDRAM MA3	33
MA2/PPI_A1/ND_ALE (Strap[6])	IO	SDRAM MA2	34
MA1/PPI_A0/ND_RE# (Strap[5])	IO	SDRAM MA1	35
MA0/PPI_AM1 (I2C_En_)	IO	SDRAM MA0	36
UDQM/PPI_A22/SPI_SI	O	SDRAM DQM for D15~D8	57
MD15/PPI_A18	IO	SDRAM D15	67
MD14/PPI_A17	IO	SDRAM D14	66
MD13/PPI_A16	IO	SDRAM D13	65
MD12/PPI_A15	IO	SDRAM D12	64
MD11/PPI_A14	IO	SDRAM D11	62
MD10/PPI_A13	IO	SDRAM D10	61
MD9/PPI_A12	IO	SDRAM D9	59
MD8/PPI_A11	IO	SDRAM D8	58
LDQM/PPI_A21/SPI_SO	O	SDRAM DQM for D7~D0	46
MD7/PPI_D7/ND_D7	IO	SDRAM D7	48

Pin Name	Type	Functionality Description (T302BZ)	Pin #
MD6/PPI_D6/ND_D6	IO	SDRAM D6	50
MD5/PPI_D5/ND_D5	IO	SDRAM D5	51
MD4/PPI_D4/ND_D4	IO	SDRAM D4	52
MD3/PPI_D3/ND_D3	IO	SDRAM D3	53
MD2/PPI_D2/ND_D2	IO	SDRAM D2	54
MD1/PPI_D1/ND_D1	IO	SDRAM D1	55
MD0/PPI_D0/ND_D0	IO	SDRAM D0	56
SPI NOR Flash Interface (Note: SPI, PPI NOR and NAND are mutually exclusive on oard)			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	SPI NOR Chip Enable	68
MCAS#/PPI_OE#/SPI_SCK	O	SPI NOR Clock	43
LDQM/PPI_A21/SPI_SO	O	SPI Serial Data Output (to input of the flash)	46
UDQM/PPI_A22/SPI_SI	I	SPI Serial Data Input (from output of the flash)	57
PPI NOR Flash Interface			
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	PPI NOR Chip Enable	68
MCAS#/PPI_OE#/SPI_SCK	O	PPI NOR OE#	43
MWE#/PPI_WE#/ND_WE#	O	PPI NOR WE#	44
UDQM/PPI_A22/SPI_SI	O	PPI NOR A22	57
LDQM/PPI_A21/SPI_SO	O	PPI NOR A21	46
MBA1/PPI_A20 (MA12_SDR)	IO	PPI NOR A20	39
MBA0/PPI_A19 (EJTAG_En_)	IO	PPI NOR A19	40
MD15/PPI_A18	IO	PPI NOR A18	67
MD14/PPI_A17	IO	PPI NOR A17	66
MD13/PPI_A16	IO	PPI NOR A16	65
MD12/PPI_A15	IO	PPI NOR A15	64
MD11/PPI_A14	IO	PPI NOR A14	62
MD10/PPI_A13	IO	PPI NOR A13	61
MD9/PPI_A12	IO	PPI NOR A12	59
MD8/PPI_A11	IO	PPI NOR A11	58
MA11/PPI_A10	O	PPI NOR A10	29
MA10/PPI_A9	O	PPI NOR A9	38
MA9/PPI_A8	O	PPI NOR A8	28
MA8/PPI_A7	O	PPI NOR A7	26
MA7/PPI_A6	O	PPI NOR A6	25
MA6/PPI_A5	O	PPI NOR A5	24
MA5/PPI_A4	O	PPI NOR A4	22
MA4/PPI_A3	O	PPI NOR A3	21
MA3/PPI_A2/ND_CLE (Strap[7])	IO	PPI NOR A2	33
MA2/PPI_A1/ND_ALE (Strap[6])	IO	PPI NOR A1	34
MA1/PPI_A0/ND_RE# (Strap[5])	IO	PPI NOR A0	35
MA0/PPI_AM1 (I2C_En_)	IO	PPI NOR A-1	36
MD7/PPI_D7/ND_D7	IO	PPI NOR D7	48
MD6/PPI_D6/ND_D6	IO	PPI NOR D6	50
MD5/PPI_D5/ND_D5	IO	PPI NOR D5	51
MD4/PPI_D4/ND_D4	IO	PPI NOR D4	52
MD3/PPI_D3/ND_D3	IO	PPI NOR D3	53
MD2/PPI_D2/ND_D2	IO	PPI NOR D2	54
MD1/PPI_D1/ND_D1	IO	PPI NOR D1	55
MD0/PPI_D0/ND_D0	IO	PPI NOR D0	56
NAND Flash Interface			

Pin Name	Type	Functionality Description (T302BZ)	Pin #
FLASH_CE# (PPI_CE#/SPI_CS#/ND_CE#)	O	NAND Chip Enable	68
MA3/PPI_A2/ND_CLE (Strap[7])	IO	NAND_CLE	33
MA2/PPI_A1/ND_ALE (Strap[6])	IO	NAND_ALE	34
MA1/PPI_A0/ND_RE# (Strap[5])	IO	NAND_RE#	35
MWE#/PPI_WE#/ND_WE#	O	NAND_WE#	44
ND_RDY_BYSN/VPWMP/GPIO14/xD_RE#	I	NAND_RDY_BSY#	69
ND_WP#/VCKP/GPIO15/xD_WE#	O	NAND_WP#	70
MD7/PPI_D7/ND_D7	IO	NAND_D7	48
MD6/PPI_D6/ND_D6	IO	NAND_D6	50
MD5/PPI_D5/ND_D5	IO	NAND_D5	51
MD4/PPI_D4/ND_D4	IO	NAND_D4	52
MD3/PPI_D3/ND_D3	IO	NAND_D3	53
MD2/PPI_D2/ND_D2	IO	NAND_D2	54
MD1/PPI_D1/ND_D1	IO	NAND_D1	55
MD0/PPI_D0/ND_D0	IO	NAND_D0	56
UART Interface			
SDA/RS232TX/xD_CLE	O	UART_TX	72
SCL/RS232RX/xD_ALE	I	UART_RX	73
ETJAG Interface			
SD_CD#/TCK	I	EJTAG_TCK	87
MS_CLK/SD_D1/CF_RESET_/TMS	I	EJTAG_TMS	88
MS_INS/TDI	I	EJTAG_TDI	86
(MS/SD/CF_)PWR_ON#/TRST#	I	EJTAG_TRST#	89
xD_D5/CF_D5/SD_CMD/TDO	O	EJTAG_TDO	92
Flash Card Power Interface			
(MS/SD/CF_)PWR_ON#/TRST#	O	Power On/Off for Flash card. (0: ON, 1: Off)	89
SD/MMC Card Interface			
SD_CD#/TCK	I	SD Card Detect	87
MS_CLK/SD_CLK/TMS	O	SD CLK	88
xD_D5/CF_D5/SD_CMD/TDO	IO	SD CMD	92
xD_D3/CF_D3/MS_D3/SD_D3	IO	SD D3	94
xD_D2/CF_D2/MS_D2/SD_D2	IO	SD D2	95
xD_D1/CF_D1/MS_D1/SD_D1	IO	SD D1	96
xD_D0/CF_D0/MS_D0/SD_D0	IO	SD D0	97
xD_D4/CF_D4/MS_BS/SD_WP	I	SD WP	93
MS/MS Pro Card Interface			
MS_INS/TDI	I	MS Card Insert	86
MS_CLK/SD_CLK/TMS	O	MS CLK	88
xD_D4/CF_D4/MS_BS/SD_WP	O	MS BS	93
xD_D3/CF_D3/MS_D3/SD_D3	IO	MS D3	94
xD_D2/CF_D2/MS_D2/SD_D2	IO	MS D2	95
xD_D1/CF_D1/MS_D1/SD_D1	IO	MS D1	96
xD_D0/CF_D0/MS_D0/SD_D0	IO	MS D0	97
XD/SM Card Interface			
MA12/xD_CD#/SM_CD#	I	XD/SM Card Detect	30
MCKE/xD_CE#/SM_CE#	O	XD/SM Chip Enable	31
xD_RDY_BSY#/CF_RDY_BSY#/ VCKN/PWM4/ND1_CE#	I	XD/SM RDY_BSY#	71

Pin Name	Type	Functionality Description (T302BZ)	Pin #
SCL/RS232RX/xD_ALE	O	XD/SM ALE	73
SDA/RS232TX/xD_CLE	O	XD/SM CLE	72
PWM1/xD_WP#/ND1_CE#/VCKP	O	XD/SM WP#	98
CPH2/sD0/xD_RE#/VPWMP/PWM4	O	XD/SM RE#	107
CPH3/sD1/xD_WE#/VCKP/ND1_CE#	O	XD/SM WE#	108
xD_D7/CF_D7	IO	XD/SM D7	90
xD_D6/CF_D6	IO	XD/SM D6	91
xD_D5/CF_D5/SD_CMD/TDO	IO	XD/SM D5	92
xD_D4/CF_D4/MS_BS/SD_WP	IO	XD/SM D4	93
xD_D3/CF_D3/MS_D3/SD_D3	IO	XD/SM D3	94
xD_D2/CF_D2/MS_D2/SD_D2	IO	XD/SM D2	95
xD_D1/CF_D1/MS_D1/SD_D1	IO	XD/SM D1	96
xD_D0/CF_D0/MS_D0/SD_D0	IO	XD/SM D0	97
I2C Interface			
SDA/RS232TX/xD_CLE	IO	I2C_SDA	72
SCL/RS232RX/xD_ALE	IO	I2C_SCL	73
LCD TCON			
HSO/POL/VCOM	O	Hsync to panel, or Horizontal Polarity output or VCOM	102
VSO/STH1	O	Vsync to panel or Horizontal Start Pulse 1 Signal	103
DEO/INVO/STH2	O	Horizontal Output Data enable, or INVO or Horizontal Start Pulse 2 Signal	104
CPH1/CLKO	O	Clocks to panel	106
Q1H	O	Panel polarity control	109
LP/OEH/VCOM_I	O	Latch pulse for column driver	110
GCLK/CKV	O	Gate driver clock	111
GOE/OEV	O	Gate driver output enable	112
STV1 (SPI_Boot)	O	Gate driver start pulse 1	113
STV2 (NOR_Boot)	O	Gate driver start pulse 2	114
LCD Analog Output and Panel Backlight control			
IOB	O	B-channel analog output	118
IOG	O	G-channel analog output	119
IOR	O	R-channel analog output	120
VBGF	I	DAC voltage reference output	121
IOV	O	Composite Video Encoder output	123
RSETV	I	DAC reference current adjust for TV out	124
VCOMAMP	O	VCOM Amplify	126
VCOMDC	O	VCOM DC	127
VFB	I	Feedback of Lamp current (DC2DC)	1
VFBI	I	Feedback of Lamp current (LED or CCFL)	2
PWM2 (PWM_DC)	O	PWM output for DC2DC	99
PWM3 (PWM_LED or VPWMN)	O	PWM output for LED or VPWMN for CCFL	101
Audio I^2S Interface			
I2S_BCLK	O	Audio I^2S Bit clock output	18
I2S_SDO	O	Audio I^2S Serial data output	19
Misc.			
X12MI	I	12 MHz crystal input	16
X12MO	O	12 MHz crystal output	17

Pin Name	Type	Functionality Description (T302BZ)	Pin #
SAR1	I	SARADC for keypads sense	128
PWM4/ND1_CE#/VCKP/I2S_WSO	O	PWM4 output	74
Analog Power			
VD33ADAC	P33A	Audio DAC power 3.3V	4
OTG_VDDA	P33A	OTG power 3.3V	81
VD5A	P50A	Video DAC power 5.0V	117
VD33DAC	P33A	Video DAC power 3.3V	125
VD33PWM	P33A	PWM power 3.3V	125
Digital Power			
VDD33	P33	Digital IO power 3.3 V	27, 45, 63, 105
VDD18	P18	Core power 1.8V	15, 47, 84, 116
OTG_VDDL	P18	OTG VDDU 1.8V	76
Battery Power (3.3V)			
VDD33	P33	Battery Power for RTC IO, 3.3 V	6
Battery Power (1.8V)			
VDD18	P18	Battery Power for RTC core, 1.8V	7
GND (Analog)			
VS33ADAC	GNDA	Audio DAC Ground	3
PLL_GND	GNDA	PLL Ground	5
OTG_VSSA	GNDA	OTG VS33	80
VS33DAC	GNDA	Video DAC Ground	122
GND (Digital)			
GND	GND	Digital Ground	14, 23, 37, 49, 60, 75, 100, 115

Hardware Trapping Pins of T302BZ

Pin #	Pin Symbol	Trapping Name	0 (pull-down) Determines :	1 (pull-up) Determines :
114	STV2/sD7 (NOR_Boot)	NOR_Boot	Boot from NAND	Boot from NOR
113	STV1/sD6 (SPI_Boot)	SPI_Boot	Boot from PPI NOR	Boot from SPI NOR
40	MBA0/PPI_A19 (EJTAG_En_)	EJTAG_En_	EJTAG Enable (no Flash Card allowed)	SD present
39	MBA1/PPI_A20 (MA12_SDR)	MA12_SDR	Pin-33/34 as MA12/MCKE	
36	MA0/PPI_AM1 (I2C_En_)	I2C_En_	Pin-70/71 as I2C func.	Pin-70/71 as UART func.
35	MA1/PPI_A0/ND_RE# (Strap[5])	Trap_5	Reserved	Reserved
34	MA2/PPI_A1/ND_ALE (Strap[6])	Trap_6	Reserved	Reserved
33	MA3/PPI_A2/ND_CLE (Strap[7])	Trap_7	Reserved	Reserved
21	MA4/PPI_A3 (Strap[8])	Trap_8		
22	MA5/PPI_A4 (Strap[9])	Trap_9	Trap[9:8] / ND_CE0# (or the primary ND_CE0#) from 00 / FLASH_CE# (pin # 75) 01 / CPH3 (pin # 119) --- Reserved 10 / xD_RDY_BSY# (pin # 78) --- Reserved 11 / PWM4 (pin # 81)	
24	MA6/PPI_A5 (Strap[10])	Trap_10	ND_CE1# at non-FLASH_CE# pin, and configured though firmware	ND_CE1# at FLASH_CE# pin

2 Theory of Operations

2.1 The CPU

T302B embedded an internal on-chip MIPS32 4Kec CPU core with MMU (Memory Management Unit). This CPU core implements the MIPS32 Release 2 Architecture and includes a Multiply/Divide Unit that implements single cycle MAC instructions, which enable DSP algorithms to be performed efficiently. It allows 32-bit x 16-bit MAC instructions to be issued every cycle, while a 32-bit x 32-bit MAC instruction can be issued every 2 cycles. MIPS32 instruction cache and data caches are both 8KB with 4-way set associative.

- **Audio/Voice compression and decompression by the CPU**

With maximum operational clock frequency up to 120 MHz and separate instruction cache and data caches both 8KB with 4-way set associative, the major tasks of the CPU are , but not limit to, for running O.S., system control and user interface and some graphic programming, and USB protocol stack. Besides, many application programs are all suitable to run on the CPU. For example, it is natural to rely on the CPU core to run audio/music & voice compression and decompression for recording and playback with the assist of the enhanced MAC support inside the core.

In order save power, the T302B adapts an easy way to allow S/W to adjust the clock frequency of the CPU (and the whole chip) dynamically or on the way. That is , the S/W can easily slowdown or speed up the clock frequency of the CPU to fit current operational computing power requirement just through simple register setting without rebooting the system.

2.2 The Hardwired JPEG and Motion-JPEG decompression engine

One of the major building blocks inside T302B is the hardwired JPEG and Motion-JPEG decompression engine. The major features of this JPEG engine are

- Support JPEG baseline profile, which used in digital camera, with YcbCr-444/YcbCr-422/YcbCr-420 and gray-level encoding.
- The maximum image size to be decoded is 8192x8192 YcbCr-444.
- The upper limit of decompression speed for Motion-JPEG is 640x480@30fps with operational clock frequency of 120 MHz.
- In order to minimize the required external buffer in SDRAM for a large image size, an intelligent segmentation mechanism for bitstream input buffer and reconstruction image buffer are adopted. With this, it is possible to minimize the total size of SDRAM required to build a digital photo frame supporting image size up to 16Mpixel down to 8MB.
- An optimized frequency domain first-level scaling down algorithm is adopted to speed up the decompression speed for large size image to be displayed on a relative small LCD panel.

Image rotation function is also built in hardware to speed up the rendering process for popular photos which shot with the vertical dimension larger than horizontal dimension.

2.3 On-chip Video DAC for TV-out display

There are cost-effective 10-bit on-chip video D/A converters for NTSC/PAL standard signals output to TV set. It's easy to display image and video on home TV everywhere.

2.4 On-chip audio DAC for recording and playback

There are cost-effective 12-bit on-chip DAC converters for audio playback.

2.5 On-chip SAR

With this on-chip SAR, low-resolution A/D converter, the key pads function can be easily implemented.

2.6 USB 2.0 high speed OTG controller up to 480 Mb/s

In conjunction with built-in USB 2.0 PHY, this USB 2.0 high speed OTG controller can operate as an USB device to connect to PC up to 480 Mb/s in physical layer. No HNP is supported to allow role change after connection is set up.

2.7 Flash Card reader interface

All available flash cards are supported by the flash card host controllers in T302B through the flash card reader interface. Including,

- SD/MMC
- MS/MS pro
- Smart Media
- Compact Flash

The DMA mode of all the flash card host controllers can be enabled to transfer data between system memory and flash cards to have best performance while still with minimum intervention of the CPU. Then CPU can be reserved for other computation intensive tasks like audio decompression.

2.8 Descriptor-based DMA engine

T302B has built-in a descriptor based DMA engine which supports the following functions:

- Memory to Memory copy, -- this is useful for data movement in SDRAM with the CPU only to program the DMA engine.
- Memory to IO device, IO device to Memory data copy – all high throughput IO devices can improve performance through this mode. The IO device controllers with request channel to the DMA engine are – CF, SD/MMC, MS/Mspro, xD/SmartMedia, NOR flash, NAND flash and I2S for external audio codecs.
- IO device to IO device data copy.

2.9 On-chip peripherals

The on-chip peripherals and other system blocks of T302B include,

- I2S interface for external audio codec with high quality – Besides the built-in on-chip 12-bit audio/voice A/D, D/A data converter, T302B also support the I2S interface for high quality external audio codec with 16-bit or higher resolution.
- 2-wire serial bus interface – 2-wire SCL and SDA
- EJTAG is built-in the MIPS CPU core to help software development process.
- UART – TX and RX is supported by T302B to connect to UART interface for data communication. This UART interface can also serve as the com port to connect to PC for system S/W development.
- GPIOs – multifunction GPIOs support is possible.
- The interrupt controller, System timer and Watch dog timer– the basic indispensable building blocks are there.

2.10 Power Management Unit

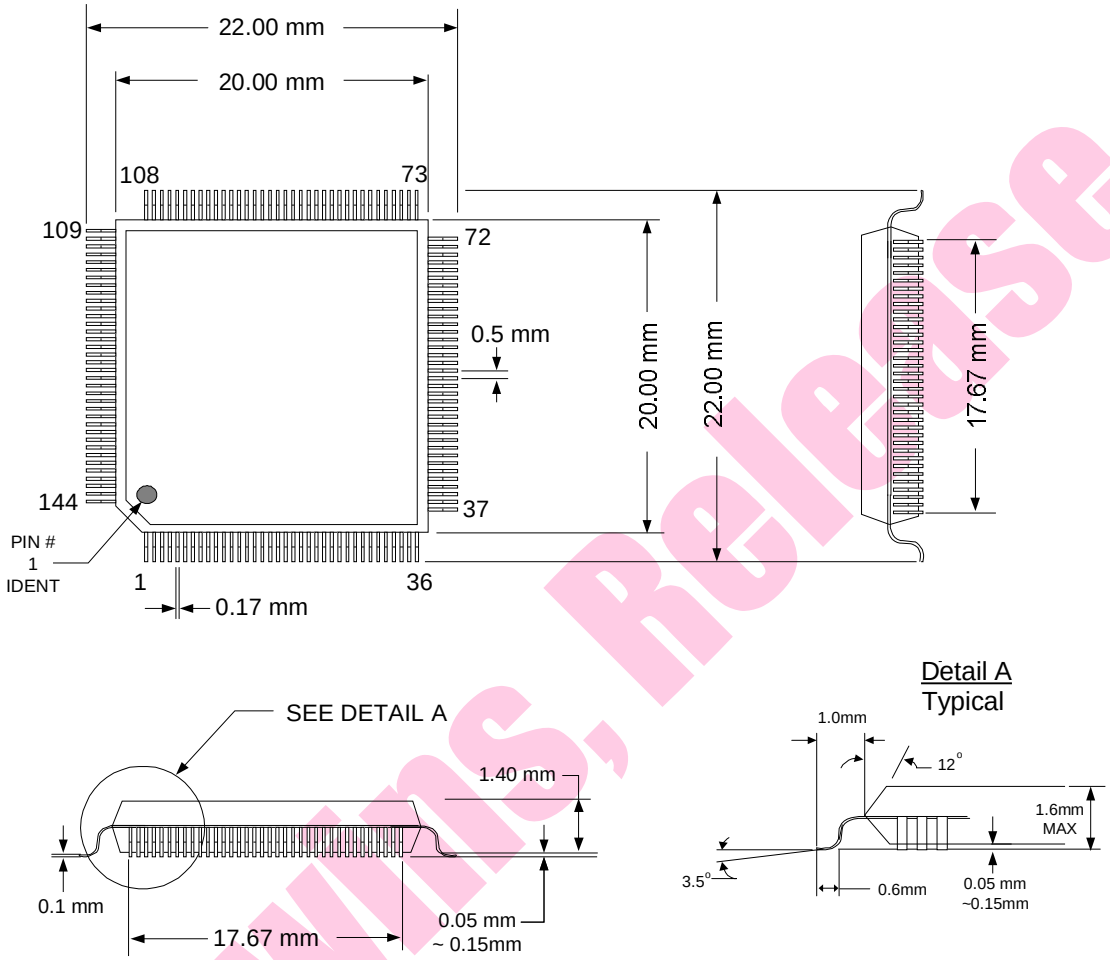
For portable application, the power consumption plays an important role. T302B has a power management unit with the following features to allow the system using the only necessary power for the tasks without any waste.

- Dynamic operational clock frequency adjustments – With only control register programming by the S/W, the built-in PLLs, clock dividers can be set to different values to dynamically adjust the clock frequencies for different hardware modules and the CPU and the SDRAM interface depending the application's needs.
- T302B supports 2 separate power domains – main power and battery power and there are 3 modes to consume power at different degree,
  1. Operational Mode – dynamic clock frequency adjustment can be applied to use minimum power for work
  2. Suspend Mode – All clocks source are stopped, the system can resume by external triggers.
  3. Shutdown mode – the main power is cut off only battery power is active.

2.11 Built-in Real-Time Clock (RTC) for alarm function

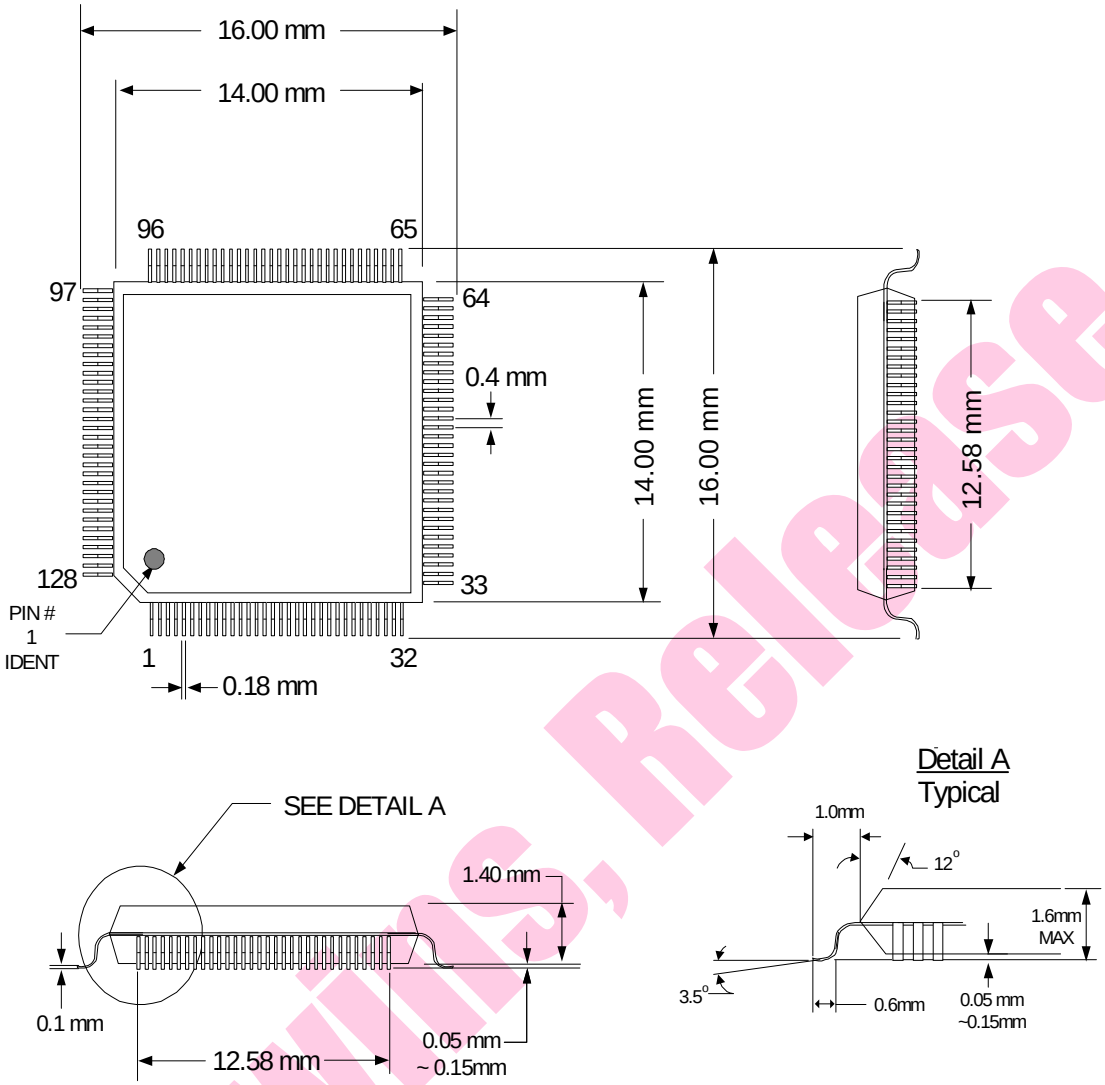
T302B has built-in Real-Time clock for alarm function. In order to save power for alarm function, the system S/W will bring T302B into shutdown mode to leave only battery power active to support the operation of the RTC, the main power for other functional blocks is shutting down. While the alarm tick is reached, the RTC module will turn on the main power before going to interrupt the CPU for ringing.

3 Package Dimensions



144 LQFP 20 X 20 X 1.4 mm

Figure 3-1 144-pin LQFP Dimensions.



128 LQFP 14 X 14 X 1.4 mm

Figure 3-2 128-pin LQFP Dimensions.

3.1 Absolute Maximum Rating

Table 3-1 Min AND Max Temperature

	Parameter	Min	Max	Unit
Topr	Operation Temperature	-20	+85	℃
Tstg	Storage Temperature	-65	+150	℃

4 Ordering Information

Table 4-1

Part No.	Package
T302BC, T302BI, T302BD T302BT, T302BV	144 LQFP
T302BA, T302BZ	128 LQFP

5 Revisions Note

Table 5-1

Revisions	Description of changes	Date	Note
0.1	First draft	SEP. 25, 2006	
0.9	Preliminary Release	OCT.25, 2007	
1.00	First brief spec. release	JAN.31, 2008	
1.01	Add T302BI, T302BU, T302BB pin definition & package	Mar. 14, 2008	
1.05	Add T302BD, T302BV, T302BA, T302BZ packages Remove T302BB package	June 26, 2008	

6 General Disclaimer

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