AVR32/64SD20/28/32/48

AVR® SD Product Brief

Introduction

The AVR® SD Family microcontrollers, designed in compliance with the ISO 26262 and IEC 61508 functional safety standards, use the AVR® CPU with a hardware multiplier running at clock speeds up to 20 MHz. They include 32/64 KB of Flash, 4/8 KB of SRAM, and 256 bytes of EEPROM. The microcontrollers are available in 20-, 28-, 32- and 48-pin packages. The family uses our latest technologies, with a flexible and low-power architecture, including an Event System, accurate analog features, and advanced digital peripherals. The AVR® SD provides a dual-core lockstep CPU, Single-Error Correcting and Double-Error Detecting (SECDED) ECC on Flash, EEPROM and SRAM, Error Controller, and Program and Debug Interface Disable (PDID) for functional safety.

Features

- AVR CPU in Dual-Core Lockstep (DCLS) Configuration
  - Running at up to 20 MHz
  - Single-cycle I/O access
  - Two-level interrupt controller
  - Two-cycle hardware multiplier
  - Supply voltage range: 2.7-5.5V
- Memories
  - 32 /64 KB in-system-programmable Flash memory with ECC
  - 4/8 KB SRAM with ECC
  - 256B EEPROM with ECC
  - 512B of user row in Non-Volatile Memory (NVM) that can keep data during chip-erase and be programmed while the device is locked
  - 256B of Boot Row for cryptographic keys, only readable from the Boot Section
- System
  - Power-On Reset (POR)
  - Brown-Out Detector (BOD) with programmable levels
  - Voltage Regulator Monitor (VREGMON)
  - Clock Options
    - High-precision internal oscillator with selectable frequency up to 20 MHz
    - PLL up to 48 MHz for high-frequency operation of the TCD
    - Internal 32.768 kHz oscillator
    - External 32.768 kHz crystal oscillator
    - External clock input
    - High-frequency external crystal oscillator
  - Clock Failure Detection (CFD)

  - Clock Frequency Measurement (CFM)
  - Single-pin Unified Program and Debug Interface (UPDI)
  - Three sleep modes
    - Idle with all peripherals running for immediate wake-up
    - Standby with a configurable operation of selected peripherals
    - Power-Down with full data retention
  - Automated Cyclic Redundancy Check (CRCSCAN) program memory scan
    - Verify the integrity of the entire Flash section, application code, and/or boot section
    - CRC-16-CCITT or CRC-32 (IEEE 802.3)
  - External interrupt on all general-purpose pins
- Peripherals
  - 6-channel Event System for predictable and CPU-independent inter-peripheral signaling
  - One 16-bit Timer/Counter type A (TCA) with three compare channels for PWM and waveform generation
  - Up to four 16-bit Timer/Counter type B (TCB) with input capture for capture and signal measurements
  - One 12-bit Timer/Counter type D (TCD) optimized for power control
  - One 16-bit Real-Time Counter (RTC) that can run from an external crystal or internal oscillator
  - Up to three USARTs
    - Operation modes: RS-485, LIN client, host SPI and IrDA
    - Fractional baud rate generator, auto-baud, and start-of-frame detection
  - Two SPI with host/client operation modes
  - Two I^2C with simultaneous host/client operation (dual mode) and dual address match
  - One Configurable Custom Logic (CCL) with up to six programmable Lookup Tables (LUTs)
  - Two 10-bit, 100 ksps, Analog-to-Digital Converters (ADC)
  - One 10-bit Digital-to-Analog Converter (DAC)
  - Three Analog Comparators (AC)
  - Two Zero Cross Detectors (ZCD)
  - Internal 2.048V, 4.096V and 2.500V voltage references, and external reference option
- System Integrity Functions
  - Error Controller (ERRCTRL)
    - Central interface for fault detection
    - Fault handling in hardware according to programmable severity
    - Optional Heartbeat output
    - Optional tri-stating of all I/O pins in case of fault
  - Program and Debug Interface Disable (PDID)
  - Parity on data buses
  - Dual Watchdogs
    - Synchronous Watchdog Timer (SWDT)
    - Watchdog Timer (WDT) with window mode and separate on-chip oscillator with clock failure detection
  - Voltage Level Monitor (VLM) with interrupt
- I/O and Packages
  - Up to 40 programmable I/O pins

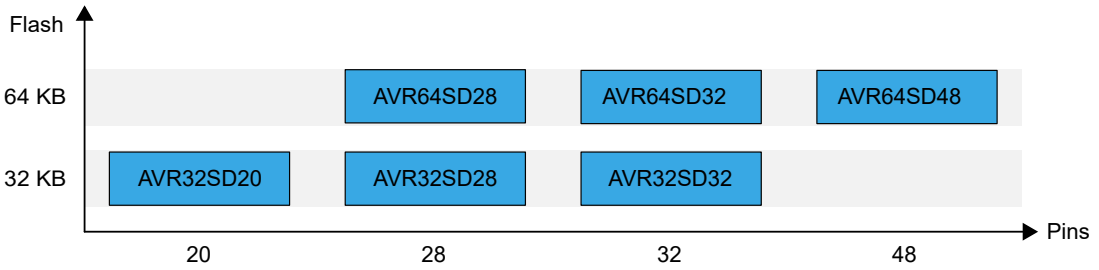
  - Multi-voltage I/O with built-in voltage level converters
  - 20-pin SSOP
  - 28-pin VQFN (WF), SSOP, and SPDIP
  - 32-pin VQFN (WF) and TQFP
  - 48-pin VQFN (WF) and TQFP
- Temperature Ranges
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

AVR® SD Family Overview

The figure below shows the AVR SD devices, laying out pin count variants and memory sizes:

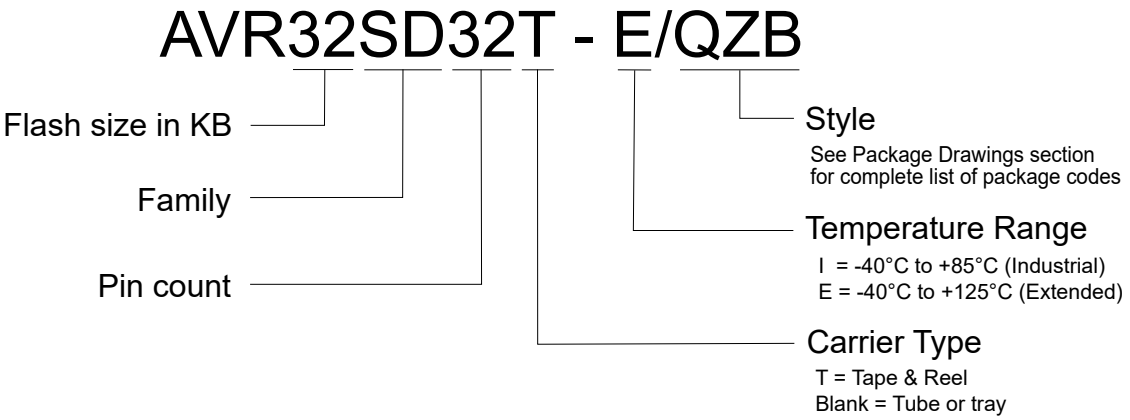
- Vertical migration is possible without code modification, as these devices are fully pin and feature compatible
- Horizontal migration to the left reduces the pin count and, therefore, the available features

Figure 1. AVR SD Family Overview



The name of a device in the AVR SD Family is decoded as follows:

Figure 2. AVR® SD Device Designations



Memory Overview

The following table shows the memory overview of the entire AVR SD family.

Table 1. Memory Overview

Devices	AVR32SD20 AVR32SD28 AVR32SD32	AVR64SD28 AVR64SD32 AVR64SD48
Flash memory with ECC	32 KB	64 KB
SRAM with ECC	4 KB	8 KB
EEPROM	256B	256B
User row	512B	512B
Cryptographic key storage	256B	256B

Peripheral Overview

The following table shows the peripheral overview of the entire AVR SD family.

Table 2. Peripheral Overview

Feature	AVR32SD20	AVR32SD28 AVR64SD28	AVR32SD32 AVR64SD32	AVR64SD48
Pins	**20**	**28**	**32**	**48**
Max. frequency (MHz)	20	20	20	20
Clock Controller (CLKCTRL) with Clock Failure Detection (CFD) and Clock Frequency Measurement (CFM)	1	1	1	1
Clock Failure Detection (CFD)	2	2	2	2
Clock Frequency Measurement (CFM)	2	2	2	2
16-bit Timer/Counter type A (TCA)	1	1	1	1
16-bit Timer/Counter type B (TCB)	4	4	4	4
12-bit Timer/Counter type D (TCD)	1	1	1	1
Real-Time Counter (RTC)	1	1	1	1
USART	2	3	3	3
SPI	2	2	2	2
TWI/I^2C[1]	1[1]	1[1]	2[1]	2[1]
10-bit ADC (channels)	2 (13)	2 (19)	2 (19)	2 (24)
Analog Comparator (AC)	3	3	3	3
Digital-to-Analog Converter (DAC)	1	1	1	1
Zero Cross Detector (ZCD)	2	2	2	2
Configurable Custom Logic Look-up Table (CCL LUT)	6	6	6	6
Error Controller (ERRCTRL)	1	1	1	1
Synchronous Watchdog Timer (SWDT)	1	1	1	1
Watchdog Timer (WDT)	1	1	1	1
Event System (EVSYS) channels	6	6	6	6
General Purpose I/O	15	21	25	40
PORT	PA[7:0], PC[3:1], PD[7:4]	PA[7:0], PC[3:0], PD[7:1], PF[1:0]	PA[7:0], PC[3:0], PD[7:1], PF[5:0]	PA[7:0], PB[5:0], PC[7:0], PD[7:0], PE[3:0], PF[5:0]
PORT pins with MVIO capability	PC[3:1]	PC[3:0]	PC[3:0]	PC[7:0]
External interrupts	15	21	25	40
CRCSCAN	1	1	1	1
Unified Program and Debug Interface (UPDI)	1	1	1	1

Note:

1. The TWI/I^2C can operate simultaneously as host and client on different pins.

Table of Contents

1. Functional Safety Concept

The devices of the AVR SD Family are general purpose microcontrollers designed according to the ISO 26262 and IEC 61508 safety standards to avoid systematic device faults.

The device family aims to mitigate risks and prevent failures that could lead to hazardous situations, minimize the required development of complex and time-consuming software diagnostics, and reduce the fault detection time for faults in vital functions down to 1 ms.

The AVR SD devices feature autonomous hardware fault detection mechanisms to detect, correct, and report random hardware faults and transient faults in the CPU and the infrastructure it relies upon. This Core-Independent Safety (CIS) makes the devices of the AVR SD Family highly suitable for safety-critical applications with strict safety requirements and demands for fast fault handling. The AVR SD devices suit for safety-critical applications with ISO 26262 (ASIL C) and IEC 61508 (SIL 2) safety requirements.

The primary Core-Independent Safety (CIS) features for the AVR SD devices are:

- Error controller, able to autonomously set the device in a safe state upon detection of a critical fault
- Dual CPU core in lock step configuration with redundant comparators
- ECC protection of Flash, EEPROM and SRAM memories
- Parity protection of data bus, with redundant control signals
- CRC and ECC protection of device configuration and calibration fuses
- Clock frequency monitor and failure detection
- Over- and under-voltage detectors for the internal voltage regulator (VREGMON)
- Dual watchdogs to detect hardware and software faults (WDT and SWDT)
- Stack monitor to detect software faults
- Redundant operation of most peripherals through duplication
- Various other integrity check mechanisms

Functional safety documentation and software are available. These are complemented by a rich set of safety-qualified MPLAB® development tools.

2. Security Concept

The AVR SD devices are general purpose microcontrollers that offer fundamental security features to implement secure firmware upgrades and authenticate the application firmware. When using the security features correctly, they protect against remote attacks and some PCB-level attacks where the application code is attempted modified to change the product functionality.

The cornerstone of the security features is the *Program and Debug Interface Disable (PDID)*, a mechanism preventing access to the device's reprogrammable Flash memory over the programming interface (UPDI). After the PDID is activated, the programming interface (UPDI) is prevented from making any changes to the device. The programming interface (UPDI) can still read out the device information and CRC status, and also the contents of the Flash memory, as long as the device is not locked.

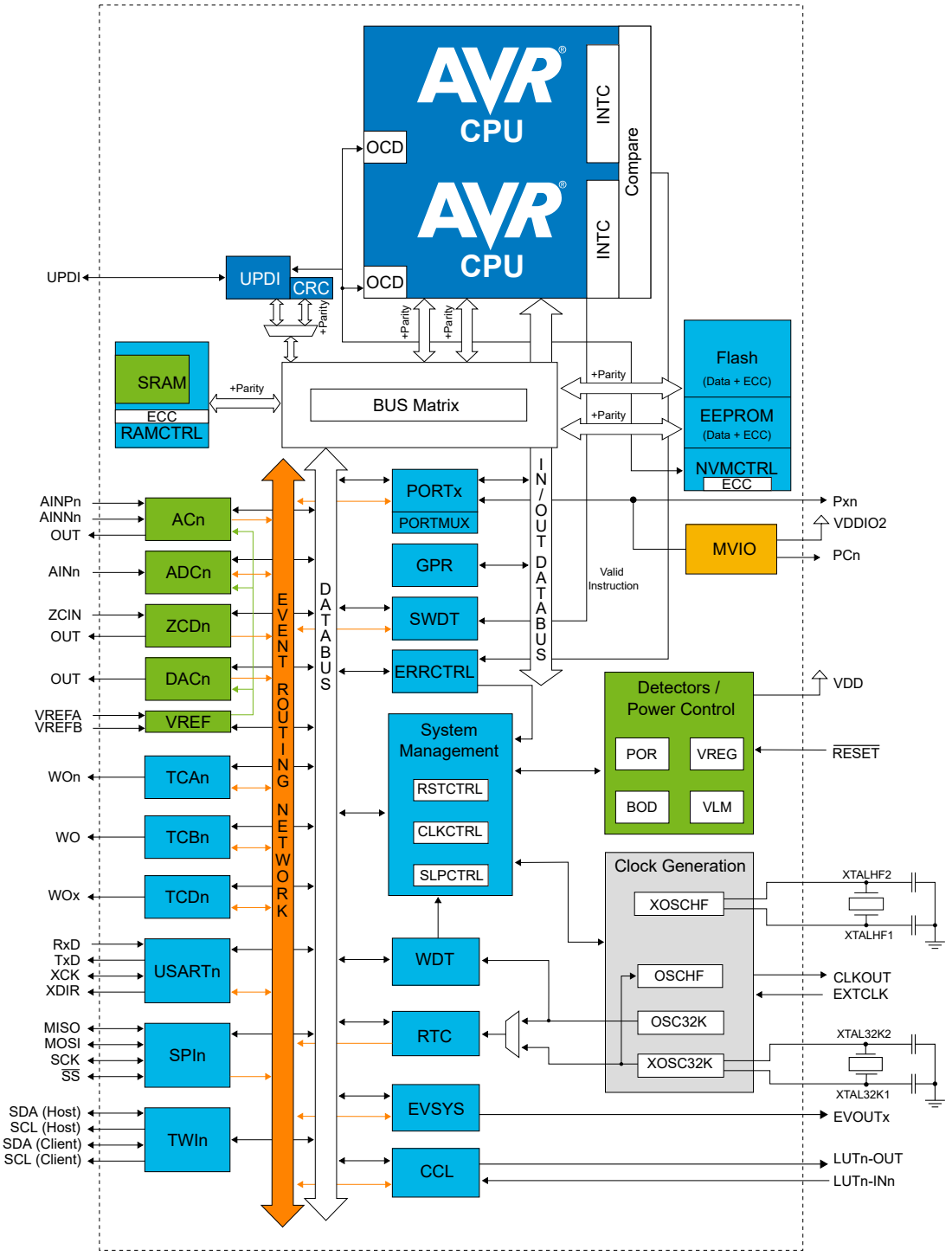
The only way to program the device after activating the PDID is by using software stored in the Boot Code section of the Flash to update the Application Code section software. This application-specific software must be able to receive new data and program the Application Code section. It is impossible to alter code stored in the Boot Code section using this mechanism, as the Boot Code section is only accessible using the programming interface (UPDI).

In addition, there is a separate storage space accessible only by code in the Boot Code section, which can hold any data that is intended to be accessible only from the Boot Code section. One example of this is a cryptographic key to be used to validate data that are sent to a bootloader to update the application software on the device.

This creates a two-layer security: The device is prevented from being erased or reprogrammed over the programming interface (UPDI), and by that, the code in the Boot Code section is protected. Secondly, the code in the Boot Code section can use a cryptographic key (that is only accessible by code in this section of Flash) to verify that any new application code that is received for the device software update is authentic.

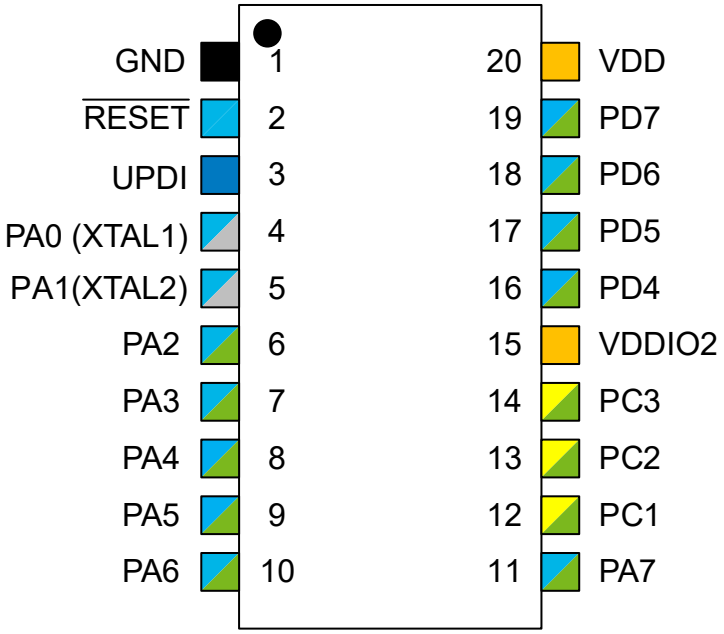
Using the *Program and Debug Interface Disable (PDID)* in software requires cryptographic competencies to ensure conformity to cyber-security standards such as ISO/SAE DIS 21434.

3. Block Diagram



4. Pinout

4.1 20-Pin SSOP



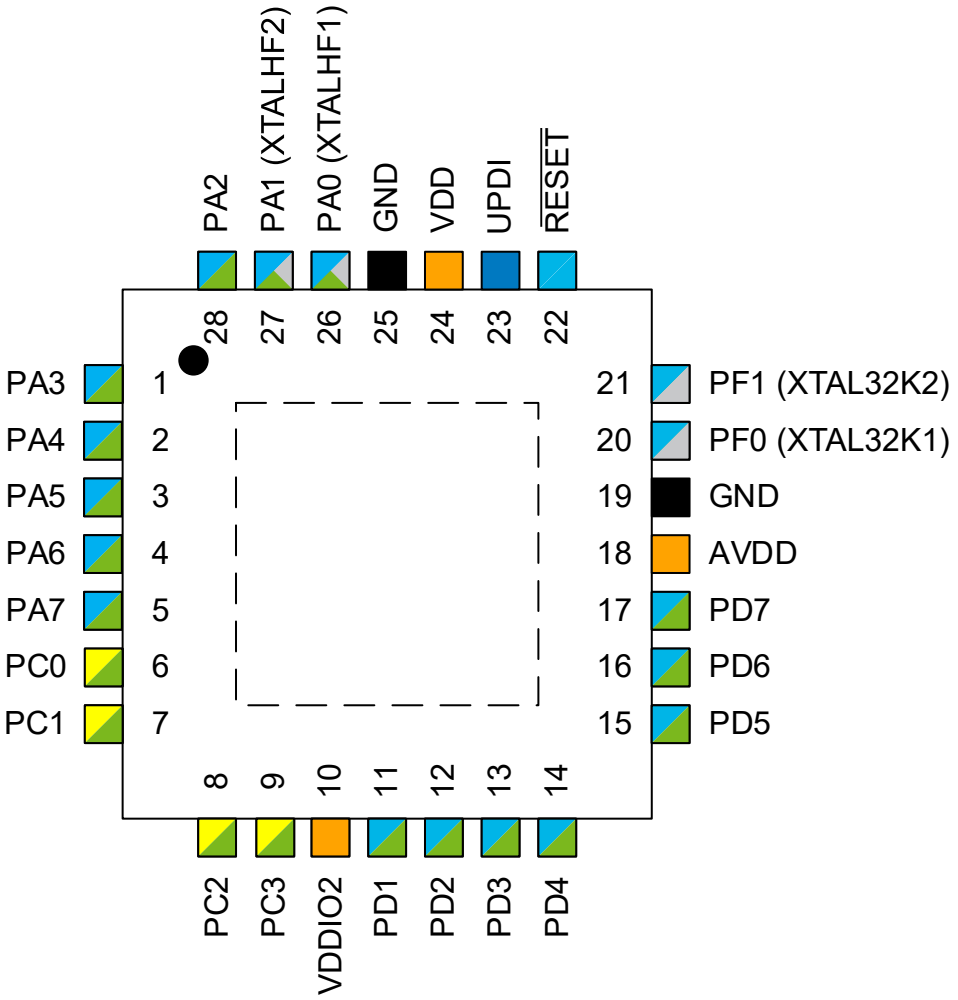
Power

- Power Supply
- Ground
- Pin on VDD Power Domain
- Pin on VDDIO2 Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- Digital Function Only
- Analog Function

4.2 28-Pin VQFN



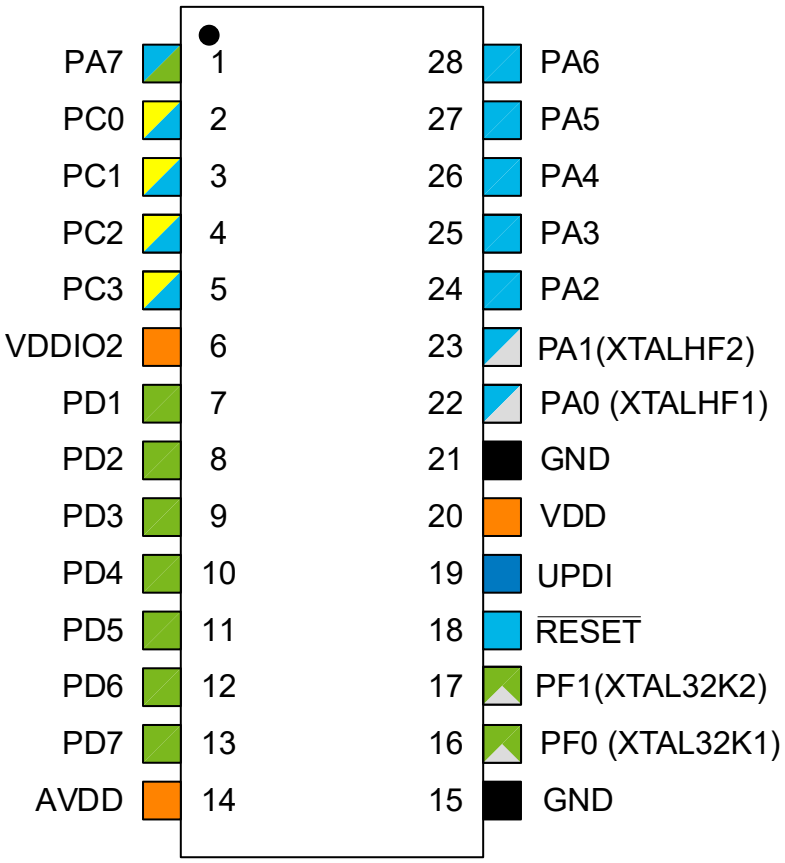
Power

- Power Supply
- Ground
- Pin on VDD Power Domain
- Pin on VDDIO2 Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- Digital Function Only
- Analog Function

4.3 28-Pin SSOP and SPDIP



Note: For the AVR SD Family of devices, AVDD is internally connected to VDD (not separate power domains).

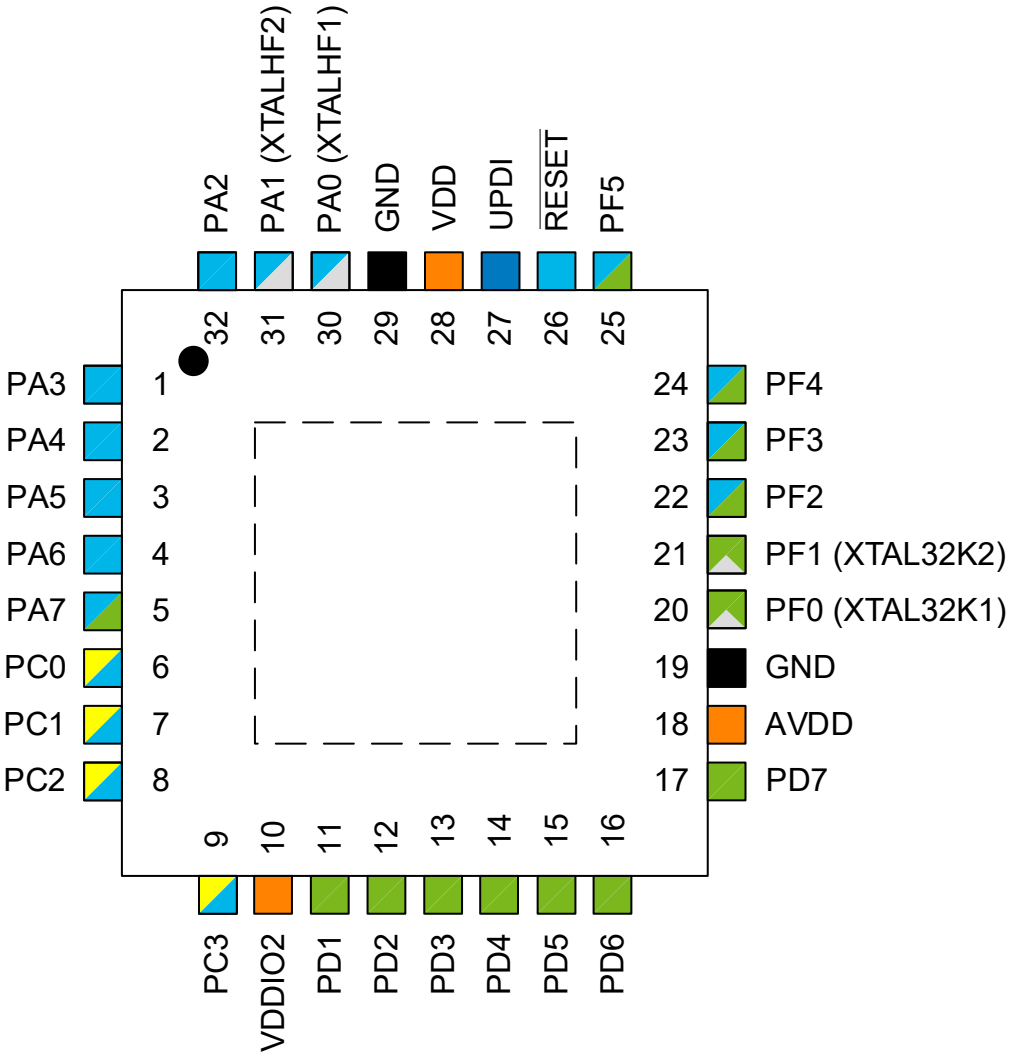
Power

- Power Supply
- Ground
- Pin on VDD Power Domain
- Pin on AVDD Power Domain
- Pin on VDDIO2 Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- Digital Function Only
- Analog Function

4.4 32-Pin VQFN and TQFP



Note: For the AVR SD Family of devices, AVDD is internally connected to VDD (not separate power domains).

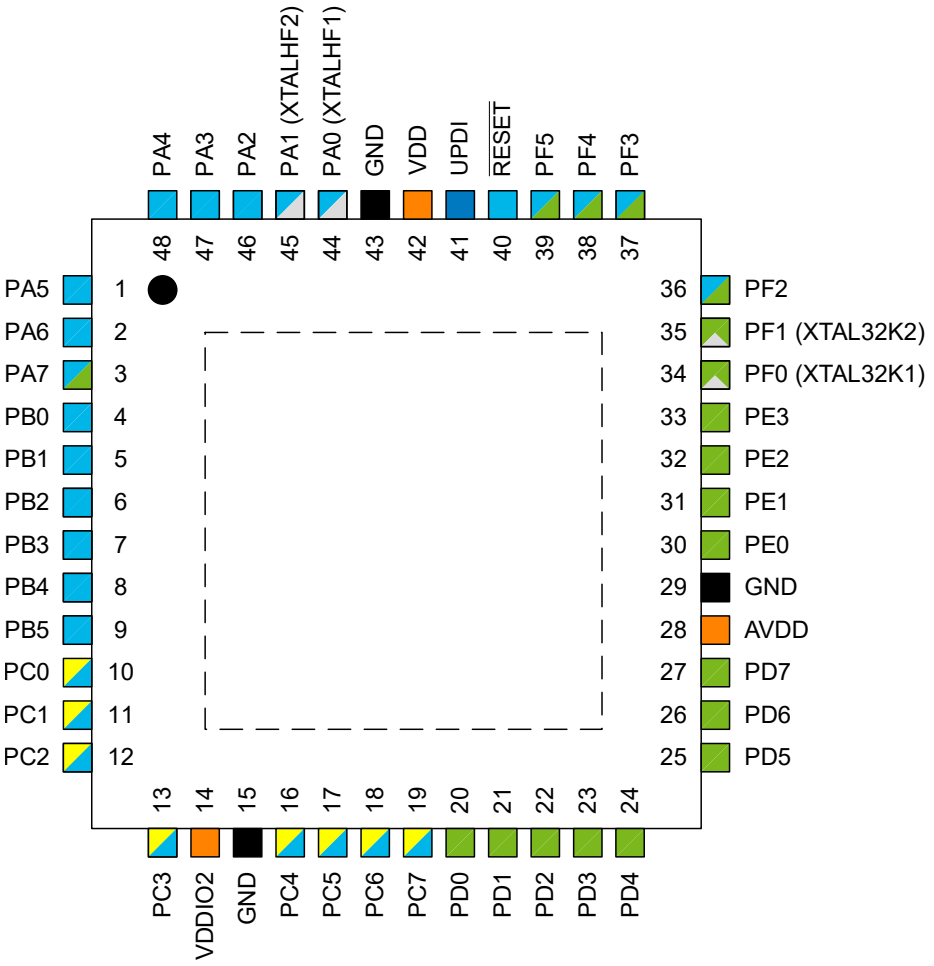
Power

- Power Supply
- Ground
- Pin on VDD Power Domain
- Pin on AVDD Power Domain
- Pin on VDDIO2 Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- Digital Function Only
- Analog Function

4.5 48-Pin VQFN and TQFP



Note: For the AVR SD Family of devices, AVDD is internally connected to VDD (not separate power domains).

Power

- Power Supply
- Ground
- Pin on VDD Power Domain
- Pin on AVDD Power Domain
- Pin on VDDIO2 Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- Digital Function Only
- Analog Function

5. I/O Multiplexing and Considerations

5.1 I/O Multiplexing

VQFN48/ TQFP48	VQFN32/ TQFP32	SOIC28/SSOP28/ SPDIP28	VQFN28	SOIC20	Pin name(1,2)	Special	ADCn	ACn	DACO	ZCDn	USARTn	SPIn	TWIn(4)	TCAn	TCBn	TCD0	EVSYS	CCL-LUTn	ERRCTRL
44	30	22	26	4	PA0	XTALHF1 EXTCLK					0, TxD	0, MOSI(3)	0, SDA(HC)(3)	0, WO0				0, IN0	
45	31	23	27	5	PA1	XTALHF2					0, RxD	0, MISO(3)	0, SCL(HC)(3)	0, WO1				0, IN1	
46	32	24	28	6	PA2	TWI Fm+	AIN22				0, XCK 0, TxD(3)		0, SDA(HC)	0, WO2	0, WO		EVOUTA	0, IN2	HEART
47	1	25	1	7	PA3	TWI Fm+	AIN23				0, XDIR 0, RxD(3)		0, SCL(HC)	0, WO3	1, WO			0, OUT	
48	2	26	2	8	PA4		AIN24				0, TxD(3)	0, MOSI		0, WO4		WOA			HEART(3)
1	3	27	3	9	PA5		AIN25				0, RxD(3)	0, MISO		0, WO5		WOB			
2	4	28	4	10	PA6		AIN26				0, XCK(3)	0, SCK				WOC		0, OUT(3)	HEART(3)
3	5	1	5	11	PA7	CLKOUT	AIN27	0, OUT 1, OUT 2, OUT		0, OUT 3, OUT	0, XDIR(3)	0, $\overline{SS}$				WOD	EVOUTA(3)		HEART(3)
4	-	-	-	-	PB0						3, TxD			0, WO0(3)				4, IN0	
5	-	-	-	-	PB1						3, RxD			0, WO1(3)				4, IN1	
6	-	-	-	-	PB2						3, XCK		1, SDA(C) 1, SDA(HC)(3)	0, WO2(3)			EVOUTB	4, IN2	
7	-	-	-	-	PB3						3, XDIR		1, SCL(C) 1, SCL(HC)(3)	0, WO3(3)				4, OUT	
8	-	-	-	-	PB4						3, TxD(3)	1, MOSI(3)		0, WO4(3)	2, WO(3)	WOA(3)			
9	-	-	-	-	PB5						3, RxD(3)	1, MISO(3)		0, WO5(3)	3, WO	WOB(3)			
10	6	2	6	-	PC0		AIN28				1, TxD	1, MOSI 0, MOSI(3) 0, SCK(3)		0, WO0(3)	2, WO			1, IN0	
11	7	3	7	12	PC1		AIN29				1, RxD 0, TxD(3)	1, MISO 0, MISO(3) 0, $\overline{SS}$(3) 0, MOSI(3)		0, WO1(3)	3, WO(3)			1, IN1	
12	8	4	8	13	PC2	TWI Fm+	AIN30	0, AINN3 1, AINN3		3, ZCIN	1, XCK 0, RxD(3)	1, SCK 0, SCK(3) 0, MISO(3)	0, SDA(C) 0, SDA(HC)(3)	0, WO2(3)			EVOUTC	1, IN2	
13	9	5	9	14	PC3	TWI Fm+	AIN31	0, AINP4 1, AINP4			1, XDIR 0, XCK(3)	1, $\overline{SS}$ 0, $\overline{SS}$(3) 0, SCK(3)	0, SCL(C) 0, SCL(HC)(3)	0, WO3(3)				1, OUT	
14	10	6	10	15	VDDIO2														
15	-	-	-	-	GND														
16	-	-	-	-	PC4						1, TxD(3)	1, MOSI(3)		0, WO4(3)					
17	-	-	-	-	PC5						1, RxD(3)	1, MISO(3)		0, WO5(3)					
18	-	-	-	-	PC6			0, OUT(3) 1, OUT(3) 2, OUT(3)			1, XCK(3)	1, SCK(3)	0, SDA(C)(3)		4, WO(3)			1, OUT(3)	
19	-	-	-	-	PC7					0, ZCOUT(3) 3, ZCOUT(3)	1, XDIR(3)	1, $\overline{SS}$(3)	0, SCL(C)(3)				EVOUTC(3)		
20	-	-	-	-	PD0		AIN0	0, AINN1 1, AINN1 2, AINN2						0, WO0(3)				2, IN0	
21	11	7	11	-	PD1		AIN1			0, ZCIN				0, WO1(3)				2, IN1	
22	12	8	12	-	PD2		AIN2	0, AINP0 1, AINP0 2, AINP0						0, WO2(3)			EVOUTD	2, IN2	
23	13	9	13	-	PD3		AIN3	0, AINN0 1, AINP1						0, WO3(3)				2, OUT	
24	14	10	14	16	PD4	VREFB	AIN4	1, AINP2 2, AINP1			0, TxD(3)	0, MOSI(3)		0, WO4(3)		WOC(3)			HEART(3)
25	15	11	15	17	PD5		AIN5	1, AINN0			0, RxD(3)	0, MISO(3)		0, WO5(3)		WOD(3)			
26	16	12	16	18	PD6		AIN6	0, AINP3 1, AINP3 2, AINP3	OUT		0, XCK(3) 1, TxD(3)	0, SCK(3)						2, OUT(3)	
27	17	13	17	19	PD7	VREFA	AIN7	0, AINN2 1, AINN2 2, AINN0/ AINN2			0, XDIR(3) 1, RxD(3)	0, $\overline{SS}$(3)					EVOUTD(3)		
28	18	14	18	20	VDD														
29	19	15	19	1	GND														
30	-	-	-	-	PE0		AIN8	0, AINP1			4, TxD	0, MOSI(3)		0, WO0(3)					
31	-	-	-	-	PE1		AIN9	2, AINP2			4, RxD	0, MISO(3)		0, WO1(3)					
32	-	-	-	-	PE2		AIN10	0, AINP2			4, XCK	0, SCK(3)		0, WO2(3)			EVOUTE		
33	-	-	-	-	PE3		AIN11				4, XDIR	0, $\overline{SS}$(3)		0, WO3(3)					
34	20	16	20	-	PF0	XTAL32K1	AIN16				2, TxD			0, WO0(3)		WOA(3)		3, IN0	
35	21	17	21	-	PF1	XTAL32K2	AIN17				2, RxD			0, WO1(3)		WOB(3)		3, IN1	
36	22	-	-	-	PF2	TWI Fm+	AIN18				2, XCK		1, SDA(HC)	0, WO2(3)		WOC(3)	EVOUTF	3, IN2	
37	23	-	-	-	PF3	TWI Fm+	AIN19				2, XDIR		1, SCL(HC)	0, WO3(3)		WOD(3)		3, OUT	
38	24	-	-	-	PF4		AIN20				2, TxD(3)			0, WO4(3)	0, WO(3)				

.....continued

VQFN48/ TQFP48	VQFN32/ TQFP32	SOIC28/SSOP28/ SPDIP28	VQFN28	SOIC20	Pin name(1,2)	Special	ADCn	ACn	DAC0	ZCDn	USARTn	SPIn	TWIn(4)	TCAn	TCBn	TCD0	EVSYS	CCL-LUTn	ERRCTRL
39	25	-	-	-	PF5		AIN21				2, RxD(3)			0, WO5(3)	1, WO(3)				HEART(3)
40	26	18	22	2	RESET	RESET													
41	27	19	23	3	UPDI	UPDI													
42	28	20	24	-	VDD														
43	29	21	25	-	GND														

Notes:

1. Pin names are of type P*xn*, with *x* being the PORT instance (A, B, C, ...) and *n* the pin number. Notation for signals is PORT*x*_PIN*n*. All pins can be used as event inputs.
2. All pins can be used for external interrupt, where pins P*x*2 and P*x*6 of each port have full asynchronous detection.
3. Alternative pin positions. To select alternative pin positions, refer to the *Port Multiplexer* section.
4. TWI pins are marked *HC* if they can be used as TWI Host or Client pins and *C* if they can only be used as TWI Client pins.

6. Revision History

Doc. Rev.	Date	Description
E	10/2024	Initial public release
A-D	06/2022 - 02/2024	Not published

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