Dual and Quad 25MHz, 600V/µs Op Amps

FEATURES

- **25MHz Gain Bandwidth**
- **600V/µs Slew Rate**
- **2.5mA Maximum Supply Current per Amplifier**
- Unity-Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 8nV/√Hz Input Noise Voltage
- 600µV Maximum Input Offset Voltage
- 500nA Maximum Input Bias Current
- 120nA Maximum Input Offset Current
- 20V/mV Minimum DC Gain, R_L=1k
- 115ns Settling Time to 0.1%, 10V Step
- 220ns Settling Time to 0.01%, 10V Step
- ±12.5V Minimum Output Swing into 500Ω
- ±3V Minimum Output Swing into 150Ω
- Specified at ±2.5V, ±5V, and ±15V
- LT1358 is Available in 8-Pin PDIP and SO Packages
- LT1359 is Available in 14-Pin PDIP, 14-Pin and 16-Pin SO Packages

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

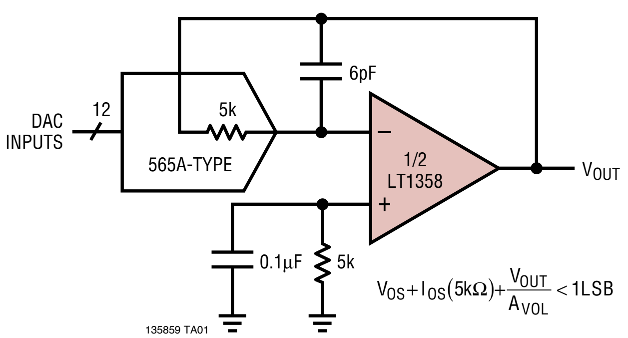
DESCRIPTION

The LT1358/LT1359 are dual and quad low power high speed operational amplifiers with outstanding AC and DC performance. The amplifiers feature much lower supply current and higher slew rate than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with matched high impedance inputs and the slewing performance of a current feedback amplifier. The high slew rate and single stage design provide excellent settling characteristics which make the circuit an ideal choice for data acquisition systems. Each output drives a 500Ω load to ±12.5V with ±15V supplies and a 150Ω load to ±3V on ±5V supplies. The amplifiers are stable with any capacitive load making them useful in buffer applications.

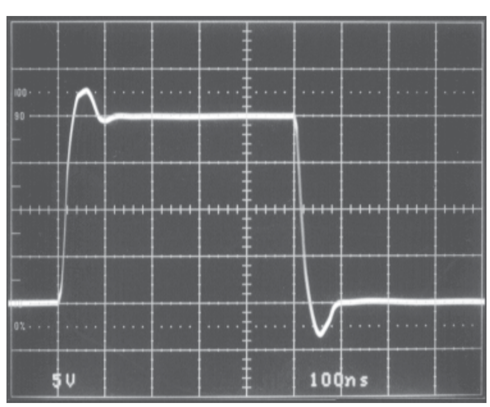
The LT1358/LT1359 are members of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For a single amplifier version of the LT1358/LT1359 see the LT1357 data sheet. For higher bandwidth devices with higher supply currents see the LT1360 through LT1365 data sheets. For lower supply current amplifiers see the LT1354 and LT1355/LT1356 data sheets. Singles, duals, and quads of each amplifier are available.

TYPICAL APPLICATION

DAC I-to-V Converter



A_V = –1 Large-Signal Response

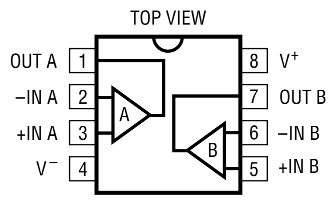


135859fb

ABSOLUTE MAXIMUM RATINGS (Note 1)

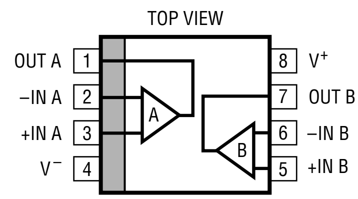
Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage
(Transient Only) (Note 2) .... ±10V
Input Voltage .... $\pm V_S$
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range (Note 7) ...–40°C to 85°C
Specified Temperature Range (Note 8) ....–40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package .... 150°C
Storage Temperature Range ....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



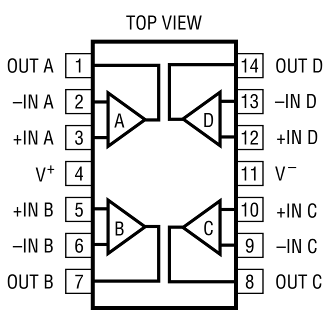
N8 PACKAGE
8-LEAD PDIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1358CN8 LT1358IN8

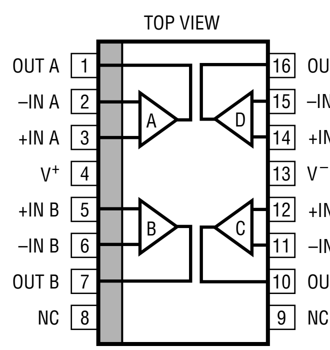


S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

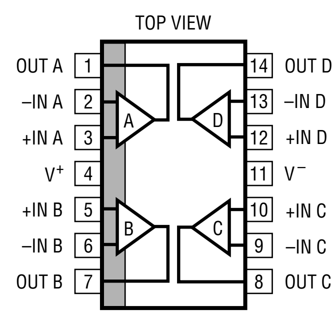
ORDER PART NUMBER	S8 PART MARKING
LT1358CS8 LT1358IS8	1358 1358I



N PACKAGE
14-LEAD PDIP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 150°C/W



S PACKAGE
14-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 160°C/W

ORDER PART NUMBER	ORDER PART NUMBER	ORDER PART NUMBER
LT1359CN LT1359IN	LT1359CS LT1359IS	LT1359CS14 LT1359IS14

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF   Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V ±5V ±2.5V		0.2 0.2 0.3	0.6 0.6 0.8	mV mV mV
I_{OS}	Input Offset Current		±2.5V to ±15V		40	120	nA
I_B	Input Bias Current		±2.5V to ±15V		120	500	nA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		8		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		0.8		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	$V_{CM} = ±12V$	±15V	35	80		MΩ
	Input Resistance	Differential	±15V		6		MΩ
C_{IN}	Input Capacitance		±15V		3		pF
	Input Voltage Range$^+$		±15V ±5V ±2.5V	12.0 2.5 0.5	13.4 3.5 1.1		V V V
	Input Voltage Range$^-$		±15V ±5V ±2.5V		−13.2 −3.3 −0.9	−12.0 −2.5 −0.5	V V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = ±12V$ $V_{CM} = ±2.5V$ $V_{CM} = ±0.5V$	±15V ±5V ±2.5V	83 78 68	97 84 75		dB dB dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2.5V$ to ±15V		92	106		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = ±12V$, $R_L = 1k$ $V_{OUT} = ±10V$, $R_L = 500Ω$ $V_{OUT} = ±2.5V$, $R_L = 1k$ $V_{OUT} = ±2.5V$, $R_L = 500Ω$ $V_{OUT} = ±2.5V$, $R_L = 150Ω$ $V_{OUT} = ±1V$, $R_L = 500Ω$	±15V ±15V ±5V ±5V ±5V ±2.5V	20 7 20 7 1.5 7	65 25 45 25 6 30		V/mV V/mV V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$ $R_L = 150Ω$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$	±15V ±15V ±5V ±5V ±2.5V	13.3 12.5 3.5 3.0 1.3	13.8 13.0 4.0 3.3 1.7		±V ±V ±V ±V ±V
I_{OUT}	Output Current	$V_{OUT} = ±12.5V$ $V_{OUT} = ±3V$	±15V ±5V	25 20	30 25		mA mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = ±3V$	±15V	30	42		mA
SR	Slew Rate	$A_V = −2$, (Note 4)	±15V ±5V	300 150	600 220		V/µs V/µs
	Full Power Bandwidth	10V Peak, (Note 5) 3V Peak, (Note 5)	±15V ±5V		9.6 11.7		MHz MHz
GBW	Gain Bandwidth	f = 200kHz, $R_L = 2k$	±15V ±5V ±2.5V	18 15	25 22 20		MHz MHz MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10%-90%, 0.1V	±15V ±5V		8 9		ns ns
	Overshoot	$A_V = 1$, 0.1V	±15V ±5V		27 27		% %
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V ±5V		9 11		ns ns
t_s	Settling Time	10V Step, 0.1%, $A_V = −1$ 10V Step, 0.01%, $A_V = −1$ 5V Step, 0.1%, $A_V = −1$ 5V Step, 0.01%, $A_V = −1$	±15V ±15V ±5V ±5V		115 220 110 380		ns ns ns ns

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
	Differential Gain	f = 3.58MHz, $A_V = 2$, $R_L = 1k$	±15V ±5V		0.1 0.1		% %
	Differential Phase	f = 3.58MHz, $A_V = 2$, $R_L = 1k$	±15V ±5V		0.50 0.35		Deg Deg
R_O	Output Resistance	$A_V = 1$, f = 100kHz	±15V		0.3		Ω
	Channel Separation	$V_{OUT} = ±10V$, $R_L = 500Ω$	±15V	100	113		dB
I_S	Supply Current	Each Amplifier Each Amplifier	±15V ±5V		2.0 1.9	2.5 2.4	mA mA

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the temperature range $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V ±5V ±2.5V	● ● ●			0.8 0.8 1.0	mV mV mV
	Input V_{OS} Drift	(Note 6)	±2.5V to ±15V	●		5	8	μV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			180	nA
I_B	Input Bias Current		±2.5V to ±15V	●			750	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = ±12V$ $V_{CM} = ±2.5V$ $V_{CM} = ±0.5V$	±15V ±5V ±2.5V	● ● ●	81 77 67			dB dB dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2.5V$ to ±15V		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = ±12V$, $R_L = 1k$ $V_{OUT} = ±10V$, $R_L = 500Ω$ $V_{OUT} = ±2.5V$, $R_L = 1k$ $V_{OUT} = ±2.5V$, $R_L = 500Ω$ $V_{OUT} = ±2.5V$, $R_L = 150Ω$ $V_{OUT} = ±1V$, $R_L = 500Ω$	±15V ±15V ±5V ±5V ±5V ±2.5V	● ● ● ● ● ●	15 5 15 5 1 5			V/mV V/mV V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$ $R_L = 150Ω$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$	±15V ±15V ±5V ±5V ±2.5V	● ● ● ● ●	13.2 12.2 3.4 2.8 1.2			±V ±V ±V ±V ±V
I_{OUT}	Output Current	$V_{OUT} = ±12.2V$ $V_{OUT} = ±2.8V$	±15V ±5V	● ●	24.4 18.7			mA mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = ±3V$	±15V	●	25			mA
SR	Slew Rate	$A_V = –2$, (Note 4)	±15V ±5V	● ●	225 125			V/μs V/μs
GBW	Gain Bandwidth	f = 200kHz, $R_L = 2k$	±15V ±5V	● ●	15 12			MHz MHz
	Channel Separation	$V_{OUT} = ±10V$, $R_L = 500Ω$	±15V	●	98			dB
I_S	Supply Current	Each Amplifier Each Amplifier	±15V ±5V	● ●			2.9 2.8	mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range –40°C ≤ T_A ≤ 85°C, V_{CM} = 0V unless otherwise noted. (Note 8)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V ±5V ±2.5V	● ● ●			1.3 1.3 1.5	mV mV mV
	Input V_{OS} Drift	(Note 6)	±2.5V to ±15V	●		5	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			300	nA
I_B	Input Bias Current		±2.5V to ±15V	●			900	nA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V V_{CM} = ±2.5V V_{CM} = ±0.5V	±15V ±5V ±2.5V	● ● ●	80 76 66			dB dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k V_{OUT} = ±10V, R_L = 500Ω V_{OUT} = ±2.5V, R_L = 1k V_{OUT} = ±2.5V, R_L = 500Ω V_{OUT} = ±2.5V, R_L = 150Ω V_{OUT} = ±1V, R_L = 500Ω	±15V ±15V ±5V ±5V ±5V ±2.5V	● ● ● ● ● ●	10.0 2.5 10.0 2.5 0.6 2.5			V/mV V/mV V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV R_L = 150Ω, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV	±15V ±15V ±5V ±5V ±2.5V	● ● ● ● ●	13.0 12.0 3.4 2.6 1.2			±V ±V ±V ±V ±V
I_{OUT}	Output Current	V_{OUT} = ±12V V_{OUT} = ±2.6V	±15V ±5V	● ●	24.0 17.3			mA mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	●	24			mA
SR	Slew Rate	A_V = –2, (Note 4)	±15V ±5V	● ●	180 100			V/µs V/µs
GBW	Gain Bandwidth	f = 200kHz, R_L = 2k	±15V ±5V	● ●	14 11			MHz MHz
	Channel Separation	V_{OUT} = ±10V, R_L = 500Ω	±15V	●	98			dB
I_S	Supply Current	Each Amplifier Each Amplifier	±15V ±5V	● ●			3.0 2.9	mA mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Differential inputs of ±10V are appropriate for transient operation only, such as during slewing. Large, sustained differential inputs will cause excessive power dissipation and may damage the part. See Input Considerations in the Applications Information section of this data sheet for more details.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

Note 5: Full power bandwidth is calculated from the slew rate measurement: FPBW = (SR)/2πV_P.

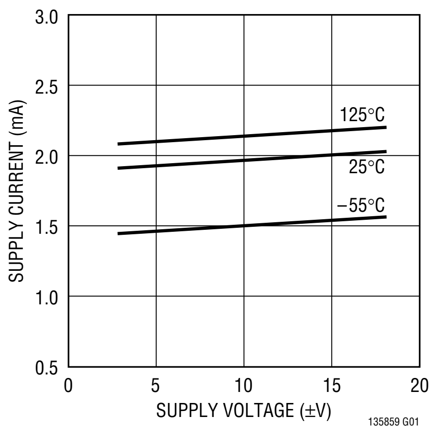
Note 6: This parameter is not 100% tested.

Note 7. The LT1358C/LT1359C and LT1358I/LT1359I are guaranteed functional over the operating temperature range of –40°C to 85°C.

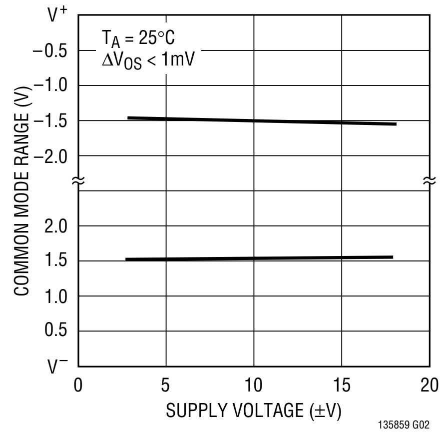
Note 8: The LT1358C/LT1359C are guaranteed to meet specified performance from 0°C to 70°C. The LT1358C/LT1359C are designed, characterized and expected to meet specified performance from –40°C to 85°C, but are not tested or QA sampled at these temperatures. The LT1358I/LT1359I are guaranteed to meet specified performance from –40°C to 85°C.

TYPICAL PERFORMANCE CHARACTERISTICS

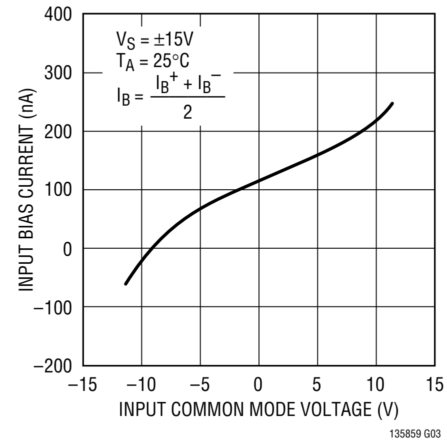
Supply Current vs Supply Voltage and Temperature



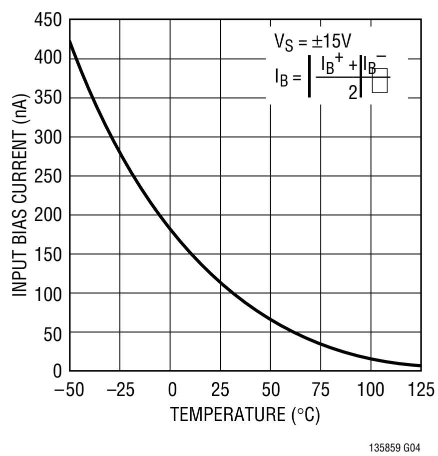
Input Common Mode Range vs Supply Voltage



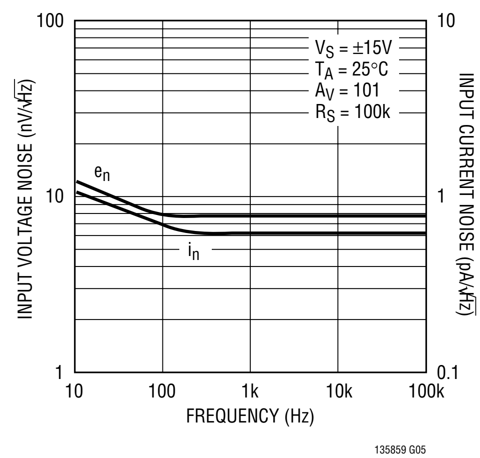
Input Bias Current vs Input Common Mode Voltage



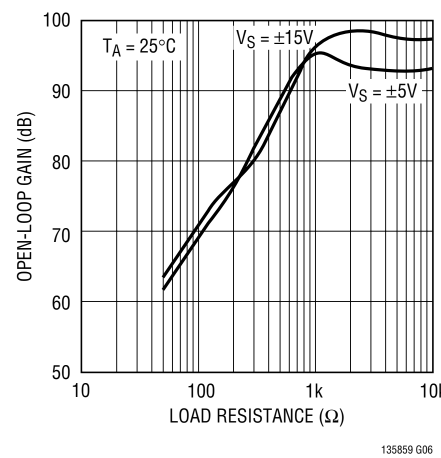
Input Bias Current vs Temperature



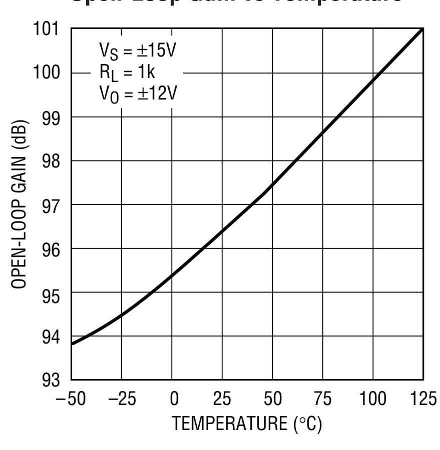
Input Noise Spectral Density



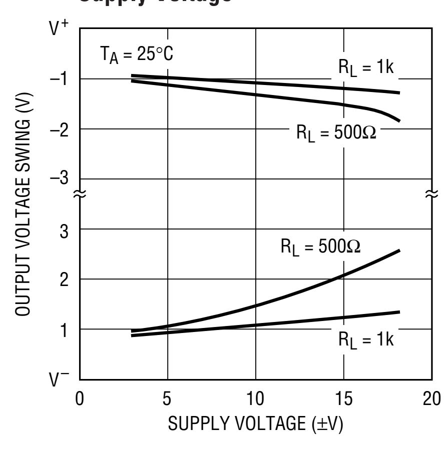
Open-Loop Gain vs Resistive Load



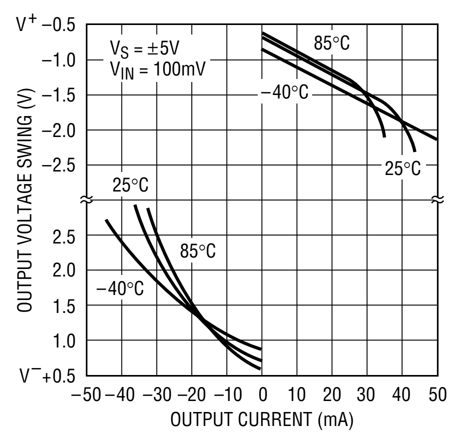
Open-Loop Gain vs Temperature



Output Voltage Swing vs Supply Voltage

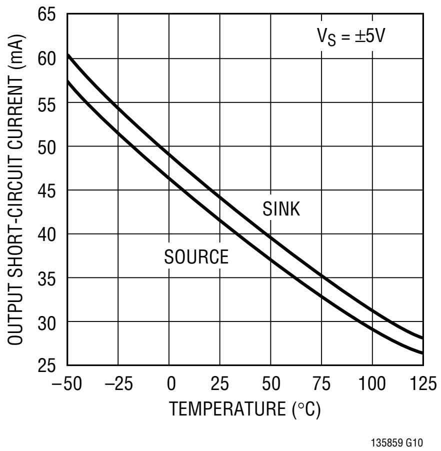


Output Voltage Swing vs Load Current

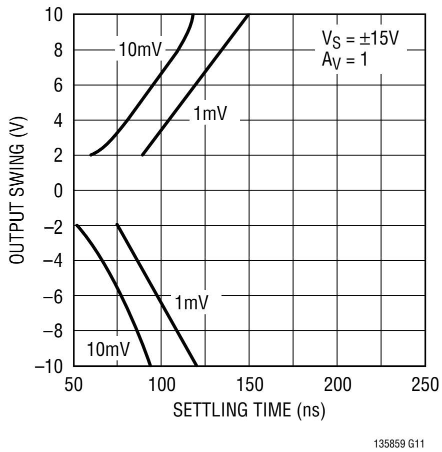


TYPICAL PERFORMANCE CHARACTERISTICS

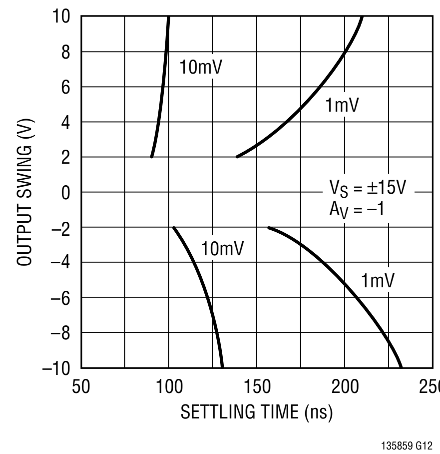
Output Short-Circuit Current vs Temperature



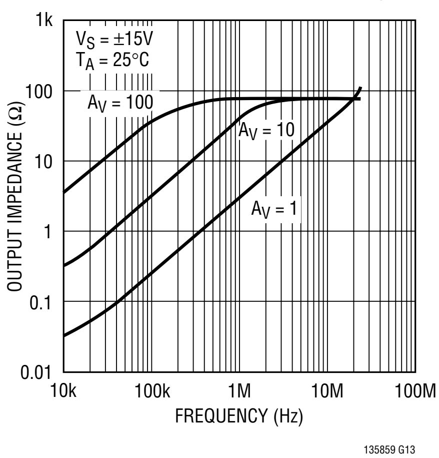
Settling Time vs Output Step (Noninverting)



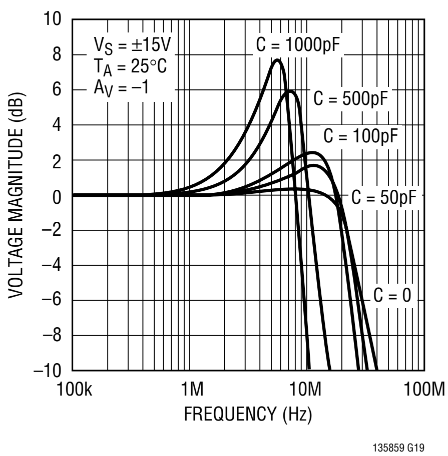
Settling Time vs Output Step (Inverting)



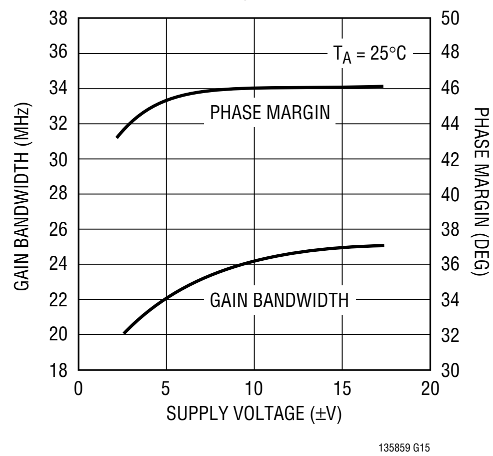
Output Impedance vs Frequency



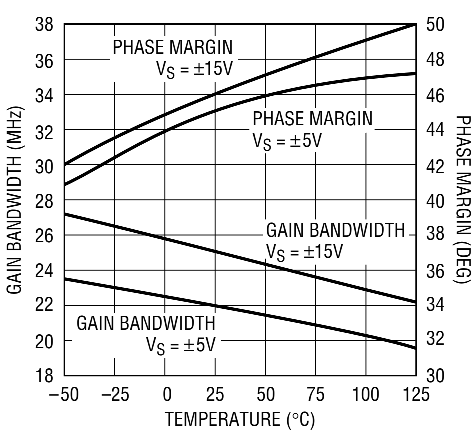
Frequency Response vs Capacitive Load



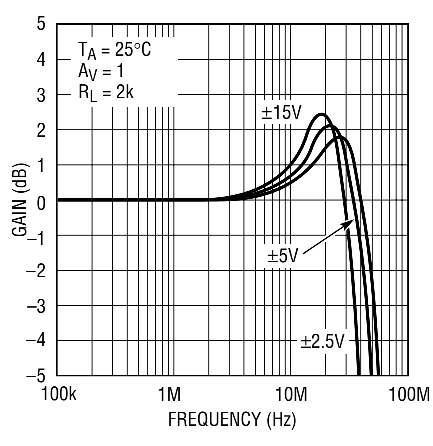
Gain Bandwidth and Phase Margin vs Supply Voltage



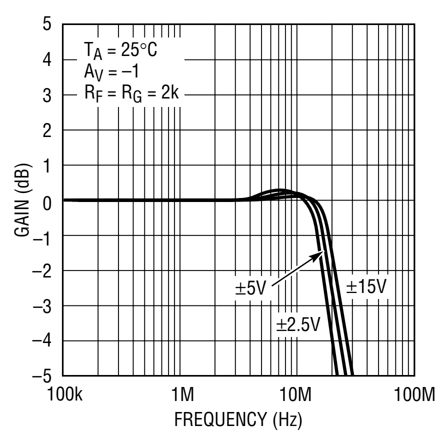
Gain Bandwidth and Phase Margin vs Temperature



Frequency Response vs Supply Voltage ($A_V = 1$)

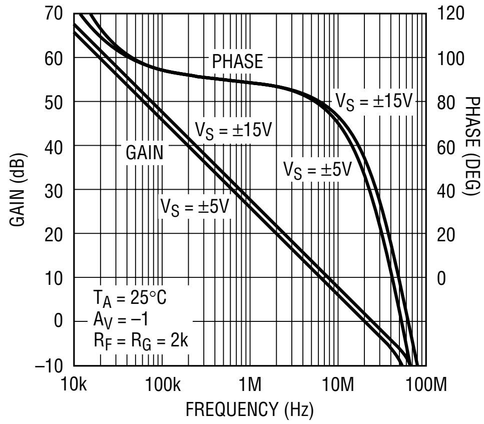


Frequency Response vs Supply Voltage ($A_V = –1$)



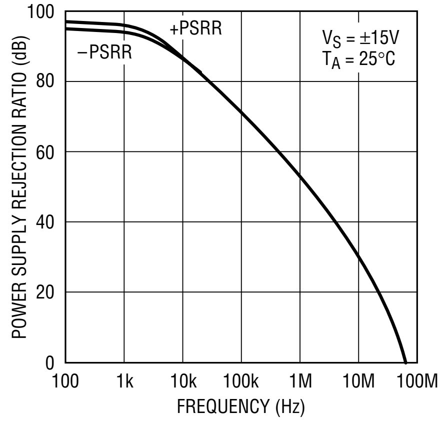
TYPICAL PERFORMANCE CHARACTERISTICS

Gain and Phase vs Frequency



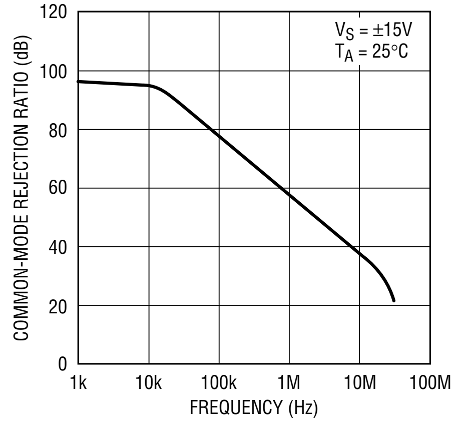
135859 G14

Power Supply Rejection Ratio vs Frequency



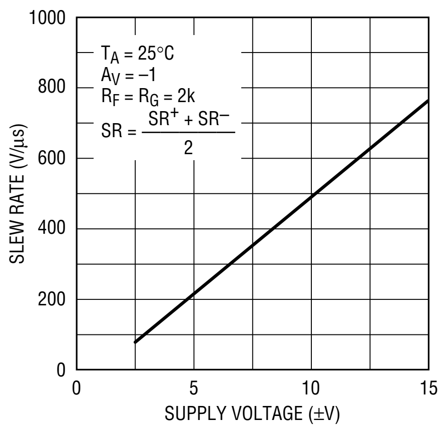
135859 G20

Common Mode Rejection Ratio vs Frequency



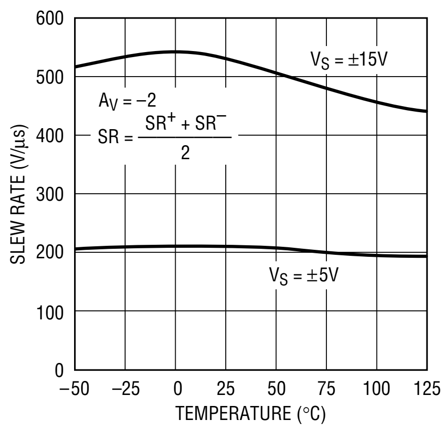
135859 G21

Slew Rate vs Supply Voltage



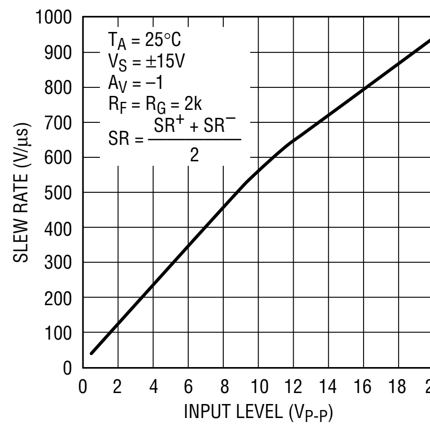
135859 G22

Slew Rate vs Temperature



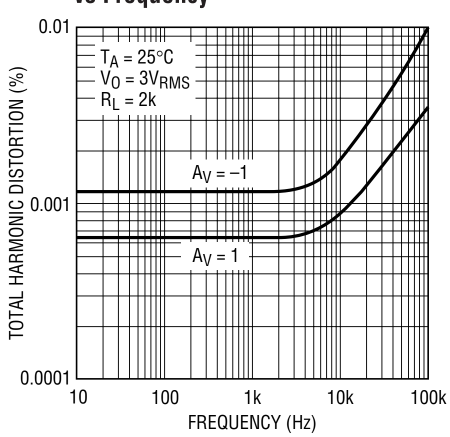
135859 G23

Slew Rate vs Input Level



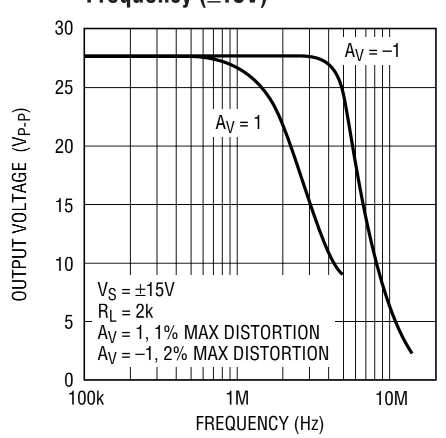
135859 G24

Total Harmonic Distortion vs Frequency



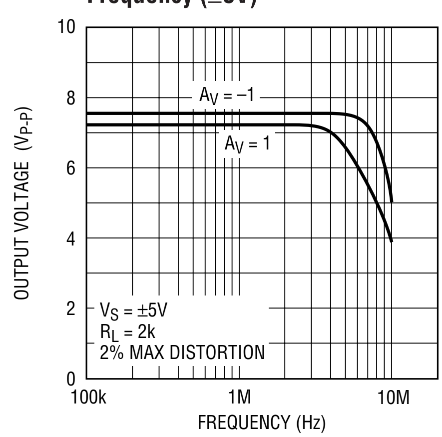
135859 G25

Undistorted Output Swing vs Frequency (±15V)



135859 G26

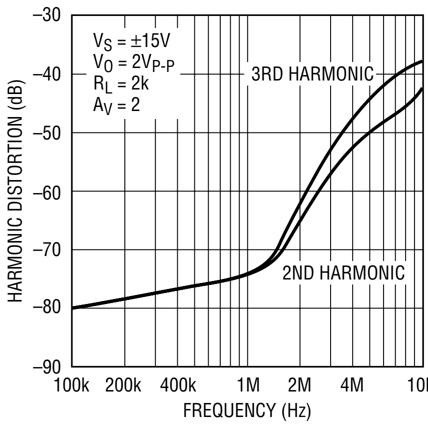
Undistorted Output Swing vs Frequency (±5V)



135859 G27

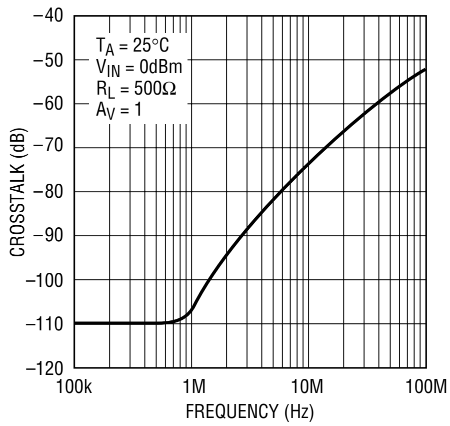
TYPICAL PERFORMANCE CHARACTERISTICS

2nd and 3rd Harmonic Distortion vs Frequency



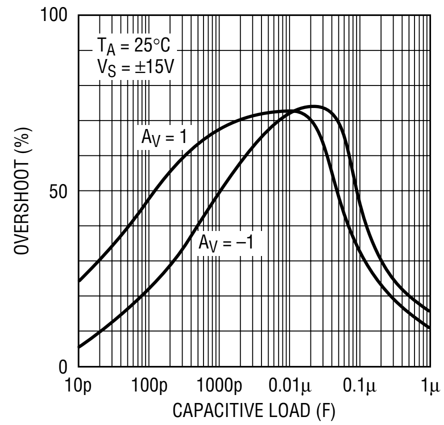
135859 G28

Crosstalk vs Frequency



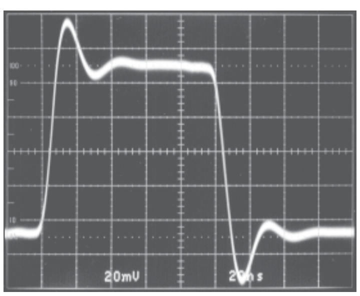
135859 G29

Capacitive Load Handling



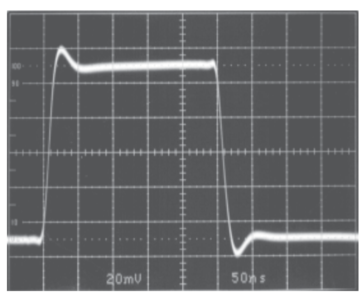
135859 G30

Small-Signal Transient (A_V = 1)



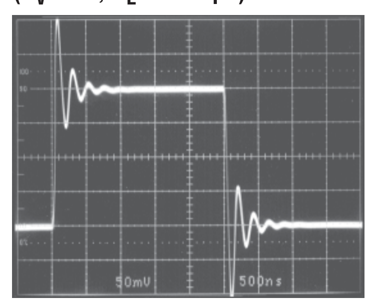
135859 G31

Small-Signal Transient (A_V = –1)



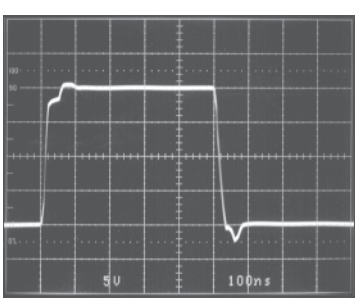
135859 G32

Small-Signal Transient (A_V = –1, C_L = 1000pF)



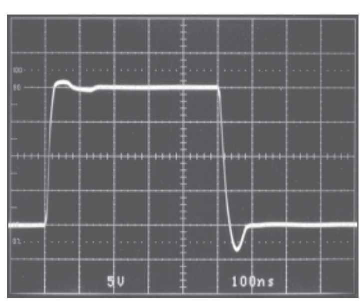
135859 G33

Large-Signal Transient (A_V = 1)



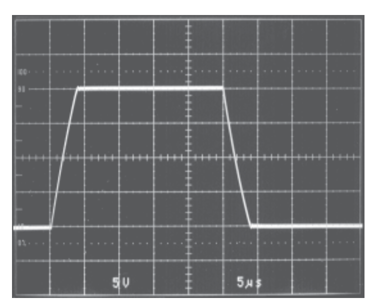
135859 G34

Large-Signal Transient (A_V = –1)



135859 G35

Large-Signal Transient (A_V = 1, C_L = 10,000pF)



135859 G36

APPLICATIONS INFORMATION

Layout and Passive Components

The LT1358/LT1359 amplifiers are easy to use and tolerant of less than ideal layouts. For maximum performance (for example, fast 0.01% settling) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01μF to 0.1μF). For high drive current applications use low ESR bypass capacitors (1μF to 10μF tantalum).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking or oscillations. If feedback resistors greater than 5k are used, a parallel capacitor of value

$$C_F > R_G \times C_{IN} / R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1358/LT1359 are stable with any capacitive load. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

Input Considerations

Each of the LT1358/LT1359 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on NPN/PNP beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

The inputs can withstand transient differential input voltages up to 10V without damage and need no clamping or source resistance for protection. Differential inputs, however, generate large supply currents (tens of mA) as required for high slew rates. If the device is used with sustained differential inputs, the average supply current will increase, excessive power dissipation will result and the part may be damaged. **The part should not be used as a comparator, peak detector or other open-loop application with large, sustained differential inputs**. Under normal, closed-loop operation, an increase of power dissipation is only noticeable in applications with large slewing outputs and is proportional to the magnitude of the differential input voltage and the percent of the time that the inputs are apart. Measure the average supply current for the application in order to calculate the power dissipation.

APPLICATIONS INFORMATION

Circuit Operation

The LT1358/LT1359 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive a 500Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1358/LT1359 are tested for slew rate in a gain of –2 so higher slew rates can be expected in gains of 1 and –1, and lower slew rates in higher gain configurations.

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity-gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

Power Dissipation

The LT1358/LT1359 combine high speed and large output drive in small packages. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1358N8: $T_J = T_A + (P_D \times 130°C/W)$
LT1358S8: $T_J = T_A + (P_D \times 190°C/W)$
LT1359N: $T_J = T_A + (P_D \times 110°C/W)$
LT1359S: $T_J = T_A + (P_D \times 150°C/W)$
LT1359S14: $T_J = T_A + (P_D \times 160°C/W)$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). For each amplifier P_{DMAX} is:

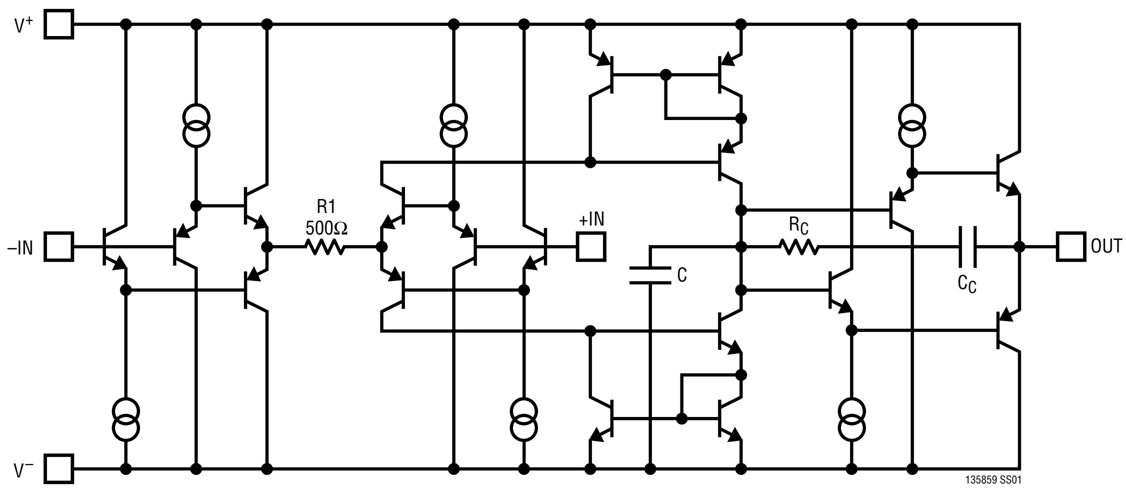
$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + (V^+/2)^2/R_L$$

Example: LT1358 in S8 at 70°C, $V_S = \pm15V$, $R_L = 500\Omega$

$$P_{DMAX} = (30V)(2.9mA) + (7.5V)^2/500\Omega = 200mW$$

$$T_{JMAX} = 70°C + (2 \times 200mW)(190°C/W) = 146°C$$

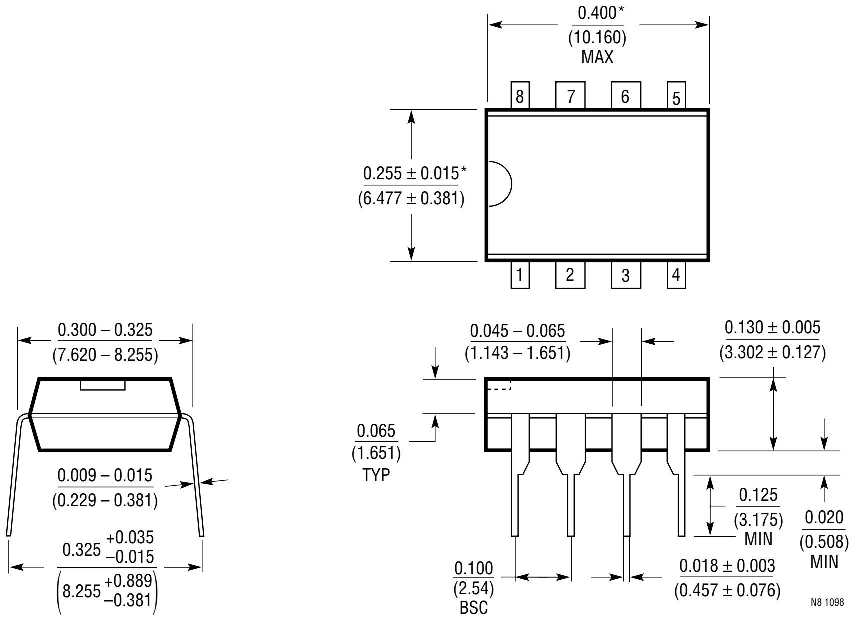
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

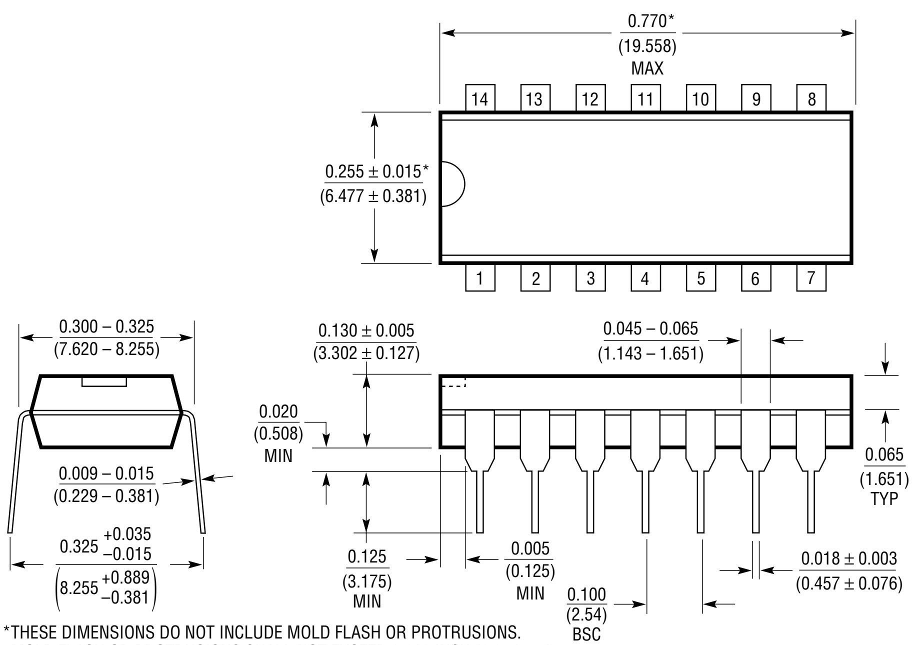
Dimension in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N Package
14-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

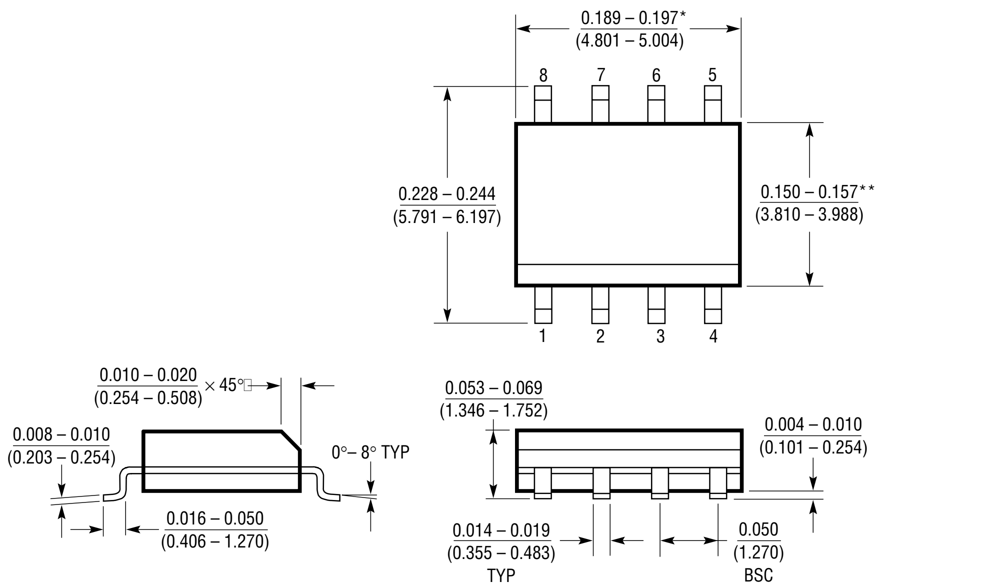


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

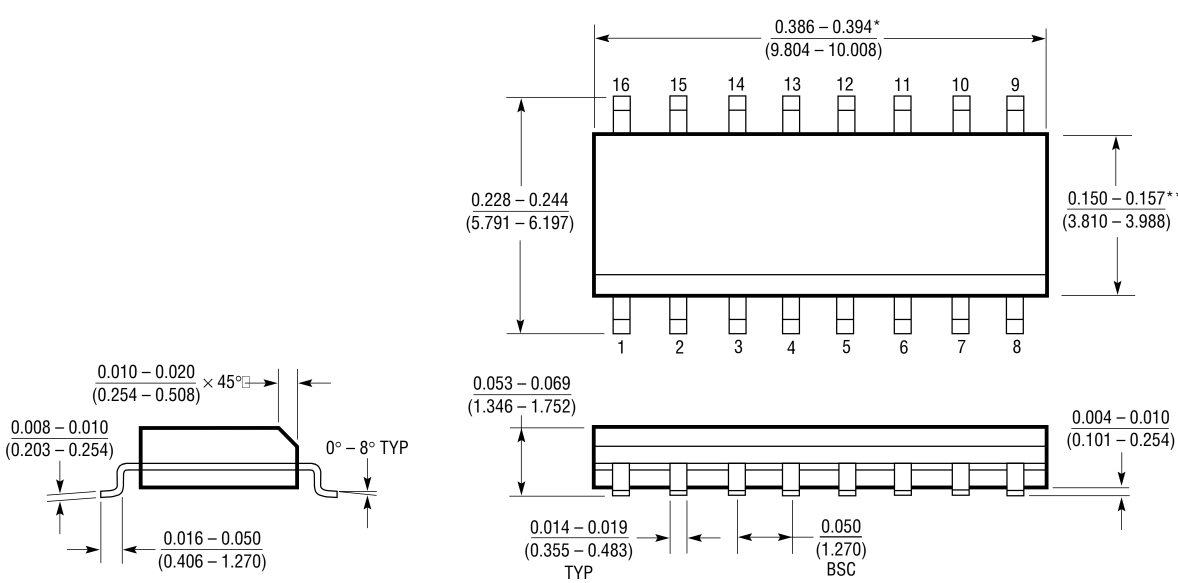


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 1298

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



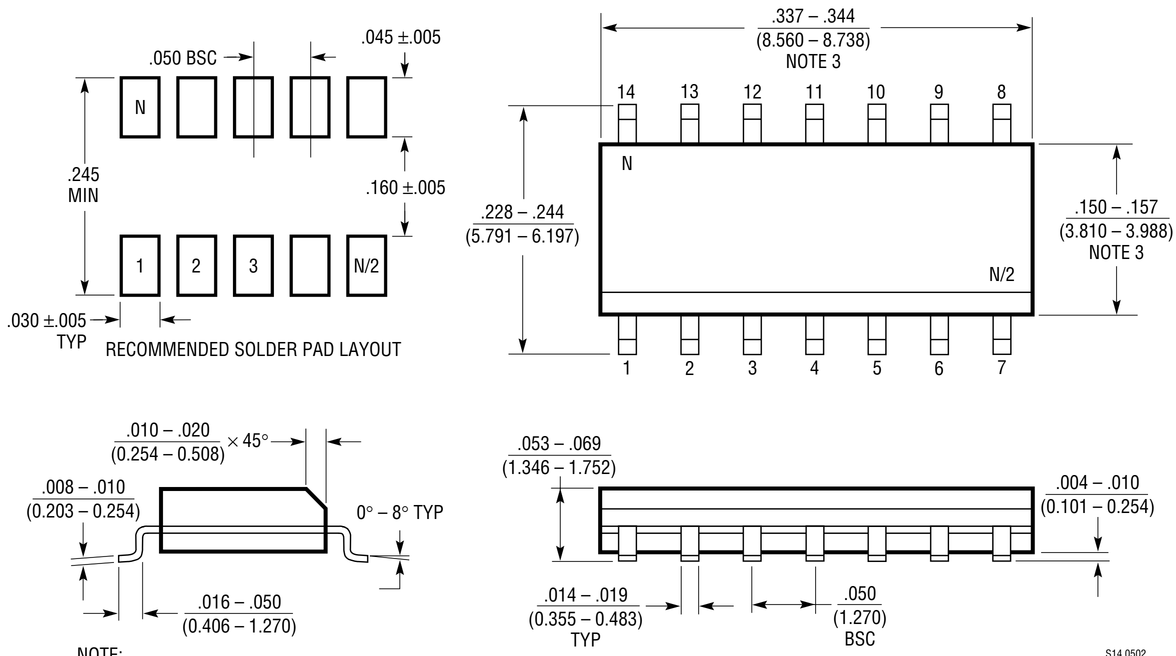
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S16 1098

PACKAGE DESCRIPTION
Dimension in inches (millimeters) unless otherwise noted.

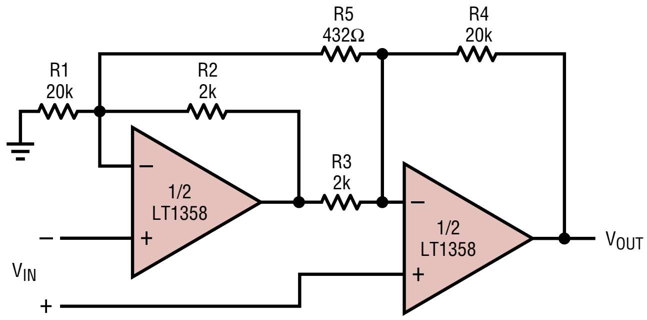
S Package
14-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

TYPICAL APPLICATIONS

Instrumentation Amplifier

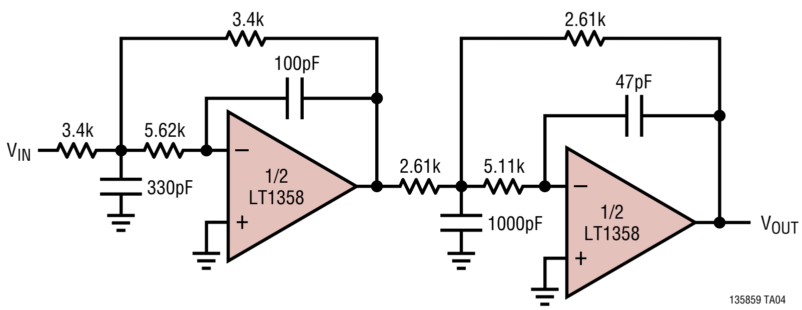


$$A_V = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R5}\right] = 104$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 250kHz

135859 TA03

200kHz, 4th Order Butterworth Filter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1357	25MHz, 600V/µs Op Amp	Single Version of LT1358/LT1359
LT1361/LT1362	Dual and Quad 50MHz, 800V/µs Op Amps	Faster Version of LT1358/LT1359, V_{OS} = 1mV, I_S = 4mA/Amplifier
LT1355/LT1356	Dual and Quad 12MHz, 400V/µs Op Amps	Lower Power Version of LT1358/LT1359, V_{OS} = 0.8mV, I_S = 1mA/Amplifier
LT1812/LT1813/ LT1814	Single/Dual/Quad 100MHz, 750V/µs Op Amps	3.6mA/Amplifier, SOT-23, MSOP-8 and SSOP-16 Packages

135859fb

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT/LT 1005 REV B • PRINTED IN USA