# EL5003C
## High Speed CRT Amplifier



## Features

- Input buffer
- 7.5 V/V nominal gain
- +0 dB to −50 dB gain control
- Clamp/DC-restore
- 300 MHz small-signal bandwidth
- 300 MHz large-signal bandwidth
- 1.5 ns rise and fall time
- 12V supply

## Applications

- High resolution CRT driver
- RGB and Monochrome monitors
- HDTV video processing

## Ordering Information

| Part No. | Temp. Range | Package | Outline # |
|---|---|---|---|
| EL5003CN | −40°C to +85°C | 16-Pin P-DIP | MDP0031 |

## General Description

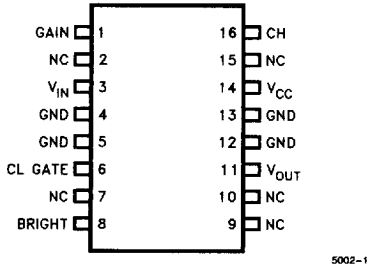
The EL5003C is a single channel high-speed CRT Amplifier which is intended for use in high resolution monochrome or RGB applications. To drive a CRT, the EL5003C is used with an external high-voltage stage which is directly connected to its output. The EL5003C contains the following blocks:

- A high-bandwidth video amplifier;
- A variable gain control for contrast adjustment; and
- Gated DC-restore circuitry for brightness control.

The EL5003C features 300 MHz of large- and small-signal bandwidth. Rise and fall times are an impressive 1.5 ns for a 4V step. The EL5003C has a voltage gain of 7.5 V/V (with 12V at the GAIN pin), and by reducing the GAIN pin voltage, the video signal can be continuously attenuated by up to 50 dB. A TTL- or CMOS-compatible HIGH signal at the CL GATE pin activates the clamp circuitry to offset the EL5003C's output signal based on the video reference voltage during the Back Porch portion of the input signal. This DC-restoration circuitry allows a constant black-level across the CRT, regardless of the DC-offset of the incoming video signal.

## Connection Diagram

**16-Pin P-DIP Package**
**Top View**



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## Absolute Maximum Ratings ($T_A$ = 25°C)

| | | | | | |
|---|---|---|---|---|---|
| $V_S$ | Supply Voltage at Pin 14 | −0.3V to 13.2V | $I_{CAP}$ | Current at Ch (Pin 4) | ±10 mA |
| $V_{IN}$ (Logic) | Logic Input at Clamp Gate (Pin 6) | −0.3V to 6V | $T_J$ | Operating Junction Temperature | 150°C |
| $V_{IN}$ (Signal) | Signal Inputs (Pins 1, 3, 8) | −0.3V to $V_S$ | $\theta_{JA}$ | Package Thermal Resistance | 56°C/W |
| $V_{CAP}$ | Voltage at Ch (Pin 16) | −0.3V to $V_S$ + 0.8V | $T_A$ | Operating Temperature Range* | −40°C to +85°C |
| $I_{OUT}$ | Output Current at $V_{OUT}$ (Pin 11) | ±36 mA | $T_{ST}$ | Storage Temperature | −65°C to +150°C |
| $I_{IN}$ | Input Current (Pins 1, 3, 6, 8) | ±5 mA | $T_{LD}$ | Lead Temperature (Soldering < 5 seconds) | 300°C |

*Note: Do not exceed operating junction temperature of 150°C.

**Important Note:**
**All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.**

| Test Level | Test Procedure |
|---|---|
| I | 100% production tested and QA sample tested per QA test plan QCX0002. |
| II | 100% production tested at $T_A$ = 25°C and QA sample tested at $T_A$ = 25°C, $T_{MAX}$ and $T_{MIN}$ per QA test plan QCX0002. |
| III | QA sample tested per QA test plan QCX0002. |
| IV | Parameter is guaranteed (but not tested) by Design and Characterization Data. |
| V | Parameter is typical value at $T_A$ = 25°C for information purposes only. |

## Electrical Characteristics

See Test Circuit (Figure 1); $T_A = T_J$ = 25°C, $V_{CC} = V_G$ = 12V, $V_{CL}$ = 2V, S1 Open, S2 Open, unless otherwise noted.

| Parameter | Description | Conditions | Temp | Min | Typ | Max | Test Level | Units |
|---|---|---|---|---|---|---|---|---|
| $I_S$ | Supply Current | $V_{CL}$ = 0.8V | 25°C | | 65 | 72 | I | mA |
| $V_{REF}$ | Video Input Reference Voltage | | 25°C | 2.5 | 2.7 | 2.9 | I | V |
| $I_{VID}$ | Video Input Bias Current | S2 Closed, $V_{IN}$ = 2.7V | 25°C | −20 | 0 | 20 | I | µA |
| $R_{IN}$ | Video Input Impedance | S2 Closed, $V_{IN}$ = 2.7V to 3.4V | 25°C | 7 | 9 | 11 | I | kΩ |
| $V_{CLL}$ | Clamp Gate Low Input Voltage | Clamp Comparator Off | 25°C | 0.8 | | | IV | V |
| $V_{CLH}$ | Clamp Gate High Input Voltage | Clamp Comparator On | 25°C | | | 2 | IV | V |
| $I_{CLL}$ | Clamp Gate Low Input Current | $V_{CL}$ = 0.8V | 25°C | −20 | −10 | | I | µA |
| $I_{CLH}$ | Clamp Gate High Input Current | $V_{CL}$ = 2V | 25°C | −2 | −0.2 | 2 | I | µA |
| $I_{CAP}^+$ | Clamp Capacitor Charge Current | S1 Closed, $V_{CH}$ = 7V | 25°C | | −2.5 | −1.7 | I | mA |
| $I_{CAP}^-$ | Clamp Capacitor Discharge Current | S1 Closed, $V_{CH}$ = 11V | 25°C | 1.7 | 2.5 | | I | mA |

## Electrical Characteristics — Contd.

See Test Circuit (Figure 1); $T_A = T_J = 25°C$, $V_{CC} = V_G = 12V$, $V_{CL} = 2V$, S1 Open, S2 Open, unless otherwise noted.

| Parameter | Description | Conditions | Temp | Min | Typ | Max | Test Level | Units |
|---|---|---|---|---|---|---|---|---|
| $I_{LEAK}$ | Clamp Capacitor Leakage Current | $V_{CL} = 0.8V$ | 25°C | | 15 | 30 | I | µA |
| $V_{OUTL}$ | Video Output Low Voltage | S1 Closed, $V_{CH} = 7V$, $V_{CL} = 0.8V$ | 25°C | | 1 | 1.2 | I | V |
| $V_{OUTH}$ | Video Output High Voltage | S1 Closed, $V_{CH} = 11V$, $V_{CL} = 0.8V$ | 25°C | 9 | 9.5 | | I | V |
| $V_{REF(Comp)}$ | Comparator Reference Voltage | | 25°C | 2.1 | 2.18 | 2.25 | I | mV |
| $A_V$ max | Video Amplifier Gain | S2 Closed, $V_{CL} = 0.8V$, $V_{IN} = 2.7V$ to 3.4V | 25°C | 6 | 7.5 | 9 | I | V/V |
| $\Delta A_V$ 6.85V | Attenuation @ $V_G = 6.85V$ | $V_G = 6.85V$ (Note 1) | 25°C | −5.5 | −6 | −6.5 | I | dB |
| $\Delta A_V$ 0V | Attenuation @ $V_G = 0V$ | $V_G = 0V$ (Note 1) | 25°C | −38 | −50 | | I | dB |
| THD | Video Amplifier Distortion | $V_G = 6.85V$, $V_{CL} = 0.8V$, $V_{OUT} = 1\ V_{PP}$, $f = 12$ kHz | 25°C | | 0.3 | | V | % |
| SSBW | Small-Signal Bandwidth | $V_G = 12V$, $V_{CL} = 0.8V$, $V_{OUT} = 100\ mV_{PP}$ | 25°C | | 300 | | V | MHz |
| LSBW | Large-Signal Bandwidth | $V_G = 12V$, $V_{CL} = 0.8V$, $V_{OUT} = 4\ V_{PP}$ | 25°C | | 300 | | V | MHz |
| $t_r$, $t_f$ | Output Rise Time, Fall Time | $V_{CL} = 0.8V$, $V_{OUT} = 4\ V_{PP}$ | 25°C | | 1.5 | 2 | IV | ns |

Note 1: S2 Closed, $V_{CL} = 0.8V$, $V_{IN} = 2.7V$ to 3.4V, Referred to $V_G = 12V$ data.

## EL5003C Test Circuit

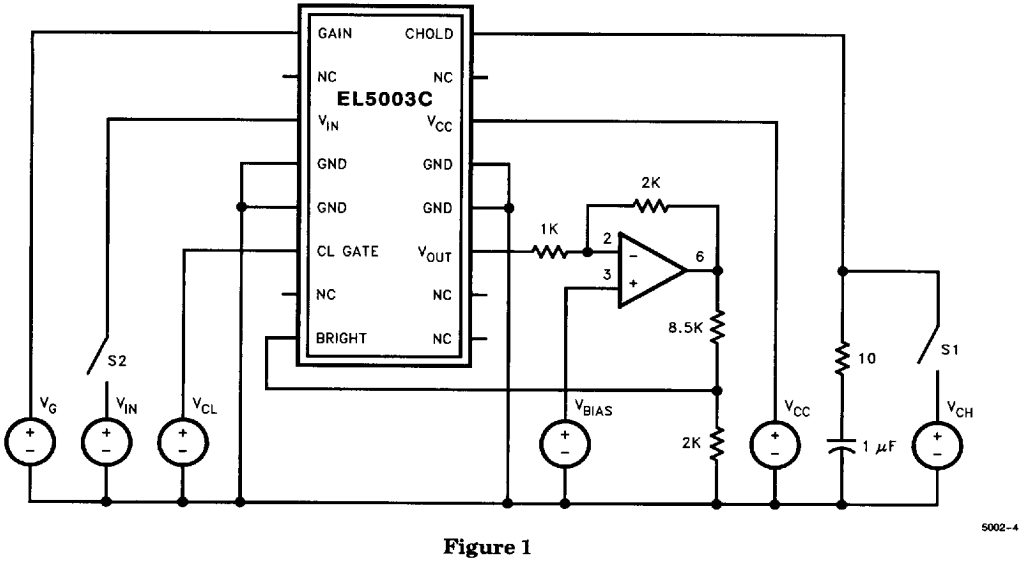
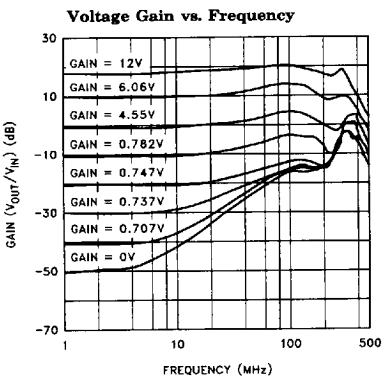



**Figure 1**

# EL5003C
## High Speed CRT Amplifier

## Performance Curves

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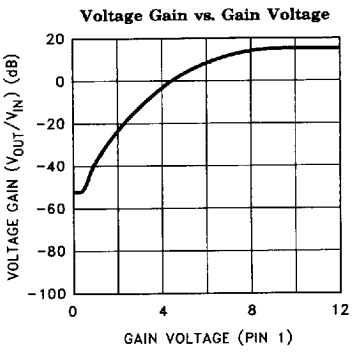


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## EL5003C Block Diagram

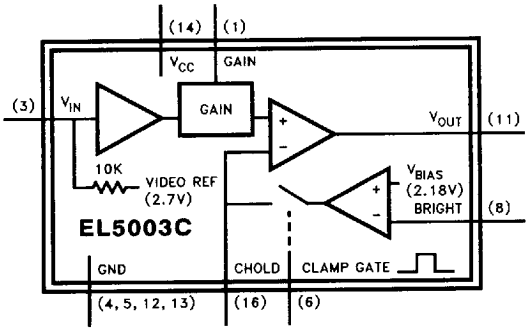


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**Figure 2**

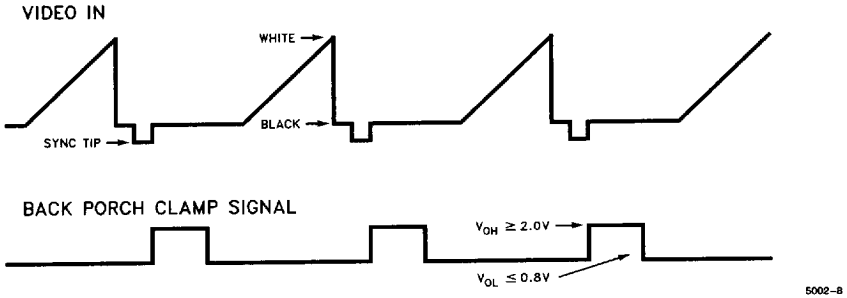


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**Figure 3**

## Applications Information

### Product Description

As seen in the block diagram (Figure 2), the EL5003C CRT Amplifier consists of an input buffer, a gain control, a post-amplifier, and DC-restore circuitry which combine to allow control of both the contrast (gain) and brightness (offset) of a video signal when driving an external high-voltage stage connected to the cathode of a CRT.

If we describe the EL5003C functionality by first following the video input signal path, we find that an AC-coupled video signal is applied to $V_{IN}$ (Pin 3), which is internally biased to 2.7V through a 10 kΩ resistor. The video signal is then buffered and passes through a variable attenuator which is controlled by the GAIN pin (Pin 1). Attenuation ranges from 0 dB (GAIN pin at 12V) to −50 dB (GAIN pin at 0V), and is used to vary the contrast level of the outgoing video signal. The signal is then amplified by the post-amplifier with a gain of 7.5 V/V, and exits at $V_{OUT}$ (Pin 11). The output stage is self-biasing and does not need an external pull-down resistor for proper operation.

The DC-restore portion of the EL5003C is switchable, and is enabled by placing a TTL- or CMOS-compatible HIGH signal at the CLAMP GATE pin (Pin 6). When enabled, the DC-restore circuitry adds a controlled DC-offset to the EL5003C's internal post-amplifier so that the output of the EL5003C correctly biases the external high-voltage amplifier connected to $V_{OUT}$. This controlled variation of the EL5003C's output offset voltage is used to vary the brightness of the CRT when the external high-voltage amplifier is DC-coupled to the CRT cathode. If AC-coupling is used in the high-voltage stage, the DC-restore portion of the EL5003C can be used to properly bias the output stage transistors of the external high-voltage stage.

In normal applications, this clamping function is enabled by an external back-porch clamp signal which appears during the black level reference period of the video signal following the horizontal sync pulse (Figure 3). This allows DC-restoration to occur at the beginning of each horizontal scan line.

To accomplish the DC-restoration, the EL5003C requires an external high-voltage output stage with inverting gain. The EL5003C contains an amplifier which compares an internal 2.18V reference voltage with an external feedback voltage provided at the BRIGHT pin (Pin 8). When using a high-voltage output stage which is DC-coupled to the CRT cathode (Figure 4), the external feedback voltage is normally provided by a high-impedance resistor-divider from the final output at the CRT cathode. When using a high-voltage output stage with AC-coupled brightness (Figure 5), the external feedback voltage is normally provided by a high-impedance resistor-divider from the output of the contrast portion of the high-voltage output stage, i.e. before the coupling capacitor. In this case, the brightness control of the EL5003C is used to set the biasing of the output stage transistors, and the DC-restoration occurs with separate external circuitry after the coupling capacitor.

The output of the DC-restore amplifier is used to charge (or discharge) an external 1 μF capacitor located at the CHOLD pin (Pin 16) until the voltage applied to the BRIGHT pin (Pin 8) matches the 2.18V internal bias voltage. For proper operation of the EL5003C, the capacitor should also have a 10Ω resistor placed in series with it. In turn, the voltage held on this capacitor is used to drive the internal circuitry creating the DC-offset required for proper DC-restoration.

The EL5003C is designed for use on +12V (Pin 14) and Ground (Pins 4, 5, 12, and 13). The remaining package pins (2, 7, 9, 10, 15) are not connected internally and should be grounded for best operation.

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## Applications Information — Contd.

### DC-Coupling vs AC-Coupling in the Output Stage

The EL5003C can easily be used with a high-voltage output stage which is either AC- or DC-coupled to the CRT. DC-coupling is less complex because the EL5003C controls both brightness and contrast, but the DC-coupled signal to the CRT can have about 40V of peak-to-peak contrast voltage on top of about 80V of brightness voltage. These large voltages require external transistors capable of sustaining more than 100V of breakdown.

AC-coupling has advantages in terms of power dissipation and transistor cost. It allows the approximately 40V of peak-to-peak contrast voltage to be created by the output stage, independent of the brightness voltage. This signal would then be AC-coupled to the CRT where the additional brightness voltage would be added. By AC-coupling, the breakdown requirements of the transistors in the high-voltage output stage are reduced from about 100V to about 60V. This reduction in breakdown voltage allows the use of less expensive (or higher performance) transistors, and the power-dissipation in the high-voltage output stage is reduced to about 50% of the DC-coupled application.

The disadvantage of AC-coupling is that the brightness control of the EL5003C will only affect the biasing of the high-voltage output stage, and not the actual brightness voltage applied to the CRT. To correctly set the brightness, an additional DC-restore is required to perform the clamping after the coupling capacitor.

### DC-Coupled Monochrome Application

Figure 4 is an example using the EL5003C in a DC-coupled Monochrome application. The 1k pot R1 is used for contrast control, where 12V at the GAIN pin (Pin 1) provides 0 dB of attenuation, and 0V provides 50 dB of attenuation. C1 is used to AC-couple the video signal to the EL5003C. A value of 10 $\mu$F is suggested for C1 so that the voltage droop from the EL5003's 8 k$\Omega$ input impedance remains acceptably low during each horizontal scan. C2 is charged or discharged by the DC-restore circuitry to offset the output voltage of the EL5003C. A value of 1 $\mu$F is suggested for C2 so that the input bias currents of the DC-restore circuitry have a minimal effect on output voltage droop during each horizontal scan. R2 has been added in series with C2 to improve stability of the DC-restore circuitry. A value of 10$\Omega$ is suggested for R2. R10 has been included to further reduce the voltage droop during each horizontal scan by adding a bleed current to approximately cancel the bias current of the DC-restoration circuitry. A value of 330 k$\Omega$ for R10 provides enough bleed current into C2 to center the droop current about 0 $\mu$A over variations in gain and offset. C5 and C6 have been added for supply bypassing of the EL5003C. It is important that C6 be as close as possible to the $V_{CC}$ pin (Pin 14), with C5 nearly as close as C6. Recommended values are 0.1 $\mu$F ceramic for C6, and 4.7 $\mu$F tantalum for C5.

Looking at the components in the high-voltage output stage, R3 and C3 have been chosen for reasonable biasing and peaking of the gain. R3 has a suggested value of 15$\Omega$, and C3 has a suggested value of 10 pF. R4 and L1 create the proper biasing and peaking at the gain node of the output stage. With R4 = 220$\Omega$ and L1 = 0.1 $\mu$H, the output stage has a voltage gain of about 10 V/V. Q1 is a Motorola LT1001A NPN transistor used in a common-emitter configuration. It is responsible for setting up the biasing of the entire high-voltage output stage. It has a low breakdown-voltage, so it is cascoded by transistor Q2 which is a Motorola LT1817 NPN transistor. Both Q1 and Q2 may require some series resistance at their base for proper stability of the high-voltage output stage. R5 and R6 provide some degeneration for the output transistors Q3 and Q4. R5 and R6 have values of 10$\Omega$, while Q3 is a Motorola LT5839 PNP transistor and Q4 is a Motorola LT1839 NPN transistor. C4 helps maintain the dynamic performance of the high-voltage output stage over frequency. It has a recommended value of 1000 pF. D1 and D2 are large, slow rectifier diodes with no more than 600 mV of forward bias at 70 mA. D1 and D2 remain predominantly capacitive at high frequencies, and they should be connected with short leads between the bases of Q3 and Q4.

## Applications Information — Contd.

R7, R8, and R9 are used to determine the voltage at the CRT after DC-restoration. R8 has a suggested value of 100 kΩ, R9 has a suggested value of 2 kΩ, and R7 is a potentiometer with a suggested value of 3 kΩ. When DC-restoration has been gated on (CLAMP GATE is HIGH) then in steady-state, we know that the voltage at the wiper of the potentiometer R7 will match the internal VBIAS of the EL5003C (2.18V). So, for example, if the wiper is at the top of R7, then there is a 21:1 resistor divider between the cathode of the CRT and Pin 8 of the EL5003C. If Pin 8 is at 2.18V in steady state, then the CRT voltage is at 45.78V. Similarly, if the wiper is at the bottom of R7, then there is a 51.5:1 resistor divider, and the CRT is at 112.27V. This should provide more than enough brightness range for most applications.

For this example, the high-voltage supply has been chosen at 120V under the assumption that the G1 connection of the CRT is grounded. However, for most modern high speed monochrome applications, G1 is either driven differentially with respect to the CRT cathode, or biased below ground to allow a lower final supply voltage.

### AC-Coupled Monochrome Application

Figure 5 shows an example of an AC-coupled monochrome application. The basic circuit is very similar to the DC-coupled application of Figure 4, with the addition of an AC-coupling capacitor C8 and a relatively simple secondary DC-restore circuit at the high-voltage stage output. In addition, the 120V power supply of Figure 4 has been reduced to 60V, and another 120V supply has been added after the coupling capacitor. The value of the divider resistor R8 has also changed from 100 kΩ to 51 kΩ due to the reduction in supply voltage.

The external DC-restore circuitry has the advantage of being quite simple, but has the disadvantage of clamping on the most positive voltage of the outgoing signal (which is the most negative voltage of the incoming signal). In most applications, this corresponds to the sync-tip voltage rather than the black-reference voltage. In practice, these voltages are usually well correlated, so DC-restoration to the sync-tip is not generally an issue.

Just as in the DC-coupled application above, this example assumes that G1 of the CRT is grounded. In most modern high speed monochrome circuits, G1 is either driven differentially with respect to the CRT cathode, or biased below ground to allow a lower supply voltage for the high-voltage stage.

### AC-Coupled Color Application

The color application of Figure 6 is based on the monochrome application of Figure 5. The 3 channels are each identical to the monochrome application, except for gain and contrast control. In this application, contrast is varied with a main contrast potentiometer, while each channel has an additional potentiometer for contrast trim. Similarly, there is a main brightness potentiometer, and an additional brightness trim potentiometer for each channel.

### Power Dissipation

The EL5003C has been packaged in a 16-Pin PDIP with a special leadframe for improved power dissipation. This package allows almost twice the power dissipation of a regular package by connecting the internal die-attach area directly to pins 4, 5, 12, and 13 (the GND connection of the EL5003C). Heat is conducted via these 4 leads, out of the package, and into the PC-board. It is therefore highly recommended that a socket not be used, and that as much ground plane as possible be connected to the GND pins.

Under the conditions listed above, the package thermal resistance is 56°C/W. At a maximum supply current of 72 mA, and an absolute maximum supply voltage of 13.2V, worst-case quiescent power dissipation is:

$$PD(\text{Quiescent}) = 13.2V \times 72\ mA = 950\ mW.$$

If we assume 15 pF of load capacitance and that the output is slewing at (0.8 × 4V) ÷ 1.5 ns, we get a slew-rate of 2.13 V/ns and a slewing current of 32 mA. If we assume that the output is slewing half of the time, we get an additional worst-case power dissipation of:

$$PD(\text{Active}) = 0.5 \times 13.2V \times 32\ mA = 211\ mW.$$

## Applications Information — Contd.

The total power dissipation is then:

$P_{D(Total)} = 950\ mW + 211\ mW = 1.16W.$

The maximum die temperature is then:

$T_{MAX}(die) = T_{MAX}(ambient) + (1.16W) \times (56°C/W) = 140°C.$

Even under this worst-case scenario, the die temperature remains below the absolute rating of 150°C.

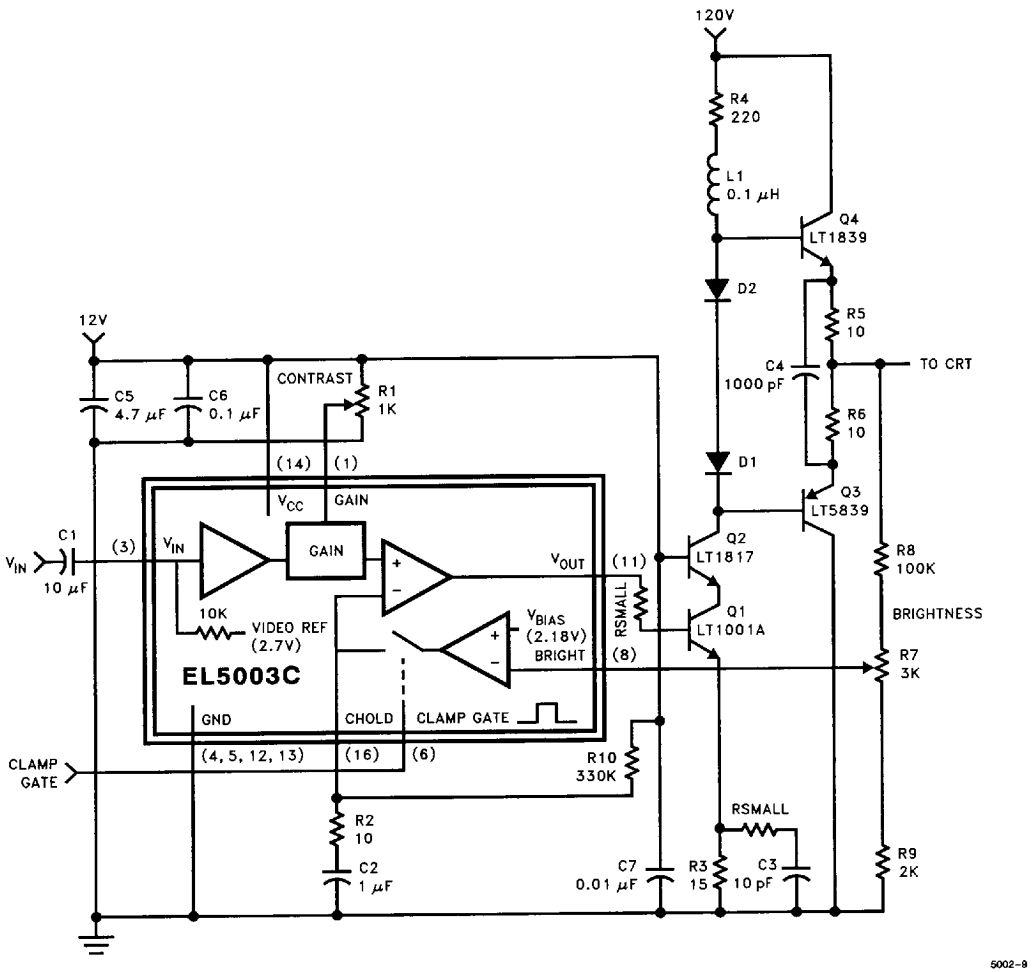


**Figure 4. Monochrome Application Example HV-Stage DC-Coupled to CRT Cathode**

## Applications Information — Contd.

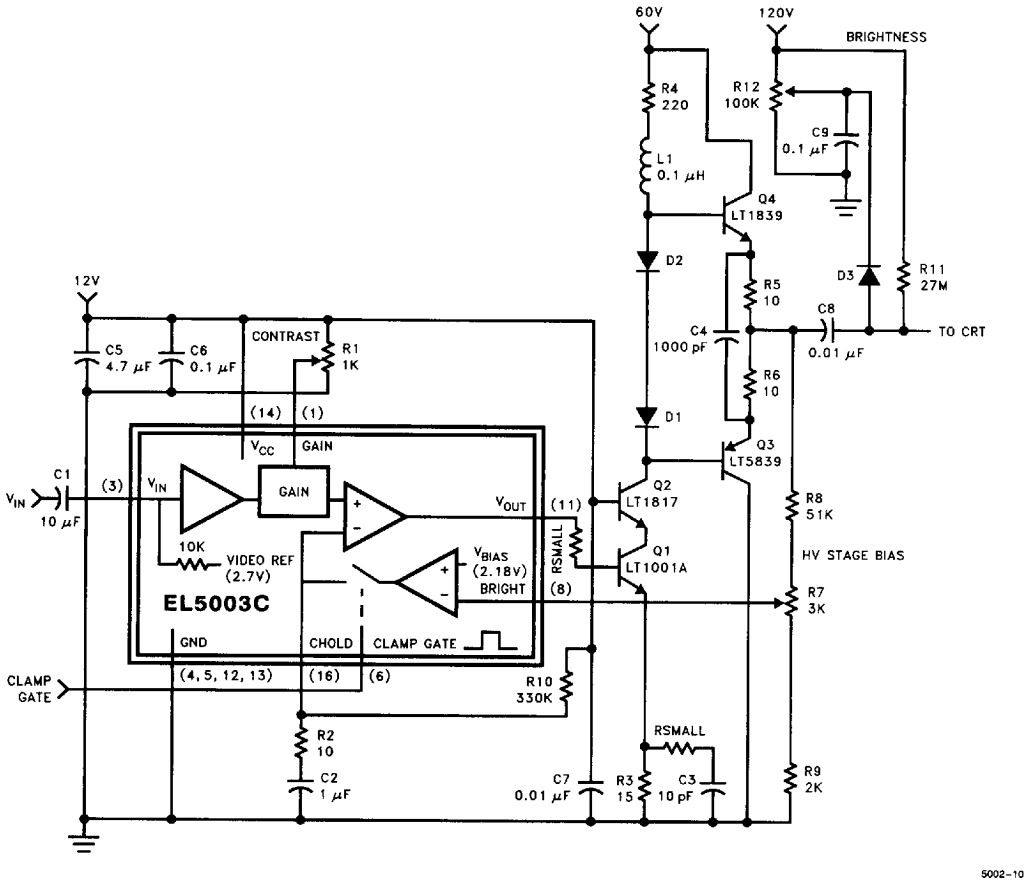


**Figure 5. Monochrome Application Example**
**HV-Stage AC-Coupled to CRT Cathode**

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## Applications Information — Contd.

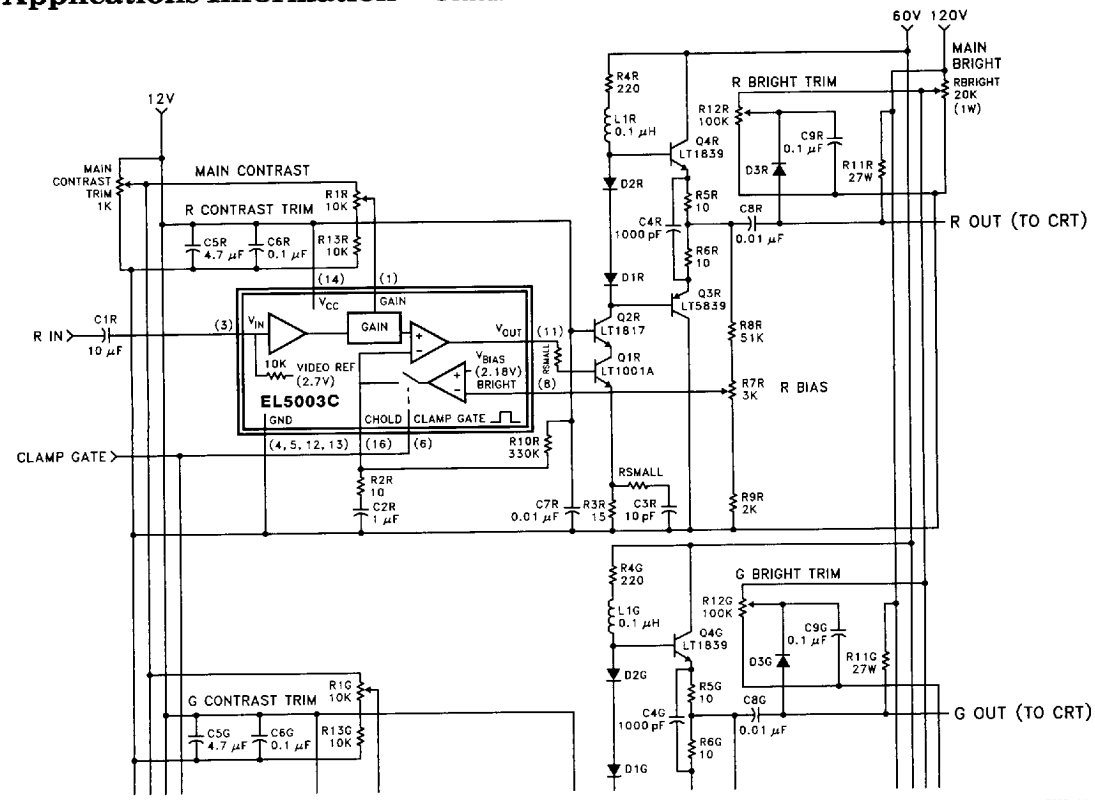


**Figure 6. Color Application Example: HV-Stage AC-Coupled to CRT Cathode**

## Applications Information — Contd.

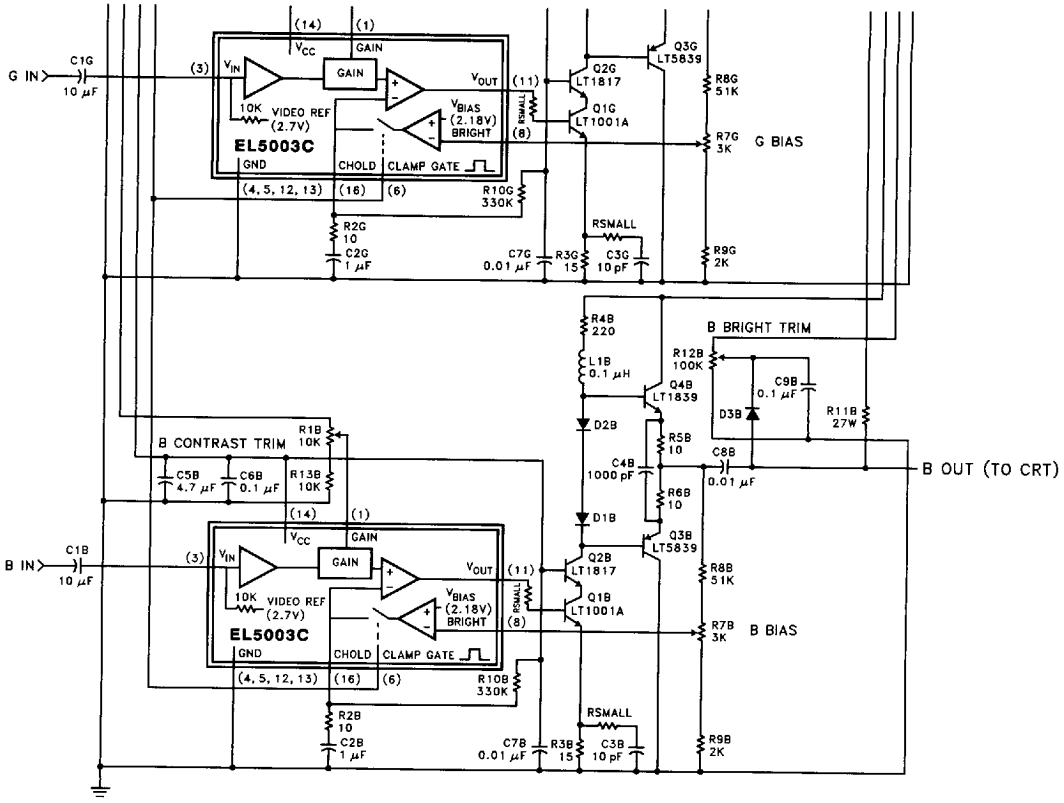


**Figure 6. Color Application Example: HV-Stage AC-Coupled to CRT Cathode — Contd.**