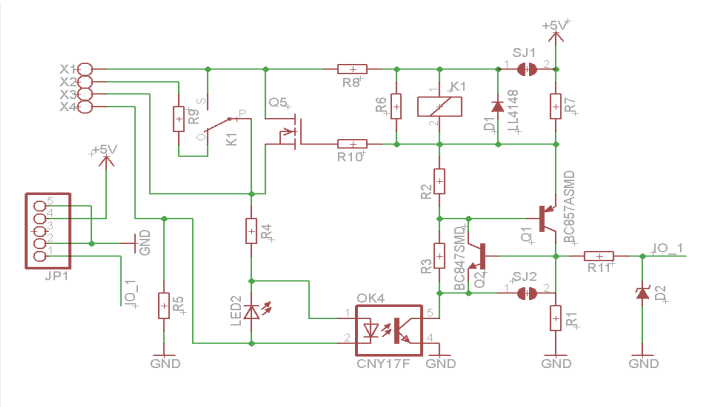
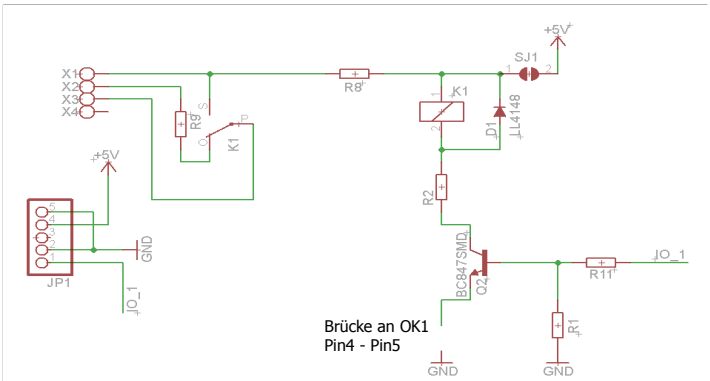
**Multi-IO Bestückungsvarianten**




| | | | |
|---|---|---|---|
| R1 | | SJ1 | |
| R2 | | SJ2 | |
| R3 | | | |
| R4 | | | |
| R5 | | | |
| R6 | | | |
| R7 | | | |
| R8 | | | |
| R9 | | | |
| R10 | | | |

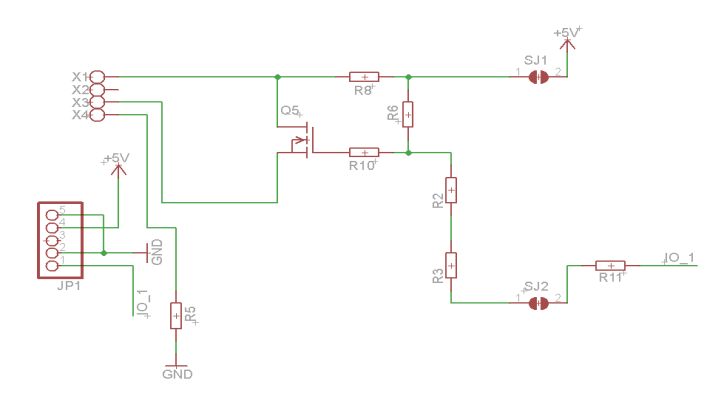
Komplettschaltplan




| | | | |
|---|---|---|---|
| R1 | 10k | SJ1 | gebrückt |
| R2 | 0R | SJ2 | offen |
| R3 | entf. | | |
| R4 | entf. | | |
| R5 | entf. | | |
| R6 | entf. | | |
| R7 | entf. | | |
| R8 | 0R | | |
| R9 | 0R | | |
| R10 | entf. | | |
| R11 | 10k | | |

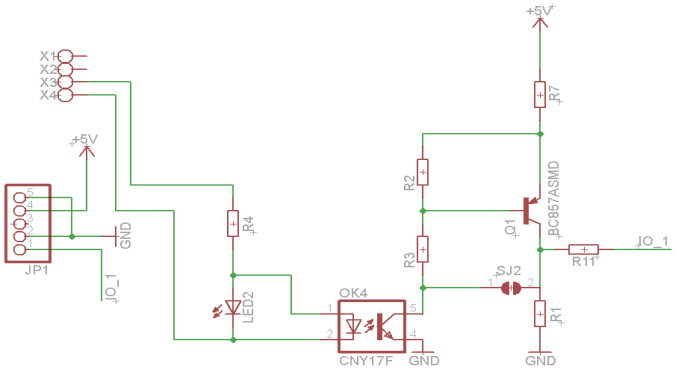
Wahlweise R8 o. SJ1

Variante Relaisausgang



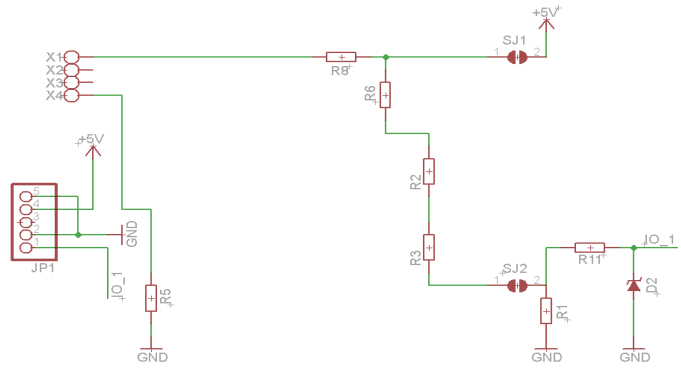

| | | | |
|---|---|---|---|
| R1 | entf. | SJ1 | offen |
| R2 | 0R | SJ2 | gebrückt |
| R3 | 0R | | |
| R4 | entf. | | |
| R5 | 0R | | |
| R6 | 10k | | |
| R7 | entf. | | |
| R8 | 0R | | |
| R9 | entf. | | |
| R10 | 0R | | |
| R11 | 0R | | |

Variante Fet-Schaltausgang



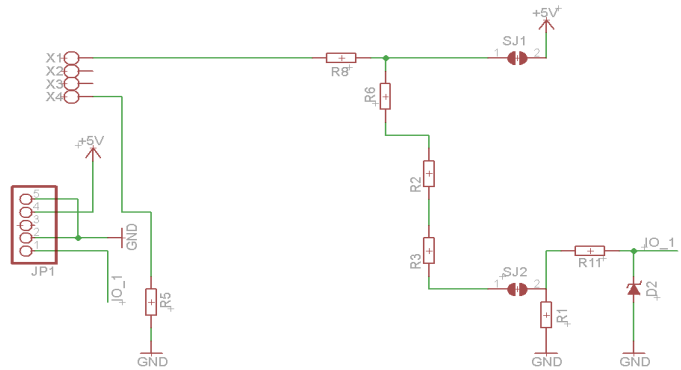

| | | | |
|---|---|---|---|
| R1 | 10k | SJ1 | offen |
| R2 | 10k | SJ2 | offen |
| R3 | 10k | | |
| R4 | tbd | | |
| R5 | entf. | | |
| R6 | entf. | | |
| R7 | entf. | | |
| R8 | entf. | | |
| R9 | entf. | | |
| R10 | entf. | | |
| R11 | 0R | | |

Variante Schalteingang optisch isoliert




| | | | |
|---|---|---|---|
| R1 | entf. | SJ1 | offen |
| R2 | 0R | SJ2 | gebrückt |
| R3 | 0R | | |
| R4 | entf. | | |
| R5 | 0R | | |
| R6 | 0R | | |
| R7 | entf. | | |
| R8 | 0R | | |
| R9 | entf. | | |
| R10 | 0R | | |
| R11 | 0R | | |

Variante analoger Eingang




| | | | |
|---|---|---|---|
| R1 | tbd | SJ1 | offen |
| R2 | 10k | SJ2 | offen |
| R3 | tbd | | |
| R4 | entf. | | |
| R5 | entf. | | |
| R6 | entf. | | |
| R7 | entf. | | |
| R8 | entf. | | |
| R9 | entf. | | |
| R10 | entf. | | |
| R11 | 0R | | |

Variante analoger Eingang mit R3/R1 als Spannungsteiler