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| | |
|---|---|
| **Left document:** | CH32V003DS0.pdf |
| **Right document:** | CH32V003DS0.pdf |

## What is this document?

This is a comparison of two documents. The two documents are interleaved such that the left document is displayed on even pages and the right document is displayed on odd pages.

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## Overview

CH32V003 series is an industrial-grade general-purpose microcontroller designed based on QingKe RISC-V2A core, which supports 48MHz system main frequency in the product function. The series features wide voltage, single-wire serial debug interface, low-power consumption and ultra-small package. It provides commonly used peripheral functions, built-in 1 group of DMA controller, 1 group of 10-bit analog-to-digital conversion ADC, 1 group of op-amp comparator, multiple timers, standard communication interfaces such as USART, I2C, SPI, etc. The rated operating voltage of the product is 3.3V or 5V, and the operating temperature range is -40℃～85℃ industrial- grade.

## Features

- **Core**
  - QingKe 32-bit RISC-V core, RV32EC instruction set
  - Fast programmable interrupt controller + hardware interrupt stack
  - Support 2-level interrupt nesting
  - Support system main frequency 48MHz
- **Memory**
  - 2KB volatile data storage area SRAM
  - 16KB program memory CodeFlash
  - 1920B BootLoader
  - 64B non-volatile system configuration memory
  - 64B user-defined memory
- **Power management and low-power consumption**
  - System power supply $V_{DD}$: 3.3V or 5V
  - Low-power mode: Sleep, Standby
- **Clock & Reset**
  - Built-in factory-trimmed 24MHz RC oscillator
  - Built-in 128KHz RC oscillator
  - High-speed external 4~25MHz oscillator
  - Power on/down reset, programmable voltage detector
- **1 group of 1-channel general-purpose DMA controller**
  - 7 channels, support ring buffer
  - Support TIMx/ADC /USART/I2C/SPI
- **1 group of OPA and comparator: connected with ADC and TIM2**
- **1 group of 10-bit ADC**
  - Analog input range: 0~$V_{DD}$
  - 8 external signals + 2 internal signals
  - Support external delayed triggering
- **Multiple timers**
  - 1 16-bit advanced-control timers, with dead zone control and emergency brake; can offer PWM complementary output for motor control
  - 1 16-bit general-purpose timers, provide input capture/output comparison/PWM/pulse counting/incremental encoder input
  - 2 watchdog timers (independent watchdog and window watchdog)
  - SysTick: 32-bit counter
- **Communication interfaces**
  - 1 USART interfaces
  - 1 I2C interfaces
  - 1 SPI interfaces
- **GPIO port**
  - 3 groups of GPIO ports, 18 I/O ports
  - Mapping 1 external interrupt
- **Security features: 64-bit unique ID**
- **Debug mode: 1-wire serial debug interface (SDI)**
- **Package: SOP, TSSOP or QFN**

# CH32V003 Datasheet

V1.7

## Overview

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- **Communication interfaces**
  - USART interface
  - I2C interface
  - SPI interface
- **GPIO port**
  - 3 groups of GPIO ports, 18 I/O ports
  - Mapping 1 external interrupt
- **Security features: 96-bit unique ID**
- **Debug mode: 1-wire serial debug interface (SDI)**
- **Package: SOP, TSSOP or QFN**

| Model | Flash memory | SRAM | Pin No. | General-purpose I/O | Advanced-control timer | General-purpose timer | Watchdog | System clock source | ADC Channel No. | SPI | I2C | USART | Package Form |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CH32V003F4P6 | 16K | 2K | 20 | 18 | 1 | 1 | 2 | 3 | 8 | 1 | 1 | 1 | TSSOP20 |
| CH32V003F4U6 | | | | | | | | | | | | | QFN20 |
| CH32V003A4M6 | 16K | 2K | 16 | 14 | 1 | 1 | 2 | 3 | 6 | - | 1 | 1 | SOP16 |
| CH32V003J4M6 | 16K | 2K | 8 | 6 | 1 | 1 | 2 | 3 | 6 | | 1 | 1 | SOP8 |

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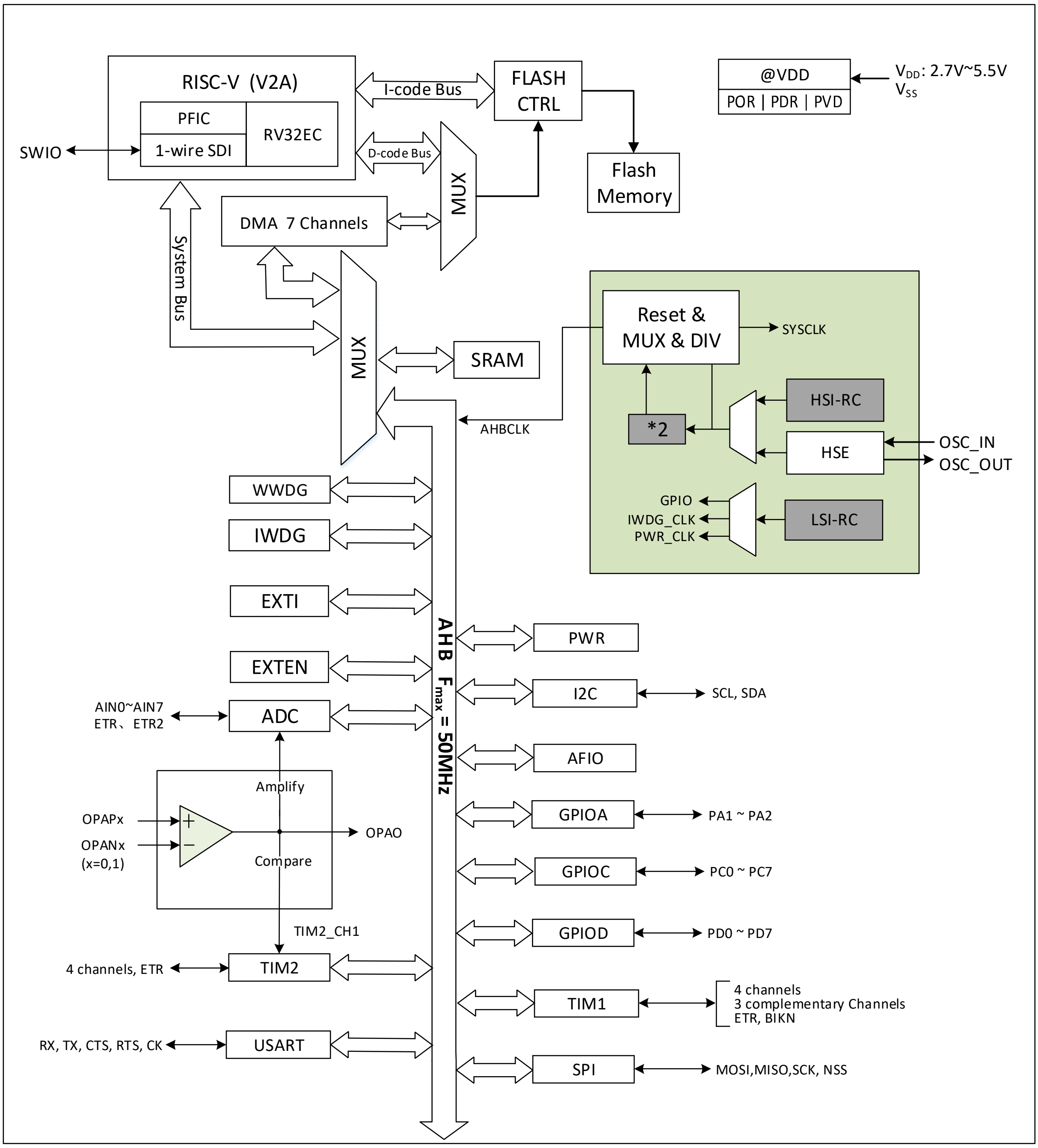
# Chapter 1 Specification

## 1.1 System architecture

The microcontroller is based on the RISC-V instruction set of QingKe V2A design, and its architecture includes the core, arbitration unit, DMA module, SRAM storage and other parts of the interaction through multiple groups of buses. The design integrates a general-purpose DMA controller to reduce CPU load and improve access efficiency, and also has data protection mechanisms and automatic clock switching protection to increase system stability. The following diagram shows the overall architecture of the product.

Figure 1-1 System block diagram



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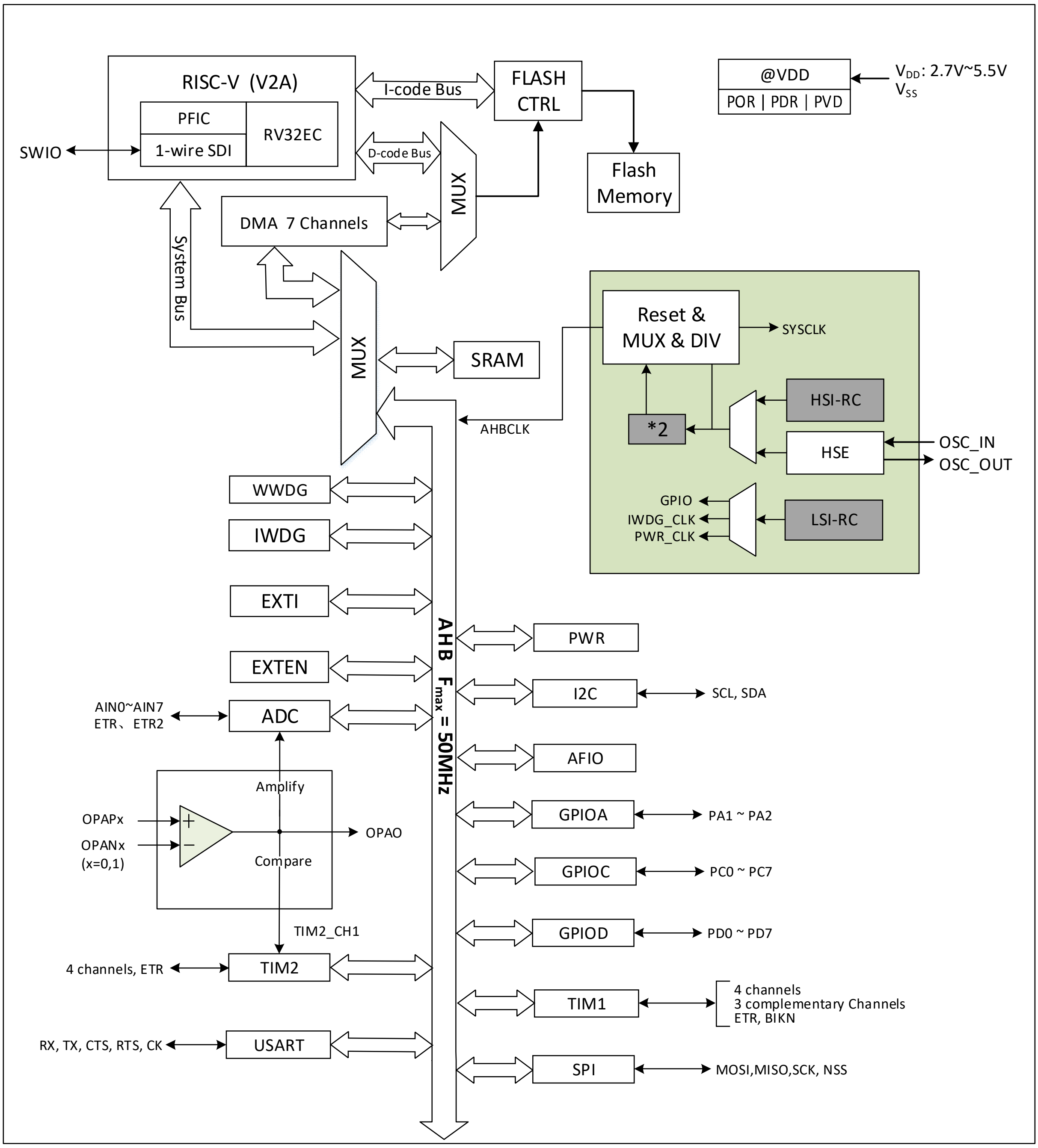
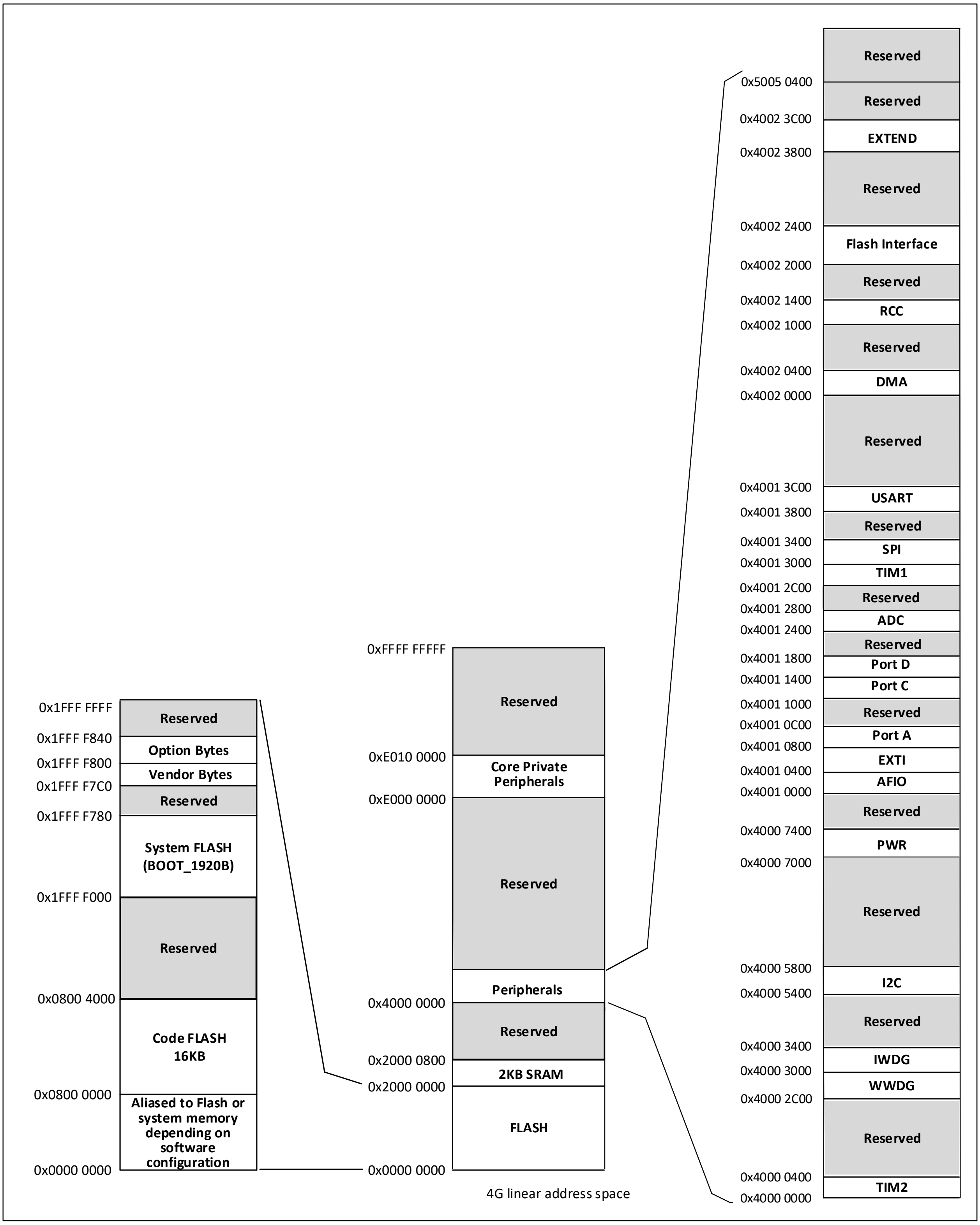


## 1.2 Memory map

Figure 1-2 Memory address map



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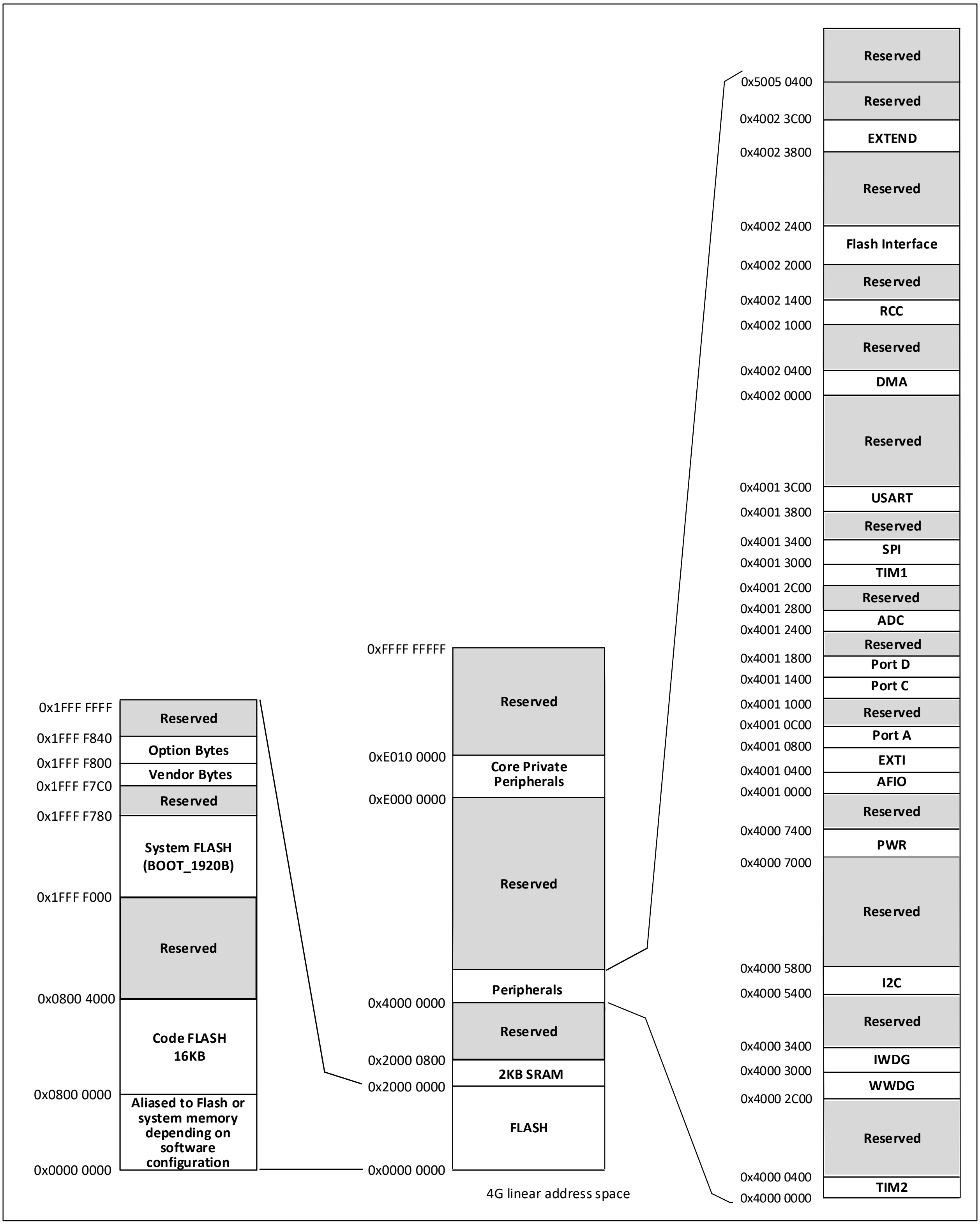

## 1.3 Clock tree

Three groups of clock sources are introduced into the system: internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI), external high-frequency oscillator (HSE), and external low-frequency oscillator (LSE). Among them, the low-frequency clock source provides the clock reference for RTC and independent watchdog. The high-frequency clock source is directly or indirectly output as system clock (SYSCLK) via 2X frequency. The system clock is then provided by each prescaler to provide the AHB domain in peripheral control clock and sampling or output clock. Some modules need to be directly provided by the PLL clock.

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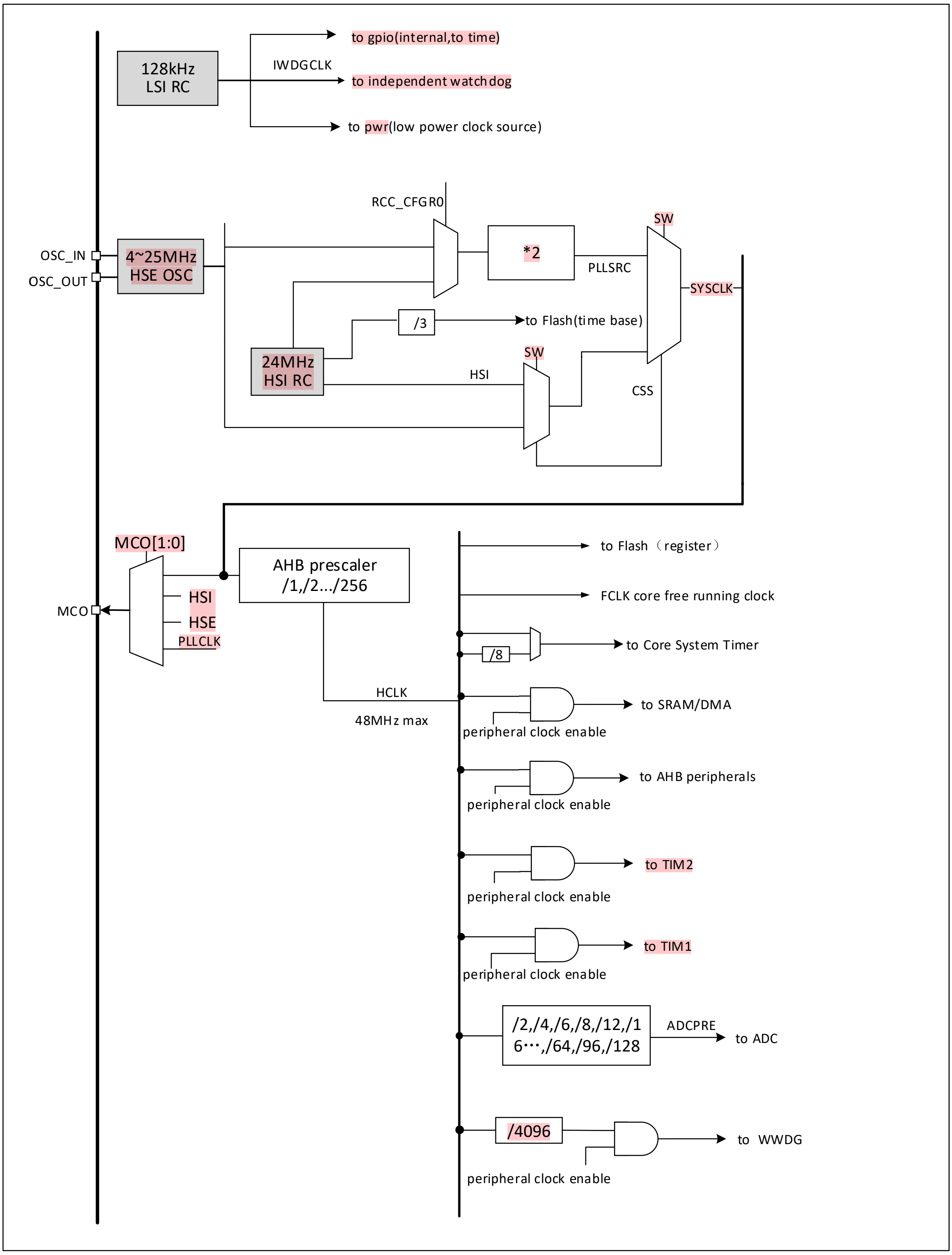

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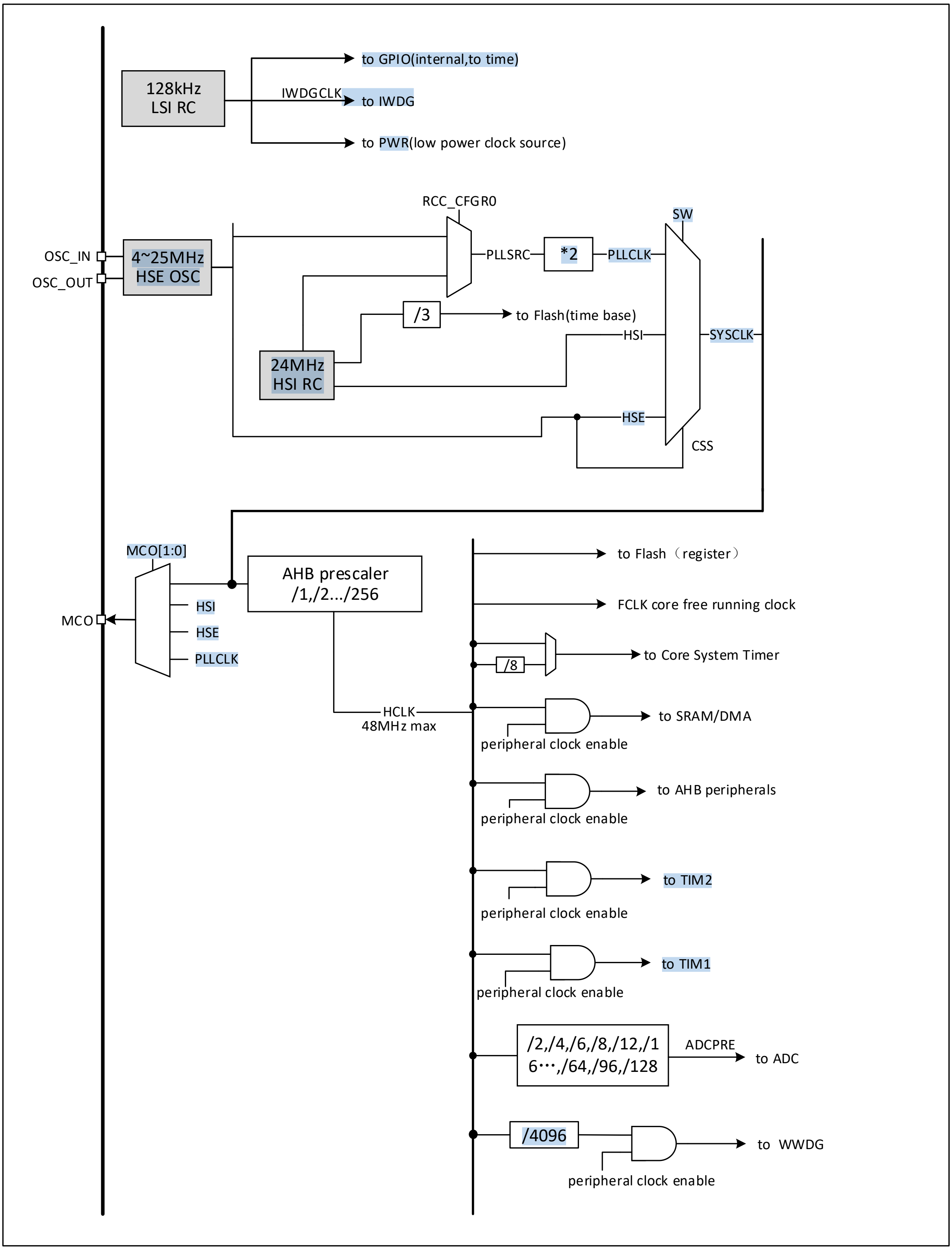

# 1.4 Functional description

## 1.4.1 RISC-V2A processor

The RISC-V2A supports the EC subset of the RISC-V instruction set. The processor is managed internally in a modular fashion and contains units such as a fast programmable interrupt controller (PFIC), extended instruction support, and more. The bus is connected to an external unit module to enable interaction between the external function module and the core. RV32EC instruction set, small-end data mode.

The processor with its minimal instruction set, multiple operating modes, and modular custom expansion can be flexibly applied to different scenarios of microcontroller design, such as small area low-power embedded scenarios.

- Support machine mode
- Fast Programmable Interrupt Controller (PFIC)
- 2-level hardware interrupt stack
- 1-wire serial debug interface (SDI)
- Custom extended commands

## 1.4.2 On-chip memory and boot mode

Built-in 2K bytes SRAM area for data storage, data loss after power down.

Built-in 16K bytes of program flash memory storage (Code FLASH) for user applications and constant data storage.

Built-in 1920 bytes of system storage (System FLASH) for system bootloader storage (factory-cured bootloader)

64 bytes are used for the system non-volatile configuration information storage area and 64 bytes are used for the user select word storage area.

Support Boot and user code jumping to each other.

## 1.4.3 Power supply scheme

$V_{DD}$ = 2.7～5.5V: Power supply for some I/O pins and internal voltage regulator ($V_{DD}$ performance gradually deteriorates if less than 2.9V when using ADC).

## 1.4.4 Power supply monitor

This product integrates a power-on reset (POR)/power-down reset (PDR) circuit, which is always in working condition to ensure that the system is in supply. It works when the power exceeds 2.7V; when $V_{DD}$ is lower than the set threshold ($V_{POR/PDR}$), the device is placed in the reset state without using an external reset circuit.

In addition, the system is equipped with a programmable voltage monitor (PVD), which needs to be turned on by software to compare the voltage of $V_{DD}$ power supply with the set threshold $V_{PVD}$.Turn on the corresponding edge interrupt of PVD, and you can receive interrupt notification when $V_{DD}$ drops to the PVD threshold or rises to the PVD threshold. Refer to Chapter 4 for the values of $V_{POR/PDR}$ and $V_{PVD}$.

## 1.4.5 Voltage regulator

After reset, the regulator is automatically turned on, and there are 3 operation modes according to the application mode.

- ON mode: Normal operation, providing stable core power.
- Low-power mode: When the CPU enters Stop mode, system automatically enters Standby mode.

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### 1.4.6 Low-power mode

The system supports 2 low-power modes, which can be selected for low-power consumption, short start-up time and multiple wake-up events to achieve the best balance.

- Sleep mode

In Sleep mode, only the CPU clock is stopped, but all peripheral clocks are powered normally and the peripherals are in a working state. This mode is the shallowest low-power mode, but it is the fastest mode to wake up the system.
Exit condition: any interrupt or wake-up event.

- Standby mode

The PDDS and SLEEPDEEP bits are set, and the WFI/WFE instruction is executed to enter. The power supply of the kernel part is turned off, and the RC oscillator of HSI and the HSE crystal oscillator are also turned off, and the lowest power consumption can be achieved in this mode.
Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, where EXTI signal includes one of 18 external I/O ports, output of PVD, AWU auto-wakeup.

### 1.4.7 Fast Programmable Interrupt Controller (PFIC)

The product's built-in Fast Programmable Interrupt Controller (PFIC) supports up to 255 interrupt vectors, providing flexible interrupt management capabilities with minimal interrupt latency. The current product manages 4 core private interrupts and 23 peripheral interrupt management, with other interrupt sources reserved. the registers of PFIC are all accessible in machine privileged mode.

- 2 individually maskable interrupts
- Provide a non-maskable interrupt NMI
- Hardware interrupt stack (HPE) support without instruction overhead
- Provide 2-way meter-free interrupt (VTF)
- Vector table supports address or command mode
- Support 2-level interrupt nesting
- Support break tail link function

### 1.4.8 External interrupt/event controller (EXTI)

The external interrupt/event controller contains a total of 8 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured with its trigger event (rising or falling edge or double edge) and can be individually masked; the pending register maintains the status of all interrupt requests. EXTI can detect clock cycles with pulse widths less than the internal AHB. 18 general purpose I/O ports are optionally connected to the same external interrupt source.

### 1.4.9 General-purpose DMA controller

The system has built-in 1 group of general-purpose DMA controllers, manages 8 channels in total, and flexibly handles high-speed data transmission from memory to memory, peripherals to memory, and memory to peripherals, and supports ring buffer mode. Each channel has a dedicated hardware DMA request logic to support one or more peripherals' access requests to the memory. The access priority, transfer length, source address and destination address of the transfer can be configured.

The main peripherals used by DMA include: general-purpose/advanced-control/basic timers TIMx, DAC,

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The main peripherals used by DMA include: general-purpose/advanced-control/basic timers TIMx, DAC, USART, I2C and SPI.

*Note: DMA and CPU access the system SRAM after arbitration by the arbiter.*

### 1.4.10 Clock and boot

The system clock source HSI is turned on by default. After the clock is not configured or reset, the internal 24MHz RC oscillator is used as the default CPU clock, and then an external 4~25MHz clock or PLL clock can be additionally selected. When the clock security mode is turned on, if the HSE is used as the system clock (directly or indirectly), the system clock will automatically switch to the internal RC oscillator when the external clock is detected to be invalid, and the HSE and PLL will be automatically turned off at the same time; in low-power consumption mode, the system will automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

### 1.4.11 Analog-to-digital converter (ADC)

The product is embedded with a 10-bit analog/digital converter (ADC) that shares up to eight external channels and two internal channel samples, with programmable channel sampling times for single, continuous, sweep or intermittent conversion. Provides analog watchdog function allows very accurate monitoring of one or more selected channels for monitoring channel signal voltages. Supports external event-triggered transitions with trigger sources including internal signals from the on-chip timer and external pins. Support for using DMA operation. Supports external trigger delay function. When this function is enabled, the controller delays the trigger signal according to the configured delay time when an external trigger edge is generated, and the ADC conversion is triggered as soon as the delay time is reached.

### 1.4.12 Timer and watchdog

The timers in the system include an advanced-control timer, a general-purpose timer, two watchdog timers and system time base timer.

- Advanced-control timer

The advanced-control timer is a 16-bit auto-loading up/down counter with a 16-bit programmable prescaler. In addition to the complete general-purpose timer function, it can be regarded as a three-phase PWM generator distributed to 6 channels, with a complementary PWM output function with dead zone insertion, allowing the timer to be updated after a specified number of counter cycles to repeat counting cycle, braking function, etc. Many functions of the advanced-control timer are the same as the general timer, and the internal structure is also the same. Therefore, the advanced-control timer can cooperate with other TIM timers through the timer link function to provide synchronization or event link functions.

- General-purpose timer

The general-purpose timer is a 16-bit or 32-bit auto-loading up/down counter with a programmable 16-bit prescaler and 4 independent channels. Each channel supports input capture, output comparison, and PWM generation and single pulse mode output. It can also work with advanced-control timers through the timer link function to provide synchronization or event link functions. In Debug mode, the counter can be frozen while the PWM outputs are disabled, thereby cutting off the switches controlled by these outputs. Any general-purpose timer can be used to generate PWM output. Each timer has an independent DMA request mechanism. These timers can also process signals from incremental encoders, as well as digital outputs from 1 to 3 Hall sensors.

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- Independent watchdog

The independent watchdog is a configurable 12-bit down counter that supports 7 frequency division factors. The clock is provided by an internal independent 128 KHz RC oscillator (LSI); because the LSI is independent of the main clock, it can run in Stop and Standby modes. IWDG is outside the main program and can work completely independently. Therefore, it is used to reset the entire system when a problem occurs, or as a free timer to provide timeout management for the application. It can be configured as software or hardware to start the watchdog through the option byte. In Debug mode, the counter can be frozen.

- Window Watchdog

The window watchdog is a 7-bit down counter and can be set to free-running. It can be used to reset the entire system when a problem occurs. It is driven by the main clock and has an early warning interrupt function; in Debug mode, the counter can be frozen.

- SysTick Timer

QingKe microprocessor core comes with a 32-bit incremental counter for generating SYSTICK exceptions (exception number: 15), which can be used exclusively in real-time operating systems to provide a "heartbeat" rhythm for the system, or as a standard 32-bit counter. It has an automatic reload function and a programmable clock source.

### 1.4.13 Communication interface

#### 1.4.13.1 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The product provides 1 group of Universal Synchronous/Asynchronous Receiver Transmitters (USART). It supports full-duplex asynchronous communication, synchronous one-way communication and half-duplex single-wire communication. It also supports LIN (Local Interconnect Network), compatible with ISO7816 smart card protocol and IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation. It also allows multi-processor communication. It uses a fractional baud rate generator system and supports DMA operation continuous communication.

#### 1.4.13.2 Serial Peripheral Interface (SPI)

1 serial peripherals interface (SPI) provide master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8 or 16-bit selection, hardware CRC generation/check for reliable communication, and continuous communication support for DMA operation.

#### 1.4.14.3 I2C bus

1 I2C bus interface, able to work in multi-master mode or slave mode, complete with all I2C bus specific timing, protocols, arbitration, etc., supporting both standard and fast communication speeds.

The I2C interface provides 7-bit or 10-bit addressing and supports dual slave address addressing in 7-bit slave mode. A hardware CRC generator/checker is built-in.

### 1.4.14 General-purpose input and output (GPIO)

The system provides 3 groups of GPIO ports with a total of 18 GPIO pins. Each pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals. Except for ports with analog input functions, all GPIO pins have high current passing capabilities. A locking mechanism is provided to freeze the I/O configuration to avoid accidental writing to the I/O register.

- Independent watchdog

The independent watchdog is a configurable 12-bit down counter that supports 7 frequency division factors. The clock is provided by an internal independent 128 KHz RC oscillator (LSI); because the LSI is independent of the main clock, it can run in Stop and Standby modes. IWDG is outside the main program and can work completely independently. Therefore, it is used to reset the entire system when a problem occurs, or as a free timer to provide timeout management for the application. It can be configured as software or hardware to start the watchdog through the option byte. In Debug mode, the counter can be frozen.

- Window Watchdog

The window watchdog is a 7-bit down counter and can be set to free-running. It can be used to reset the entire system when a problem occurs. It is driven by the main clock and has an early warning interrupt function; in Debug mode, the counter can be frozen.

- SysTick Timer

QingKe microprocessor core comes with a 32-bit incremental counter for generating SYSTICK exceptions (exception number: 15), which can be used exclusively in real-time operating systems to provide a "heartbeat" rhythm for the system, or as a standard 32-bit counter. It has an automatic reload function and a programmable clock source.

### 1.4.13 Communication Interface

#### 1.4.13.1 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The product provides 1 group of Universal Synchronous/Asynchronous Receiver Transmitters (USART). It supports full-duplex asynchronous communication, synchronous one-way communication and half-duplex single-wire communication. It also supports LIN (Local Interconnect Network), compatible with ISO7816 smart card protocol and IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation. It also allows multi-processor communication. It uses a fractional baud rate generator system and supports DMA operation continuous communication.

#### 1.4.13.2 Serial Peripheral Interface (SPI)

1 serial peripherals interface (SPI) provide master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8 or 16-bit selection, hardware CRC generation/check for reliable communication, and continuous communication support for DMA operation.

#### 1.4.14.3 I2C Bus

1 I2C bus interface, able to work in multi-master mode or slave mode, complete with all I2C bus specific timing, protocols, arbitration, etc., supporting both standard and fast communication speeds.

The I2C interface provides 7-bit or 10-bit addressing and supports dual slave address addressing in 7-bit slave mode. A hardware CRC generator/checker is built-in.

### 1.4.14 General-purpose Input and Output (GPIO)

The system provides 3 groups of GPIO ports with a total of 18 GPIO pins. Each pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals. Except for ports with analog input functions, all GPIO pins have high current passing capabilities. A locking mechanism is provided to freeze the I/O configuration to avoid accidental writing to the I/O register.

The I/O pins in the system is provided by $V_{DD}$. Changing the $V_{DD}$ power supply will change the high value of the I/O pin output level to adapt to the external communication interface level. Please refer to the pin description for specific pins.

### 1.4.15 Operational amplifier/comparator (OPA)

The product has a built-in set of op-amps/comparators, with internal selection associated to the ADC and TIM2 (CH1) peripherals, whose inputs and outputs can be selected by changing the configuration for multiple channels. Support for external analog small signals are amplified and fed into the ADC to achieve small signal ADC conversion, can also complete the signal comparator function, the comparison results from the GPIO output or directly into the TIMx input channel.

### 1.4.16 1-wire serial debug interface (SDI)

The core comes with a 1-wire serial debug interface, SWIO pin (Single Wire Input Output). The default debug interface pin function is turned on after system power on or reset.

The I/O pins in the system is provided by $V_{DD}$. Changing the $V_{DD}$ power supply will change the high value of the I/O pin output level to adapt to the external communication interface level. Please refer to the pin description for specific pins.

### 1.4.15 Operational Amplifier/Comparator (OPA)

The product has a built-in set of op-amps/comparators, with internal selection associated to the ADC and TIM2 (CH1) peripherals, whose inputs and outputs can be selected by changing the configuration for multiple channels. Support for external analog small signals are amplified and fed into the ADC to achieve small signal ADC conversion, can also complete the signal comparator function, the comparison results from the GPIO output or directly into the TIMx input channel.

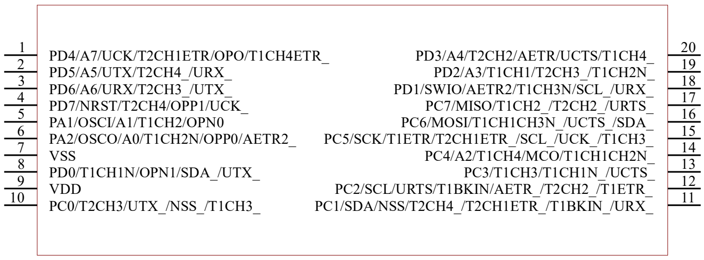
### 1.4.16 1-wire Serial Debug Interface (SDI)

The core comes with a 1-wire serial debug interface, SWIO pin (Single Wire Input Output). The default debug interface pin function is turned on after system power on or reset. The HSI clock must be turned on when using the 1-wire emulation debug interface.

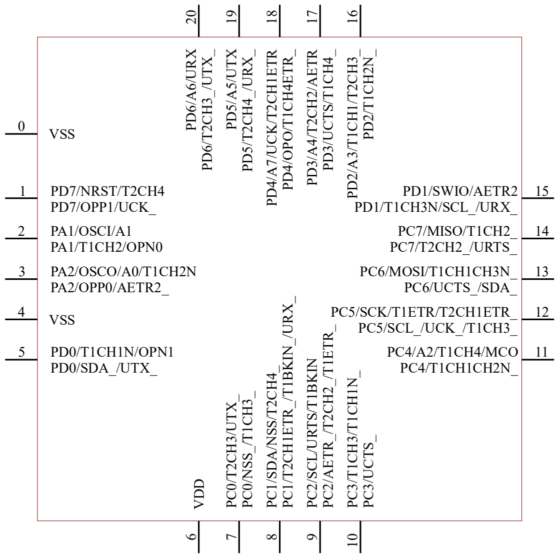
# Chapter 2 Pinouts and Pin Definition

## 2.1 Pinouts

CH32V003F4P6




CH32V003F4U6

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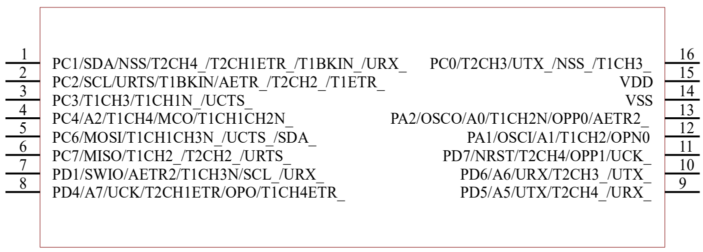

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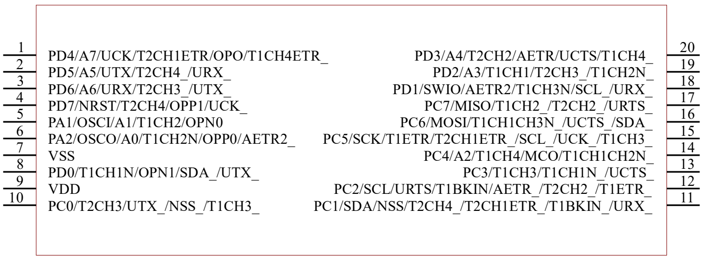
## 2.1 Pinouts

CH32V003F4P6

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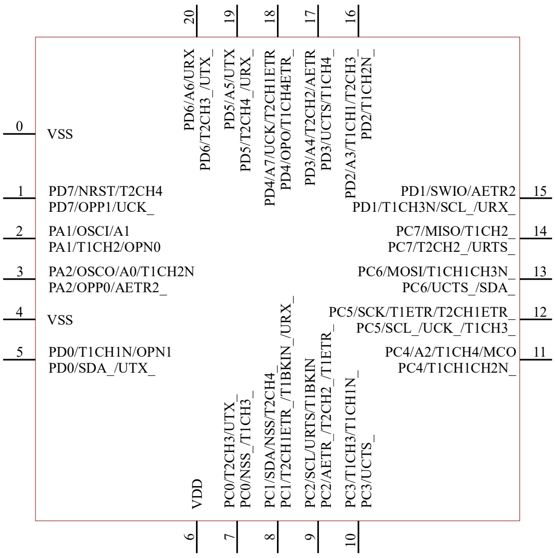


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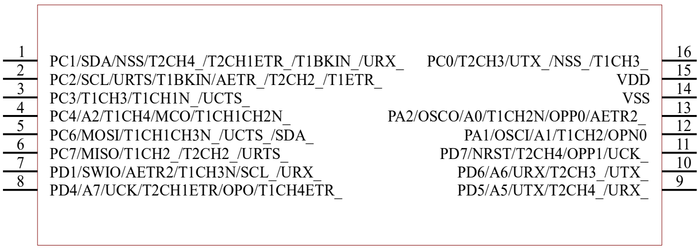

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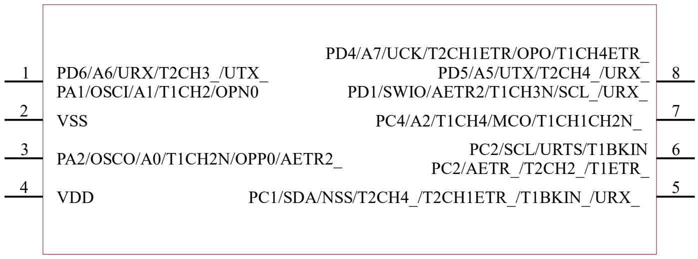



*Note: The multiplexed functions in the pin diagram are abbreviated.*

Example: A: ADC, A7 (ADC_IN7)

T: TIME, T2CH4 (TIM2_CH4)

U: USART, URX (USART_RX)

OP: OPA, OPO (OPA_OUT), OPP1 (OPA_P1)

OSCI (OSCIN)

OSCO (OSCOUT)

SDA (I2C_SDA)

SCL (I2C_SCL)

SCK (SPI_SCK)

NSS (SPI_NSS)

MOSI (SPI_MOSI)

MISO (SPI_MISO)

AETR(ADC_ETR)

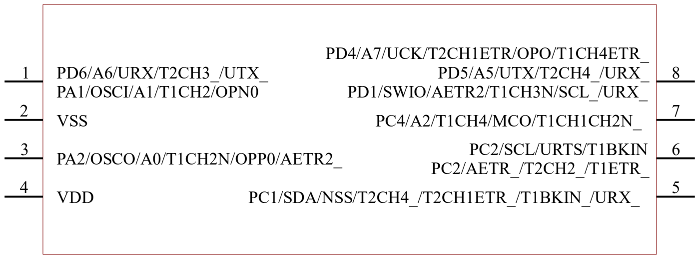
## 2.2 Pin description

Table 2-1 Pin definitions

*Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.*

| Pin No. | | | | Pin name | Pin type | Main function (after reset) | Default alternate function | Remapping function |
|---|---|---|---|---|---|---|---|---|
| SOP16 | TSSOP20 | QFN20 | SOP8 | | | | | |
| - | - | 0 | - | VSS | P | VSS | - | - |
| 8 | 1 | 18 | 8 | PD4 | I/O/A | PD4 | UCK/T2CH1ETR[1]/A7/OPO | TIETR_2/T1CH4_3 |
| 9 | 2 | 19 | 8 | PD5 | I/O/A | PD5 | UTX/A5 | T2CH4_3/URX_2 |
| 10 | 3 | 20 | 1 | PD6 | I/O/A | PD6 | URX/A6 | T2CH3_3/UTX_2 |
| 11 | 4 | 1 | - | PD7 | I/O/A | PD7 | NRST/T2CH4/OPP1 | UCK_1/UCK_2/T2CH4_2 |
| 12 | 5 | 2 | 1 | PA1 | I/O/A | PA1 | T1CH2/A1/OPN0 | OSCI/T1CH2_2 |
| 13 | 6 | 3 | 3 | PA2 | I/O/A | PA2 | TICH2N/A0/OPP0 | OSCO/AETR2_1/TICH2N_2 |
| 14 | 7 | 4 | 2 | VSS | P | VSS | - | - |
| - | 8 | 5 | - | PD0 | I/O/A | PD0 | TICH1N/OPN1 | SDA_1/UTX_1/TICH1N_2 |
| 15 | 9 | 6 | 4 | VDD | P | VDD | - | - |

CH32V003J4M6




*Note: The multiplexed functions in the pin diagram are abbreviated.*

Example: A: ADC, A7 (ADC_IN7)
T: TIME, T2CH4 (TIM2_CH4)
U: USART, URX (USART_RX)
OP: OPA, OPO (OPA_OUT), OPP1 (OPA_P1)
OSCI (OSCIN)
OSCO (OSCOUT)
SDA (I2C_SDA)
SCL (I2C_SCL)
SCK (SPI_SCK)
NSS (SPI_NSS)
MOSI (SPI_MOSI)
MISO (SPI_MISO)
AETR(ADC_ETR)

## 2.2 Pin Description

Table 2-1 Pin definitions

*Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.*

| Pin No. | | | | Pin name | Pin type | Main function (after reset) | Default alternate function | Remapping function |
|---|---|---|---|---|---|---|---|---|
| SOP16 | TSSOP20 | QFN20 | SOP8 | | | | | |
| - | - | 0 | - | VSS | P | VSS | - | - |
| 8 | 1 | 18 | 8 | PD4 | I/O/A | PD4 | UCK/T2CH1ETR(1)/A7/OPO | TIETR_2/T1CH4_3 |
| 9 | 2 | 19 | 8 | PD5 | I/O/A | PD5 | UTX/A5 | T2CH4_3/URX_2 |
| 10 | 3 | 20 | 1 | PD6 | I/O/A | PD6 | URX/A6 | T2CH3_3/UTX_2 |
| 11 | 4 | 1 | - | PD7 | I/O/A | PD7 | NRST/T2CH4/OPP1 | UCK_1/UCK_2/T2CH4_2 |
| 12 | 5 | 2 | 1 | PA1 | I/O/A | PA1 | T1CH2/A1/OPN0 | OSCI/T1CH2_2 |
| 13 | 6 | 3 | 3 | PA2 | I/O/A | PA2 | T1CH2N/A0/OPP0 | OSCO/AETR2_1/T1CH2N_2 |
| 14 | 7 | 4 | 2 | VSS | P | VSS | - | - |
| - | 8 | 5 | - | PD0 | I/O/A | PD0 | T1CH1N/OPN1 | SDA_1/UTX_1/T1CH1N_2 |
| 15 | 9 | 6 | 4 | VDD | P | VDD | - | - |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 16 | 10 | 7 | - | PC0 | I/O | PC0 | T2CH3 | NSS_1/UTX_3/T2CH3_2 /T1CH3_1 |
| 1 | 11 | 8 | 5 | PC1 | I/O/FT | PC1 | SDA/NSS | T1BKIN_1/T2CH4_1 T2CH1ETR(1)_2/URX_3 /T2CH1ETR(1)_3/T1BKIN_3 |
| 2 | 12 | 9 | 6 | PC2 | I/O/FT | PC2 | SCL/URTS/T1BKIN | AETR_1/T2CH2_1 /T1ETR_3/URTS_1 /T1BKIN_2 |
| 3 | 13 | 10 | - | PC3 | I/O | PC3 | T1CH3 | T1CH1N_1/UCTS_1 /T1CH3_2/T1CH1N_3 |
| 4 | 14 | 11 | 7 | PC4 | I/O/A | PC4 | T1CH4/MCO/A2 | T1CH2N_1/T1CH4_2 /T1CH1_3 |
| - | 15 | 12 | - | PC5 | I/O/FT | PC5 | SCK/T1ETR | T2CH1ETR(1)_1/SCL_2 /SCL_3/UCK_3/T1ETR_1 /T1CH3_3/SCK_1 |
| 5 | 16 | 13 | - | PC6 | I/O/FT | PC6 | MOSI | T1CH1_1/UCTS_2/SDA_2 /SDA_3/UCTS_3/T1CH3N_3 /MOSI_1 |
| 6 | 17 | 14 | - | PC7 | I/O | PC7 | MISO | T1CH2_1/URTS_2 /T2CH2_3/URTS_3 /T1CH2_3/MISO_1 |
| 7 | 18 | 15 | 8 | PD1 | I/O/A | PD1 | SWIO/T1CH3N/AETR2 | SCL_1/URX_1/T1CH3N_1 /T1CH3N_2 |
| - | 19 | 16 | - | PD2 | I/O/A | PD2 | T1CH1/A3 | T2CH3_1/T1CH2N_3 /T1CH1_2 |
| - | 20 | 17 | - | PD3 | I/O/A | PD3 | A4/T2CH2/AETR/UCTS | T2CH2_2/T1CH4_1 |

*Note: 1. TIM2_CH1, TIM2_ETR;*

*2. The value after the underline of the remapping function indicates the configuration value of the corresponding bit in the AFIO register. For example: T1CH4_3 indicates that the corresponding bit of the AFIO register is configured as 11b;*

*3. Explanation of table abbreviations:*

*I = TTL/CMOS level Schmitt input.*

*O = CMOS level tri-state output.*

*P = power supply.*

*FT = 5V tolerant.*

*A = Analog signal input or output.*

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 16 | 10 | 7 | - | PC0 | I/O | PC0 | T2CH3 | NSS_1/UTX_3/T2CH3_2 /T1CH3_1 |
| 1 | 11 | 8 | 5 | PC1 | I/O/FT | PC1 | SDA/NSS | T1BKIN_1/T2CH4_1 T2CH1ETR(1)_2/URX_3 /T2CH1ETR(1)_3/T1BKIN_3 |
| 2 | 12 | 9 | 6 | PC2 | I/O/FT | PC2 | SCL/URTS/T1BKIN | AETR_1/T2CH2_1 /T1ETR_3/URTS_1 /T1BKIN_2 |
| 3 | 13 | 10 | - | PC3 | I/O | PC3 | T1CH3 | T1CH1N_1/UCTS_1 /T1CH3_2/T1CH1N_3 |
| 4 | 14 | 11 | 7 | PC4 | I/O/A | PC4 | T1CH4/MCO/A2 | T1CH2N_1/T1CH4_2 /T1CH1_3 |
| - | 15 | 12 | - | PC5 | I/O/FT | PC5 | SCK/T1ETR | T2CH1ETR(1)_1/SCL_2 /SCL_3/UCK_3/T1ETR_1 /T1CH3_3/SCK_1 |
| 5 | 16 | 13 | - | PC6 | I/O/FT | PC6 | MOSI | T1CH1_1/UCTS_2/SDA_2 /SDA_3/UCTS_3/T1CH3N_3 /MOSI_1 |
| 6 | 17 | 14 | - | PC7 | I/O | PC7 | MISO | T1CH2_1/URTS_2 /T2CH2_3/URTS_3 /T1CH2_3/MISO_1 |
| 7 | 18 | 15 | 8 | PD1 | I/O/A | PD1 | SWIO/T1CH3N/AETR2 | SCL_1/URX_1/T1CH3N_1 /T1CH3N_2 |
| - | 19 | 16 | - | PD2 | I/O/A | PD2 | T1CH1/A3 | T2CH3_1/T1CH2N_3 /T1CH1_2 |
| - | 20 | 17 | - | PD3 | I/O/A | PD3 | A4/T2CH2/AETR/UCTS | T2CH2_2/T1CH4_1 |

*Note: 1. TIM2_CH1, TIM2_ETR;*

*2. The value after the underline of the remapping function indicates the configuration value of the corresponding bit in the AFIO register. For example: T1CH4_3 indicates that the corresponding bit of the AFIO register is configured as 11b;*

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*O = CMOS level tri-state output.*

*P = power supply.*

*FT = 5V tolerant.*

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## 2.3 Pin alternate functions

*Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.*

Table 2-2 Pin alternate and remapping functions

| Alternate / Pin | ADC | TIM1 | TIM2 | USART | SYS | I2C | SPI | SWIO | OPA |
|---|---|---|---|---|---|---|---|---|---|
| PA1 | A1 | T1CH2/T1CH2_2 | | | OSCI | | | | OPN0 |
| PA2 | A0/AETR2_1 | T1CH2N/T1CH2N_2 | | | OSCO | | | | OPP0 |
| PC0 | | T1CH3_1 | T2CH3/T2CH3_2 | UTX_3 | | | NSS_1 | | |
| PC1 | | T1BKIN_1/T1BKIN_3 | T2CH4_1/T2CH1ETR(1)_2 /T2CH1ETR(1)_3 | URX_3 | | SDA | NSS | | |
| PC2 | AETR_1 | T1BKIN/T1ETR_3 /T1BKIN_2 | T2CH2_1 | URTS/URTS_1 | | SCL | | | |
| PC3 | | T1CH3/T1CH1N_1 T1CH3_2/T1CH1N_3 | | UCTS_1 | | | | | |
| PC4 | A2 | T1CH4/T1CH2N_1 /T1CH4_2/T1CH1_3 | | | MCO | | | | |
| PC5 | | T1ETR/T1CH3_3 /T1ETR_1 | T2CH1ETR(1)_1 | UCK_3 | | SCL_2/SCL_3 | SCK/SCK_1 | | |
| PC6 | | T1CH1_1/T1CH3N_3 | | UCTS_2/UCTS_3 | | SDA_2/SDA_3 | MOSI/MOSI_1 | | |
| PC7 | | T1CH2_1/T1CH2_3 | T2CH2_3 | URTS_2/URTS_3 | | | MISO/MISO_1 | | |
| PD0 | | T1CH1N/T1CH1N_2 | | UTX_1 | | SDA_1 | | | OPN1 |
| PD1 | AETR2 | T1CH3N/T1CH3N_1 /T1CH3N_2 | | URX_1 | | SCL_1 | | SWIO | |
| PD2 | A3 | T1CH1/T1CH2N_3 /T1CH1_2 | T2CH3_1 | | | | | | |
| PD3 | A4/AETR | T1CH4_1 | T2CH2/T2CH2_2 | UCTS | | | | | |
| PD4 | A7 | T1ETR_2/T1CH4_3 | T2CH1ETR(1) | UCK | | | | | OPO |
| PD5 | A5 | | T2CH4_3 | UTX/URX_2 | | | | | |
| PD6 | A6 | | T2CH3_3 | URX/UTX_2 | | | | | |
| PD7 | | | T2CH4/T2CH4_2 | UCK_1/UCK_2 | NRST | | | | OPP1 |

*Note: TIM2_CH1、TIM2_ETR.*

## 2.3 Pin Alternate Functions

*Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.*

Table 2-2 Pin alternate and remapping functions

| Alternate / Pin | ADC | TIM1 | TIM2 | USART | SYS | I2C | SPI | SWIO | OPA |
|---|---|---|---|---|---|---|---|---|---|
| PA1 | A1 | T1CH2/T1CH2_2 | | | OSCI | | | | OPN0 |
| PA2 | A0/AETR2_1 | T1CH2N/T1CH2N_2 | | | OSCO | | | | OPP0 |
| PC0 | | T1CH3_1 | T2CH3/T2CH3_2 | UTX_3 | | | NSS_1 | | |
| PC1 | | T1BKIN_1/T1BKIN_3 | T2CH4_1/T2CH1ETR(1)_2 /T2CH1ETR(1)_3 | URX_3 | | SDA | NSS | | |
| PC2 | AETR_1 | T1BKIN/T1ETR_3 /T1BKIN_2 | T2CH2_1 | URTS/URTS_1 | | SCL | | | |
| PC3 | | T1CH3/T1CH1N_1 T1CH3_2/T1CH1N_3 | | UCTS_1 | | | | | |
| PC4 | A2 | T1CH4/T1CH2N_1 /T1CH4_2/T1CH1_3 | | | MCO | | | | |
| PC5 | | T1ETR/T1CH3_3 /T1ETR_1 | T2CH1ETR(1)_1 | UCK_3 | | SCL_2/SCL_3 | SCK/SCK_1 | | |
| PC6 | | T1CH1_1/T1CH3N_3 | | UCTS_2/UCTS_3 | | SDA_2/SDA_3 | MOSI/MOSI_1 | | |
| PC7 | | T1CH2_1/T1CH2_3 | T2CH2_3 | URTS_2/URTS_3 | | | MISO/MISO_1 | | |
| PD0 | | T1CH1N/T1CH1N_2 | | UTX_1 | | SDA_1 | | | OPN1 |
| PD1 | AETR2 | T1CH3N/T1CH3N_1 /T1CH3N_2 | | URX_1 | | SCL_1 | | SWIO | |
| PD2 | A3 | T1CH1/T1CH2N_3 /T1CH1_2 | T2CH3_1 | | | | | | |
| PD3 | A4/AETR | T1CH4_1 | T2CH2/T2CH2_2 | UCTS | | | | | |
| PD4 | A7 | T1ETR_2/T1CH4_3 | T2CH1ETR(1) | UCK | | | | | OPO |
| PD5 | A5 | | T2CH4_3 | UTX/URX_2 | | | | | |
| PD6 | A6 | | T2CH3_3 | URX/UTX_2 | | | | | |
| PD7 | | | T2CH4/T2CH4_2 | UCK_1/UCK_2 | NRST | | | | OPP1 |

*Note: TIM2_CH1、TIM2_ETR.*

# Chapter 3 Electrical Characteristics

## 3.1 Test conditions

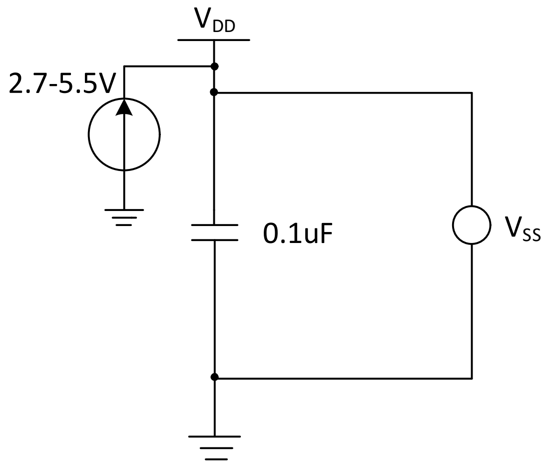
Unless otherwise specified and marked, all voltages are referenced to $V_{SS}$.

All minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency. Typical values are based on normal temperature (25°C) and $V_{DD}$ = 3.3V or 5V environment, which are given only as design guidelines.

The data based on comprehensive evaluation, design simulation or technology characteristics are not tested in production. On the basis of comprehensive evaluation, the minimum and maximum values refer to sample tests. Unless otherwise specified that is tested, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 3-1 Typical circuit for conventional power supply




## 3.2 Absolute maximum ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Table 3-1 Absolute maximum ratings

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_A$ | Ambient temperature during operation | -40 | 85 | °C |
| $T_S$ | Ambient temperature during storage | -40 | 125 | °C |
| $V_{DD}$-$V_{SS}$ | External main supply voltage ($V_{DD}$) | -0.3 | 5.5 | V |
| $V_{IN}$ | Input voltage on the FT (5V tolerant) pin | $V_{SS}$-0.3 | 5.5 | V |
| | Input voltage on other pins | $V_{SS}$-0.3 | $V_{DD}$+0.3 | |
| $\|\triangle V_{DD\_x}\|$ | Variations between different main power supply pins | | 50 | mV |
| $\|\triangle V_{SS\_x}\|$ | Variations between different ground pins | | 50 | mV |

# Chapter 3 Electrical Characteristics

## 3.1 Test Conditions

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All minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency. Typical values are based on normal temperature (25°C) and $V_{DD}$ = 3.3V or 5V environment, which are given only as design guidelines.

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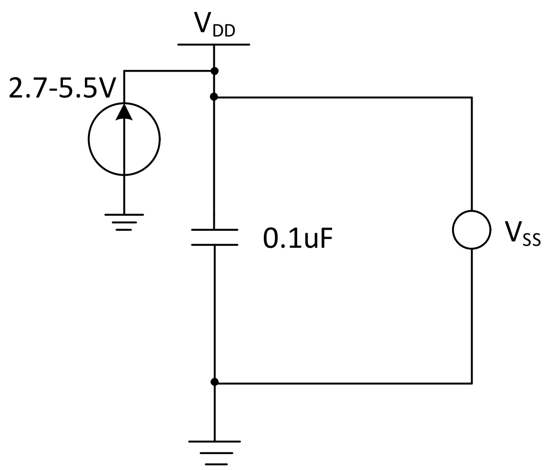



## 3.2 Absolute Maximum Ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Table 3-1 Absolute maximum ratings

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_A$ | Ambient temperature during operation | -40 | 85 | ℃ |
| $T_S$ | Ambient temperature during storage | -40 | 125 | ℃ |
| $V_{DD}$-$V_{SS}$ | External main supply voltage ($V_{DD}$) | -0.3 | 5.5 | V |
| $V_{IN}$ | Input voltage on the FT (5V tolerant) pin | $V_{SS}$-0.3 | 5.5 | V |
| | Input voltage on other pins | $V_{SS}$-0.3 | $V_{DD}$+0.3 | |
| $\|\triangle V_{DD\_x}\|$ | Variations between different main power supply pins | | 50 | mV |
| $\|\triangle V_{SS\_x}\|$ | Variations between different ground pins | | 50 | mV |

| | | | | |
|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model, non-contact) | 4K | | V |
| $I_{VDD}$ | Total current into $V_{DD}$ power lines (supply current) | | 100 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground lines (outflow current) | | 80 | |
| $I_{I/O}$ | Sink current on any I/O and control pin | | 20 | |
| | Output current on any I/O and control pin | | -20 | |
| $I_{INJ(PIN)}$ | OSC_IN pin of HSE | | +/-4 | |
| | Injected current on other pins | | +/-4 | |
| $\sum I_{INJ(PIN)}$ | Total injected current on all I/Os and control pins | | +/-20 | |

## 3.3 Electrical characteristics

### 3.3.1 Operating conditions

Table 3-2 General operating conditions

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $F_{HCLK}$ | Internal AHB clock frequency | | | 50 | MHz |
| $V_{DD}$ | Standard operating voltage | ADC not used | 2.7 | 5.5 | V |
| | | Use ADC (recommended) | 2.8 | 5.5 | |
| $T_A$ | Ambient temperature | | -40 | 85 | ℃ |
| $T_J$ | Junction temperature range | | -40 | 105 | ℃ |

Table 3-3 Power-on and power-down conditions

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | | 0 | ∞ | us/V |
| | $V_{DD}$ fall time rate | | 30 | ∞ | |

### 3.3.2 Embedded reset and power control block characteristics

Table 3-4 Reset and voltage monitor (For PDR, select high threshold gear)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$(1) | Programmable voltage detector level selection | PLS[2:0] = 000 (rising edge) | | 2.85 | | V |
| | | PLS[2:0] = 000 (falling edge) | | 2.7 | | V |
| | | PLS[2:0] = 001 (rising edge) | | 3.05 | | V |
| | | PLS[2:0] = 001 (falling edge) | | 2.9 | | V |
| | | PLS[2:0] = 010 (rising edge) | | 3.3 | | V |
| | | PLS[2:0] = 010 (falling edge) | | 3.15 | | V |
| | | PLS[2:0] = 011 (rising edge) | | 3.5 | | V |
| | | PLS[2:0] = 011 (falling edge) | | 3.3 | | V |
| | | PLS[2:0] = 100 (rising edge) | | 3.7 | | V |
| | | PLS[2:0] = 100 (falling edge) | | 3.5 | | V |
| | | PLS[2:0] = 101 (rising edge) | | 3.9 | | V |
| | | PLS[2:0] = 101 (falling edge) | | 3.7 | | V |
| | | PLS[2:0] = 110 (rising edge) | | 4.1 | | V |

| | | | | |
|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model, non-contact) | 4K | | V |
| $I_{VDD}$ | Total current into $V_{DD}$ power lines (supply current) | | 100 | mA |
| $I_{Vs}$ | Total current out of $V_{SS}$ ground lines (outflow current) | | 80 | |
| $I_{I/O}$ | Sink current on any I/O and control pin | | 20 | |
| | Output current on any I/O and control pin | | -20 | |
| $I_{INJ(PIN)}$ | OSC_IN pin of HSE | | +/-4 | |
| | Injected current on other pins | | +/-4 | |
| $\sum I_{INJ(PIN)}$ | Total injected current on all I/Os and control pins | | +/-20 | |

## 3.3 Electrical Characteristics

### 3.3.1 Operating Conditions

Table 3-2 General operating conditions

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $F_{HCLK}$ | Internal AHB clock frequency | | | 50 | MHz |
| $V_{DD}$ | Standard operating voltage | ADC not used | 2.7 | 5.5 | V |
| | | Use ADC (recommended) | 2.8 | 5.5 | |
| $T_A$ | Ambient temperature | | -40 | 85 | ℃ |
| $T_J$ | Junction temperature range | | -40 | 105 | ℃ |

Table 3-3 Power-on and power-down conditions

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | | 0 | ∞ | us/V |
| | $V_{DD}$ fall time rate | | 20 | ∞ | |

### 3.3.2 Built-in Reset and Power Control Block Characteristics

Table 3-4 Reset and voltage monitor (For PDR, select high threshold gear)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$(1) | Programmable voltage detector level selection | PLS[2:0] = 000 (rising edge) | | 2.85 | | V |
| | | PLS[2:0] = 000 (falling edge) | | 2.7 | | V |
| | | PLS[2:0] = 001 (rising edge) | | 3.05 | | V |
| | | PLS[2:0] = 001 (falling edge) | | 2.9 | | V |
| | | PLS[2:0] = 010 (rising edge) | | 3.3 | | V |
| | | PLS[2:0] = 010 (falling edge) | | 3.15 | | V |
| | | PLS[2:0] = 011 (rising edge) | | 3.5 | | V |
| | | PLS[2:0] = 011 (falling edge) | | 3.3 | | V |
| | | PLS[2:0] = 100 (rising edge) | | 3.7 | | V |
| | | PLS[2:0] = 100 (falling edge) | | 3.5 | | V |
| | | PLS[2:0] = 101 (rising edge) | | 3.9 | | V |
| | | PLS[2:0] = 101 (falling edge) | | 3.7 | | V |
| | | PLS[2:0] = 110 (rising edge) | | 4.1 | | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | PLS[2:0] = 110 (falling edge) | | 3.9 | | V |
| | | PLS[2:0] = 111 (rising edge) | | 4.4 | | V |
| | | PLS[2:0] = 111 (falling edge) | | 4.2 | | V |
| $V_{PVDhyst}$ | PVD hysteresis | | | 0.18 | | V |
| $V_{POR/PDR}$ | Power-on/power-down reset threshold | Rising edge | 2.32 | 2.5 | 2.68 | V |
| | | Falling edge | 2.3 | 2.48 | 2.66 | V |
| $V_{PDRhyst}$ | PDR hysteresis | | | 20 | | mV |
| $t_{RSTTEMPO}$ | Power on reset | | 12 | 17 | 22 | mS |
| | Other resets | | | 300 | | uS |

*Note: 1. Normal temperature test value.*

### 3.3.3 Embedded reference voltage

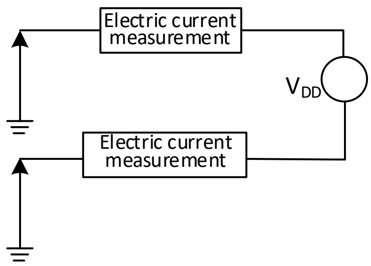
Table 3-5 Embedded reference voltage

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | $T_A$ = -40℃~85℃ | 1.17 | 1.2 | 1.23 | V |
| $T_{S\_vrefint}$ | ADC sampling time when reading the internal reference voltage | | 3 | | 500 | $1/f_{ADC}$ |

### 3.3.4 Supply current characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, the software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2 Current consumption measurement




The microcontroller is in the following conditions:

Normal temperature VDD = 3.3V or 5V case, when testing: all IO ports configured with pull-down inputs; HSI on when testing HSE, HSE off when testing HSI, HSE= 24M, HIS= 24M (calibrated); system clock source CLK*2 when FHCLK= 48MHz, 16MHz; clock on all peripherals only when turning on all peripherals. Enables or disables power consumption of all peripheral clocks.

| | | | | | | |
|---|---|---|---|---|---|---|
| | | PLS[2:0] = 110 (falling edge) | | 3.9 | | V |
| | | PLS[2:0] = 111 (rising edge) | | 4.4 | | V |
| | | PLS[2:0] = 111 (falling edge) | | 4.2 | | V |
| $V_{PVDhyst}$ | PVD hysteresis | | | 0.18 | | V |
| $V_{POR/PDR}$ | Power-on/power-down reset threshold | Rising edge | 2.32 | 2.5 | 2.68 | V |
| | | Falling edge | 2.3 | 2.48 | 2.66 | V |
| $V_{PDRhyst}$ | PDR hysteresis | | | 20 | | mV |
| $t_{RSTTEMPO}$ | Power on reset | | 1 | 1.5(2) | 21 | mS |
| | Other resets | | | 300 | | uS |

*Note: 1. Normal temperature test value.*

*2. The user configuration bit RST_MODE can increase the power-on reset delay.*

### 3.3.3 Embedded Reference Voltage

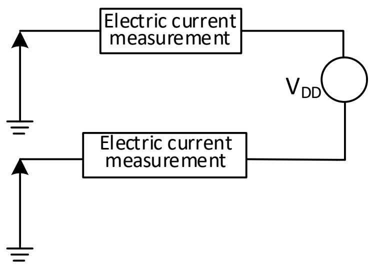
Table 3-5 Embedded reference voltage

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | $T_A$ = -40℃~85℃ | 1.17 | 1.2 | 1.23 | V |
| $T_{S\_vrefint}$ | ADC sampling time when reading the internal reference voltage | | 3 | | 500 | $1/f_{ADC}$ |

### 3.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, the software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2 Current consumption measurement




The microcontroller is in the following conditions:

Normal temperature VDD = 3.3V or 5V case, when testing: all IO ports configured with pull-down inputs; HSI on when testing HSE, HSE off when testing HSI, HSE= 24M, HSI= 24M (calibrated); system clock source CLK*2 when FHCLK= 48MHz, 16MHz; clock on all peripherals only when turning on all peripherals. Enables or disables power consumption of all peripheral clocks.

Table 3-6-1 Typical current consumption in Run mode, data processing code runs from the internal Flash ($V_{DD}$ = 3.3V)

| Symbol | Parameter | Condition | | Typ. | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled | All peripherals disabled | |
| $I_{DD}$(1) | Supply current in Run mode | External clock | $F_{HCLK}$ = 48MHz | 7.0 | 4.6 | mA |
| | | | $F_{HCLK}$ = 24MHz | 5.2 | 4.2 | |
| | | | $F_{HCLK}$ = 16MHz | 4.6 | 3.8 | |
| | | | $F_{HCLK}$ = 8MHz | 3.1 | 2.7 | |
| | | | $F_{HCLK}$ = 750KHz | 1.8 | 1.8 | |
| | | Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency. | $F_{HCLK}$ = 48MHz | 6.3 | 3.9 | |
| | | | $F_{HCLK}$ = 24MHz | 4.3 | 3.1 | |
| | | | $F_{HCLK}$ = 16MHz | 3.9 | 3.1 | |
| | | | $F_{HCLK}$ = 8MHz | 2.3 | 1.9 | |
| | | | $F_{HCLK}$ = 750KHz | 1.1 | 1.0 | |

*Note: 1. The above are measured parameters.*

*2. When VDD < 3V, the current power consumption will increase.*

Table 3-6-2 Typical current consumption in Run mode, data processing code runs from the internal Flash ($V_{DD}$ = 5V)

| Symbol | Parameter | Condition | | Typ. | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled | All peripherals disabled | |
| $I_{DD}$(1) | Supply current in Run mode | External clock | $F_{HCLK}$ = 48MHz | 8.0 | 5.6 | mA |
| | | | $F_{HCLK}$ = 24MHz | 6.4 | 5.6 | |
| | | | $F_{HCLK}$ = 16MHz | 5.8 | 5.0 | |
| | | | $F_{HCLK}$ = 8MHz | 3.8 | 3.4 | |
| | | | $F_{HCLK}$ = 750KHz | 2.2 | 2.1 | |
| | | Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency. | $F_{HCLK}$ = 48MHz | 7.3 | 4.9 | |
| | | | $F_{HCLK}$ = 24MHz | 5.3 | 4.1 | |
| | | | $F_{HCLK}$ = 16MHz | 5.0 | 4.3 | |
| | | | $F_{HCLK}$ = 8MHz | 3.1 | 2.7 | |
| | | | $F_{HCLK}$ = 750KHz | 1.4 | 1.4 | |

*Note: 1. The above are measured parameters.*

Table 3-7-1 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM ($V_{DD}$ = 3.3V)

| Symbol | Parameter | Condition | | Typ. | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled | All peripherals disabled | |
| $I_{DD}$(1) | Supply | External clock | $F_{HCLK}$ = 48MHz | 4.9 | 2.5 | mA |

Table 3-6-1 Typical current consumption in Run mode, data processing code runs from the internal Flash ($V_{DD}$ = 3.3V)

| Symbol | Parameter | Condition | | Typ. All peripherals enabled | Typ. All peripherals disabled | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$(1) | Supply current in Run mode | External clock | $F_{HCLK}$ = 48MHz | 7.4 | 5.2 | mA |
| | | | $F_{HCLK}$ = 24MHz | 5.6 | 4.5 | |
| | | | $F_{HCLK}$ = 16MHz | 4.7 | 3.9 | |
| | | | $F_{HCLK}$ = 8MHz | 3.0 | 2.6 | |
| | | | $F_{HCLK}$ = 750KHz | 1.7 | 1.7 | |
| | | Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency. | $F_{HCLK}$ = 48MHz | 6.4 | 4.0 | |
| | | | $F_{HCLK}$ = 24MHz | 4.6 | 3.5 | |
| | | | $F_{HCLK}$ = 16MHz | 4.0 | 3.3 | |
| | | | $F_{HCLK}$ = 8MHz | 2.4 | 2.0 | |
| | | | $F_{HCLK}$ = 750KHz | 1.1 | 1.1 | |

*Note: 1. The above are measured parameters.*
*2. When VDD < 3V, the current power consumption will increase.*

Table 3-6-2 Typical current consumption in Run mode, data processing code runs from the internal Flash ($V_{DD}$ = 5V)

| Symbol | Parameter | Condition | | Typ. All peripherals enabled | Typ. All peripherals disabled | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$(1) | Supply current in Run mode | External clock | $F_{HCLK}$ = 48MHz | 9.0 | 6.8 | mA |
| | | | $F_{HCLK}$ = 24MHz | 7.1 | 6.0 | |
| | | | $F_{HCLK}$ = 16MHz | 5.9 | 5.1 | |
| | | | $F_{HCLK}$ = 8MHz | 3.7 | 3.3 | |
| | | | $F_{HCLK}$ = 750KHz | 2.1 | 2.0 | |
| | | Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency. | $F_{HCLK}$ = 48MHz | 7.4 | 5.1 | |
| | | | $F_{HCLK}$ = 24MHz | 5.7 | 4.6 | |
| | | | $F_{HCLK}$ = 16MHz | 5.2 | 4.4 | |
| | | | $F_{HCLK}$ = 8MHz | 3.2 | 2.8 | |
| | | | $F_{HCLK}$ = 750KHz | 1.5 | 1.4 | |

*Note: 1. The above are measured parameters.*

Table 3-7-1 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM ($V_{DD}$ = 3.3V)

| Symbol | Parameter | Condition | | Typ. All peripherals enabled | Typ. All peripherals disabled | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$(1) | Supply | External clock | $F_{HCLK}$ = 48MHz | 4.7 | 2.4 | mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| | current in Sleep mode (In this case, peripheral power supply and clock are maintained) | | $F_{HCLK}$ = 24MHz | 2.9 | 1.7 | |
| | | | $F_{HCLK}$ = 16MHz | 2.5 | 1.7 | |
| | | | $F_{HCLK}$ = 8MHz | 1.7 | 1.3 | |
| | | | $F_{HCLK}$ = 750KHz | 1.2 | 1.1 | |
| | | Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency. | $F_{HCLK}$ = 48MHz | 4.2 | 1.8 | |
| | | | $F_{HCLK}$ = 24MHz | 2.2 | 1.0 | |
| | | | $F_{HCLK}$ = 16MHz | 1.8 | 1.0 | |
| | | | $F_{HCLK}$ = 8MHz | 1.0 | 0.6 | |
| | | | $F_{HCLK}$ = 750KHz | 0.4 | 0.4 | |

*Note: 1. The above are measured parameters.*

Table 3-7-2 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM ($V_{DD}$ = 5V)

| Symbol | Parameter | Condition | | Typ. | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled | All peripherals disabled | |
| $I_{DD}$(1) | Supply current in Sleep mode (In this case, peripheral power supply and clock are maintained) | External clock | $F_{HCLK}$ = 48MHz | 4.9 | 2.5 | mA |
| | | | $F_{HCLK}$ = 24MHz | 2.9 | 1.7 | |
| | | | $F_{HCLK}$ = 16MHz | 2.5 | 1.7 | |
| | | | $F_{HCLK}$ = 8MHz | 1.7 | 1.3 | |
| | | | $F_{HCLK}$ = 750KHz | 1.2 | 1.1 | |
| | | Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency. | $F_{HCLK}$ = 48MHz | 4.2 | 1.8 | |
| | | | $F_{HCLK}$ = 24MHz | 2.2 | 1.0 | |
| | | | $F_{HCLK}$ = 16MHz | 1.8 | 1.0 | |
| | | | $F_{HCLK}$ = 8MHz | 1.0 | 0.6 | |
| | | | $F_{HCLK}$ = 750KHz | 0.4 | 0.4 | |

*Note: 1. The above are measured parameters.*

Table 3-8 Typical current consumption in Standby mode

| Symbol | Parameter | Condition | | Typ. | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Standby mode | LSI on | $V_{DD}$ = 3.3V | 10.5 | uA |
| | | | $V_{DD}$ = 5V | 11.1 | |
| | | LSI off | $V_{DD}$ = 3.3V | 9.0 | |
| | | | $V_{DD}$ = 5V | 9.6 | |

*Note: The above are measured parameters.*

### 3.3.5 External clock source characteristics

Table 3-9 From external high-speed clock

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{HSE\_ext}$ | External clock frequency | | 4 | 24 | 25 | MHz |
| $V_{HSEH}$(1) | OSC_IN input pin high level | | $0.8V_{DD}$ | | $V_{DD}$ | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | current in Sleep mode (In this case, peripheral power supply and clock are maintained) | | $F_{HCLK}$ = 24MHz | 2.8 | 1.7 | |
| | | | $F_{HCLK}$ = 16MHz | 2.5 | 1.7 | |
| | | | $F_{HCLK}$ = 8MHz | 1.7 | 1.3 | |
| | | | $F_{HCLK}$ = 750KHz | 1.2 | 1.1 | |
| | | Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency. | $F_{HCLK}$ = 48MHz | 4.1 | 1.7 | |
| | | | $F_{HCLK}$ = 24MHz | 2.1 | 1.0 | |
| | | | $F_{HCLK}$ = 16MHz | 1.8 | 1.0 | |
| | | | $F_{HCLK}$ = 8MHz | 1.0 | 0.6 | |
| | | | $F_{HCLK}$ = 750KHz | 0.5 | 0.4 | |

*Note: 1. The above are measured parameters.*

Table 3-7-2 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM ($V_{DD}$ = 5V)

| Symbol | Parameter | Condition | | Typ. | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled | All peripherals disabled | |
| $I_{DD}$(1) | Supply current in Sleep mode (In this case, peripheral power supply and clock are maintained) | External clock | $F_{HCLK}$ = 48MHz | 4.7 | 2.4 | mA |
| | | | $F_{HCLK}$ = 24MHz | 2.8 | 1.7 | |
| | | | $F_{HCLK}$ = 16MHz | 2.5 | 1.7 | |
| | | | $F_{HCLK}$ = 8MHz | 1.7 | 1.3 | |
| | | | $F_{HCLK}$ = 750KHz | 1.2 | 1.1 | |
| | | Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency. | $F_{HCLK}$ = 48MHz | 4.1 | 1.7 | |
| | | | $F_{HCLK}$ = 24MHz | 2.1 | 1.0 | |
| | | | $F_{HCLK}$ = 16MHz | 1.8 | 1.0 | |
| | | | $F_{HCLK}$ = 8MHz | 0.1 | 0.6 | |
| | | | $F_{HCLK}$ = 750KHz | 0.5 | 0.4 | |

*Note: 1. The above are measured parameters.*

Table 3-8 Typical current consumption in Standby mode

| Symbol | Parameter | Condition | | Typ. | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Standby mode | LSI on | $V_{DD}$ = 3.3V | 9.1 | uA |
| | | | $V_{DD}$ = 5V | 9.4 | |
| | | LSI off | $V_{DD}$ = 3.3V | 7.6 | |
| | | | $V_{DD}$ = 5V | 8.0 | |

*Note: 1. The above are measured parameters.*

*2. The test conditions are: at room temperature VDD = 3.3V or 5V, test the initial master frequency HSI = 24M, all IO ports are configured with pull-down inputs.*

### 3.3.5 External Clock Source Characteristics

Table 3-9 From external high-speed clock

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|

| | | | | | | |
|---|---|---|---|---|---|---|
| | voltage | | | | | |
| $V_{HSEL}$(1) | OSC_IN input pin low-level voltage | | 0 | | $0.2V_{DD}$ | V |
| $C_{in(HSE)}$ | OSC_IN input capacitance | | | 5 | | pF |
| $DuCy_{(HSE)}$ | Duty cycle | | 40 | 50 | 60 | % |
| $I_L$ | OSC_IN input leakage current | | | | ±1 | uA |

*Note: 1. Failure to meet this condition may cause level recognition error.*

Figure 3-3 External high-frequency clock source circuit

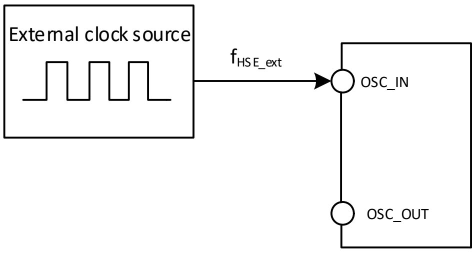



Table 3-10 High-speed external clock generated from a crystal/ceramic resonator

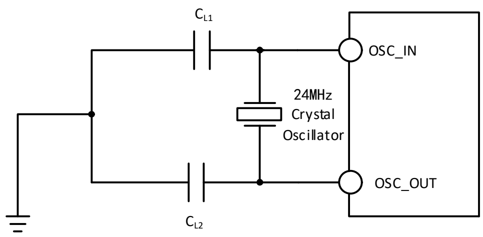
| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{OSC\_IN}$ | Resonator frequency | | 4 | 24 | 25 | MHz |
| $R_F$ | Feedback resistance | | | 250 | | kΩ |
| C | Recommended load capacitance and corresponding crystal series impedance $R_S$ | $R_S = 60\Omega$(1) | | 20 | | pF |
| $I_2$ | HSE drive current | $V_{DD} = 3.3V$, 20p load | | 0.32 | | mA |
| $g_m$ | Oscillator transconductance | Startup | | 6.8 | | mA/V |
| $t_{SU(HSE)}$ | Startup time | $V_{DD}$ is stable, 24M crystal | | 2 | | ms |

*Note 1: It is recommended that the ESR of 25M crystal should not exceed 60 Ω, and it can be relaxed if it is lower than 25M.*

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, generally $C_{L1} = C_{L2}$.

Figure 3-4 Typical circuit of external 24M crystal



| | | | | | | |
|---|---|---|---|---|---|---|
| $F_{HSE\_ext}$ | External clock frequency | | 4 | 24 | 25 | MHz |
| $V_{HSEH}$(1) | OSC_IN input pin high level voltage | | $0.8V_{DD}$ | | $V_{DD}$ | V |
| $V_{HSEL}$(1) | OSC_IN input pin low-level voltage | | 0 | | $0.2V_{DD}$ | V |
| $C_{in(HSE)}$ | OSC_IN input capacitance | | | 5 | | pF |
| $DuCy_{(HSE)}$ | Duty cycle | | 40 | 50 | 60 | % |
| $I_L$ | OSC_IN input leakage current | | | | ±1 | uA |

*Note: 1. Failure to meet this condition may cause level recognition error.*

Figure 3-3 External high-frequency clock source circuit

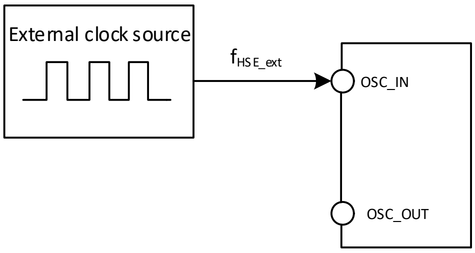



Table 3-10 High-speed external clock generated from a crystal/ceramic resonator

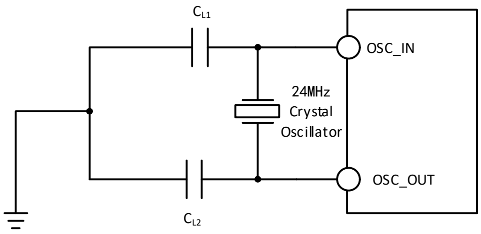
| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{OSC\_IN}$ | Resonator frequency | | 4 | 24 | 25 | MHz |
| $R_F$ | Feedback resistance | | | 250 | | kΩ |
| C | Recommended load capacitance and corresponding crystal series impedance $R_S$ | $R_S = 60\Omega$(1) | | 20 | | pF |
| $I_2$ | HSE drive current | $V_{DD} = 3.3V$, 20p load | | 0.32 | | mA |
| $g_m$ | Oscillator transconductance | Startup | | 6.8 | | mA/V |
| $t_{SU(HSE)}$ | Startup time | $V_{DD}$ is stable, 24M crystal | | 2 | | ms |

*Note 1: It is recommended that the ESR of 25M crystal should not exceed 60 Ω, and it can be relaxed if it is lower than 25M.*

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, generally $C_{L1} = C_{L2}$.

Figure 3-4 Typical circuit of external 24M crystal



### 3.3.6 Internal clock source characteristics

Table 3-11 Internal high-speed (HSI) RC oscillator characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{HSI}$ | Frequency (after calibration) | | | 24 | | MHz |
| $DuCy_{HSI}$ | Duty cycle | | 45 | 50 | 55 | % |
| $ACC_{HSI}$ | Accuracy of HSI oscillator (after calibration) | TA = 0°C～70°C | -1.2 | | 1.6 | % |
| | | TA = -40°C～85°C | -2.2 | | 2.2 | % |
| $t_{SU(HSI)}$ | HSI oscillator startup stabilization time | | | 10 | | us |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | 120 | 180 | 270 | uA |

Table 3-12 Internal low-speed (LSI) RC oscillator characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{LSI}$ | Frequency | | 100 | 128 | 150 | KHz |
| $DuCy_{LSI}$ | Duty cycle | | 45 | 50 | 55 | % |
| $t_{SU(LSI)}$ | LSI oscillator startup stabilization time | | | 80 | | us |
| $I_{DD(LSI)}$ | LSI oscillator power consumption | | | 1.5 | | uA |

### 3.3.7 Wakeup time from low-power mode

Table 3-13 Wakeup time from low-power mode(1)

| Symbol | Parameter | Condition | Typ. | Unit |
|---|---|---|---|---|
| $t_{wusleep}$ | Wakeup from Sleep mode | Wake up using HSI RC clock | 30 | us |
| $t_{WUSTDBY}$ | Wakeup from Standby mode | LDO stabilization time + HSI RC clock wake up + code load time(2) (take 128K as example) | 200 | us |

*Note: The above parameters are measured parameters.*

### 3.3.8 Memory characteristics

Table 3-14 Flash memory characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{ERASE\_64}$ | Page (64 bytes) programming time | $T_A$ = -20°C～85°C | 2.4 | | 3.1 | ms |
| $t_{ERASE}$ | Page (64 bytes) erase time | $T_A$ = -20°C～85°C | 2.4 | | 3.1 | ms |
| $t_{prog}$ | 16-bit programming time | $T_A$ = -20°C～85°C | 2.4 | | 3.1 | ms |
| $t_{ME}$ | Whole chip erase time | $T_A$ = -20°C～85°C | 2.4 | | 3.1 | ms |
| $V_{prog}$ | Programming voltage | | 2.8 | | 5.5 | V |

Table 3-15 Flash memory endurance and data retention

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $N_{END}$ | Endurance | $T_A$ = 25°C | 10K | 80K(1) | | times |

### 3.3.6 Internal Clock Source Characteristics

Table 3-11 Internal high-speed (HSI) RC oscillator characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{HSI}$ | Frequency (after calibration) | | | 24 | | MHz |
| $DuCy_{HSI}$ | Duty cycle | | 45 | 50 | 55 | % |
| $ACC_{HSI}$ | Accuracy of HSI oscillator (after calibration) | TA = 0°C～70°C | -1.2 | | 1.6 | % |
| | | TA = -40°C～85°C | -2.2 | | 2.2 | % |
| $t_{SU(HSI)}$ | HSI oscillator startup stabilization time | | | 10 | | us |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | 120 | 180 | 270 | uA |

Table 3-12 Internal low-speed (LSI) RC oscillator characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{LSI}$ | Frequency | | 100 | 128 | 150 | KHz |
| $DuCy_{LSI}$ | Duty cycle | | 45 | 50 | 55 | % |
| $t_{SU(LSI)}$ | LSI oscillator startup stabilization time | | | 80 | | us |
| $I_{DD(LSI)}$ | LSI oscillator power consumption | | | 1.5 | | uA |

### 3.3.7 Wakeup Time from Low-power Mode

Table 3-13 Wakeup time from low-power mode(1)

| Symbol | Parameter | Condition | Typ. | Unit |
|---|---|---|---|---|
| $t_{wusleep}$ | Wakeup from Sleep mode | Wake up using HSI RC clock | 30 | us |
| $t_{WUSTDBY}$ | Wakeup from Standby mode | LDO stabilization time + HSI RC clock wake up + code load time(2) (take 128K as example) | 200 | us |

*Note: The above parameters are measured parameters.*

### 3.3.8 Memory Characteristics

Table 3-14 Flash memory characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{ERASE\_64}$ | Page (64 bytes) programming time | $T_A$ = -20°C~85°C | 2.4 | | 3.1 | ms |
| $t_{ERASE}$ | Page (64 bytes) erase time | $T_A$ = -20°C~85°C | 2.4 | | 3.1 | ms |
| $t_{prog}$ | 16-bit programming time | $T_A$ = -20°C~85°C | 2.4 | | 3.1 | ms |
| $t_{ME}$ | Whole chip erase time | $T_A$ = -20°C~85°C | 2.4 | | 3.1 | ms |
| $V_{prog}$ | Programming voltage | | 2.8 | | 5.5 | V |

Table 3-15 Flash memory endurance and data retention

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $N_{END}$ | Endurance | $T_A$ = 25°C | 10K | 80K(1) | | times |
| $t_{RET}$ | Data retention | | 10 | | | year |

| | | | | | | |
|---|---|---|---|---|---|---|
| $t_{RET}$ | Data retention | | 10 | | | year |

*Note: The endurance parameter is actual measured, which is not guaranteed.*

### 3.3.9 I/O port characteristics

Table 3-16 General-purpose I/O static characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Standard I/O pin, input high level voltage | | 0.22*($V_{DD}$-2.7)+1.55 | | $V_{DD}$+0.3 | V |
| | FT I/O pin, input high level voltage | | 0.22*($V_{DD}$-2.7)+1.55 | | 5.5 | V |
| $V_{IL}$ | Standard I/O pin, input low-level voltage | | -0.3 | | 0.19*($V_{DD}$-2.7)+0.65 | V |
| | FT I/O pin, input low-level voltage | | -0.3 | | 0.19*($V_{DD}$-2.7)+0.65 | V |
| $V_{hys}$ | Schmitt trigger voltage hysteresis | | 150 | | | mV |
| $I_{lkg}$ | Input leakage current | Standard I/O port | | | 1 | uA |
| | | FT I/O port | | | 3 | |
| $R_{PU}$ | Weak pull-up equivalent resistance | | 35 | 45 | 55 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistance | | 35 | 45 | 55 | kΩ |
| $C_{I/O}$ | I/O pin capacitance | | | 5 | | pF |

Output drive current characteristics

GPIO (General-Purpose Input/Output Port) can sink or output up to ±8mA current, and sink or output ±20mA current (not strictly to $V_{OL}$/$V_{OH}$). In user applications, the total driving current of all I/O pins cannot exceed the absolute maximum ratings given in Section 3.2:

Table 3-17 Output voltage characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level when 8 pins are sunk | TTL port, $I_{I/O}$ = +8mA | | 0.4 | V |
| $V_{OH}$ | Output high level when 8 pins are sourced | 2.7V< $V_{DD}$ <5.5V | $V_{DD}$-0.4 | | |
| $V_{OL}$ | Output low level when 8 pins are sunk | CMOS port, $I_{I/O}$ = +8mA | | 0.4 | V |
| $V_{OH}$ | Output high level when 8 pins are sourced | 2.7V< $V_{DD}$ <5.5V | 2.3 | | |
| $V_{OL}$ | Output low level when 8 pins are sunk | $I_{I/O}$ = +20mA | | 1.3 | V |
| $V_{OH}$ | Output high level when 8 pins are sourced | 2.7V< $V_{DD}$ <5.5V | $V_{DD}$-1.3 | | |

*Note: In the above conditions, if multiple I/O pins are driven at the same time, the total current cannot exceed the absolute maximum ratings given in Table 3.2. In addition, when multiple I/O pins are driven at the same time, the current on the power/ground point is very large, which will cause the voltage drop to make the internal I/O voltage not reach the power supply voltage in the table, resulting in the drive current being less than the nominal value.*

*Note: The endurance parameter is actual measured, which is not guaranteed.*

### 3.3.9 I/O Port Characteristics

Table 3-16 General-purpose I/O static characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Standard I/O pin, input high level voltage | | 0.22*($V_{DD}$-2.7)+1.55 | | $V_{DD}$+0.3 | V |
| | FT I/O pin, input high level voltage | | 0.22*($V_{DD}$-2.7)+1.55 | | 5.5 | V |
| $V_{IL}$ | Standard I/O pin, input low-level voltage | | -0.3 | | 0.19*($V_{DD}$-2.7)+0.65 | V |
| | FT I/O pin, input low-level voltage | | -0.3 | | 0.19*($V_{DD}$-2.7)+0.65 | V |
| $V_{hys}$ | Schmitt trigger voltage hysteresis | | 150 | | | mV |
| $I_{lkg}$ | Input leakage current | Standard I/O port | | | 1 | uA |
| | | FT I/O port | | | 3 | |
| $R_{PU}$ | Weak pull-up equivalent resistance | | 35 | 45 | 55 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistance | | 35 | 45 | 55 | kΩ |
| $C_{I/O}$ | I/O pin capacitance | | | 5 | | pF |

Output drive current characteristics

GPIO (General-Purpose Input/Output Port) can sink or output up to ±8mA current, and sink or output ±20mA current (not strictly to $V_{OL}/V_{OH}$). In user applications, the total driving current of all I/O pins cannot exceed the absolute maximum ratings given in Section 3.2:

Table 3-17 Output voltage characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level when 8 pins are sunk | TTL port, $I_{I/O}$ = +8mA<br>2.7V< $V_{DD}$ <5.5V | | 0.4 | V |
| $V_{OH}$ | Output high level when 8 pins are sourced | | $V_{DD}$-0.4 | | |
| $V_{OL}$ | Output low level when 8 pins are sunk | CMOS port, $I_{I/O}$ = +8mA<br>2.7V< $V_{DD}$ <5.5V | | 0.4 | V |
| $V_{OH}$ | Output high level when 8 pins are sourced | | 2.3 | | |
| $V_{OL}$ | Output low level when 8 pins are sunk | $I_{I/O}$ = +20mA<br>2.7V< $V_{DD}$ <5.5V | | 1.3 | V |
| $V_{OH}$ | Output high level when 8 pins are sourced | | $V_{DD}$-1.3 | | |

*Note: In the above conditions, if multiple I/O pins are driven at the same time, the total current cannot exceed the absolute maximum ratings given in Table 3.2. In addition, when multiple I/O pins are driven at the same time, the current on the power/ground point is very large, which will cause the voltage drop to make the internal I/O voltage not reach the power supply voltage in the table, resulting in the drive current being less than the nominal value.*

Table 3-18 Input/output AC characteristics

| MODEx[1:0] configuration | Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| 10 (2MHz) | $F_{max(I/O)out}$ | Maximum frequency | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 2 | MHz |
| | $t_{f(I/O)out}$ | Output high to low fall time | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 125 | ns |
| | $t_{r(I/O)out}$ | Output low to high rise time | | | 125 | ns |
| 01 (10MHz) | $F_{max(I/O)out}$ | Maximum frequency | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 10 | MHz |
| | $t_{f(I/O)out}$ | Output high to low fall time | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 25 | ns |
| | $t_{r(I/O)out}$ | Output low to high rise time | | | 25 | ns |
| 11 (30MHz) | $F_{max(I/O)out}$ | Maximum frequency | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 30 | MHz |
| | $t_{f(I/O)out}$ | Output high to low fall time | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 10 | ns |
| | $t_{r(I/O)out}$ | Output low to high rise time | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 10 | ns |
| | $t_{EXTIpw}$ | The EXTI controller detects the pulse width of the external signal | | 10 | | ns |

### 3.3.10 NRST pin characteristics

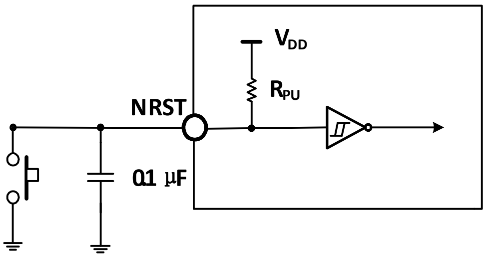
Table 3-19 External reset pin characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST input low-level voltage | | -0.3 | | $0.28*(V_{DD}-1.8)+0.6$ | V |
| $V_{IH(NRST)}$ | NRST input high-level voltage | | $0.41*(V_{DD}-1.8)+1.3$ | | $V_{DD}+0.3$ | V |
| $V_{hys(NRST)}$ | NRST Schmitt Trigger voltage hysteresis | | 150 | | | mV |
| $R_{PU}$(1) | Weak pull-up equivalent resistance | | 35 | 45 | 55 | kΩ |

*Note: 1. The pull-up resistor is a real resistor in series with a switchable PMOS implementation. The resistance of this PMOS/NMOS switch is very small (approximately 10%).*

Circuit reference design and requirements:

Figure 3-5 Typical circuit of external reset pin




### 3.3.11 TIM timer characteristics

Table 3-20 TIMx characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|

Table 3-18 Input/output AC characteristics

| MODEx[1:0] configuration | Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| 10 (2MHz) | $F_{max(I/O)out}$ | Maximum frequency | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 2 | MHz |
| | $t_{f(I/O)out}$ | Output high to low fall time | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 125 | ns |
| | $t_{r(I/O)out}$ | Output low to high rise time | | | 125 | ns |
| 01 (10MHz) | $F_{max(I/O)out}$ | Maximum frequency | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 10 | MHz |
| | $t_{f(I/O)out}$ | Output high to low fall time | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 25 | ns |
| | $t_{r(I/O)out}$ | Output low to high rise time | | | 25 | ns |
| 11 (30MHz) | $F_{max(I/O)out}$ | Maximum frequency | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 30 | MHz |
| | $t_{f(I/O)out}$ | Output high to low fall time | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 10 | ns |
| | $t_{r(I/O)out}$ | Output low to high rise time | CL = 50pF, $V_{DD}$ = 2.7-5.5V | | 10 | ns |
| | $t_{EXTIpw}$ | The EXTI controller detects the pulse width of the external signal | | 10 | | ns |

### 3.3.10 NRST Pin Characteristics

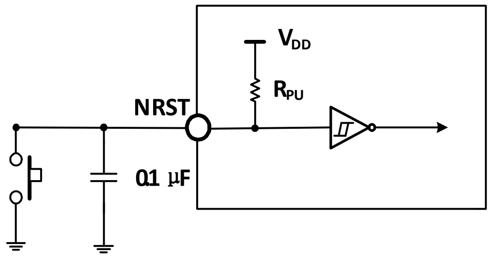
Table 3-19 External reset pin characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST input low-level voltage | | -0.3 | | 0.28*($V_{DD}$-1.8)+0.6 | V |
| $V_{IH(NRST)}$ | NRST input high-level voltage | | 0.41*($V_{DD}$-1.8)+1.3 | | $V_{DD}$+0.3 | V |
| $V_{hys(NRST)}$ | NRST Schmitt Trigger voltage hysteresis | | 150 | | | mV |
| $R_{PU}$(1) | Weak pull-up equivalent resistance | | 35 | 45 | 55 | kΩ |

*Note: 1. The pull-up resistor is a real resistor in series with a switchable PMOS implementation. The resistance of this PMOS/NMOS switch is very small (approximately 10%).*

Circuit reference design and requirements:

Figure 3-5 Typical circuit of external reset pin




### 3.3.11 TIM Timer Characteristics

Table 3-20 TIMx characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer reference clock | | 1 | | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 48MHz | 13.9 | | ns |
| $F_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 48MHz | 0 | 36 | MHz |
| $R_{esTIM}$ | Timer resolution | | | 16 | 位 |
| $t_{COUNTER}$ | 16-bit counter clock cycle when the internal clock is selected | | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 48MHz | 0.0139 | 910 | us |
| $t_{MAX\_COUNT}$ | Maximum possible count | | | 65535 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 48MHz | | 59.6 | s |

### 3.3.12 I2C interface characteristics

Figure 3-6 I2C bus timing diagram

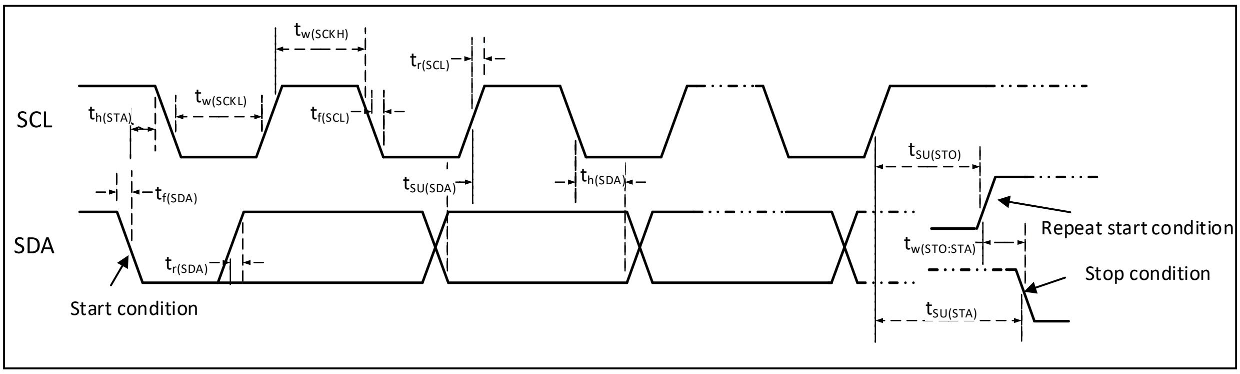



Table 3-21 I2C interface characteristics

| Symbol | Parameter | Standard I2C | | Fast I2C | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{w(SCKL)}$ | SCL clock low time | 4.7 | | 1.2 | | us |
| $t_{w(SCKH)}$ | SCL clock high time | 4.0 | | 0.6 | | us |
| $t_{SU(SDA)}$ | SDA data setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | | 0 | 900 | ns |
| $t_{r(SDA)}/t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | 20 | | ns |
| $t_{f(SDA)}/t_{f(SCL)}$ | SDA and SCL fall time | | 300 | | | ns |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | | 0.6 | | us |
| $t_{SU(STA)}$ | Repeated start condition setup time | 4.7 | | 0.6 | | us |
| $t_{SU(STO)}$ | Stop condition setup time | 4.0 | | 0.6 | | us |
| $t_{w(STO:STA)}$ | Time from stop condition to start condition (bus free) | 4.7 | | 1.2 | | us |
| $C_b$ | Capacitive load for each bus | | 400 | | 400 | pF |

| | | | | | |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer reference clock | | 1 | | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 48MHz | 20.8 | | ns |
| $F_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 48MHz | 0 | 24 | MHz |
| $R_{esTIM}$ | Timer resolution | | | 16 | bit |
| $t_{COUNTER}$ | 16-bit counter clock cycle when the internal clock is selected | | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 48MHz | 0.0208 | 1363 | us |
| $t_{MAX\_COUNT}$ | Maximum possible count | | | 65535 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 48MHz | | 1363 | s |

### 3.3.12 I2C Interface Characteristics

Figure 3-6 I2C bus timing diagram

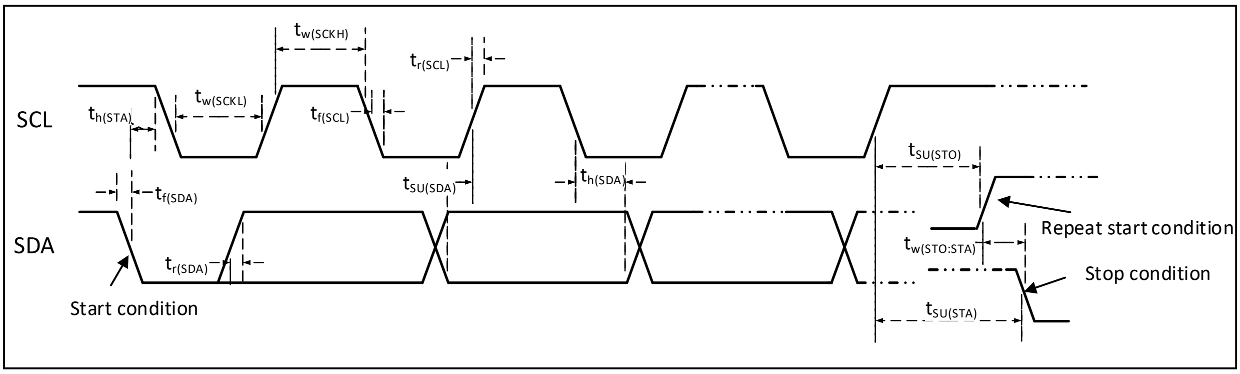



Table 3-21 I2C interface characteristics

| Symbol | Parameter | Standard I2C | | Fast I2C | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{w(SCKL)}$ | SCL clock low time | 4.7 | | 1.2 | | us |
| $t_{w(SCKH)}$ | SCL clock high time | 4.0 | | 0.6 | | us |
| $t_{SU(SDA)}$ | SDA data setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | | 0 | 900 | ns |
| $t_{r(SDA)}/t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | 20 | | ns |
| $t_{f(SDA)}/t_{f(SCL)}$ | SDA and SCL fall time | | 300 | | | ns |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | | 0.6 | | us |
| $t_{SU(STA)}$ | Repeated start condition setup time | 4.7 | | 0.6 | | us |
| $t_{SU(STO)}$ | Stop condition setup time | 4.0 | | 0.6 | | us |
| $t_{w(STO:STA)}$ | Time from stop condition to start condition (bus free) | 4.7 | | 1.2 | | us |
| $C_b$ | Capacitive load for each bus | | 400 | | 400 | pF |

### 3.3.13 SPI interface characteristics

Figure 3-7 SPI timing diagram in Master mode

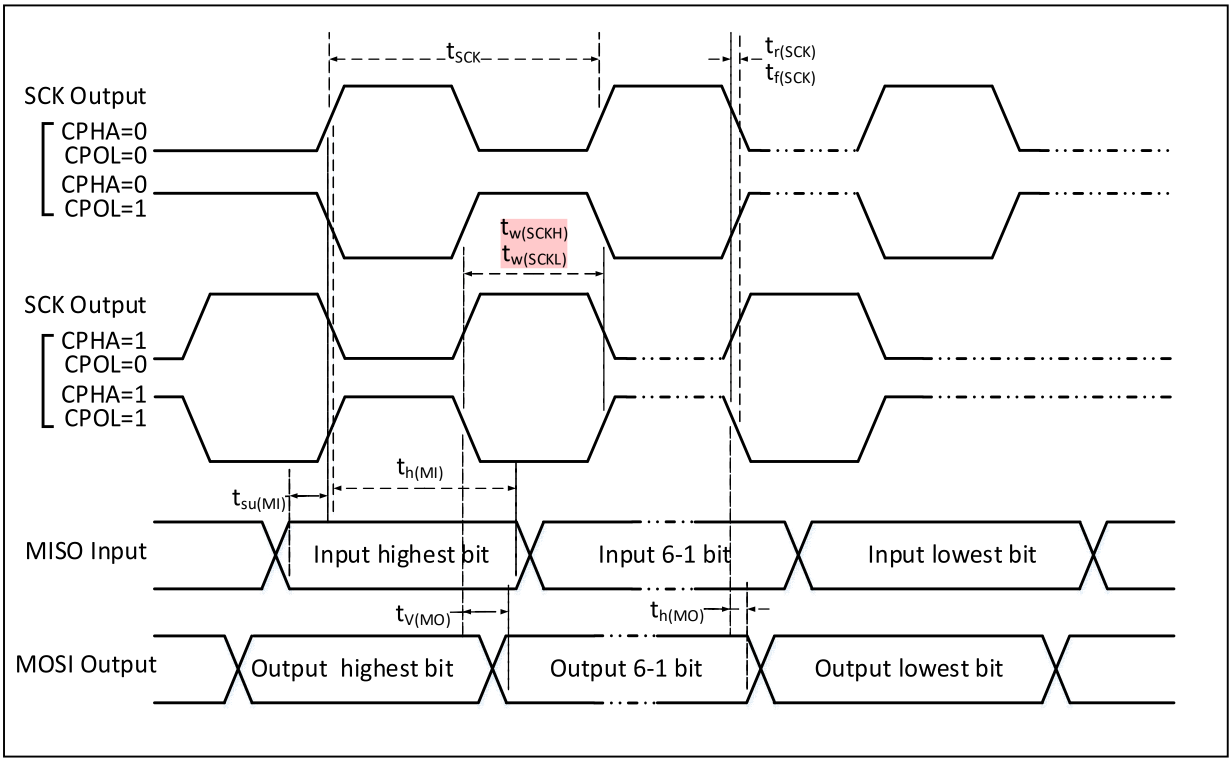
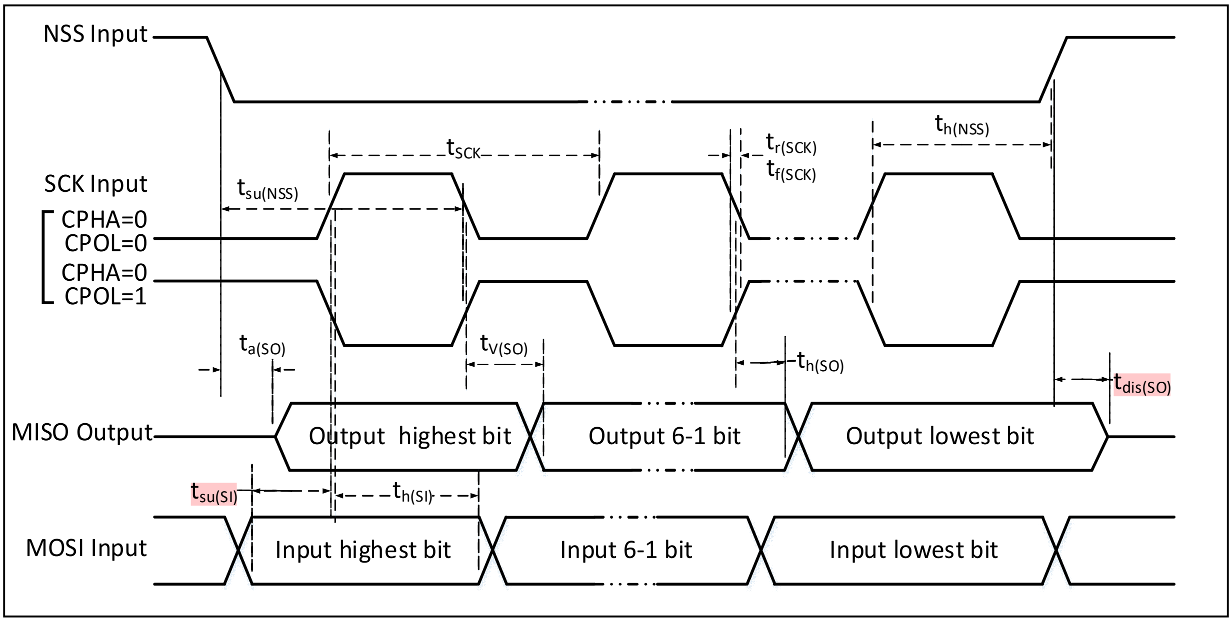



Figure 3-8 SPI timing diagram in Slave mode (CPHA = 0)



### 3.3.13 SPI Interface Characteristics

Figure 3-7 SPI timing diagram in Master mode

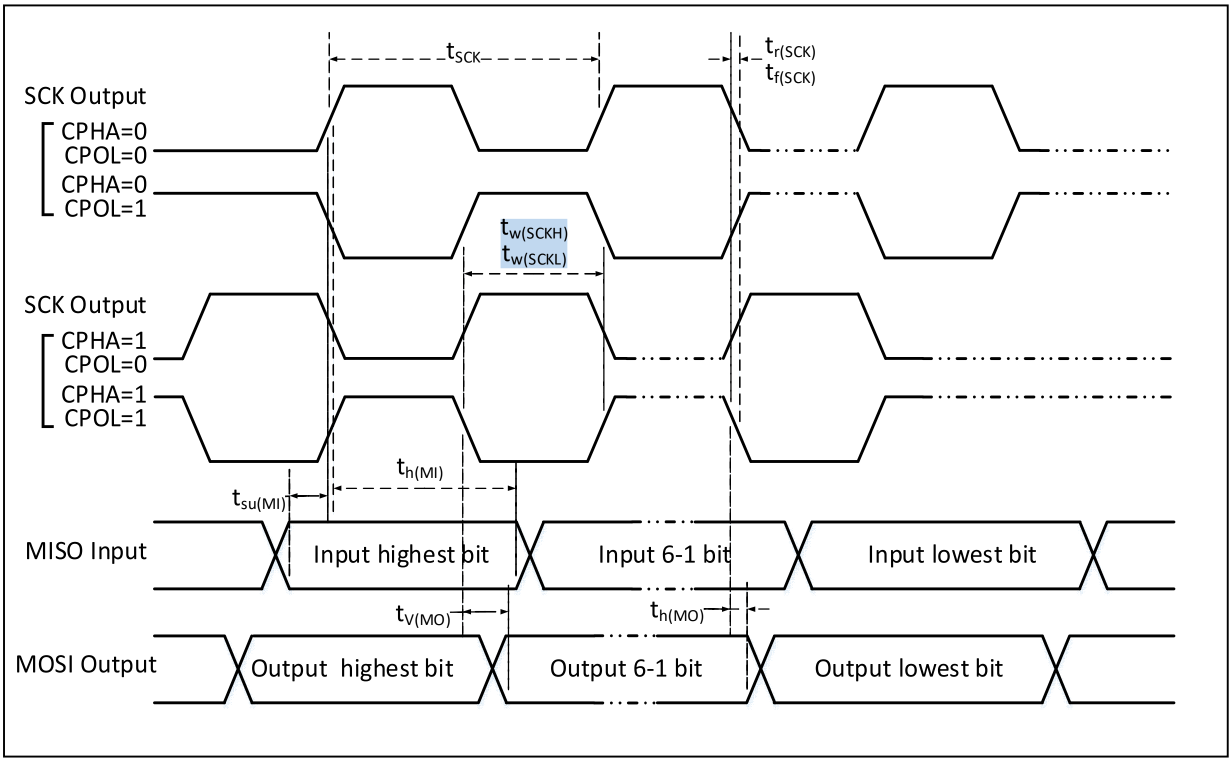



Figure 3-8-1 SPI timing diagram in Slave mode (CPHA = 0, CPOL=0)

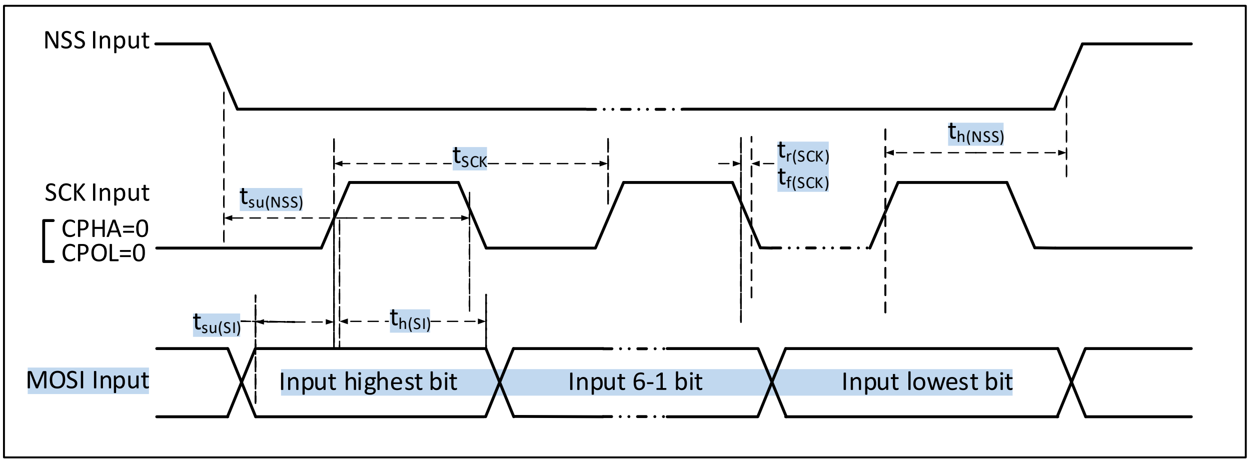


Figure 3-9 SPI timing diagram in Slave mode (CPHA = 1)

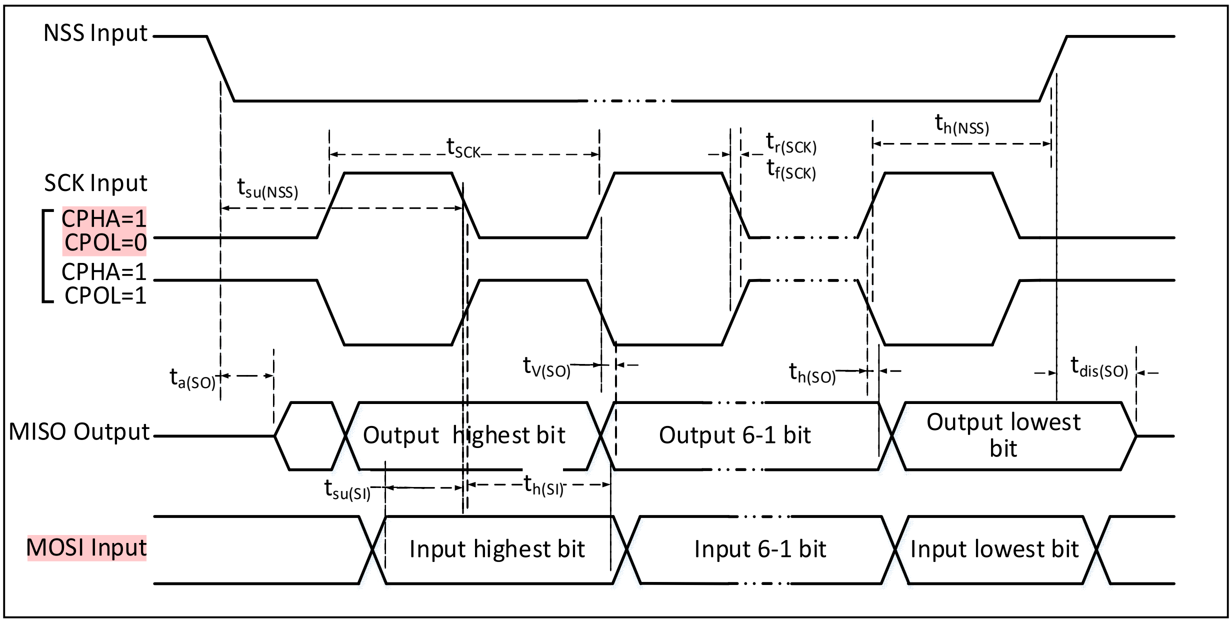



Table 3-22 SPI interface characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{SCK}/t_{SCK}$ | SPI clock frequency | Master mode | | 24 | MHz |
| | | Slave mode | | 24 | MHz |
| $t_{r(SCK)}/t_{f(SCK)}$ | SPI clock rise and fall time | Load capacitance:C = 30pF | | 20 | ns |
| $t_{SU(NSS)}$ | NSS setup time | Slave mode | $2t_{PCLK}$ | | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | $2t_{PCLK}$ | | ns |
| $t_{w(SCKH)}/t_{w(SCKL)}$ | SCK high and low time | Master mode, $f_{PCLK}$ = 48MHz, Prescaler factor = 2 | 30 | 70 | ns |
| $t_{SU(MI)}$ | Data input setup time | Master mode | 5 | | ns |
| $t_{SU(SI)}$ | | Slave mode | 5 | | ns |
| $t_{h(MI)}$ | Data input hold time | Master mode | 5 | | ns |
| $t_{h(SI)}$ | | Slave mode | 4 | | ns |
| $t_{a(SO)}$ | Data output access time | Slave mode, $f_{PCLK}$ = 24MHz | 0 | $1t_{PCLK}$ | ns |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 0 | 10 | ns |
| $t_{V(SO)}$ | Data output valid time | Slave mode (After enable edge) | | 5 | ns |
| $t_{V(MO)}$ | | Master mode (After enable edge) | | 5 | ns |
| $t_{h(SO)}$ | Data output hold time | Slave mode (After enable edge) | 2 | | ns |
| $t_{h(MO)}$ | | Master mode (After enable edge) | 0 | | ns |

### 3.3.14 10-bit ADC characteristics

Table 3-23 ADC characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 2.8 | | 5.5 | V |
| $I_{DD}$ | Supply current | | | 370 | | uA |

Figure 3-8-2 SPI timing diagram in Slave mode (CPHA = 0, CPOL=1)

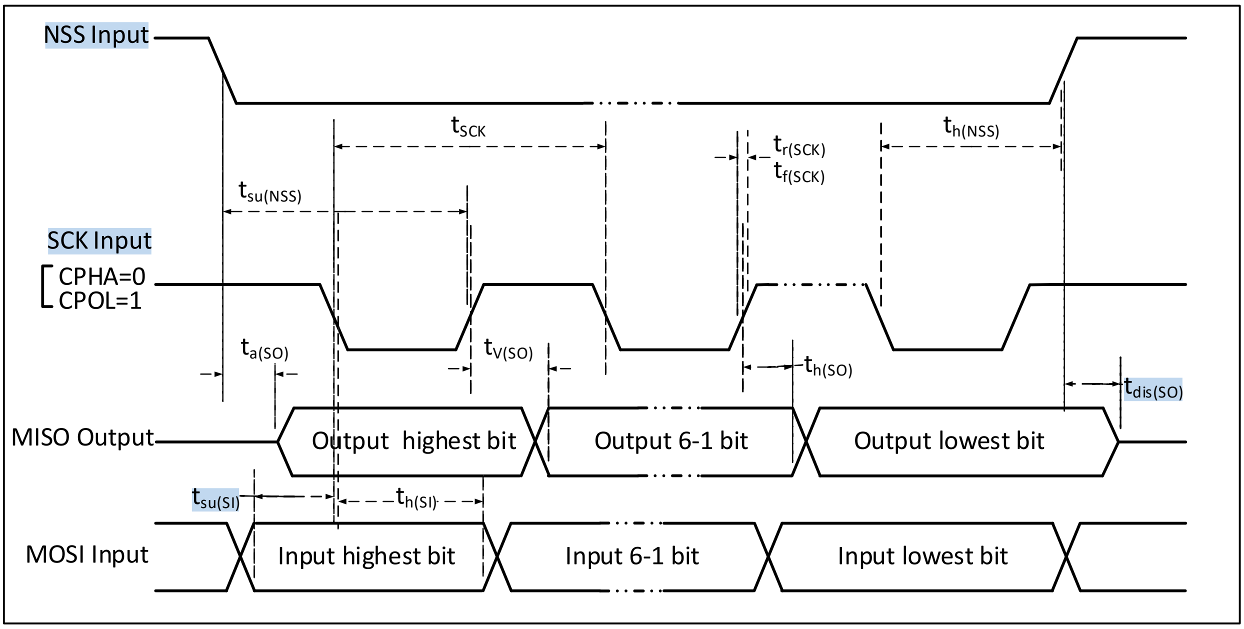



Figure 3-9-1 SPI timing diagram in Slave mode (CPHA=1, CPOL=0)

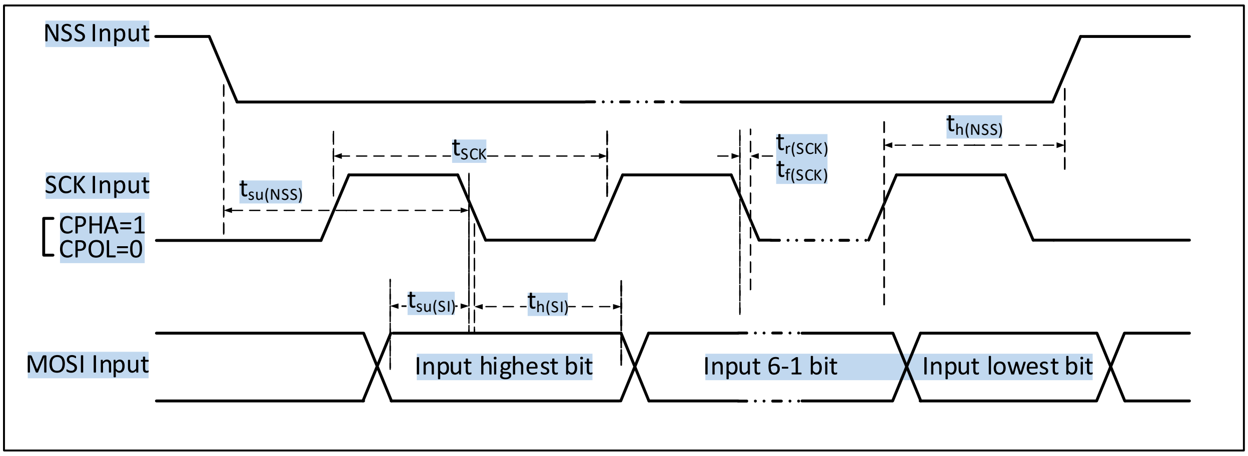


Figure 3-9-1 SPI timing diagram in Slave mode (CPHA=1, CPOL=1)

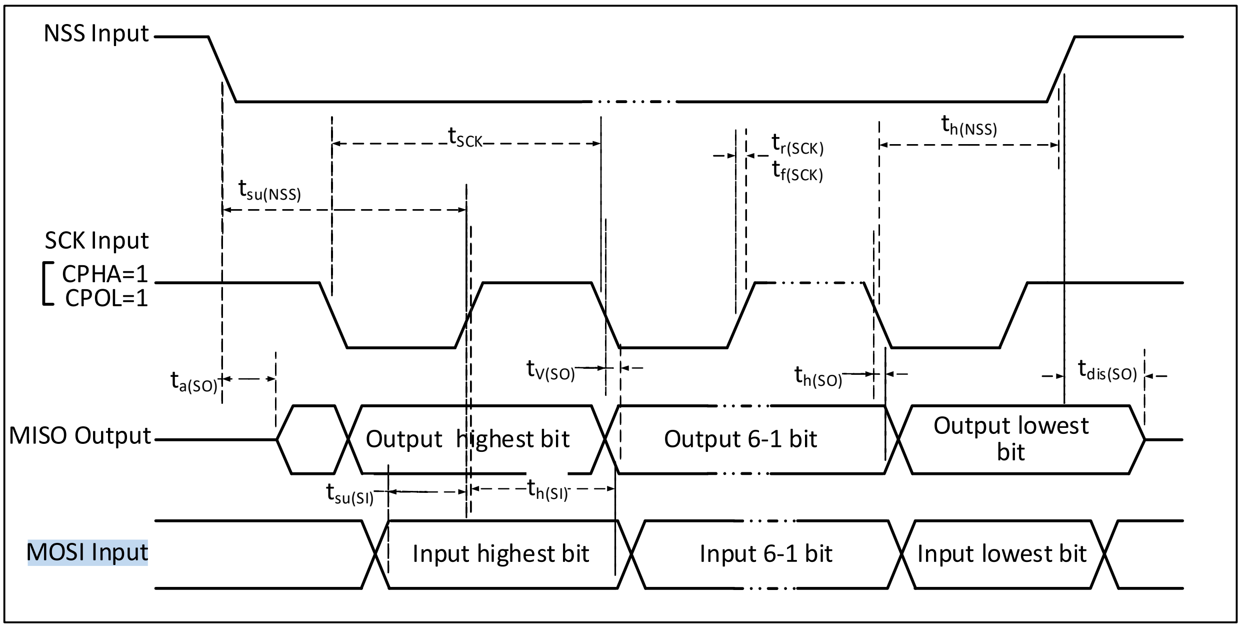



Table 3-22 SPI interface characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{SCK}/t_{SCK}$ | SPI clock frequency | Master mode | | 24 | MHz |
| | | Slave mode | | 24 | MHz |
| $t_{r(SCK)}/t_{f(SCK)}$ | SPI clock rise and fall time | Load capacitance: C = 30pF | | 20 | ns |
| $t_{SU(NSS)}$ | NSS setup time | Slave mode | $2t_{PCLK}$ | | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | $2t_{PCLK}$ | | ns |
| $t_{w(SCKH)}/t_{w(SCKL)}$ | SCK high and low time | Master mode, $f_{PCLK}$ = 48MHz, Prescaler factor = 2 | 30 | 70 | ns |
| $t_{SU(MI)}$ | Data input setup time | Master mode | 5 | | ns |
| $t_{SU(SI)}$ | | Slave mode | 5 | | ns |
| $t_{h(MI)}$ | Data input hold time | Master mode | 5 | | ns |
| $t_{h(SI)}$ | | Slave mode | 4 | | ns |
| $t_{a(SO)}$ | Data output access time | Slave mode, $f_{PCLK}$ = 24MHz | 0 | $1t_{PCLK}$ | ns |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 0 | 10 | ns |
| $t_{V(SO)}$ | Data output valid time | Slave mode (After enable edge) | | 5 | ns |
| $t_{V(MO)}$ | | Master mode (After enable edge) | | 5 | ns |
| $t_{h(SO)}$ | Data output hold time | Slave mode (After enable edge) | 2 | | ns |
| $t_{h(MO)}$ | | Master mode (After enable edge) | 0 | | ns |

### 3.3.14 10-bit ADC Characteristics

Table 3-23 ADC characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 2.8 | | 5.5 | V |
| $I_{DD}$ | Supply current | | | 370 | | uA |

| | | | | | | |
|---|---|---|---|---|---|---|
| $f_{ADC}$ | ADC clock frequency | $V_{DD}$ = 2.8 to 5.5V | 1 | | 6 | MHz |
| | | $V_{DD}$ = 3.2 to 5.5V | 1 | | 12 | |
| | | $V_{DD}$ = 4.5 to 5.5V | 1 | | 24 | |
| $V_{AIN}$ | Conversion voltage range | | $V_{SS}$ | | $V_{DD}$ | V |
| $C_{ADC}$ | Internal sample and hold capacitor | | | 3 | | pF |
| $f_S$ | Sampling rate | $f_{ADC}$ = 4 MHz | | | 285 | KHz |
| | | $f_{ADC}$ = 6 MHz | | | 430 | |
| | | $f_{ADC}$ = 12 MHz | | | 857 | |
| | | $f_{ADC}$ = 24 MHz | | | 1710 | |
| $t_s$ | Sampling time | $f_{ADC}$ = 4 MHz | | 0.75 | | us |
| | | $f_{ADC}$ = 6 MHz | | 0.5 | | |
| | | $f_{ADC}$ = 12 MHz | | 0.25 | | |
| $t_{STAB}$ | Power-on time | | | 7 | | us |
| $t_{CONV}$ | Total conversion time (including sampling time) | $f_{ADC}$ = 4 MHz | 3.5 | | | us |
| | | $f_{ADC}$ = 6 MHz | 2.33 | | | us |
| | | $f_{ADC}$ = 12 MHz | 1.17 | | | us |
| | | - | | 14 | | $1/f_{ADC}$ |

*Note: Above parameters are guaranteed by design.*

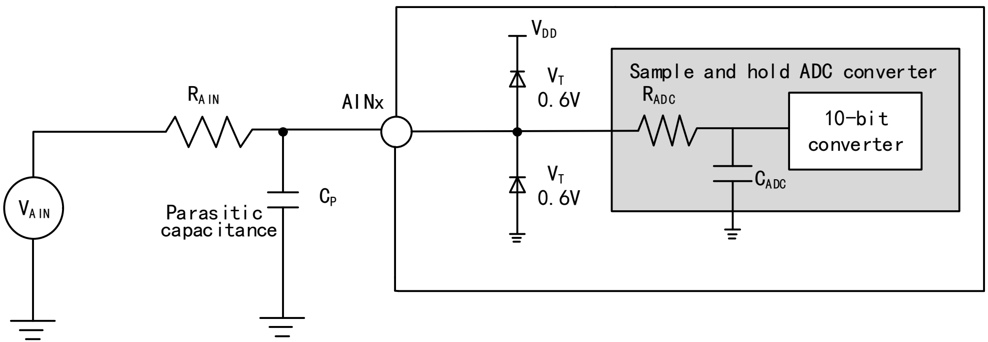
Table 3-24 ADC error ($f_{ADC}$ = 12MHz:$R_{AIN}$ < 10kΩ,$V_{DD}$ > 2.9V)($f_{ADC}$ = 24MHz:$R_{AIN}$ < 3kΩ,$V_{DD}$ = 5V)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| ET | Total data deviation | $f_{ADC}$ = 12 MHz | | 2 | 4 | LSB |
| ETF24 | $f_{ADC}$ = 24MHz total data deviation | $f_{ADC}$ = 24 MHz | | 3 | 6 | |
| EO | Misalignment error | $f_{ADC}$ = 12 MHz | | 1 | 3 | |
| EG | Gain error | $f_{ADC}$ = 12 MHz | | 1 | 2 | |
| ED | Differential nonlinearity error | $f_{ADC}$ = 12 MHz | | 0.5 | 2 | |
| EL | Integral nonlinearity error | $f_{ADC}$ = 12 MHz | | 0.6 | 2.5 | |

*Note: Source simulation.*

$C_p$ represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger $C_p$ value will reduce the conversion accuracy, the solution is to reduce the $f_{ADC}$ value.

Figure 3-10 ADC typical connection diagram



| | | | | | | |
|---|---|---|---|---|---|---|
| $f_{ADC}$ | ADC clock frequency | $V_{DD}$ = 2.8 to 5.5V | 1 | | 6 | MHz |
| | | $V_{DD}$ = 3.2 to 5.5V | 1 | | 12 | |
| | | $V_{DD}$ = 4.5 to 5.5V | 1 | | 24 | |
| $V_{AIN}$ | Conversion voltage range | | $V_{SS}$ | | $V_{DD}$ | V |
| $C_{ADC}$ | Internal sample and hold capacitor | | | 3 | | pF |
| $f_S$ | Sampling rate | $f_{ADC}$ = 4 MHz | | | 285 | KHz |
| | | $f_{ADC}$ = 6 MHz | | | 430 | |
| | | $f_{ADC}$ = 12 MHz | | | 857 | |
| | | $f_{ADC}$ = 24 MHz | | | 1710 | |
| $t_s$ | Sampling time | $f_{ADC}$ = 4 MHz | | 0.75 | | us |
| | | $f_{ADC}$ = 6 MHz | | 0.5 | | |
| | | $f_{ADC}$ = 12 MHz | | 0.25 | | |
| $t_{STAB}$ | Power-on time | | | 7 | | us |
| $t_{CONV}$ | Total conversion time (including sampling time) | $f_{ADC}$ = 4 MHz | 3.5 | | | us |
| | | $f_{ADC}$ = 6 MHz | 2.33 | | | us |
| | | $f_{ADC}$ = 12 MHz | 1.17 | | | us |
| | | - | | 14 | | $1/f_{ADC}$ |

*Note: Above parameters are guaranteed by design.*

Table 3-24 ADC error ($f_{ADC}$ = 12MHz:$R_{AIN}$ < 10kΩ,$V_{DD}$ > 2.9V)($f_{ADC}$ = 24MHz:$R_{AIN}$ < 3kΩ,$V_{DD}$ = 5V)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| ET | Total data deviation | $f_{ADC}$ = 12 MHz | | 2 | 6 | LSB |
| ETF24 | $f_{ADC}$ = 24MHz total data deviation | $f_{ADC}$ = 24 MHz | | 3 | 8 | |
| EO | Misalignment error | $f_{ADC}$ = 12 MHz | | 1 | 5 | |
| EG | Gain error | $f_{ADC}$ = 12 MHz | | 1 | 2 | |
| ED | Differential nonlinearity error | $f_{ADC}$ = 12 MHz | | 0.5 | 2 | |
| EL | Integral nonlinearity error | $f_{ADC}$ = 12 MHz | | 0.6 | 2.5 | |

*Note: Source simulation.*

$C_p$ represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger $C_p$ value will reduce the conversion accuracy, the solution is to reduce the $f_{ADC}$ value.

Figure 3-10 ADC typical connection diagram

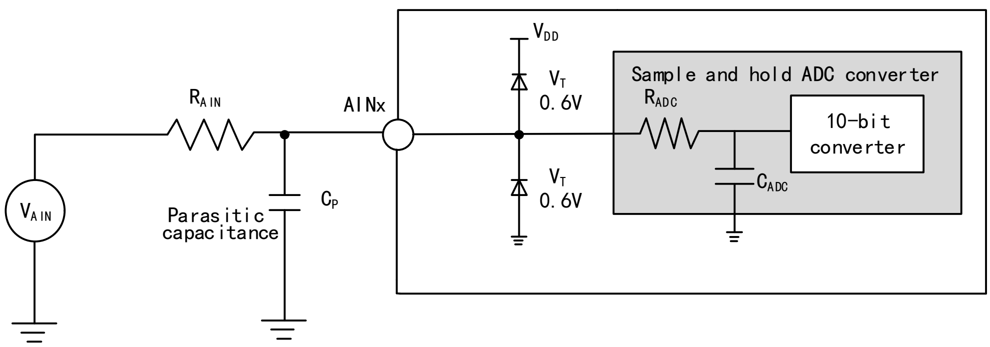
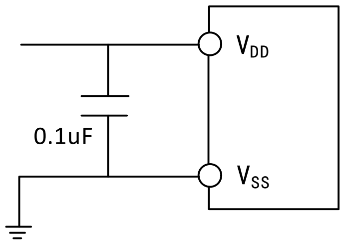


Figure 3-11 Analog power supply and decoupling circuit reference




### 3.3.15 OPA characteristics

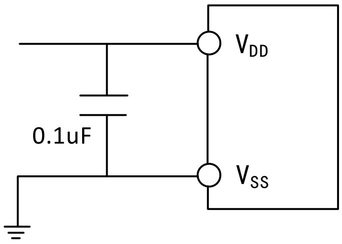
Table 3-25 OPA characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 2.8 | | 5.5 | V |
| $C_{MIR}$ | Common mode input voltage | | 0 | | $V_{DD}$ | V |
| $V_{IOFFSET}$ | Input offset voltage | | | 3 | 10 | mV |
| $I_{LOAD}$ | Drive current | | | | 1.5 | mA |
| $I_{DDOPAMP}$ | Current consumption | No load, static mode | | 273 | | uA |
| $C_{MRR}$(1) | Common mode rejection ratio | @1KHz | | 81 | | dB |
| $P_{SRR}$(1) | Power supply rejection ratio | @1KHz | | 88 | | dB |
| $A_V$(1) | Open loop gain | $C_{LOAD}$ = 50pF | | 105 | | dB |
| $G_{BW}$(1) | Unit gain bandwidth | $C_{LOAD}$ = 50pF | | 12 | | MHz |
| $P_M$(1) | Phase margin | $C_{LOAD}$ = 50pF | | 75 | | deg |
| $S_R$(1) | Slew rate limited | $C_{LOAD}$ = 50pF | | 7.7 | | V/us |
| $t_{WAKU}$(1) | Setup time from shutdown to wake up, 0.1% | Input $V_{DD}$/2, $C_{LOAD}$=50pF,$R_{LOAD}$=4kΩ | | 520 | | ns |
| $R_{LOAD}$ | Resistive load | | 4 | | | kΩ |
| $C_{LOAD}$ | Capacitive load | | | | 50 | pF |
| $V_{OHSAT}$(2) | High saturation output voltage | $R_{LOAD}$ = 4kΩ, input $V_{DD}$ | $V_{DD}$-180 | | | mV |
| | | $R_{LOAD}$ = 20kΩ, input $V_{DD}$ | $V_{DD}$-36 | | | |
| $V_{OLSAT}$(2) | Low saturation output voltage | $R_{LOAD}$ = 4kΩ, input 0 | | | 5 | mV |
| | | $R_{LOAD}$ = 20kΩ, input 0 | | | 5 | |
| EN(1) | Equivalent input voltage noise | $R_{LOAD}$ = 4kΩ, @1KHz | | 83 | | $\frac{nv}{\sqrt{Hz}}$ |
| | | $R_{LOAD}$ = 4kΩ, @10KHz | | 28 | | |

*Note: 1. Design parameters are guaranteed.*

*2. The load current limits the saturated output voltage.*

Figure 3-11 Analog power supply and decoupling circuit reference




### 3.3.15 OPA Characteristics

Table 3-25 OPA characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 2.8 | | 5.5 | V |
| $C_{MIR}$ | Common mode input voltage | | 0 | | $V_{DD}$ | V |
| $V_{IOFFSET}$ | Input offset voltage | | | ±3 | ±13 | mV |
| $I_{LOAD}$ | Drive current | | | | 1.5 | mA |
| $I_{DDOPAMP}$ | Current consumption | No load, static mode | | 273 | | uA |
| $C_{MRR}$(1) | Common mode rejection ratio | @1KHz | | 81 | | dB |
| $P_{SRR}$(1) | Power supply rejection ratio | @1KHz | | 88 | | dB |
| $A_V$(1) | Open loop gain | $C_{LOAD}$ = 50pF | | 105 | | dB |
| $G_{BW}$(1) | Unit gain bandwidth | $C_{LOAD}$ = 50pF | | 12 | | MHz |
| $P_M$(1) | Phase margin | $C_{LOAD}$ = 50pF | | 75 | | deg |
| $S_R$(1) | Slew rate limited | $C_{LOAD}$ = 50pF | | 7.7 | | V/us |
| $t_{WAKU}$(1) | Setup time from shutdown to wake up, 0.1% | Input $V_{DD}$/2, $C_{LOAD}$=50pF,$R_{LOAD}$=4kΩ | | 520 | | ns |
| $R_{LOAD}$ | Resistive load | | 4 | | | kΩ |
| $C_{LOAD}$ | Capacitive load | | | | 50 | pF |
| $V_{OHSAT}$(2) | High saturation output voltage | $R_{LOAD}$ = 4kΩ, input $V_{DD}$ | $V_{DD}$-180 | | | mV |
| | | $R_{LOAD}$ = 20kΩ, input $V_{DD}$ | $V_{DD}$-36 | | | |
| $V_{OLSAT}$(2) | Low saturation output voltage | $R_{LOAD}$ = 4kΩ, input 0 | | | 5 | mV |
| | | $R_{LOAD}$ = 20kΩ, input 0 | | | 5 | |
| EN(1) | Equivalent input voltage noise | $R_{LOAD}$ = 4kΩ, @1KHz | | 83 | | $\frac{nv}{\sqrt{Hz}}$ |
| | | $R_{LOAD}$ = 4kΩ, @10KHz | | 28 | | |

*Note: 1. Design parameters are guaranteed.*

*2. The load current limits the saturated output voltage.*

# Chapter 4 Package and Ordering Information

## Packages

| Part No. | Package | Body size | Lead pitch | Description | Packing type |
|---|---|---|---|---|---|
| CH32V003F4P6 | TSSOP20 | 4.4*6.5mm | 0.65mm | Thin Shrink Small Outline Package | Tape & Reel |
| CH32V003F4U6 | QFN20 | 3.0*3.0mm | 0.4mm | Quad Flat No-lead Package | Tape & Reel |
| CH32V003A4M6 | SOP16 | 3.9*10mm | 1.27mm | Small Outline Package | Tube |
| CH32V003J4M6 | SOP8 | 3.9*5.0mm | 1.27mm | Small Outline Package | Tape & Reel |

*Note: 1. The packing type of QFP/QFN is usually tray.*

*2. Size of tray: The size of tray is generally a uniform size (322.6*135.9*7.62). There are differences in the size of the restriction holes for different package types, and there are differences between different packaging factories for tubes, please confirm with the manufacturer for details.*

# Chapter 4 Package and Ordering Information

## Packages

| Package Form | Body Size | Pin Pitch | | Package Description | Order Model |
|---|---|---|---|---|---|
| TSSOP20 | 4.4*6.5mm | 0.65mm | 25.6mil | Thin Shrink Small Outline Package | CH32V003F4P6 |
| QFN20 | 3.0*3.0mm | 0.4mm | 15.7mil | Quad Flat No-lead Package | CH32V003F4U6 |
| SOP16 | 3.9*10.0mm | 1.27mm | 50mil | Small Outline Package | CH32V003A4M6 |
| SOP8 | 3.9*5.0mm | 1.27mm | 50mil | Small Outline Package | CH32V003J4M6 |

*Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or 10%.*

Figure 4-1 TSSOP20 package

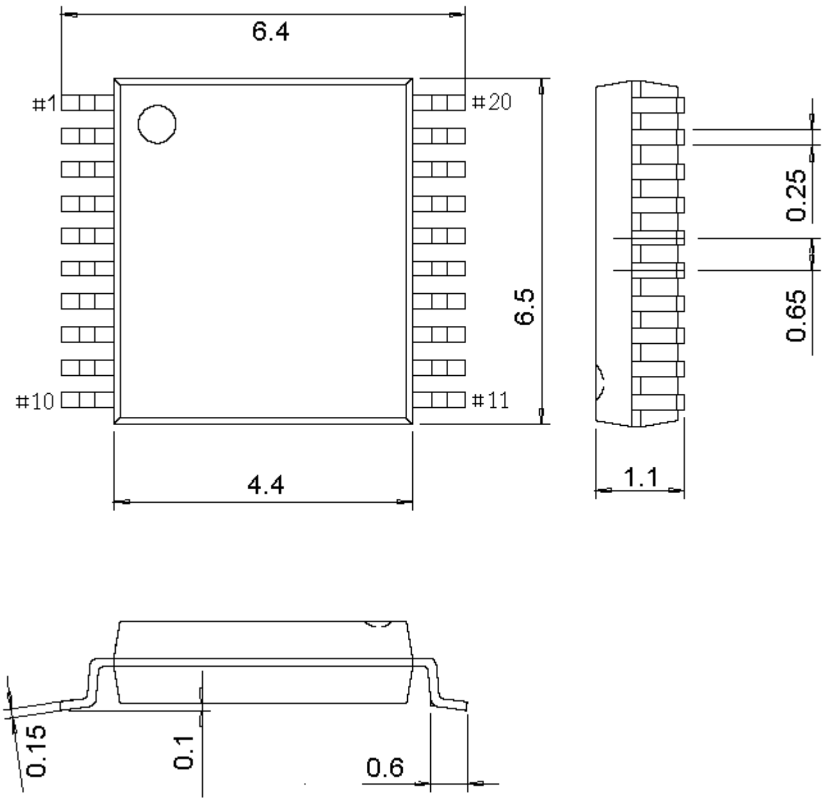
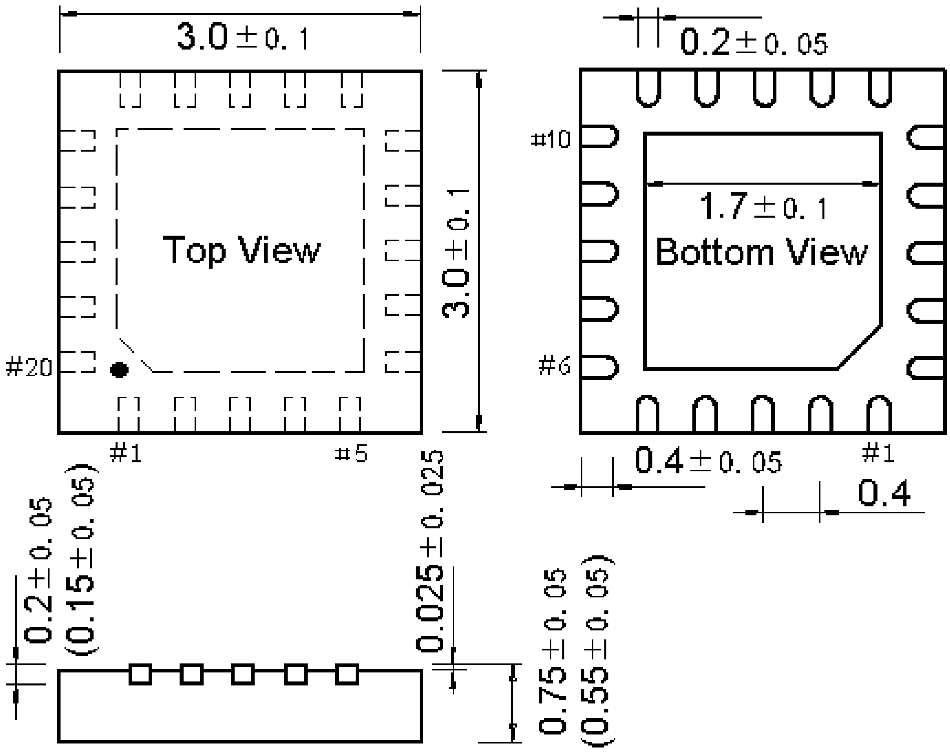



Figure 4-2 QFN20 package



*Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or 10%.*

Figure 4-1 TSSOP20 package

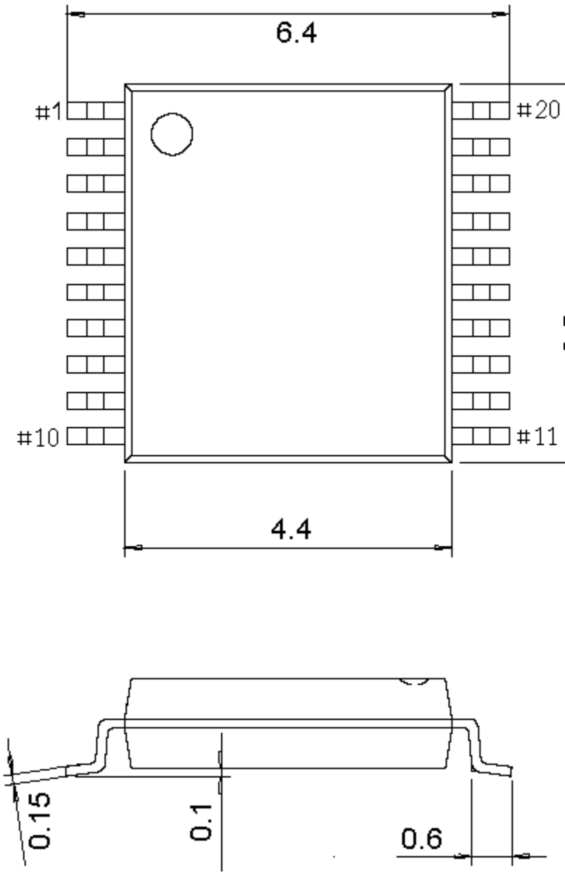



Figure 4-2 QFN20 package

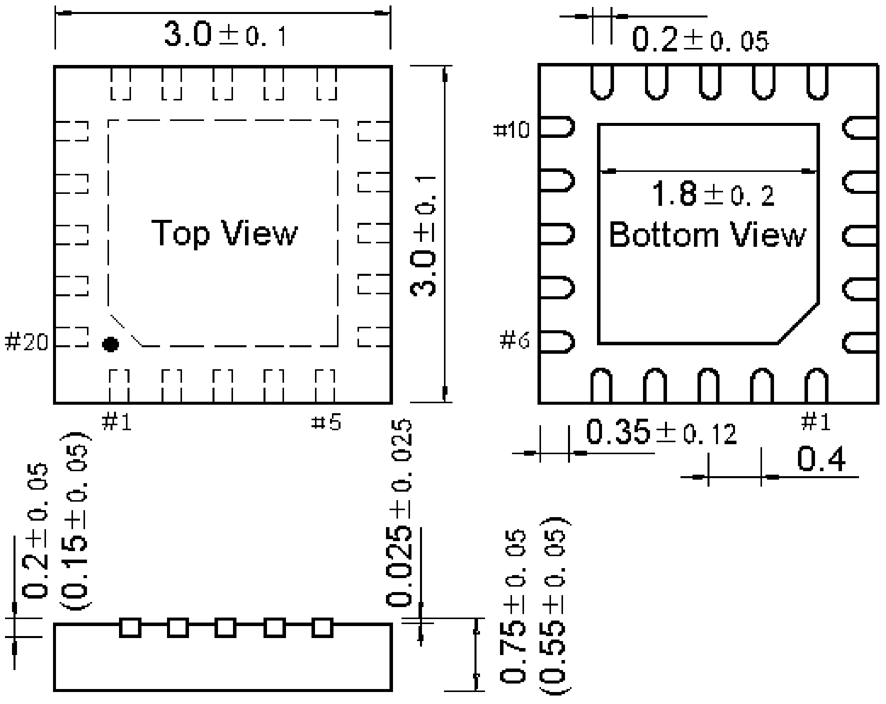


Figure 4-3 SOP16 package

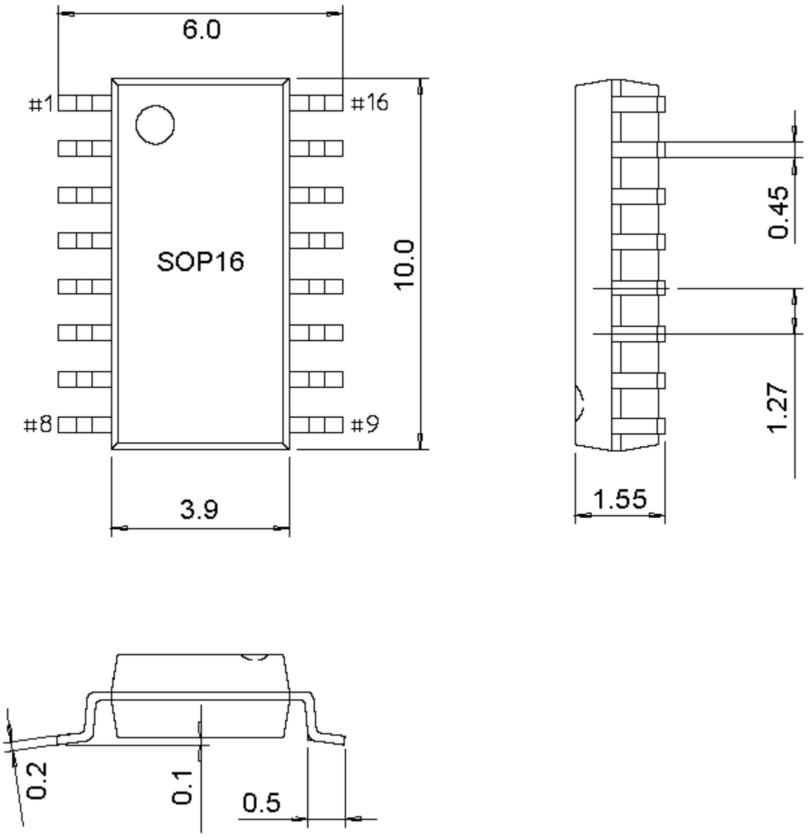



Figure 4-4 SOP8 package

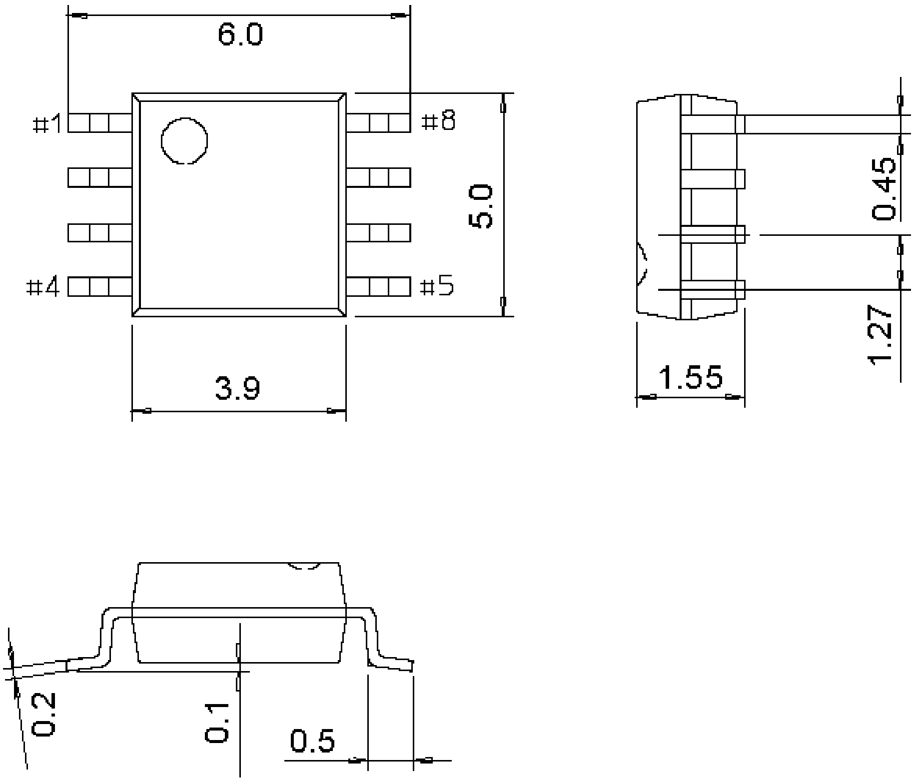


Figure 4-3 SOP16 package

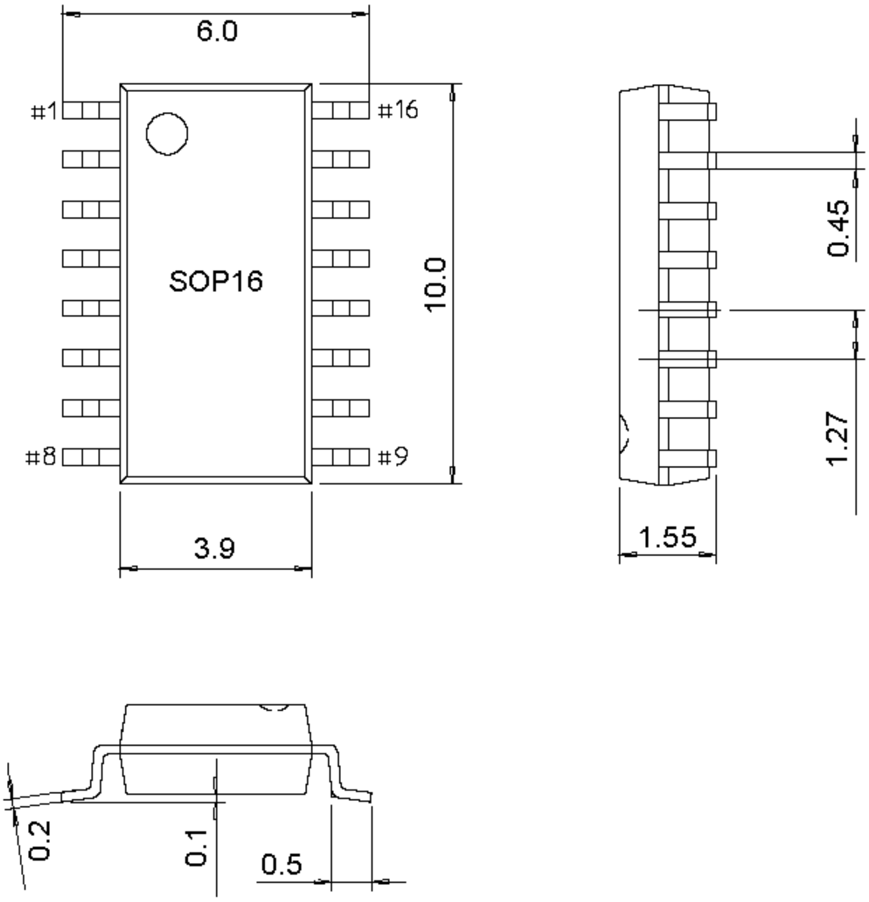
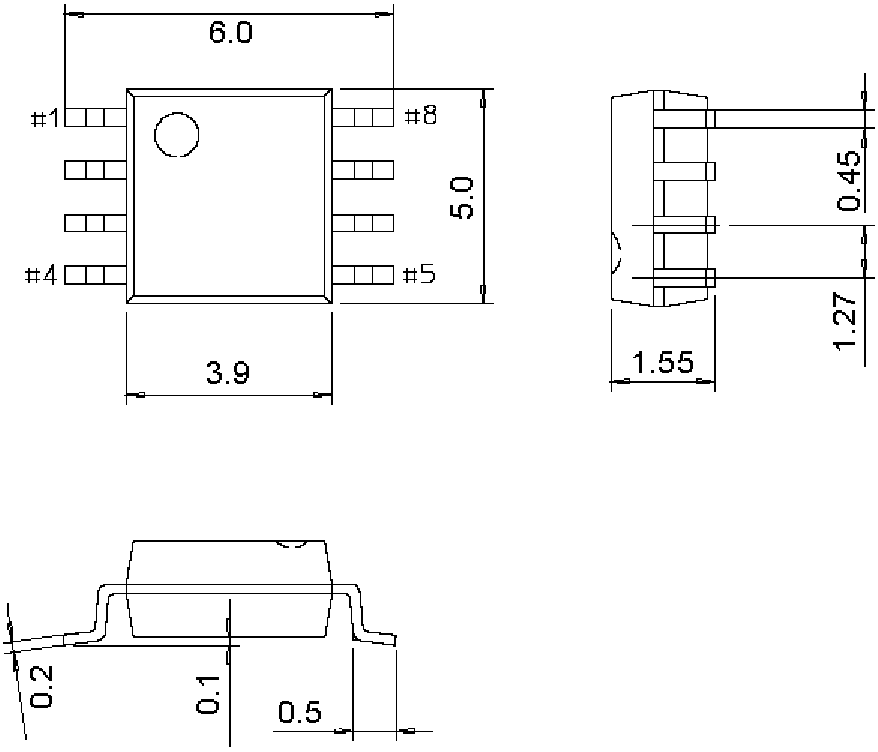



Figure 4-4 SOP8 package



# Series Product Naming Rules

Example: CH32 V 3 03 R 8 T 6

Device family

F = ARM-based, general-purpose MCU
V = QingKe RISC-V-based, general-purpose MCU
L = QingKe RISC-V-based, low power MCU
X = QingKe RISC-V-based, Dedicated architecture or special IO

Product type

0 = QingKe V2/V4 core, main frequency @48M
1 = M3/ QingKe V3/V4 core, main frequency @72M
2 = M3/ QingKe V4 non-floating-point core, main frequency @144M
3 = QingKe V4F floating-point core, main frequency @144M

Device subfamily

03 = General-purpose
05 = Connectivity (USB high-speed, SDIO, dual CAN)
07 = Interconnectivity (USB high-speed, dual CAN, Ethernet, DVP, SDIO, FSMC)
08 = Wireless (BLE5.X, CAN, USB, Ethernet)
35 = Connectivity (USB, USB PD)

Pin count

| | | |
|---|---|---|
| J = 8 pins | A = 16 pins | F = 20 pins |
| G = 28 pins | K = 32 pins | T = 36 pins |
| C = 48 pins | R = 64 pins | W = 68 pins |
| V = 100 pins | Z = 144 pins | |

Flash memory size

4 = 16 Kbytes of Flash memory
6 = 32 Kbytes of Flash memory
7 = 48 Kbytes of Flash memory
8 = 64 Kbytes of Flash memory
B = 128 Kbytes of Flash memory
C = 256 Kbytes of Flash memory

Package

T = LQFP U = QFN R = QSOP P = TSSOP M = SOP

Temperature range

6 = -40°C~85°C (industrial-grade)
7 = -40°C~105°C (automotive-grade 2)
3 = -40°C~125°C (automotive-grade 1)
D = -40°C~150°C (automotive-grade 0)

# Series Product Naming Rules

Example: CH32 V 3 03 R 8 T 6

Device family

F = ARM-based, general-purpose MCU
V = QingKe RISC-V-based, general-purpose MCU
L = QingKe RISC-V-based, low power MCU
X = QingKe RISC-V-based, Dedicated architecture or special IO

Product type

0 = QingKe V2/V4 core, main frequency @48M
1 = M3/ QingKe V3/V4 core, main frequency @72M
2 = M3/ QingKe V4 non-floating-point core, main frequency @144M
3 = QingKe V4F floating-point core, main frequency @144M

Device subfamily

03 = General-purpose
05 = Connectivity (USB high-speed, SDIO, dual CAN)
07 = Interconnectivity (USB high-speed, dual CAN, Ethernet, DVP, SDIO, FSMC)
08 = Wireless (BLE5.X, CAN, USB, Ethernet)
35 = Connectivity (USB, USB PD)

Pin count

| | | |
|---|---|---|
| J = 8 pins | A = 16 pins | F = 20 pins |
| G = 28 pins | K = 32 pins | T = 36 pins |
| C = 48 pins | R = 64 pins | W = 68 pins |
| V = 100 pins | Z = 144 pins | |

Flash memory size

4 = 16 Kbytes of Flash memory
6 = 32 Kbytes of Flash memory
7 = 48 Kbytes of Flash memory
8 = 64 Kbytes of Flash memory
B = 128 Kbytes of Flash memory
C = 256 Kbytes of Flash memory

Package

T = LQFP U = QFN R = QSOP P = TSSOP M = SOP

Temperature range

6 = -40℃~85℃ (industrial-grade)
7 = -40℃~105℃ (automotive-grade 2)
3 = -40℃~125℃ (automotive-grade 1)
D = -40℃~150℃ (automotive-grade 0)