Basic information found on archive.org for page http://www.danbbs.dk/~rmadrm/source.htm
Re-formatted, more info added, typos corrected and plausibility cross-checked with schematics by Jens Schönfeld (www.icomp.de)

ALL-03 Hardware I/O Configuration

This document describes the I/O configuration of the ALL-03 device programmer. This information would be of use in the development of special purpose software for the ALL-03 (and possibly also for the Expro-60/80).

1. I/O Control Concept:

Some basic concepts need to be explained. The main control unit is on the adapter card (SAC-201).

There are two 8-bit I/O registers on the SAC-201 that are able to control all I/O registers on the ALL-03 main module.

Register name	I/O address	accesss
IDPORT	base address+0	Write-only
DATAPORT	base address+2	read+write

The base address is the I/O address of the SAC-201 as defined by DIP switches 1 and 2. These switches allow a choice of 16 possible base addresses from 200h to 2f0h (default is 2e0).

Every register on the ALL-03 main module can be controlled by writing its ID byte to the IDPORT and then reading from or writing to the DATAPORT (the ID bytes of all registers will be shown below).

Available control pins on test-socket:

1. VOPENID: 1, 5, 6, 7, 9 to 32, 36.

2. VHHENID: 9 to 32.

3. VCCENID: 40, 36, 34, 32, to 26, 9, 7, 5, 1, 25, 24.

4. VHHENCID: 32 to 28.

5. TTLID: all 40 pins can be defined as inputs or outputs.

Note 1: Devices that cannot use the previous pin definitions will require a special purpose external adapter.

Note 2 (from Jens): Some pins added to above list/following table, as schematics show additional functionality is present.

Pin #	VOP	VHH	VCC	VHHC (high current)	TTL	GND	Textool ZIF socket	GND	TTL	VHHC (high current)	VCC	VHH	VOP	Pin#
1	✔		✔		✔	✔		✔	✔		✔			40
2					✔				✔					39
3					✔				✔					38
4					✔				✔					37
5	✔		✔		✔				✔		✔		✔	36
6	✔				✔				✔					35
7	✔		✔		✔				✔		✔			34
8					✔				✔					33
9	✔	✔	✔		✔				✔	✔	✔	✔	✔	32
10	✔	✔			✔				✔	✔	✔	✔	✔	31
11	✔	✔			✔	✔		✔	✔	✔	✔	✔	✔	30
12	✔	✔			✔			✔	✔	✔	✔	✔	✔	29
13	✔	✔			✔			✔	✔	✔	✔	✔	✔	28
14	✔	✔			✔				✔		✔	✔	✔	27
15	✔	✔			✔				✔		✔	✔	✔	26
16	✔	✔			✔				✔		✔	✔	✔	25
17	✔	✔			✔				✔		✔	✔	✔	24
18	✔	✔			✔				✔			✔	✔	23
19	✔	✔	✔		✔			✔	✔			✔	✔	22
20	✔	✔	✔		✔	✔			✔		✔	✔	✔	21

Example: We wish to write the value 7fh to #1 D/A register (ID = e5h).

Assembly Language

```
idport equ 2e0h
dataport equ 2e2h

mov ax,0e5h ;id number setting
mov dx,idport
out dx,al
jmp $+2 ; recovery time

mov ax,7fh ;data writing
mov dx,dataport
out dx,al
jmp $+2 ; recovery time
```

C Language

```
#define idport 0x02e0
#define dataport 0x02e2

Outp (idport, 0xe5) ;/* ID number setting */
Outp (dataport, 0x7f) ;/* data writing */
```

2. ALL-03 register ID Mapping and Definition:

The following describes each 8-bit register and its associated ID bytes. All registers are reset to a low output at PC power on.

Power Source D/A Voltage Level Setting register:

e5h : #1 D/A named VOPID, full scale is 25.5 volt (400 ma), resolution is 0.1 volt, minimum voltage setting is 10.2 volt

Example: Writing 255 to register e5h will set the #1 D/A to 25.5 volt, writing 102 to e5h will set the D/A to 10.2 volt.

e6h #2 D/A named VHHID, full scale is 15.3 volt (400 ma) resolution is 0.06 volt, minimum voltage setting is 5.1 volt

Example: Writing 255 to register e6h will set the #2 D/A to 15.3 volt, writing 85 to e6h will set the D/A to 5.1 volt.

e7h #3 D/A named VCCID, full scale is 10.2 volt (1A) resolution is 0.04 volt, minimum voltage setting is 0 volt.

Example: Writing 255 to register e7h will set the #2 D/A to 10.2 volt, writing 0 to e7h will set the D/A to 0 volt.

The levels of each power source can be set by the above three D/A registers. However, additional register accesses are required to apply these voltages to the specified test-socket pins.

TTL Level I/O registers:

e0h TTLID+0
e1h TTLID+1
e2h TTLID+2
e3h TTLID+3
e4h TTLID+4

LSB of e0h is assigned to pin 1, and MSB of e4h is assigned to pin 40. Each pin can be a TTL level input or output. Before inputting from the desired pin, the user must output a high to that pin.

Example: After writing an ID byte (TTLID+i) to the IDPORT, one can then output 8 bits to the DATAPORT or input 8 bits from the DATAPORT.

VOP Level Output Control registers:

e8h VOPENID+0
e9h VOPENID+1
eah VOPENID+2
ebh VOPENID+3
ech VOPENID+4

LSB of e8h is assigned to pin 1, and MSB of ech is assigned to pin 40. Writing a high to a particular bit will apply the VOP source to the relevant test-socket pin. Writing a low will disable the VOP source output to that pin.

Example: After writing ID byte VOPENID+1 to the IDPORT, and then outputting 8 bit data to the DATAPORT, VOP will be applied to the relevant test-socket pins 9 through 16 via a 22 ohm current limiting resistor.

Note 1: Test-socket pins 2,3,4,6,8 and pins 33 to 40 have no VOP control circuit, so VOP cannot be output to these pins even though the relevant bit may have been set to high.

Note 2: VOP must not be applied to any pin for more than one hour.

VHH Level Output Control registers:

f0h VHHENID+0 (register not present)
f1h VHHENID+1
f2h VHHENID+2
f3h VHHENID+3
f4h VHHENID+4 (register not present)

LSB of f0h is assigned to pin 1, and MSB of f4h is assigned to pin 40.

Writing a high to a particular bit will apply the VHH source to the relevant test-socket pin. Writing a low will disable the VHH source output to that pin.

Example: After writing ID byte VHHENID+1 to the IDPORT, and then outputting 8 bit data to the DATAPORT, VHH will be applied to the relevant test-socket pins 9 through 16 via a 22 ohm current limiting resistor.

Note: 1. Test-socket pins 1 to 8 and pins 33 to 40 have no VHH control circuit, so VHH cannot be output to these pins even though the relevant bit may have been set to high.

2. VHH must not be applied to any pin for more than one hour.

VCC Output Control:

edh VCCENID+0
eeh VCCENID+1

edh		eeh	
	b0 : pin 40		b0 : pin 27
	bl : pin 36		bl : pin 26
	b2 : pin 34		b2 : pin 9
	b3 : pin 32		b3 : pin 7
	b4 : pin 31		b4 : pin 5
	b5 : pin 30		b5 : pin 1
	b6 : pin 29		b6 : pin 25
	b7 : pin 28		b7 : pin 24

Writing a high to a particular bit will apply the VCC source to the relevant test-socket pin. Writing a low will disable the VCC source output to that pin.

Example: After writing ID byte VCCENID+0 to the IDPORT, and then outputting 8 bit data to the DATAPORT, VCC will be directly applied to the relevant test-socket pins 28 through 40.

VHHC Output to Extra Pins Control registers:

The difference between these extra pins and the previously listed VHH pins is that **these extra pins have no 22 ohm current limiting resistor** in series with the VHH source. This is to permit some PAL VCC pins to be driven at high voltage (over 12 volts) and high current.

f5h VHHENCID+0
f6h VHHENCID+1 (register not present)

Total 16 bits assigned to 16 pins on test-socket.

f5h b0-2 : not used
b3 : pin 32
b4 : pin 31
b5 : pin 30
b6 : pin 29
b7 : pin 28

Writing a high to a particular bit will apply the VHH source w/o current limit to the relevant test-socket pin. Writing a low will disable the VHH source output to that pin.

Example: After writing ID byte VCCENCID+0 to the IDPORT, and then outputting 8 bit data to the DATAPORT, VHH will be directly applied to the relevant test-socket pins 28 through 32.

"Other Pins" Control registers:

Some additional pins not previously specified will be listed here.
(note from Jens:) This register description did not reflect the schematics of the Expro-60 or the All-03 at all, so it was updated with what I believe is correct.

efh: OTHERENID
f7h: VCC+CAP

efh
b0 : part of a 3-bit value together with b6 and b7 (see further down)

bl : hi will output VOP (source – 2.4V, 10R current limiting res) to pin 7. low will disable output.

b2 : hi will output VOP (source - 2.4V, 10R current limiting res) to pin 25. low will disable output.

b3, b4, b5: oscillator and power control to pins 2/3, 18/19

b3	b4	b5	Pin#2	Pin#3	Pin#18	Pin#19
0	0	0	1	1	0	0
0	0	1	0	1	1	1
0	1	0	0	1	2.097152MHz	Pin18 inv + 2k2 pullup
0	1	1	0	1	4.194304MHz	Pin18 inv + 2k2 pullup
1	0	0	2.097152MHz	Pin#2 inverted	1	0
1	0	1	4.194304MHz	Pin#2 inverted	1	0
1	1	0	0	1	1	0 + 2k2 pullup
1	1	1	0	1	1	0 + 2k2 pullup

CAUTION (from Jens): This table is derived from exp_u5.eqn file by Alix G. It is highly implausible that pins 2 and 19 are pulled low after a reset. I believe that the equation file is wrong and needs to be re-checked. Another possibility is that the open-drain gates for U5 pins 12, 13, 18, 19 are wrong (2 are inverting and 2 are non-inverting in the All-03 schematics). Either way, this looks wrong!

Register efh Bits b0, b6, b7: GND control

b7	b6	b0	GND selected
0	0	0	PIN#20 (relay – no practical current limit) – default after reset.
0	0	1	Pin#11 500mA max (guessed limit due to transistor Vce)
0	1	0	Pin#1 500mA max (guessed limit due to transistor Vce)
0	1	1	Pin#22 500mA max (guessed limit due to transistor Vce)
1	0	0	Pin#28 500mA max (guessed limit due to transistor Vce)
1	0	1	Pin#40 500mA max (guessed limit due to transistor Vce)
1	1	0	Pin#30 500mA max (guessed limit due to transistor Vce)
1	1	1	Pin#29 500mA max (guessed limit due to transistor Vce)

Register f7h: Additional VCC and bypass cap control

b0: 1= Apply VCC to Pin#19
b1: 1= Apply VCC to Pin#20
b2: 1= Apply VCC to Pin#21
b3, b4: unused
b5: 1= Apply GND to pin#30 (500mA limit, see above)
b6: 1= add 100nF bypass capacitor to pin#30
b7: 1= add 100nF bypass capacitor to pin#32

Register f8h: This is listed as „read shift rotate“. This resides in the two PAL16R4 on U33 and U35. The two relevant signals „shift clock“ and „shift data“ are controlled by writing to register e7h bits 0 and 1 (dual-use of LSB/LSB+1 for VCC voltage control).
TODO: Investigate differences between All-03, Expro-60 and Modular Circuit MOD-EMUP.

Registers f9h up to ffh do not exist.

Appendix: Voltage drops

Voltage drops exist between the power sources and the test socket pins. These voltage drop factors need to be included in the D/A power source level settings.

These voltage drops are:

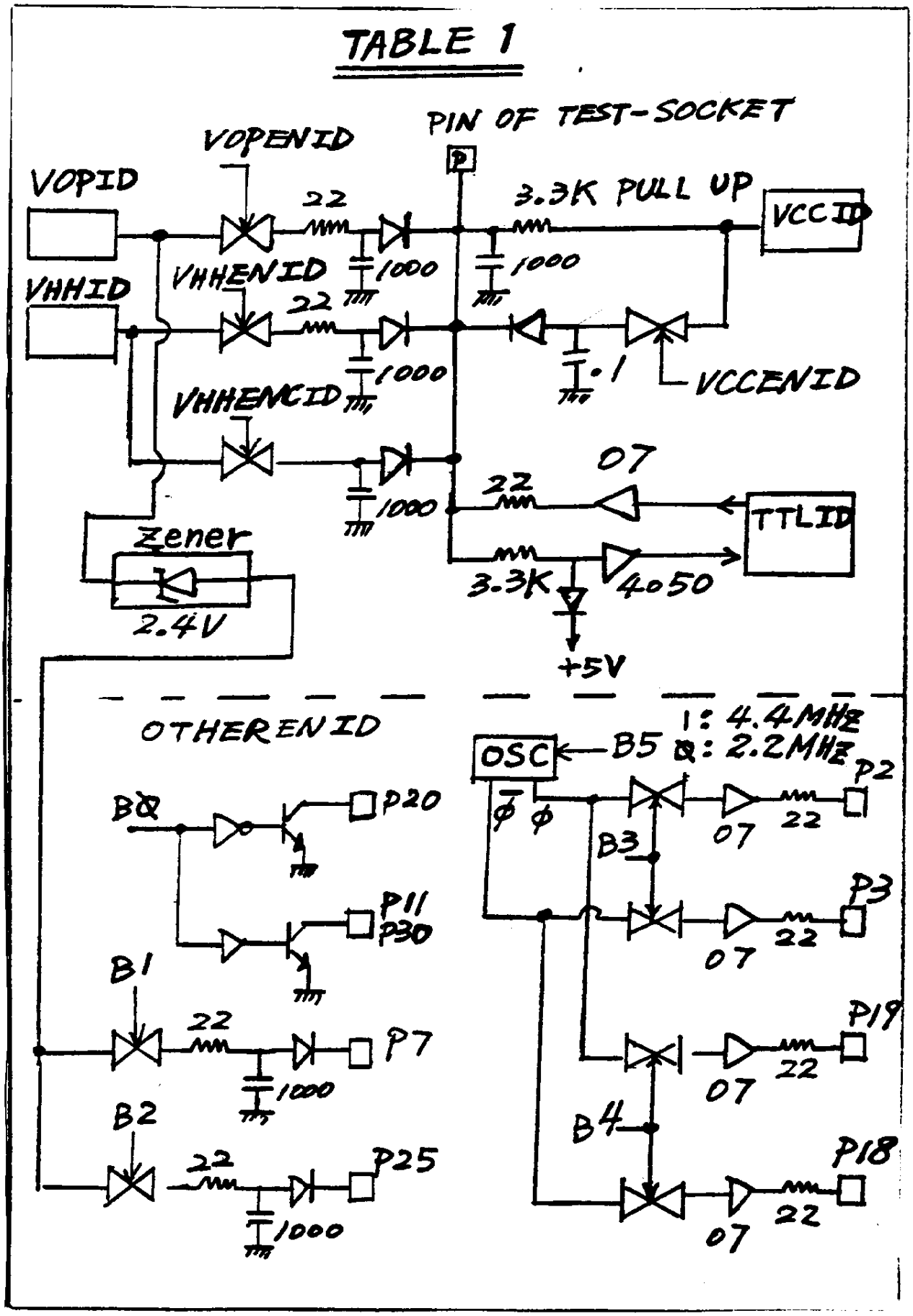
VCC drop : 0.6 v, (= 15 steps)
VHH drop : 0.6 v, (= 10 steps)
VOP drop : 0.6 v, (= 6 steps)

Example: The following code sets the #1 D/A to 21 volt:

```
outp (IDPORT, VOPID)
outp (DATAPORT, 210+6)
```

Before TTL levels can be read, or VOP, VHH, VCC voltages can be set, the user ***must*** output a high to the specified pin. Otherwise, the relevant TTL input, or the specified supply voltage will be pulled down to ground. **This will result in damage to the affected supply.**

In the Expro-40 software, we supply the source listing for TESTPRO.EXE. TESTPRO source is a good sample file for the user who wishes to develop his own software to program new devices.
TODO: Extract archive and source snippets, add to this document.



This diagram is likely more correct on the gates for P2/3, P18/19, but appears to be an earlier version of the All-03 in terms of GND programming.

Version history

June 26th, 2025:	Pulled information from archive.org, started this document
June 27th, 2025:	Pulled all schematics and PLD files from Mattieu Benoit's page
July 1st, 2025:	First public version posted to EEVBlog forum and Mikrocontroller.net