Terawins, Inc.

Advanced Information
Version 0.2

September 24, 2004

T100 Video Display Controller

Contents

1 Introduction

1.1 Features

- **Cost Effective Highly Integrated Triple ADC + + 2D Video Decoder + OSD + VBI Data Decoder+ Scaler + TCON**
  - Integrates 9-bit Triple Analog to Digital Converters (ADC) & Phase Locked Loop (PLL)
  - Scaler supports 2-D adaptive intra-field de-interlacer and non-linear 16:9 aspect ration.
  - Requires no external Frame Buffer Memory for deinterlacer.
  - Advanced On Screen Display (OSD) function
  - Programmable Timing Controller (Tcon) for Car TV applications
  - Multi-standard color decoder with 2D adaptive comb filter
  - Innovative and flexible design to reduce total system cost

Triple 9-bit Analog to Digital Converters (ADC)

- **80MSPS Conversion Rate**
  - Built-in Pre-amp, mid-level & ground clamp circuit
  - Automatic Clamp Control for CVBS, Y and C
  - Programmable Static Gain Control or Automatic Gain Control for CVBS or Y/C
  - Max Input configuration up to 9xCVBS, 3xS-video and 3xCVBS, 3xYPbPr,

Digital Video Enhancement

- **Separate Luminance and Chroma Enhancer**
  - Y Supports Luminance Peaking, DLTI, Black Level Expansion, Contrast and Brightness adjustment
  - C Supports DCTI, Saturation and Hue adjustment.

Advanced Scaling Engine

- **Two Dimensions FIR Scaler**
  - Coefficient based sharpness filters
  - 2-D edge enhancement
  - Independent vertical and horizontal scaling ratio
  - 16:9 Non-linear Aspect ratio

- **LCD Interface**
  - Provides Gamma correction for panel compensation
  - Supports image pan functions
  - Programmable Timing Controller
  - RGB Triple DAC output

- **Color Management**
  - Coef Programmable YCbCr-to-RGB Color Space Converter
  - RGB Gamma Correction

- **Built-in On Screen Display Engine**
  - 3K-word OSD SRAM memory
  - Supports font or bitmap modes
  - Supports character blinking, overlay, shadow and border functions
  - Fully programmable character mapping
  - Supports alpha blending & Zoom-in/Zoom-out function
  - Optional fonts can be stored in off-chip serial EEPROM

- **Versatile VBI Data Decoder**
  - Supports Close Caption, Wide Screen Signalling and Teletext

- **Crystal Oscillator Circuit**
  - Direct interface to a (27.0MHz) Crystal
  - Also provide a buffered clock output for external Micro-controller

- **Digital Test Pattern Generator**
  - Programmable standard & special panel burn-in test patterns
  - Support special border frame blocking mode

- **Independent Display Phase Lock Loop**
  - Generates pixel clock output to panel
  - Supports free run OSD mode

- **Serial Bus Interface**
  - Supports 2-wire (normal speed) or 4-wire (high speed) modes

- **Pulse Width Modulation Outputs**

- **Design For Testability**
  - Scan chain insertion
  - Separated analog & digital test modes

- **Power Supply: +2.5V & +3.3V**

- **Package: 100-pin TQFP**

1.2 General Description

The T100 is a highly integrated All-in-one Visual Processor that provides major cost saving solution for the portable applications. T100 has built-in high performance Triple ADCs, TCON, Triple DACs, Scaling Machine with sophisticated upscaling and downscaling algorithms. The Innovative integrated “Frame-Buffer-Less” De-interlacer can significantly reduce system cost. The T100 also integrates On Screen Display engine with 3K-word of font RAM. The device can interface to an external micro-controller through 2-wire serial bus interface.

1.3 Applications

1. 4-inch to 7-inch portable DVD or in-car TV
2. Progressive CRT TV

1.4 System Architecture

T100 Block Diagram

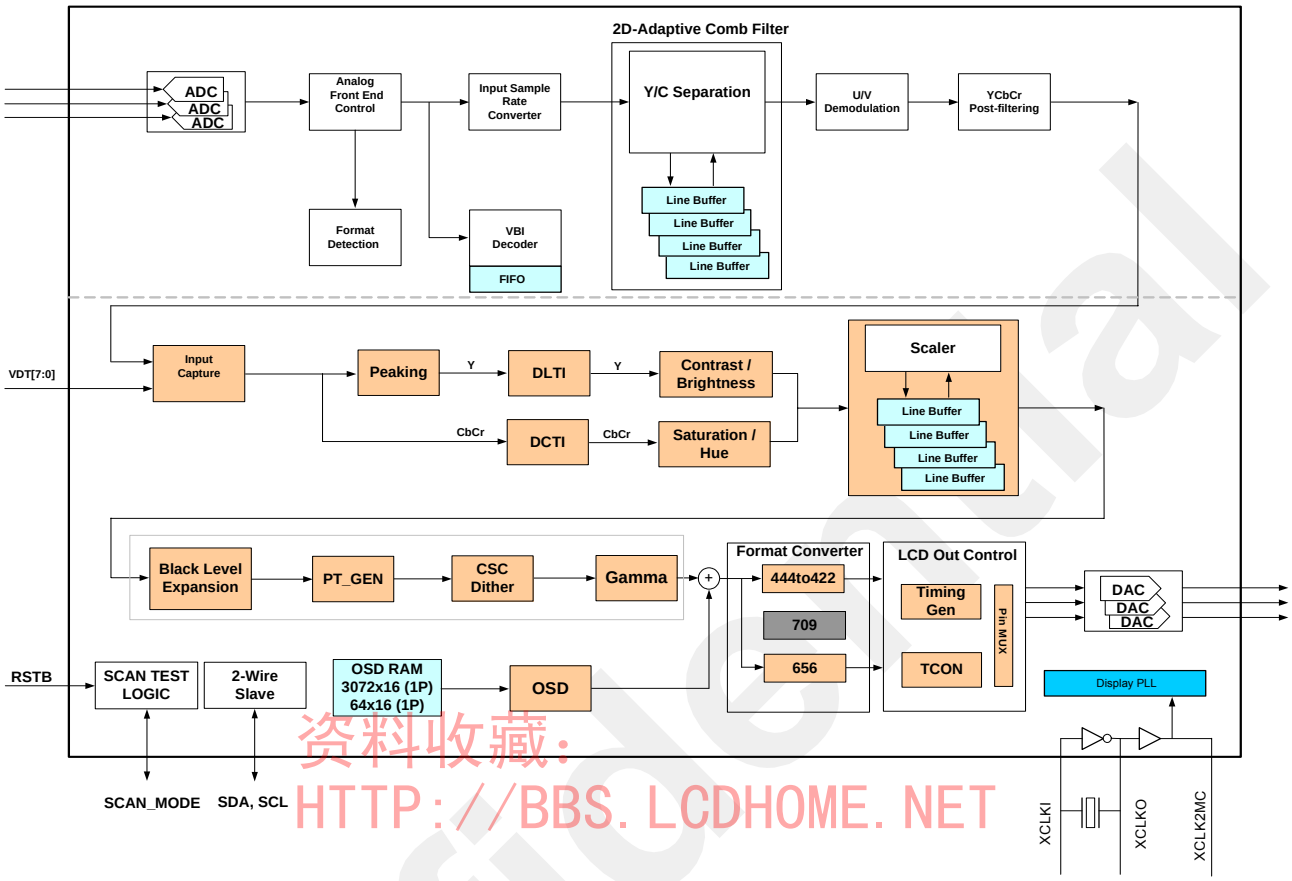


Figure1-1 System Architecture

1.5 System Configurations

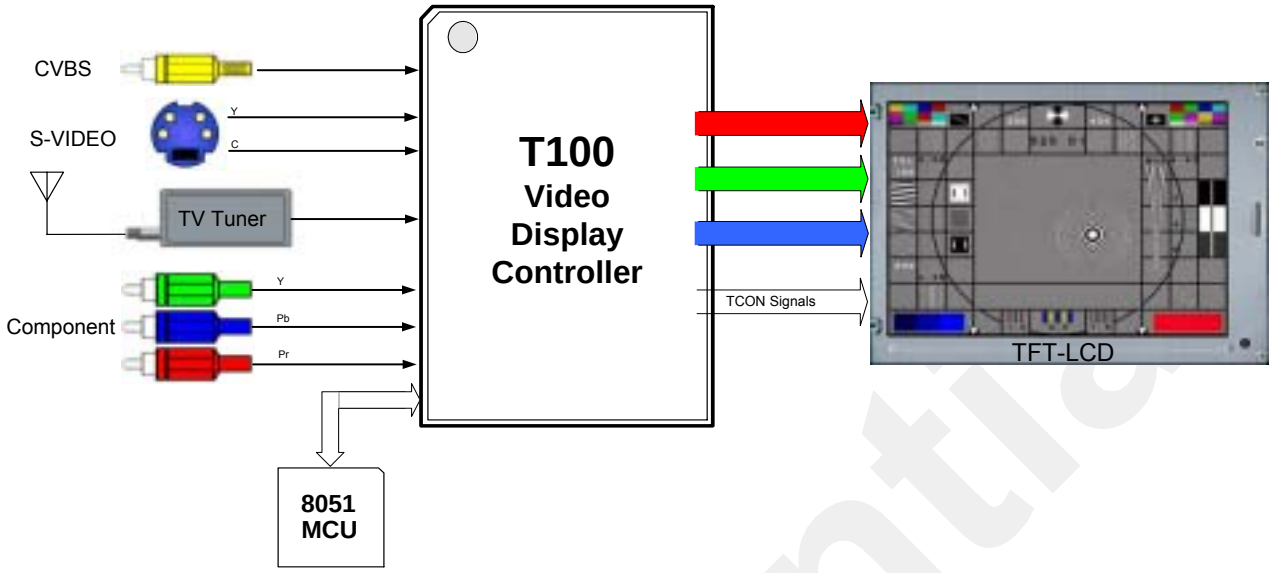


Figure 1-2 System Configurations

1.6 Pinout Diagram

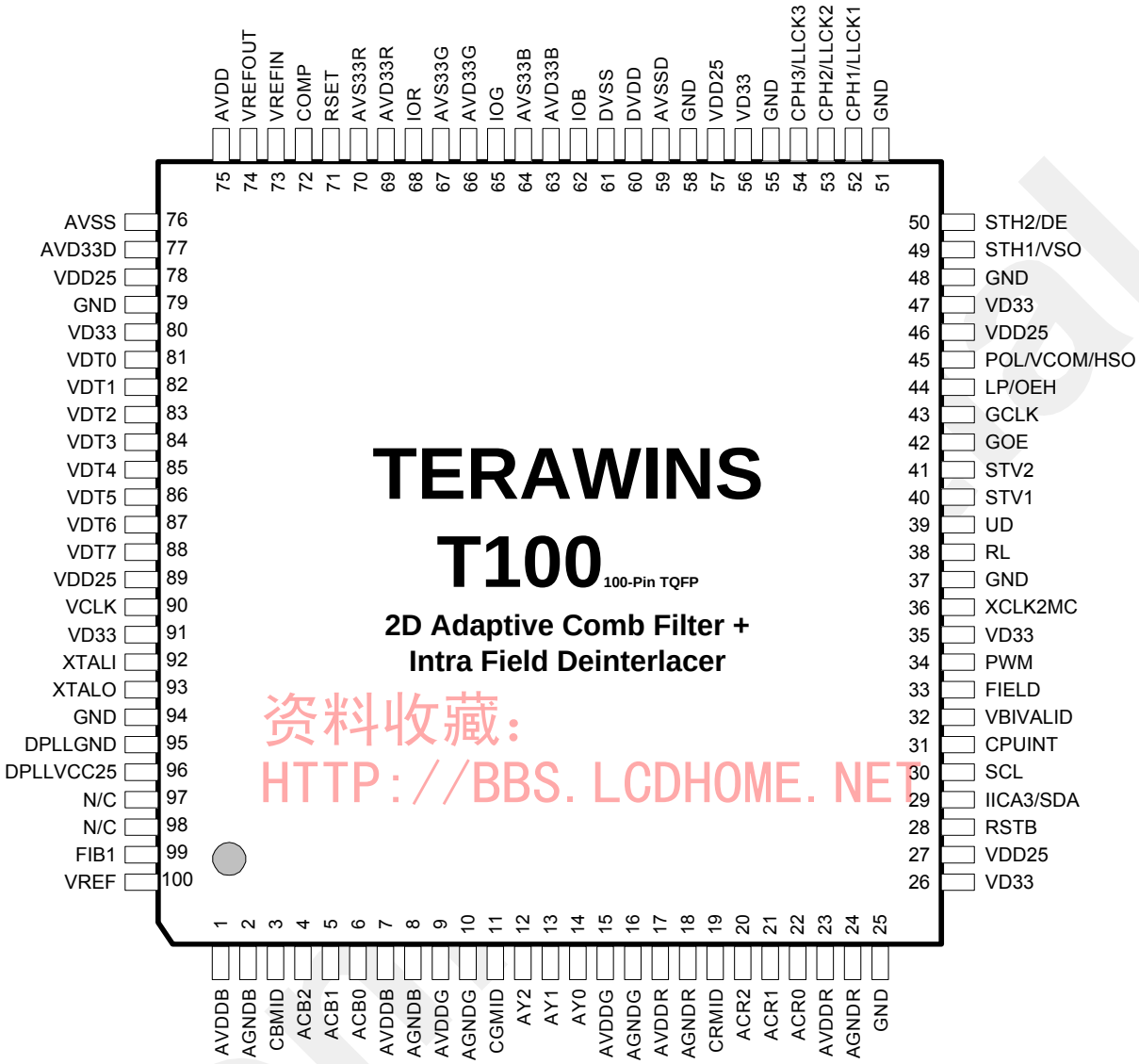


Figure1-3 Pinout Diagram

1.7 Pin Description

Table 1-1 Pin Description

Symbol	Pin #	Type	Description
Power Supplies			
VDD25	27,46,57,78, 89,96	PWR	+2.5V digital core power supply
VD33	26,35,47,56, 80,91	PWR	+3.3V digital output power supply
AVDDB	1, 7	PWR	+3.3V analog power supply for ADC channel 2
AVDDG	9, 15	PWR	+3.3V analog power supply for ADC channel 1
AVDDR	17, 23	PWR	+3.3V analog power supply for ADC channel 0
GND	25, 37,48, 51,55,58,79, 94,95	GND	Digital ground
AGNDB	2, 8	GND	Analog ground for ADC channel 2
AGNDG	10, 16	GND	Analog ground for ADC channel 1
AGNDR	18, 24	GND	Analog ground for ADC channel 0
AVD33R	69	PWR	+3.3V analog power supply for DAC channel R
AVD33G	66	PWR	+3.3V analog power supply for DAC channel G
AVD33B	63	PWR	+3.3V analog power supply for DAC channel B
AVDD	75	PWR	+2.5V Analog Power Supply for DAC
DVDD	60	PWR	+2.5V Digital Power Supply for DAC
AVD33D	77	PWR	+3.3V Analog Power Supply for DAC I/O pads
AVSS3R	70	GND	Analog ground for DAC channel R
AVSS3G	67	GND	Analog ground for DAC channel G
AVSS3B	64	GND	Analog ground for DAC channel B
AVSS	76	GND	Analog ground for DAC
DVSS	61	GND	Digital ground fro DAC
AVSSD	59	GND	Analog Ground for DAC I/O pads
Output Interface Signals			
IOR	68	AO	Channel R current output
IOG	65	AO	Channel G current output
IOB	62	AO	Channel B current output
LLCK1	52	DO	Output Data Clock
LLCK2	53	DO	Output Data Clock
LLCK3	54	DO	Output Data Clock
VSO	49	DO	Vertical Synchronization Output Control Signal.
HSO	45	DO	Horizontal Synchronization Output Control Signal.
Timing Controller Interface Signals			
STH2	50	DO	Source Driver start pulse
LP	44	DO	Latch pulse for column driver
GCLK	43	DO	Gate driver clock
GOE	42	DO	Gate driver output enable
STV1	40	DO	Gate Driver start pulse
STV2	41	DO	Gate Driver start pulse
UD	39	DO	Panel UP/Down Control
RL	38	DO	Panel Right/Left Control

Symbol	Pin #	Type	Description
2-wire serial bus Interface Signals			
SCL	30	DI	2-wire serial bus clock. Power down does not affect SCL.
SDA	29	I/O	2-wire serial bus data. Power down does not affect SDA.
Configuration interface Signals			
CPUINT	31	I/O	Internal Interrupt.
RSTB	28	DI	Whole chip reset. (Internal Pull-up)
Test Pins			
FIB1	99	AO	ADC test pin
FILED	33	DO	Field flag
VBIVALID	32	DO	VBI data valid
ADC Interface			
ACB2	4	AI	Analog input 2 of channel 2
ACB1	5	AI	Analog input 1 of channel 2
ACB0	6	AI	Analog input 0 of channel 2
AY2	12	AI	Analog input 2 of channel 1
AY1	13	AI	Analog input 1 of channel 1
AY0	14	AI	Analog input 0 of channel 1
ACR2	20	AI	Analog input 2 of channel 0
ACR1	21	AI	Analog input 1 of channel 0
ACR0	22	AI	Analog input 0 of channel 0
Video-In Interface			
VCLK	90	DI/O	ITU-656 video clock
VDT0	81	DI/O	ITU-656 video port
VDT1	82	DI/O	ITU-656 video port
VDT2	83	DI/O	ITU-656 video port
VDT3	84	DI/O	ITU-656 video port
VDT4	85	DI/O	ITU-656 video port
VDT5	86	DI/O	ITU-656 video port
VDT6	87	DI/O	ITU-656 video port
VDT7	88	DI/O	ITU-656 video port
PLL Reference Clock			
XTALI	92	DI	Output PLL reference clock input
XTALO	93	DO	Output PLL reference clock output
XCLK2MC	36	DO	Buffered XTALI for external microprocessor.
Power Management Interface Signals			
PWM	34	DO	Pulse Width Modulation for backlight control.

2 Theory of Operations

2.1 I2C Command Protocol

Before your tester writes I2C commands to T100, slave address must be set at 50h. The timing sequence can be shown as below. After 4 cycles, the tester can get started IIC commands. SDA(A3) can affect slave address. Set low for 40h. Set high for 50h.

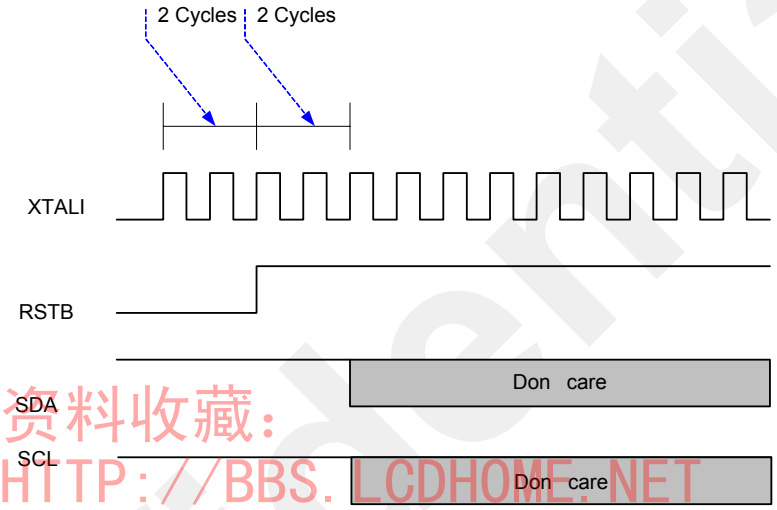


Fig 2-1 Power-up initialization

When tester issues commands to the T100, the only way the user can program the T100 is using the 2-wire serial bus protocol. This section describes the 2-wire serial bus protocol. Data transfers on the 2-wire serial bus are initiated with a START condition and are terminated with a STOP condition. Normal data on the SDA line must be stable during the high period of the SCL. The transition on the SDA is only allowed while SCL is low. The START condition is unique case and is defined by a high-to-low transition on the SDA while the SCL is high. The STOP condition is a unique case and is defined by a low-to-high transition on the SDA while the SCL is high. Each data packet on the 2-wire serial bus consists of 8 bits of data followed by an ACK bit. Data is transferred with MSB first. The transmitter releases the SDA line during the ACK bit and the receiver of data transfer must drive the SDA line low during the ACK bit to acknowledge receipt of the data. The frequency of SCL can be from 50 Khz up to 1 Mhz.

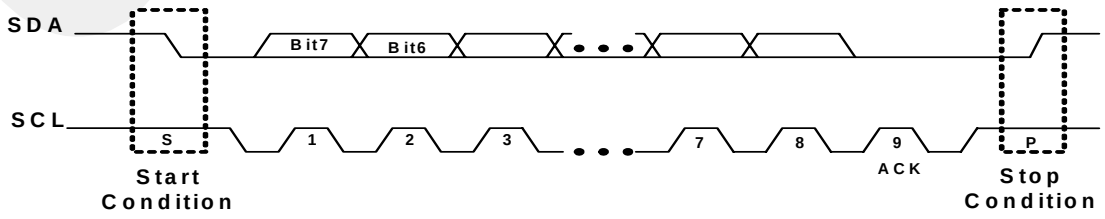


Figure 2-2 2-wire serial bus Protocol

The timing below shows a typical T100 IIC single byte write command,

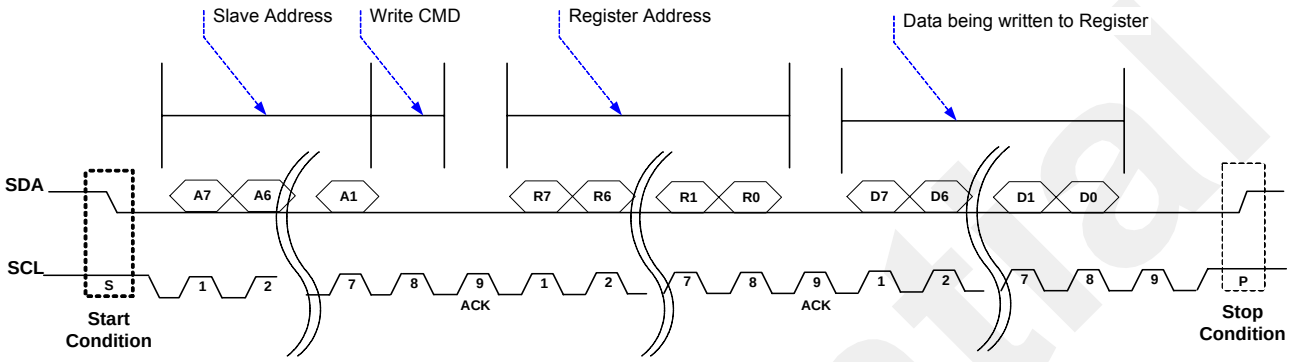


Figure 2-3 T100 IIC single byte write command

The timing below shows a typical T100 IIC single byte read command,

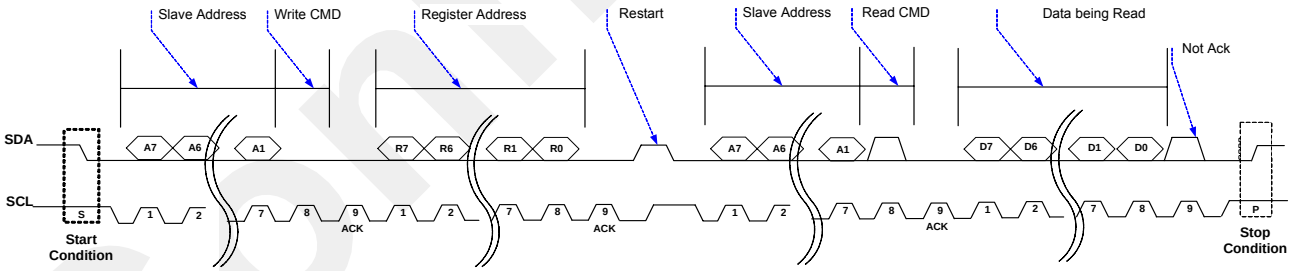


Figure 2-4 T100 IIC single byte read command

2.2 Analog Front End

T101 contains 3 ADCs in Analog Front End. Each channel of ADCs can digitalize SDTV signals from analog to digital. The figure shown below can describe how to select a SDTV signal from 3 inputs prior to ADC.

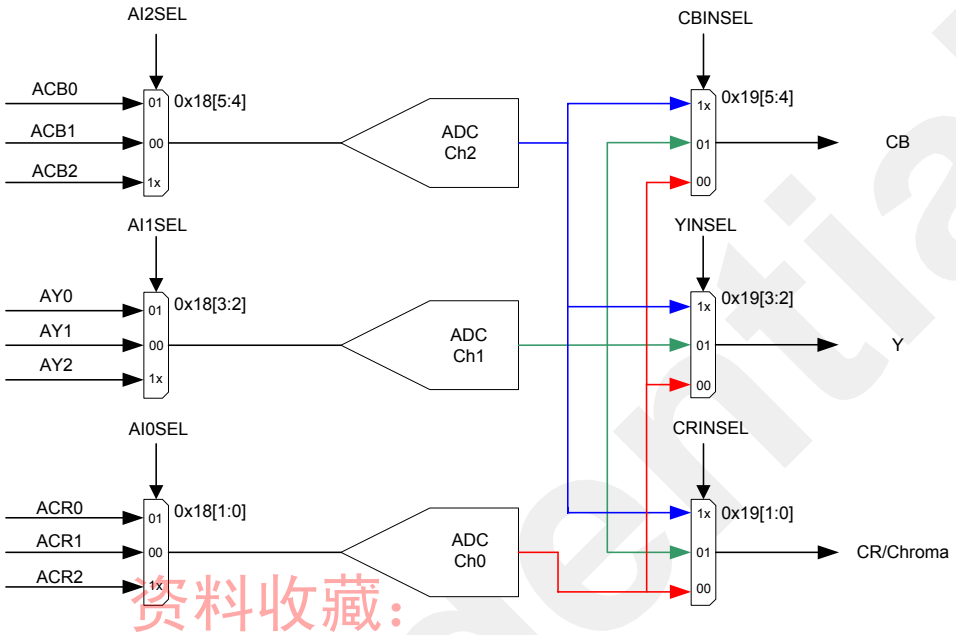


Fig 2-5 Analog Front End

2.3 Y/C Separation and Chroma Decoder

A composite video has luma(Y) and chroma(C) information mixed in the same video signal. This video signal can also be represented by the equation below,

$$CVBS = Y + U * Sin(wt) + V * \cos(wt)$$

Where $w = 2\pi f_{SC}$, f_{SC} =3.58Mhz if NTSC, f_{SC} =4.43Mhz if PAL

The figure below shows a typical composite signal. The 2-D adaptive comb filter inside T100 is designed to separate Y and C from a composite video signal.

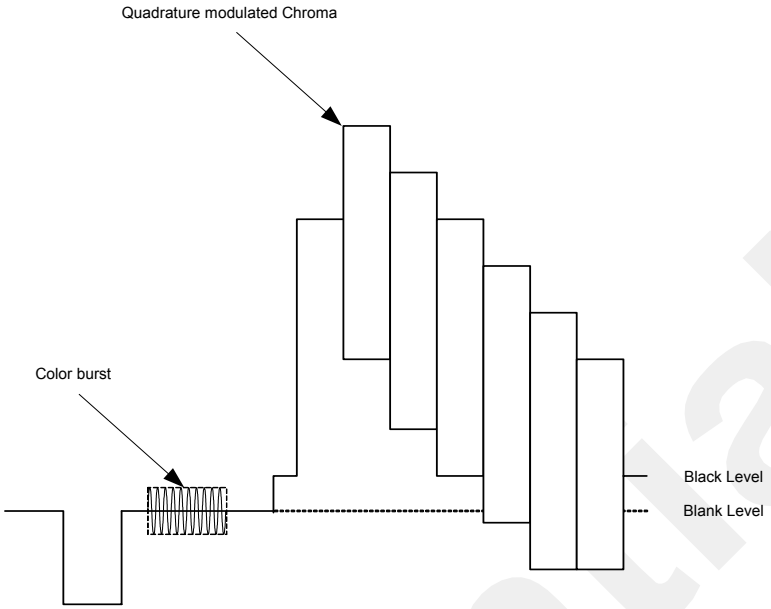


Fig 2-6

. The conventional 3-line comb filter fails to separate Y and C if there is a vertical transition. The 2-D adaptive comb filter is based on equally weighting factors that color changes along vertical and horizontal edges. Let the amount of color change along vertical and horizontal direction DCv and DCh, the weighting factor can be expressed as following equations,

$$Wh = \frac{DCv}{DCv + DCh}$$

$$Wv = \frac{DCh}{DCv + DCh}$$

By employing adaptive method, chroma can be recovered by following equation,

$$C = Ch * Wh + Cv * Wv$$

After Y/C separation, Y and C should look like waveforms shown as in following figure. Y only contains low frequency part, while C contains high frequency part which is centered around sub-carrier f_{SC}.

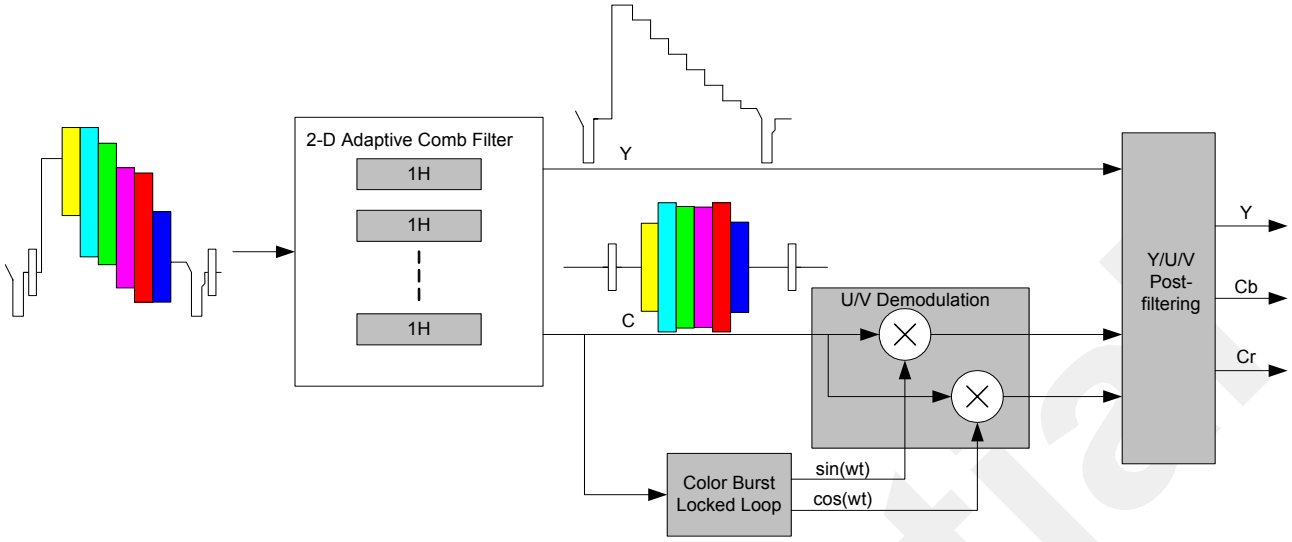


Fig 2-7

2.4 Digital Color Transient Improvement (DCTI)

Usually, a composite or S-video SDTV signal may have bandwidth limitation that causes the loss chroma detail around two different color bars. Two pictures shown below illustrate the result before and after DCTI block. Without DCTI(the upper picture), we may see color transient wider than several pixels. A slow transient edge usually blurs image. T100 DCTI algorithm can sharpen those color transient edges. The lower picture shows that chroma data is enhanced by increasing the slope of edge transient without introducing the ring effects.

Fig 2-8

2.5 Digital Luminance Transient Improvement (DLTI)

The Digital Luminance Transient Improvement is intended to sharpen luminance edge transient. The figure shown below is DLTI transfer function. DLTI doesn't increase peak-to-peak amplitude; rather it turns sloped waveforms into rectangular waveforms.

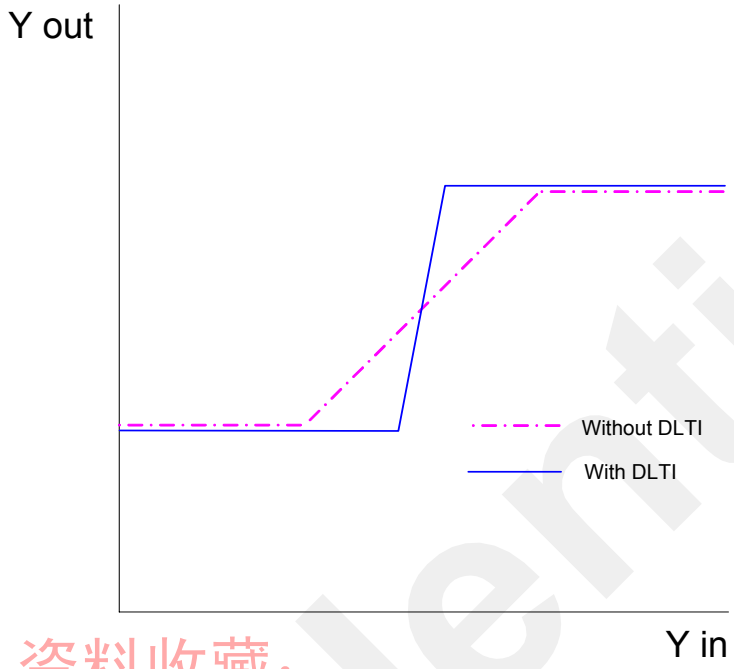


Fig 2-9

2.6 FIR Scaler

FIR Scaler can scale input H/V sizes to fit any LCD panel resolution. The flexible and independent H/V scalers allow users to program display area in 16:9 Full mode, 16:9 non-linear wide mode and 4:3 mode. FIR scaler also provides coefficient-based 2-D sharpness that can sharpen detail of picture.

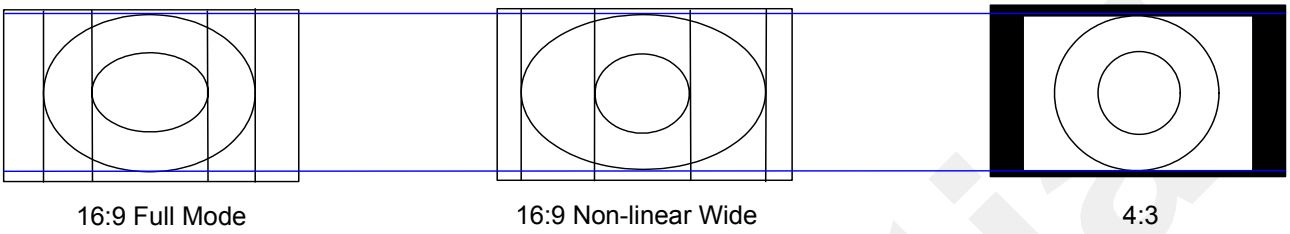


Fig 2-10

2.7 Black-Level Extension (BLE)

Black Level Expansion (BLE) can enhance image contrast that makes dark regions of image darker, while bright regions remain unchanged. The figure shown below is BLE transfer function.

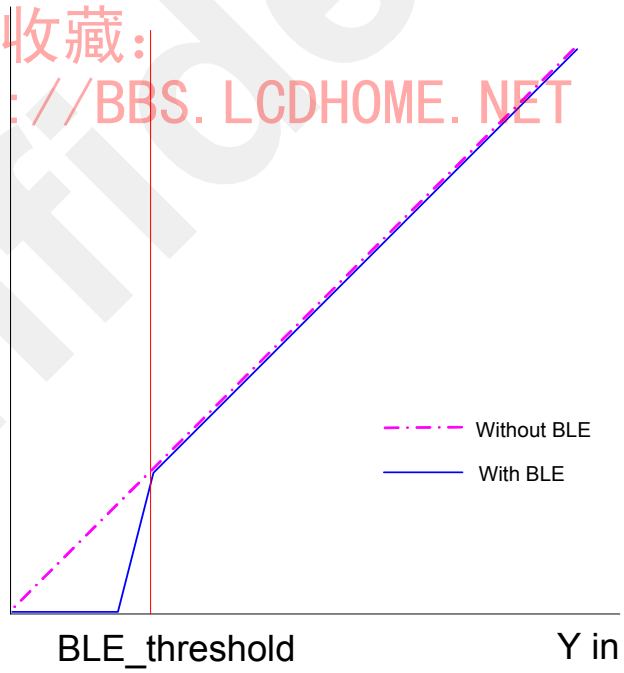


Figure 2-11 BLE

$$Yout = Yin - (Yoffset - Yin) * BLE\_Gain / 16$$

Where $Yoffset$ and BLE_Gain can be programmed by register P0_96h.

2.8 Color Space Converter

A pixel in YCbCr color space can be converted to RGB color space by using following equations,

$$R = YCoefCSC*(Y-16)+CrCoef\_R*(Cr-128)$$
$$G = YCoefCSC*(Y-16)-CrCoef\_G*(Cr-128)-CbCoef\_G*(Cb-128)$$
$$B = YCoefCSC*(Y-16)+CbCoef\_B*(Cb-128)$$

Where $YCoefCSC$ is in 1.7-bit fixed point with default 1.164. $CrCoef\_R$ in 1.7-bit fixed point with default 1.596. $CrCoef\_G$ in 0.8-bit fixed point with default 0.813. $CbCoef\_G$ in 0.8-bit fixed point with default 0.392. $CbCoef\_B$ in 2.6-bit fixed point with default 2.017

The equations shown as below correspond to a typical YCbCR-to-RGB converter. In T101, we make those coefficients adjustable.

$$R = 1.164*(Y-16)+1.596*(Cr-128)$$
$$G = 1.164*(Y-16)-0.813*(Cr-128)-0.392*(Cb-128)$$
$$B = 1.164*(Y-16)+2.017*(Cb-128)$$

2.9 Gamma Correction

The relation between input video signal and LCD panel may exist non-linear transfer function such as figure shown below,

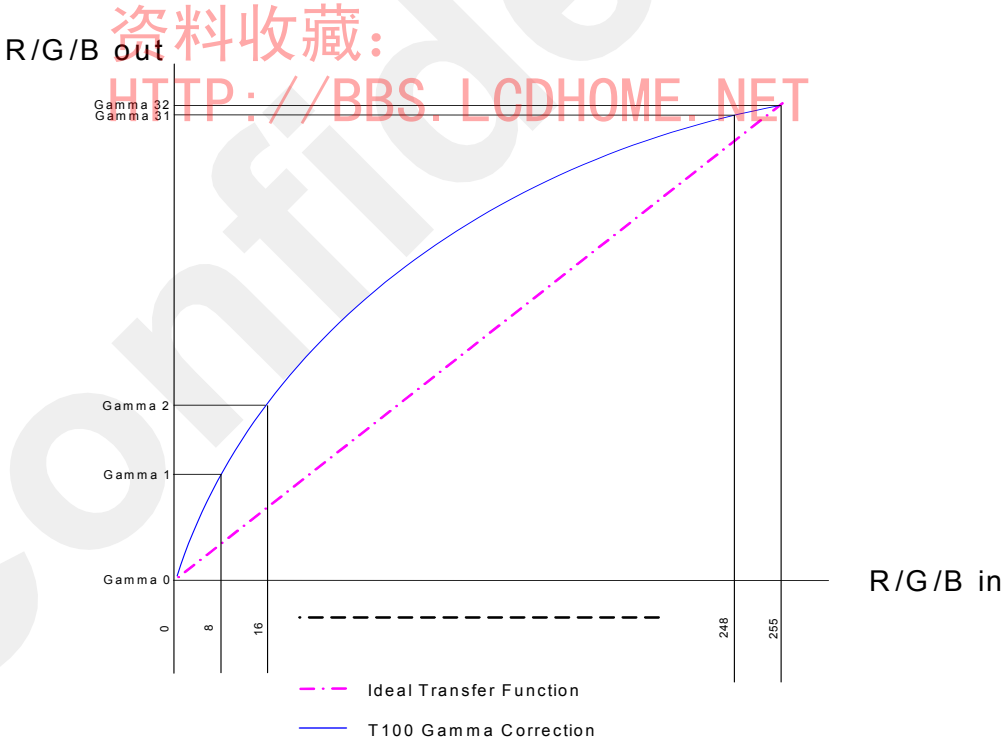


Fig 2-12

T100 uses 33-point piece-wise linear interpolation instead of RAM-based LUTs. Each point can be programmed via register at P0_93h and P0_94h.

2.10 OSD

2.10.1 OSD Access

Table 2-1 OSD Access

I/O Port	Index	Default	Description
A0h – Cfg_Index A1h – Cfg_Data	00h	00h	OSD Control Register
	01h	00h	Character Delay_1
	02h	10h	Character Delay_2
	03h	08h	Character Delay_3
	04h	09h	Character Font Size
	05h	50h	Char_RAM Base Address
	06h	00h	Character Border / Shadow Control
	07h	00h	Character Border / Shadow Color
	08h	20h	Character Height Scaling
	09h	0Ah	Blinking Control
	0Ah	00h	Bit_Map Window Size : Width/Height Upper Bits
	0Bh	80h	Bit_Map Window Size : Width
	0Ch	60h	Bit_Map Window Size : Height
	0Dh	11h	Bit_Map Dot Enlarge
	0Eh	-	OSD LUT RAM Data R/W, address automatically increased after R or W
	0Fh	00h	Char RAM Byte Access Control
	10h	00h	Window_1 Start Character Row Number / BMP Start Address LSB
	11h	00h	Window_1 End Character Row Number / BMP Start Address MSB
	12h	00h	Window_1 Start Character Column Number
	13h	00h	Window_1 End Character Column Number
	14h	00h	Window_1 Shadow Size
	1Ah	00h	Char2BP Base Address LSB
	1Bh	08h	Char2BP Base Address MSB
	1Ch	00h	Alpha Blending Control (available Revision >=02h)
	1Dh	03h	Revision ID
	1Eh	60h	Char_RAM Stop Address (available Revision >=01h)
	Other	00h	Reserved
A2h – ORAM_AL		00h	OSD RAM Low Address Port of Starting Access
A3h – ORAM_AH		00h	OSD RAM High Address Port of Starting Access
A4h – ORAM_D		00h	OSD RAM Data Port (Low Byte first, then High Byte). After two R/W, the address will be increased by 1.

2.10.2 RAM Addressing A[11:0]

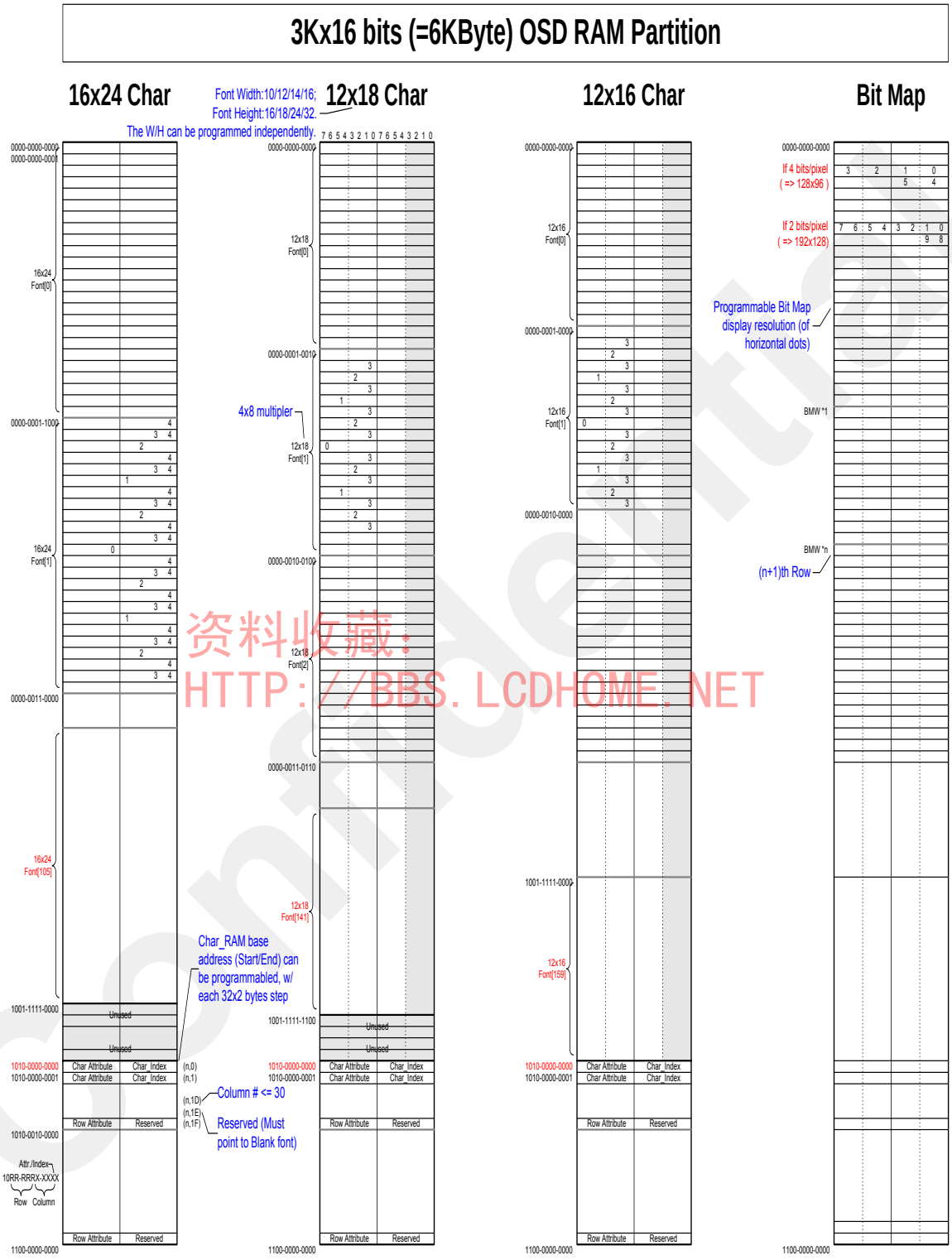


Figure 2-13 OSD RAM Partition

2.10.3 Character RAM Format

In Character Mode (contrast to Bit_Map Mode), the Characters displayed on OSD can be grouped to few rows, each row has its own row attribute (the high byte of Word #1F$_h$, ref. Section 0) which defines the behavior of current character row. And, there is maximum 30 characters in one row (Word #00$_h$ ~ #1D$_h$), each character has two bytes to define its character font number (ref. Section 0) and its colors (ref. Section 0). And the Word #1E$_h$ is reserved, which must be filled with transparent color and pointed to blank font.

2.10.3.1 Character Data **(Address to Font Select) (Default=XXXXXXXXb[1])**

Table 2-2 Character Data

7	6	5	4	3	2	1	0
CHRA[7]	CHRA[6]	CHRA[5]	CHRA[4]	CHRA[3]	CHRA[2]	CHRA[1]	CHRA[0]

Bit 7-0 CHRA[7:0] – Character Address (Index), selects the character font (i.e., 0,1,2,.. A,B,C, a,b,c,$,%,…). If the value is number N, then it selects the Nth font, and that font starting address is (N x Font_Height). The Font_Height id defined in Cfg_04h<4:3> (ref. Section 0).
Index 00h~BFh for indexing 1BP (mono colored) fonts.
Index: C0h~FFh fof indexing 2BP (color) fonts

2.10.3.2Character Attribute **(Default=XXXXXXXXb)**

Table 2-3 Character Attribute

7	6	5	4	3	2	1	0
BG_R	BG_G	BG_B	Blink	FG_R	FG_G	FG_B	FG_I

Bit 7-5 BG_R/G/B – Background R/G/B Color (Intensity=0). If all 0, then no background, i.e. transparent.
Bit 4 Blink – Enable this Character display with blinking feature. Refer to section 0 for detail blinking control.
Bit 3-0 FG_R/G/B/I or R_C2BP[3:0] – when Character Data = 00h~BFh, Foreground R/G/B/Intensity Color. If the value is set as 0000b, then there will be no foreground, i.e. transparent.
when Character Data = C0h~FFh, these 4 bits act as a pointer to one of 16 the Character 2BP color sets

2.10.3.3Row Attribute **(Default=XXXXXXXXb)**

Table 2-4 Row Attribute

7	6	5	4	3	2	1	0
RGAP_BG	RGAP[4]	RGAP[3]	RGAP[2]	RGAP[1]	RGAP[0]	CHS	CWS

Bit 7 RGAP_BG – Color Select of Row Gap. Set 1 for selecting the same color of background of current row character, 0 for selecting transparent color.
Bit 6-2 RGAP[4:0] – Row Gap (=Row Space). Inserted range is 4 x (31$_d$~0) scan lines before current Row.
Bit 1 CHS – Character Height Select. Set 1 for double height, 0 for single height.
Bit 0 CWS – Character Width Select. Set 1 for double width, 0 for single width. When set to 1, only the even numbered characters will be shown, odd numbered characters are skipped.

2.10.4 Configuration Register

2.10.4.1 Cfg_00h – OSD Control Register **(Default=00h => 18h)**

Table 2-5 Cfg_00h – OSD Control Register

7	6	5	4	3	2	1	0
OSD_En	Bit_Map	Bit2PP	Reserved	Reserved	Early_hDE	DCLK[1]	DCLK[0]

Bit 7 OSD_En – Enabling the OSD function. Set 1 for enabling, 0 for disabling OSD.
Bit 6 Bit_Map – Select Bit Mapped OSD display mode. Set 1 for Bit_Map Mode, 0 for Character Mode.
Bit 5 Bit2PP – Two bits per Pixel for Bit_Map mode. Set 1 for 2 Bits/Pixel, 0 for 4 Bits/Pixel.
Bit 4-3 Reserved.
Bit 2 Early_hDE – let OSD a little shift left.
Bit 1-0 DCLK[1:0] – Dot Clock, is divided from Pixel Clock. 00b for no divide, 01b for divided by 2, 10b for divided by 3, 11b for divided by 4 (11b is reserved and not recommended). These two bits are used for widen global OSD characters.

[1] The “b” after value means Binary; “d” means Decimal; “h” means Hex-Decimal.

2.10.4.2 Cfg_01h – Character Delay_1 **(Default=00h)**

Table 2-6 Cfg_01h – Character Delay_1

7	6	5	4	3	2	1	0
Reserved	VERTD[10]	VERTD[9]	VERTD[8]	Reserved	HORD[10]	HORD[9]	HORD[8]

Bit 7, 3 Reserved. (R/W)
Bit 6-4 VERTD[10:8] – Vertical Starting Position (Upper bits) of Character displaying. These bits with Cfg_03h, total 11 bits, become 2048 steps, with an increment one pixel per step for each field.
Bit 2-0 HORD[10:8] – Horizontal Starting Position (Upper bits) of Character displaying. These bits with Cfg_02h, total 11 bits, become 2048 steps, with an increment one pixel per step.

2.10.4.3 Cfg_02h – Character Delay_2 **(Default=10h)**

Table 2-7 Cfg_02h – Character Delay_2

7	6	5	4	3	2	1	0
HORD[7]	HORD[6]	HORD[5]	HORD[4]	HORD[3]	HORD[2]	HORD[1]	HORD[0]

Bit 7-0 HORD[7:0] – Horizontal Starting Position (Lower bits) of Character displaying. This register with Cfg_01h<2:0>, total 11 bits, become 2048 steps, with an increment one pixel per step.

2.10.4.4 Cfg_03h – Character Delay_3 **(Default=08h)**

Table 2-8 Cfg_03h – Character Delay_3

7	6	5	4	3	2	1	0
VERTD[7]	VERTD[6]	VERTD[5]	VERTD[4]	VERTD[3]	VERTD[2]	VERTD[1]	VERTD[0]

Bit 7-0 VERTD[7:0] – Vertical Starting Position (Lower bits) of Character displaying. This register with Cfg_01h<6:4>, total 11 bits become 2048 steps, with an increment one line per step for each field.

2.10.4.5 Cfg_04h – Character Font Size **(Default=09h)**

Table 2-9 Cfg_04h – Character Font Size

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	FontH[1]	FontH[0]	Reserved	FontW[1]	FontW[0]

Bit 7-5 Reserved. (R/W)
Bit 4-3 FontH [1:0] – Font Size (Height) Select. Set 00b for 16 lines, 01b for 18 lines, 10b for 24 lines, 11b for 32 lines. (default is 18 lines)
Bit 2-0 FontW [1:0] – Font Size (Width) Select. Set 00b for 10 dots, 01b for 12 dots, 10b for 14 dots, 11b for 16 dots. (default is 12 dots)

2.10.4.6 Cfg_05h – Char_RAM Base Address **(Default=50h)**

Table 2-10 Cfg_05h – Char_RAM Base Address

7	6	5	4	3	2	1	0
Reserved	CharBA[6]	CharBA[5]	CharBA[4]	CharBA[3]	CharBA[2]	CharBA[1]	CharBA[0]

Bit 7 Reserved. (R/W)
Bit 6-0 CharBA[6:0] – Programmable Character RAM Base Address. Those 7 bits become 128 steps, each step is 64 bytes (one Character Row include Char_Index, Char_Attr, Row_Attr; i.e. 31 column maximum for each Row). The actual address will be RRRR-RRRX-XXXX (The RRRR-RRR means the value of CharBA[6:0]; the X-XXXX is the nth Char Column. For trading off Font number and Character number in a single RAM (this version is 3Kx16 bits), user should carefully setting this register.

2.10.4.7 Cfg_06h – Character Border / Shadow Control **(Default=00h)**

Table 2-11 Cfg_06h – Character Border / Shadow Control

7	6	5	4	3	2	1	0
BDSEN	CSHD	ES_Only	Reserved	BDSH[1]	BDSH[0]	BDSW[1]	BDSW[0]

Bit 7 BDSEN – Character Border/Shadow Enable. 1 for enabling Border or Shadow (depends on CSHD setting, the Cfg_06h<6>).
Bit 6 CSHD – Character Shadow Selected. If BDSEN (Cfg_06h<7>) is 0, then no Border/Shadow displaying for Character; it BDSEN=1, then set this CSHD as 1 for selecting Shadow, 0 for selecting Border.
Bit 5 ES_Only – Shadow on Eastern South side of the displayed foreground dot only (due to the Northern West light source), if set to 1; else the shadow also exist on the both east & south side of displayed foreground dot.
Bit 4 Reserved.
Bit 3-2 BDSH [1:0] – Character Border/Shadow Height. Set 00b for 1 line, 01b for 2 lines, 10b for 3 lines, 11b for 4 lines. The BDSH[1:0] value must <= DCLK[1:0]; Only 00b (one line height) available in current version.
Bit 1-0 BDSW [1:0] – Character Border/Shadow Width. Set 00b for 1 pixel, 01b for 2 pixels, 10b for 3 pixels, 11b for 4 pixels. The BDSW[1:0] value must <= CHD[2:0]; Only 00b (one pixel width) available in current version.

2.10.4.8 Cfg_07h – Character Border / Shadow Color & Output Delay **(Default=00h)**

Table 2-12 Cfg_07h – Character Border / Shadow Color & Output Delay

7	6	5	4	3	2	1	0
BDS_R	BDS_G	BDS_B	BDS_Gray	Reserved	Reserved	Reserved	Reserved

Bit 7-4 BDS_R/G/B/Gray – Character Border (or Shadow) R/G/B color and Gray level select. When BDS_Gray=1, select 8 gray levels, else, select half the R/G/B value (Intensity=0) of OSD LUT color addressed by BDS_R/G/B. Note, these four bits = 0001 for black color, 0000 for half Character Background color.
Bit 3-0 Reserved.

2.10.4.9 Cfg_08h – Character Height Control **(Default=20h)**

Table 2-13 Cfg_08h – Character Height Control

7	6	5	4	3	2	1	0
CHD[2]	CHD[1]	CHD[0]	Reserved	Reserved	Reserved	Reserved	Reserved

Bit 7-0 CHD[2:0] – Character height duplicate, select the duplicate numbers of each lines (16/18/24/32). The CHD[2:0] must >= 1.
Bit 4-0 Reserved.

2.10.4.10 Cfg_09h – Blinking Control **(Default=0Ah)**

Table 2-14 Cfg_09h – Blinking Control

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	BCLK[1]	BCLK[0]	Duty[1]	Duty[0]

Bit 7-4 Reserved. (R/W)
Bit 3-2 BCLK[1:0] – Blinking Frequency Select (internal 4x BCLK for Blinking State Machine). Set 00b for Refresh Rate /16; 01b for 1/32; 10b for 1/64; 11b for 1/128.
Bit 1-0 Duty[1:0] – For adjusting the blinking duty cycle, Set:
00b for Global Blink Off, i.e., 0% Background, 100% OSD.
01b for 25% Background, 75% OSD.
10b for 50% Background, 50% OSD.
11b for 75% Background, 25% OSD.

2.11.4.11 Cfg_0Ah – Bit_Map Window Size: Width/Height Upper Bits **(Default=00h)**

Table 2-15 Cfg_0Ah – Bit_Map Window Size

7	6	5	4	3	2	1	0
Reserved	BMH[10]	BMH[9]	BMH[8]	Reserved	BMW[10]	BMW[9]	BMW[8]

Bit 7, 3 Reserved. (R/W)
Bit 6-4 BMH[10:8] – Bit Map Window Height Upper bits (only available in Bit_Map mode). Please refer to Cfg_0Ch for detail. User must be careful of the OSD RAM size limitation.
Bit 2-0 BMW[10:8] – Bit Map Window Width Upper bits (only available in Bit_Map mode). Please refer to Cfg_0Bh for detail. User must be careful of the OSD RAM size limitation.

2.10.4.12 Cfg_0Bh – Bit_Map Window Size: Width **(Default=80h)**

Table 2-16 Cfg_0Bh – Bit_Map Window Size: Width

7	6	5	4	3	2	1	0
BMW[7]	BMW[6]	BMW[5]	BMW[4]	BMW[3]	BMW[2]	BMW[1]	BMW[0]

Bit 7-0 BMW[7:0] – Bit Map Window Width Lower bits (only available in Bit_Map mode This register combined with Cfg_0Ah<2:0> and become 11 bits, i.e., 2047 steps (value 000h is not valid), each step is 4 or 8 dots depends on Bit2PP (Cfg_00h<5>) setting. When Bit2PP=0 (i.e., 4 bits/pixel), each step is 4 dots. When Bit2PP=1 (i.e., 2 bits/pixel), each step is 8 dots. User must be careful of the OSD RAM size limitation.

2.10.4.13 Cfg_0Ch – Bit_Map Window Size: Height **(Default=60h)**

Table 2-17 Cfg_0Ch – Bit_Map Window Size: Height

7	6	5	4	3	2	1	0
BMH[7]	BMH[6]	BMH[5]	BMH[4]	BMH[3]	BMH[2]	BMH[1]	BMH[0]

Bit 7-0 BMH[7:0] – Bit Map Window Height Lower bits (only available in Bit_Map mode). This register combined with Cfg_0Ah<6:4> and become 11 bits, i.e. 2048 height step: all 0 for 2048 lines, 11'h001 for 1 line, 11'h7FF for 2047 lines. User must be careful of the OSD RAM size limitation.

2.10.4.14 Cfg_0Dh – Bit_Map Dot Enlarge **(Default=11h)**

Table 2-18 Cfg_0Dh – Bit_Map Dot Enlarge

7	6	5	4	3	2	1	0
BMBigH[3]	BMBigH[2]	BMBigH[1]	BMBigH[0]	BMBigW[3]	BMBigW[2]	BMBigW[1]	BMBigW[0]

Bit 7-4 BMBigH[3:0] – Bit Map Window Vertical Enlarge (only available in Bit_Map mode). Set 0000b for 1 line per dot, 0001b for 2 lines per dot, 0010b for 3 lines, …, 1111b for 16 lines per dot.
Bit 3-0 BMBigW[3:0] – Bit Map Window Horizontal Enlarge (only available in Bit_Map mode). Set 0000b for 1 pixel per dot, 0001b for 2 pixels per dot, 0010b for 4 pixels per dot, 0011b for 6 pixels per dot, …, 1111b for 30 pixels per dot.

2.10.4.15 Cfg_0Eh – OSD Color LUT RAM Data Port **(No Default)**

Table 2-19 Cfg_0Eh – OSD Color LUT RAM Data Port

7	6	5	4	3	2	1	0
LUT_D[7]	LUT_D[6]	LUT_D[5]	LUT_D[4]	LUT_D[3]	LUT_D[2]	LUT_D[1]	LUT_D[0]

Bit 7-0 LUT_D[7:0] –The data will be written to (or read from) OSD Color LUT RAM. After each Read or Write access to LUT RAM, then the LUT address will be increased automatically.
Note: Whenever the Configuration Index is programmed from other index value to 0Eh, the OSD Color LUT RAM becomes access capable and the address pointer is reset to 0 (the starting byte). In other words, whenever the index value is programmed to non-0Eh value, the OSD Color LUT RAM can not be access, and the pointer always kept at 0.

Note: The order to fill LUT RAM is:

1. LUT[0]_Green/Blue
2. LUT[0]_0000b/Red
3. LUT[1]_Green/Blue
4. LUT[1]_0000b/Red
5. LUT[0]_Green/Blue
6. ----

31. LUT[15]_Green/Blue
32. LUT[15]_0000b/Red
33. LUT[0]_Green/Blue (wrap to beginning)
34. LUT[0]_0000b/Red

2.10.4.16 Cfg_0Fh – OSD Color LUT RAM Data Port **(No Default)**

Table 2-20 Cfg_0Fh – OSD Color LUT RAM Data Port

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRAM_ByteAccess[1:0]	

Bit 7-2 Reserved.
Bit 1-0 When CRAM_ByteAccess[1:0] = 0X: Word (2-bytes) R/W; 10: Low byte only; 11: High byte only

2.10.4.17 Cfg_10h - Window_1 Start Character Row Number **(Default=00h)**

Table 2-21 Cfg_10h - Window_1 Start Character Row Number

7	6	5	4	3	2	1	0
W1EN	W1_INT	W1RS[5]	W1RS[4]	W1RS[3]	W1RS[2]	W1RS[1]	W1RS[0]

Bit 7 W1EN – Window_1 Enable. 1 for enabled, 0 for disabled. Window_1 only can be enabled in Character mode, i.e. it is always disabled in Bit_Map mode.
Bit 6 W1_INT – Window_1 Intensity. 1 for selecting high intensity color, 0 for low intensity color.
Bit 5-0 W1RS[5:0] / BMP_StartA[5:0] – When in character mode, these bits defined as Window_1 Start @ nth Row (User must be careful of Character row number vary due to programmable Char_RAM base address). When in Bit_Map mode, these bits define the LSB of Bit mapped image starting address.

2.10.4.18 Cfg_11h - Window_1 End Character Row Number **(Default=00h)**

Table 2-22 Cfg_11h - Window_1 End Character Row Number

7	6	5	4	3	2	1	0
W1SEN	W1S_Gray	W1RE[5]	W1RE[4]	W1RE[3]	W1RE[2]	W1RE[1]	W1RE[0]

Bit 7 W1SEN – Window_1 Shadow function enabling. 1 for enabled, 0 for disabled. If HalfTone=1, the color of Window Shadow is always the half R/G/B value of background; otherwise, color will be the pre-defined
Bit 6 W1S_Gray – Window_1 Gray level select. Refer to W1S_R/G/B setting for detail.
Bit 5-0 W1RE[5:0] / BMP_StartA[11:6] – When in character mode, these bits defined as Window_1 End @ nth Row(User must be careful of Character row number vary due to programmable Char_RAM base address). When in Bit_Map mode, these bits define the MSB of Bit mapped image starting address.

2.10.4.19 Cfg_12h - Window_1 Start Character Column Number **(Default=00h)**

Table 2-23 Cfg_12h - Window_1 Start Character Column Number

7	6	5	4	3	2	1	0
W1_R	W1_G	W1_B	W1CS[4]	W1CS[3]	W1CS[2]	W1CS[1]	W1CS[0]

Bit 7-5 W1_R/G/B – Window_1 R/G/B color.
Bit 4-0 W1CS[4:0] – Window_1 Start @ nth Column, available value of n is 29d~0. (n>29d is reserved)

2.10.4.20 Cfg_13h - Window_1 End Character Column Number **(Default=00h)**

Table 2-24 Cfg_13h - Window_1 End Character Column Number

7	6	5	4	3	2	1	0
W1S_R	W1S_G	W1S_B	W1CE[4]	W1CE[3]	W1CE[2]	W1CE[1]	W1CE[0]

Bit 7-5 W1S_R/G/B – Window_1 Shadow Color of R/G/B. During display shadow area, the SHADOW output will be high, it can be used to select another 8-level gray (000b black ~ 111b light Gray) for OSD LUT (if W1S_Gray=1) or used as a half R/G/B value (Intensity=0) selection in last phase (if W1S_Gray=0).
Bit 4-0 W1CE[4:0] – Window_1 End @ nth Column, available value of n is 29d~0. (n>29d is reserved)

2.10.4.21 Cfg_14h - Window_1 Shadow Size **(Default=00h)**

Table 2-25 Cfg_14h - Window_1 Shadow Size

7	6	5	4	3	2	1	0
W1SH[3]	W1SH[2]	W1SH[1]	W1SH[0]	W1SW[3]	W1SW[2]	W1SW[1]	W1SW[0]

Bit 7-4 W1SH[3:0] – Window_1 Shadow Height. The Shadow height = W1SH[3:0] * 2 (- 0/1) lines and must <= FontH setting.
Bit 3-0 W1SW[3:0] – Window_1 Shadow Width. The Shadow Width = W1SW[3:0] * 2 pixels and must <= FontW setting.

2.10.4.22 Cfg_1Ah – Char2BP Font Base Address -1 **(Default=00h)**

Table 2-26 Cfg_1Ah – Char2BP Font Base Address -1

7	6	5	4	3	2	1	0
C2BP_BA[7]	C2BP_BA[6]	C2BP_BA[5]	C2BP_BA[4]	C2BP_BA[3]	C2BP_BA[2]	C2BP_BA[1]	C2BP_BA[0]

Bit 7-0 2BP Characters Base Address LSB.

2.10.4.23 Cfg_1Bh – Char2BP Font Base Address -2 **(Default=08h)**

Table 2-27 Cfg_1Bh – Char2BP Font Base Address -2

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	C2BP_BA[11]	C2BP_BA[10]	C2BP_BA[9]	C2BP_BA[8]

Bit 7-0 2BP Characters Base Address MSB.

2.10.4.24 Cfg_1Ch – Alpha Blending Control **(Default=00h)**

Table 2-28 Cfg_1Ch – Alpha Blending Control

7	6	5	4	3	2	1	0
FG_NoAB	Reserved	Reserved	Reserved	AB_Set[3]	AB_Set[2]	AB_Set[1]	AB_Set[0]

Bit 7 FG_NoAB – OSD Character ForeGround portion will be exclusive to be blended if set to one. Default is 0 as no matter the current displayed pixels are in Character foreground or border/shadow or background or in OSD window, all will be alpha blended with original Video source.

Bit 6-4 Reserved. (R/W)

Bit 3-0 AB_Set[3:0] – Alpha Blending percentage (n/16).
If set 0000b, alpha blending is disabled (0/16 * Original Video Source + 16/16 * OSD display);
If set 0001b, blending as 1/16 * Original Video Source + 15/16 * OSD display;
If set N, blending as N/16 * Original Video Source + (16-N)/16 * OSD display;

2.10.4.25 Cfg_1Dh – Revision ID

Table 2-29 Cfg_1Dh – Revision ID

7	6	5	4	3	2	1	0
RID[7]	RID[6]	RID[5]	RID[4]	RID[3]	RID[2]	RID[1]	RID[0]

Bit 7-0 Revision ID (Read Only).
03h for PW103, add ORAM burst write feature.

2.10.4.26 Cfg_1Eh – Char_RAM Stop Address **(Default=60h)**

Table 2-30 Cfg_1Eh – Char_RAM Stop Address

7	6	5	4	3	2	1	0
Reserved	CharEA[6]	CharEA[5]	CharEA[4]	CharEA[3]	CharEA[2]	CharEA[1]	CharEA[0]

Bit 7 Reserved. (R/W)

Bit 6-0 CharEA[6:0] – Programmable Character RAM Stop/End Address (Available if Revision ID >= 0h). Those 7 bits become 128 steps, each step is 64 bytes. The actual stop address will be RRRR-RRRX-XXXX (The RRRR-RRR means the value of CharEA[6:0]; the X-XXXX is the nth Char Column. and OSD will be displayed for Character Row >= CharBA and < CharEA.

2.10.5 Functional Description

2.10.5.1 Host Access OSD RAM

2.10.5.1.1 Writing Data

The OSD RAM size is 3Kx16, i.e., 3K word with each word is 2 bytes. The host interface is 8-bit data width, so whenever the host writes 2 times (one for data low byte, the other for data high byte) then it becomes one write with 16-bit data to OSD RAM.
Two methods to read/write OSD RAM data:

1. The original one (for all version)

   The ORAM_DL (OSD module base address + 04h) port is a temporary data port for latching lower byte of OSD RAM writing data when the host want to program Font or Character, Attribute, BMP values.
   The RAM Data Write Strobe is the Host Write to ORAM_DH (OSD module base address + 05h). Each time the host write to ORAM_DH port, it becomes a RAM write strobe with current 8 bits data and latched ORAM_DL data, total 16 bits, to OSD RAM.

2. The Burst method (for Revision number >= 02h)

   The ORAM_DL (OSD module base address + 04h) port when writing in the $1^{st}/3^{rd}/5^{th}/7^{th}$ ..times, it will latch lower byte of OSD RAM writing data when the host want to program Font or Character, Attribute, BMP values; and when writing $2^{nd}/4^{th}/6^{th}/8^{th}$ … times, it will use this 8bits data as high byte and write both two bytes to OSD RAM.

2.10.5.1.2 Reading Data

Whenever the host access the OSD RAM, the lower byte of current OSD RAM accessing data (the current RAM address pointer may be the host programmed pointer in ORAM_AL (OSD module base address + 02h) / ORAM_AH (OSD module base address + 03h) during non OSD display or the current OSD display information during OSD displaying period.
The OSD RAM pointer will not be increased when the host read ORAM_DL port, but it will be increased after access ORAM_DH port.

2.10.5.1.3 Access Address

The OSD RAM access pointer is programmed by the host write access to ORAM_AL and ORAM_AH ports. The OSD RAM size is 3Kx16, so the pointer is required to cover 3K words, i.e., 12 address lines => A[11:0]. When the host read these ORAM_AL/ORAM_AH ports, the pointer value reflects the current OSD RAM accessing pointer.

2.10.5.2 OSD Displaying in Character Mode

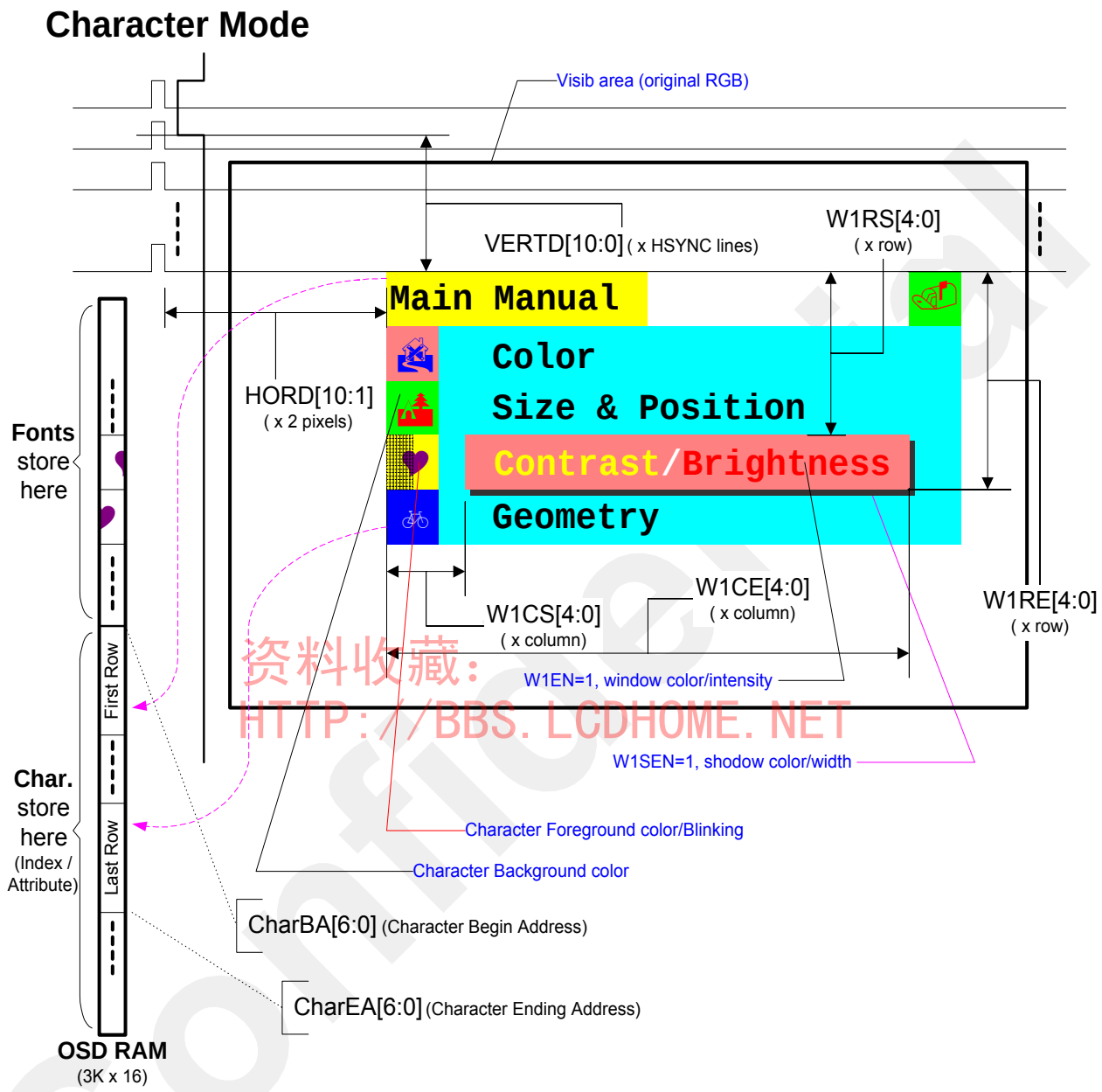


Figure 2-14

2.10.5.3 OSD LUT Color Mapping

OSD Color LUT RAM

Character Mode (Char/Window) **Character Mode (Window Shadow)**

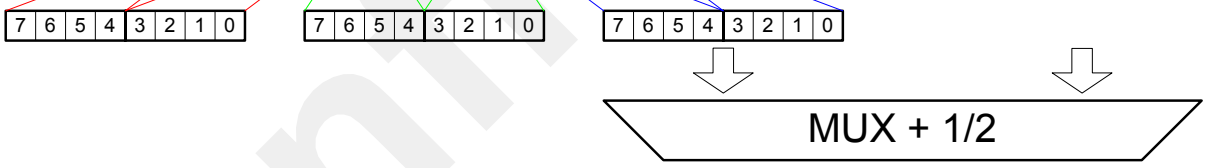
16x12 RAM

Color Value				Null				Red				Green				Blue			
R	G	B	Int	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0					11b				10b				01b			
0	0	0	1																
0	0	1	0																
0	0	1	1																
0	1	0	0																
0	1	0	1																
0	1	1	0																
0	1	1	1																
1	0	0	0																
1	0	0	1																
1	0	1	0																
1	0	1	1																
1	1	0	0																
1	1	0	1																
1	1	1	0																
1	1	1	1																

For BMP color remap

For Window Shadow with W1S_Gray=1, all R/G/B color = {W1S_R, W1S_G, W1S_B, 5'b00000};

For Char/Window, duplicate to High/Low nibble; (include Window Shadow with W1S_Gray=0)



Bit_Map Mode

4 Bits/Pixel mode: Same as Character Mode
2 Bits/Pixel mode: Refer to LUT[0], then re-direct to other LUT[1..15]

Figure 2-15

2.10.5.4 Character Mode Color Layer

Layer_1: Character Foreground Color. This is the Top layer.
Layer_2: Character Border/Shadow Color. (Gray, Non-HalfTone Half-color)
Layer_3: Window Color.
Layer_4: Window Shadow Color (Non-HalfTone).
Layer_5: Character Background Color.
Layer_6: Original Background Color (+ HalfTone Window Shadow). This is the bottom layer.

2.10.5.5 Halt Tone Display

The Halftone feature is automatically applied to the shadow area (both the Character Shadow and Window Shadow), if its shadow RGB color (the BDS_RGB or W1S_RGB settings) is set as 000b and its Gray control (the BDS_Gray or W1S_Gray settings) is set as 0. Then the displayed color will be the half of the RGB color of next lower layer.

2.10.5.6 Character Border /Shadow Consideration

Hardware Border/Shadow Calculation

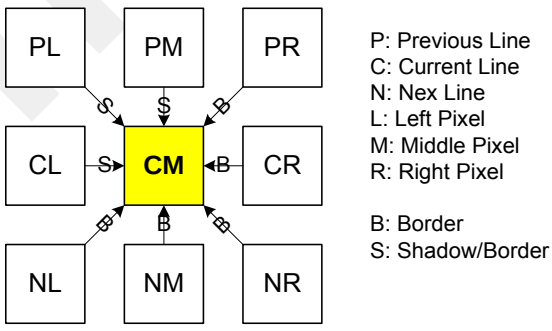


Figure 2-16

2.10.5.7 Programming Examples

2.10.5.7.1 Configuring OSD Function

To access OSD configuration registers, write register index to port A0h, and read/write data from port A1h. For example, set :

```
IOW     A0h, 1Dh        ; point to Cfg_1Dh (revision ID register).
IOR     A1h;            ; get Revision ID.
IOW     A0h, 06h        ; point to Cfg_06h (Character Border / Shadow register).
IOW     A1h, C4;        ; Set Shadow height 2 lines, width 1 line.
```

2.10.5.7.2 Fill LUT RAM

LUT RAM size is 16 (address) x 12 (width). For example, need to fill LUT RAM as:
LUT_RAM[0] = 123h, LUT_RAM[1]=F5Ah, …LUT_RAM[15]=EF0h

```
IOW     A0h, 0Eh        ; point to Cfg_0Eh (LUT RAM Data port), this will let LUT RAM be
                          ; access-able and pointer starts from 0h of LUT RAM.
IOW     A1h, 23h;       ; fill Green = 0010b and Blue = 0011h in LUT_RAM[0].
IOW     A1h, 01h;       ; fill Red = 0001b in LUT_RAM[0].
                          ; after this write, h/w will increase LUT RAM address to 1 automatically
IOW     A1h, 5Ah;       ; fill Green = 0101b and Blue = 1010h in LUT_RAM[1].
IOW     A1h, 0Fh;       ; fill Red = 1111b in LUT_RAM[1].
                          ; after this write, h/w will increase LUT RAM address to 2 automatically
. . . . . .
IOW     A1h, F0h;       ; fill Green = 1111b and Blue = 0000h in LUT_RAM[15].
IOW     A1h, 0Eh;       ; fill Red = 1110b in LUT_RAM[15].
                          ; after this write, h/w will increase LUT RAM address to 0 automatically
IOW     A0h, non-0Eh    ; Disable LUT RAM programming.
```

2.10.5.7.3 Load Fonts to OSD RAM

OSD RAM size is 3K (address: 000h ~ BFFh) x 16 (width). Fonts storing starts from address 000h. For example, loading some fonts to OSD RAM as:
Font[0] is a space (all zero), Font[1] is a character 2 with box, Font[14] is a graphic.

```
IOW     A2h, 00h        ; set OSD RAM starting access address low byte. (bit [7:0] as A[7:0])
IOW     A3h, 00h;       ; set OSD RAM starting access address high byte. (bit [3:0] as A[11:8])
                          ; then the OSD RAM address pointer is set to 000h.
IOW     A4h, 00h;       ; low byte of first row of Font[0].
IOW     A4h, 00h;       ; high byte of first row of Font[0], after this write, h/w will increase OSD
                          ;RAM address to 1 automatically
IOW     A4h, 00h;       ; low byte of 2nd row of Font[0].
IOW     A4h, 00h;       ; high byte of 2nd row of Font[0], after this write, h/w will increase OSD
                          ;RAM address to 2 automatically
. . . . . (for example, programmed font size is 18 (height) x 12 (width)
IOW     A4h, 00h;       ; low byte of 18th (last) row of Font[0].
IOW     A4h, 00h;       ; high byte of 18th row of Font[0], after this write, h/w will increase OSD
                          ;RAM address to 012h automatically
IOW     A4h, F0h;       ; low byte of first row of Font[0]. (since font width is 12, the low bye bit[3:0]
                          ; is no use)
IOW     A4h, FFh;       ; high byte of first row of Font[0], after this write, h/w will increase OSD
                          ;RAM address to 013h automatically
. . . . . .
IOW     A2h, 68h        ; set OSD RAM starting access address low byte. (bit [7:0] as A[7:0])
IOW     A3h, 01h;       ; set OSD RAM starting access address high byte. (bit [3:0] as A[11:8]),
                          ; then the OSD RAM address pointer is set to 168h = 14d * 18d.
IOW     A4h, 40h;       ; low byte of first row of Font[14].
IOW     A4h, A3h;       ; high byte of first row of Font[14],
. . . . . .
```

2.10.5.7.4 Assign Characters and its color to OSD RAM

Just like the way to load Fonts.

2.11 TCON

2.11.1 LCD Panel Pin Assignment

In this section, we illustrate those pins connected to AU 7" TFT-LCD panel module in a T100 video system.

Table 2-31 T100 Rotation Control and LCD Panel Scanning Direction

L/R	U/D	STH	STV	Reg 0xE1	Scanning Direction
1	1	STH2	STV1	0xBC	Down-to-up, left-to-right
1	0	STH2	STV2	0xF4	Up-to-down, left-to-right
0	1	STH1	STV1	0xA8	Down-to-up, right-to-left
0	0	STH1	STV2	0xE0	Up-to-down, right-to-left

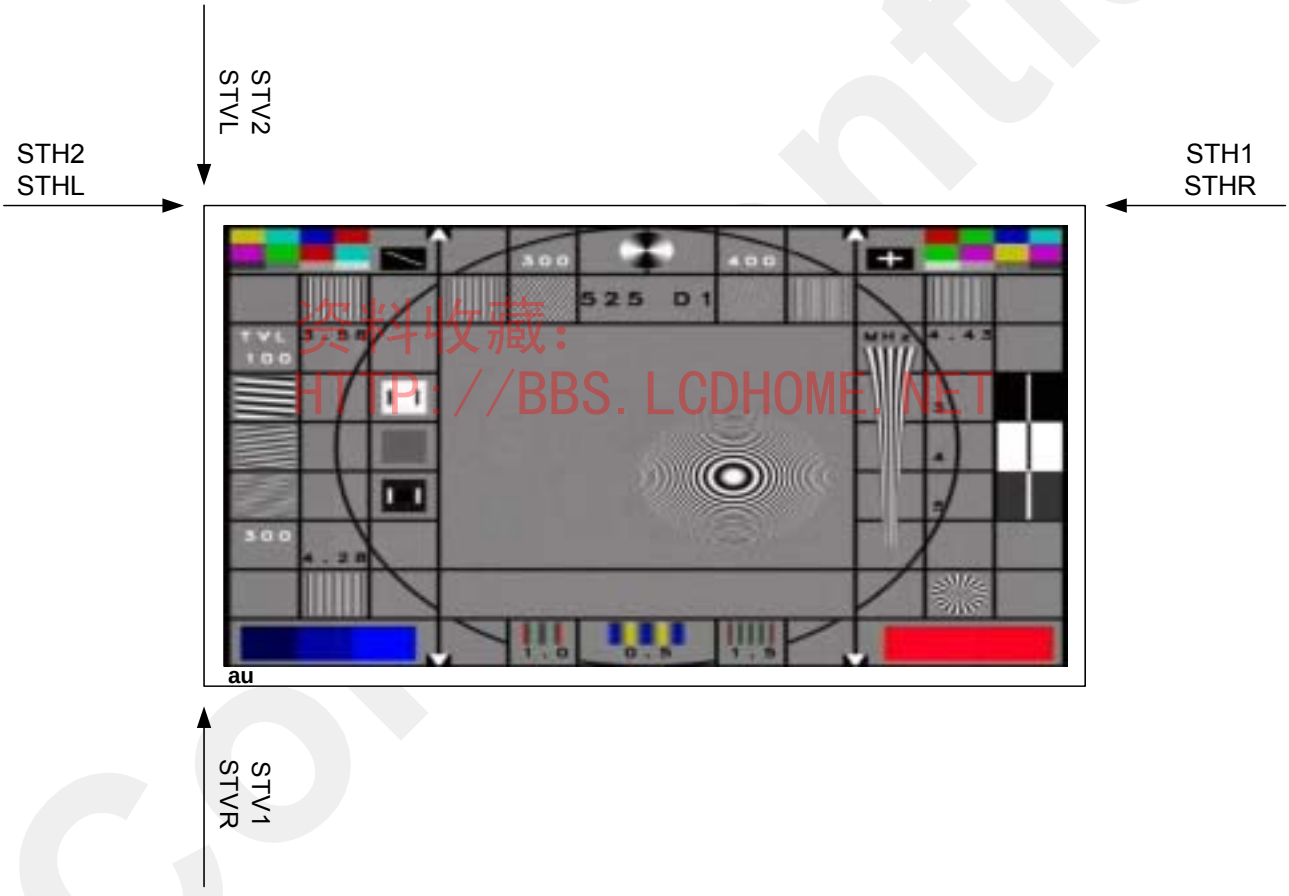


Figure 2-17 Scanning Direction of AU 7" panel

2.11.2 TCON Timing

T100 is designed for analog LCD panel. Each 24-bit color pixel must be converted into analog voltage via built-in triple DACs. The table 2-1 shows a typical setting for AU 7" panel with 10-Mhz operation clock.

Table 2-32 T100 TCON Register Set (C8 =1Bh, C9=03, CA=03h)

Reg	Reg value	Operation
0x20	0x21	Line-inverted Control
0x21	0x79	Polarity Control
0x23,0x22	0x022D	Placement of OEH
0x24	0x0C	Duration of OEH
0x26,0x25	0x024B	Placement of POL
0x28,0x27	0x021C	Placement of GCLK
0x2A,0x29	0x0029	Duration of GCLK
0x2B	0x01	Placement of STH
0x30	0x01	Enable Placement of STV
0x32,0x31	0x01FB	Placement of GOE
0x34,0x33	0x0037	Duration of GOE
0x35	0x06	Placement of STV

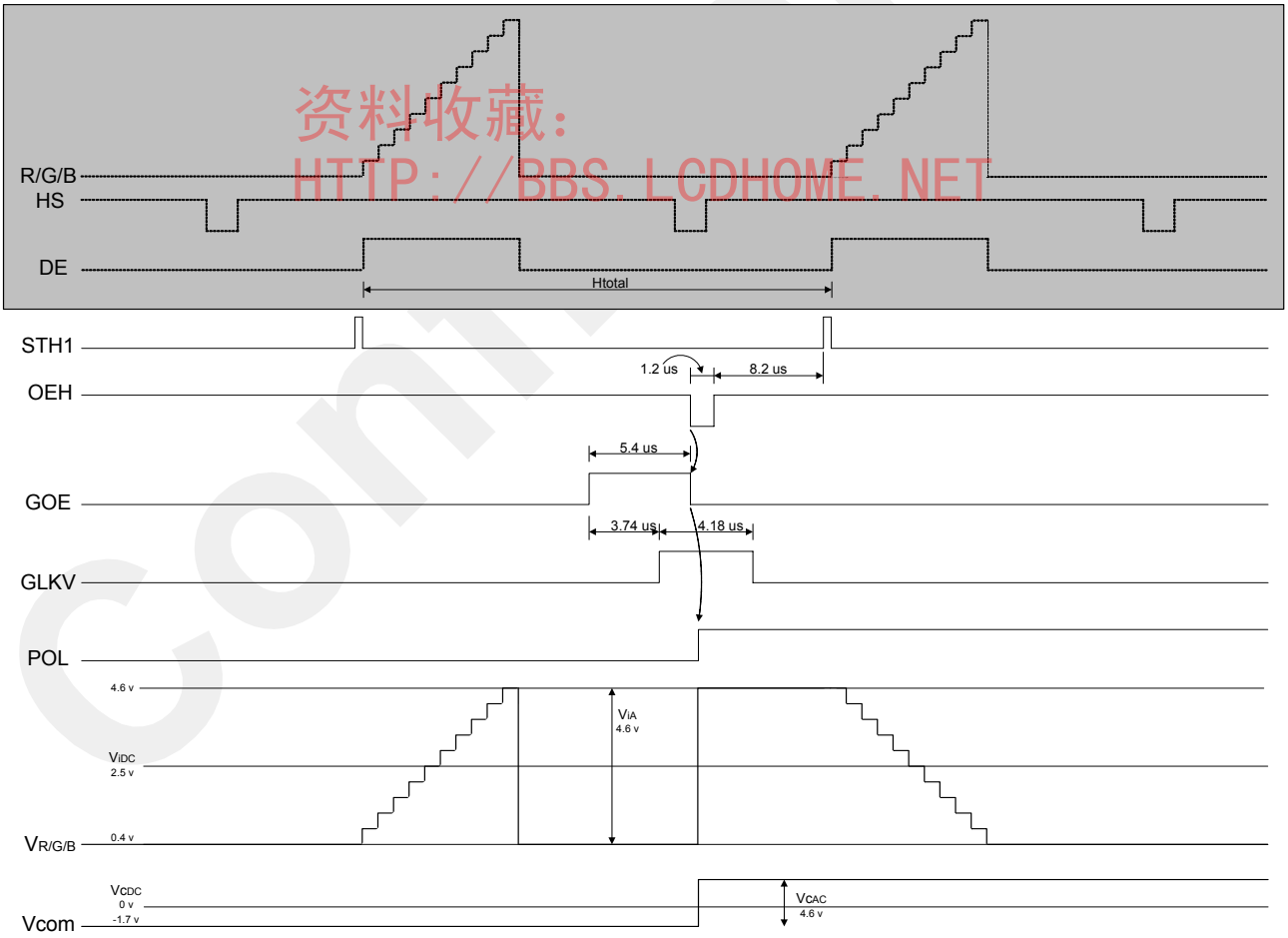


Figure 2-18 AU 7" TCON Timing Spec

The waveforms shown below illustrate TCON location counting. Each TCON signal's placement and duration are allowed to program as alike as analog LCD panels require. On the figure 2-2, the pulse placement starts counting at the leading edge of DE. After placement counter meets the value we give to {P1_27h,P1_28h}, the duration counter starts to count until the duration meets {P1_29h,P1_2Ah}. All of location counting use LLCK as counter clock.

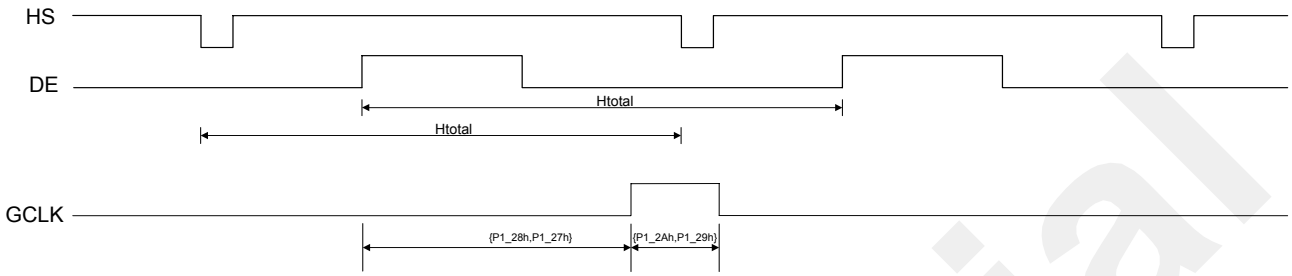


Figure 2-19 Location Counting of GCLK

3 Register Description

Serial Bus Register Set Page 0

3.1 ADC Register Set

3.1.1 ADC Channel 0 Current Register

Address Offset: 00h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-1 ADC Channel 0 Current Register

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	
[3:0]	R/W	IR	ADC channel 0 current strength

3.1.2 ADC Channel 1 Current Register

Address Offset: 01h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-2 ADC Channel 1 Current Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	IG	ADC channel 1 current strength

3.1.3 ADC Channel 2 Current Register

Address Offset: 02h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-3 ADC Channel 2 Current Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	IB	ADC channel 2 current strength

3.1.4 ADC Clamping Pulse Placement and Duration

Address Offset: 04h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-4 ADC Clamping Pulse Placement and Duration

Bit	Access	Symbol	Description
[7:5]	R/W	STIPCLPL	Clamping pulse placement
[4:0]	R/W	STIPCLDU	Clamping pulse duration

3.1.5 ADC Channel 0 Static Gain

Address Offset: 07h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-5 ADC Channel 0 Static Gain

Bit	Access	Symbol	Description
[7:0]	R/W	ADCRSG	This register can set a fixed gain for ADC channel 0 when static gain control is enabled

3.1.6 ADC Channel 1 Static Gain

Address Offset: 08h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-6 ADC Channel 1 Static Gain

Bit	Access	Symbol	Description
[7:0]	R/W	ADCGSG	This register can set a fixed gain for ADC channel 1 when static gain control is enabled

3.1.7 ADC Channel 2 Static Gain

Address Offset: 09h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-7 ADC Channel 2 Static Gain

Bit	Access	Symbol	Description
[7:0]	R/W	ADCBSG	This register can set a fixed gain for ADC channel 2 when static gain control is enabled

3.1.8 ADC ACR Channel Offset

Address Offset: 0Ah Access: Read/Write
Default Value: 80h Size: 8 bits

Table 3-8 ADC ACR Channel Offset

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_ROFF	ADC Channel 0 DC Offset Control
[1:0]	R/W	RESERVED	

3.1.9 ADC AY Channel Offset

Address Offset: 0Bh Access: Read/Write
Default Value: 80h Size: 8 bits

Table 3-9 ADC AY Channel Offset

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_GOFF	ADC Channel 1 DC Offset Control
[1:0]	R/W	RESERVED	

3.1.10 ADC ACB Channel Offset Configuration Register

Address Offset: 0Ch Access: Read/Write
Default Value: 80h Size: 8 bits

Table 3-10 ADC ACB Channel Offset Configuration Register

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_BOFF	ADC Channel 2 DC Offset Control
[1:0]	R/W	RESERVED	

3.1.11 ADC General Control Configuration Register

Address Offset: 0Dh Access: Read/Write
Default Value: 20h Size: 8 bits

Table 3-11 ADC General Control Configuration Register

Bit	Access	Symbol	Description
[7:6]	R/W	CLPMD	Clamping mode Mode 0: Fixed window Mode 1: Locked Window Mode 2: Self Bias Mode 3: Fixed Window
[5]	R/W	DCEN	DC Clamping Enable
[4]	R/W	DCSEL	Clamping Source Selection
[3]	R/W	B1S0	Slicer threshold voltage selection Mode 0: above auto bias Mode 1: below auto bias
[2]	R/W	DC_CAL_RDY	DC Calibration Ready
[1]	R/W	DC_CALEN	DC Calibration Enable
[0]	R/W	DC_CALMD	DC Calibration Mode Mode 0: minimum Mode 1: average

3.1.12 ADC Power Down Control

Address Offset: 0Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-12 ADC Power Down Control

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	PD2	1: Power down 0: Power up
[5]	R/W	PD1	1: Power down 0: Power up
[4]	R/W	PD0	1: Power down 0: Power up
[3:0]	R/W	RESERVED	

3.1.13 Reserved

Address Offset: 10h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-13 Reserved

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	

3.1.14 YPbPr Clamping Control Register

Address Offset: 11h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-14 YPbPr Clamping Control Register

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2]	R/W	BSCALE	ADC Channel 2 Clamping Mode Mode: Select 0: Clamp to ground 1: Clamp to midscale
[1]	R/W	GSCALE	ADC Channel 1 Clamping Mode Mode: Select 0: Clamp to ground 1: Clamp to midscale
[0]	R/W	RSCALE	ADC Channel 0 Clamping Mode Mode: Type 0: Clamp to ground 1: Clamp to midscale

3.1.15 Analog Source MUX Selection

Address Offset: 18h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-15 Analog Source MUX Selection

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5:4]	R/W	AI2SEL	Analog mux selection for ADC channel 1 Mode: Type 0: ACB1 1: ACB0 2: ACB2 3: ACB2
[3:2]	R/W	AI1SEL	Analog mux selection for ADC channel 1 Mode: Type 0: AY1 1: AY0 2: AY2 3: AY2

Bit	Access	Symbol	Description
[1:0]	R/W	AI0SEL	Analog mux selection for ADC channel 0 Mode 0: ACR1 Mode 1: ACR0 Mode 2: ACR2 Mode 3: ACR2

3.1.16 Y/Cb/Cr Data Switching Control

Address Offset: 19h Access: Read/Write
Default Value: 07h Size: 8 bits

Table 3-16 Y/Cb/Cr Data Switching Control

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5:4]	R/W	CBINSEL	The digitaized CB or Chroma data can be taken from one of 3 ADCs according to following table Mode 0: ADC Ch0 Mode 1: ADC Ch1 Mode 2: ADC Ch2 Mode 3: ADC Ch2
[3:2]	R/W	YINSEL	The digitaized Y or Composite data can be taken from one of 3 ADCs according to following table Mode 0: ADC Ch0 Mode 1: ADC Ch1 Mode 2: ADC Ch2 Mode 3: ADC Ch2
[1:0]	R/W	CRINSEL	The digitaized CR or Chroma data can be taken from one of 3 ADCs according to following table Mode 0: ADC Ch0 Mode 1: ADC Ch1 Mode 2: ADC Ch2 Mode 3: ADC Ch2

3.1.17 ADC Analog AGC Selection

Address Offset: 1Ah Access: Read/Write
Default Value: 42h Size: 8 bits

Table 3-17 ADC Analog AGC Selection

Bit	Access	Symbol	Description
[7:6]	R/W	AGC_GAINMD	Mode: Type 0: Positive gain 1: Positive gain 1x~2x 2: Negative gain 1x~2x 3: Negative gain
[5:3]	R/W	RESERVED	
[2]	R/W	CB_AGC_SEL	If 0, refer to ADCBSG Mode: Type 0: Static gain 1: Dynamic gain
[1]	R/W	Y_AGC_SEL	If 0, refer to ADCGSG Mode: Type 0: Static gain 1: Dynamic gain
[0]	R/W	CR_AGC_SEL	If 0, refer to ADCRSG Mode: Type 0: Static gain 1: Dynamic gain

3.1.18 Blank Sync Level

Address Offset: 1Ch Access: Read/Write
Default Value: C0h Size: 8 bits

Table 3-18 Blank Sync Level

Bit	Access	Symbol	Description
[7:0]	R/W	BLANK_SL	

3.1.19 ADC Read-back Selection

Address Offset: 1Dh Access: Read/Write
Default Value: 80h Size: 8 bits

Table 3-19 ADC Read-back Selection

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2:0]	R/W	RBK_SEL	1: Read Max of ADC data 0:Read Min of ADC data or Average of ADC data

3.1.20 ADC Read-back Data

Address Offset: 1Eh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-20 ADC Read-back Data

Bit	Access	Symbol	Description
[7:0]	R/W	RBK_ADC[7:0]	

3.1.21 ADC Read-back Data

Address Offset: 1Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-21 ADC Read-back Data

Bit	Access	Symbol	Description
[7:2]	R	RESERVED	
[1:0]	R	RBK_ADC[9:0]	

3.1.22 De-Interlaced Process & Vertical Shadow Control Register

Address Offset: 30h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-22 De-Interlaced Process & Vertical Shadow Control Register

Bit	Access	Symbol	Description
[7]	R/W	CBCR_INTERP	1: Enable CbCr interpolation 0: Disable
[6]	R/W	RESERVED	
[5]	R/W	VST_CHGSEL	1:Vsync timing change determined by 8*# of XCLK 0:Vsynnc timing change determined by # of hsync # can be assigned at Reg 0x3A
[4]	R/W	INT_EDGE	Interrupt polarity 1: positive 0: negative
[3]	R/W	LB_SIZE_FIXED	This bit control capture size for Scaler. 1: Hsize and Vsize are assigned by 54h ~57h 0: sizes assigned by input sources.
[2]	R/W	ENQKHS	Set 0 for normal operation
[1]	R/W	ITLCPRO	Set 1 for interlaced video Set 0 for non-interlaced video
[0]	R/W	ENSHDW	

3.1.23 Source Select Register

Address Offset: 31h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-23 Source Select Register

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[4]	R/W	INP_SRC_SEL	1: select digital ITU656 input 0: select analog input

Bit	Access	Symbol	Description
[3:0]	R/W	RESERVED	

3.1.24 Interrupt Status Register

Address Offset: 32h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-24 Interrupt Status Register

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R	ITLCFLM	Indicates incoming video signal is interlaced
[5:0]	R/W	INTSTS	

3.1.25 Interrupt Mask Register

Address Offset: 33h Access: Read/Write
Default Value: FFh Size: 8 bits

Table 3-25 Interrupt Mask Register

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5:0]	R/W	INTMASK	

3.1.26 Lower 8-bit Timer Counter Register

Address Offset: 35h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-26 Lower 8-bit Timer Counter Register

Bit	Access	Symbol	Description
[7:0]	R/W	TM_1MS_L [7:0]	Lower byte of the number of XCLK's in 1ms.

3.1.27 Upper 8-bit Timer Counter Register

Address Offset: 36h Access: Read/Write
Default Value: 10h Size: 8 bits

Table 3-27 Upper 8-bit Timer Counter Register

Bit	Access	Symbol	Description
[7:0]	R/W	TM_1MS_H [15:8]	Higher byte of the number of XCLK's in 1ms.

3.1.28 VSYNC Missing Counter Register

Address Offset: 37h Access: Read/Write
Default Value: 40h Size: 8 bits

Table 3-28 VSYNC Missing Counter Register

Bit	Access	Symbol	Description
[7:0]	R/W	V_MISS_CNT	

3.1.29 Lower 8-bit HSYNC Missing Counter Register

Address Offset: 38h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-29 Lower 8-bit HSYNC Missing Counter Register

Bit	Access	Symbol	Description
[7:0]	R/W	H_MISS_CNT_L[7:0]	

3.1.30 Upper 8-bit HSYNC Missing Counter Register

Address Offset: 39h Access: Read/Write
Default Value: 10h Size: 8 bits

Table 3-30 Upper 8-bit HSYNC Missing Counter Register

Bit	Access	Symbol	Description
[7:0]	R/W	H_MISS_CNT_L[15:8]	

3.1.31 VSYNC Delta Difference Result Register

Address Offset: 3Ah Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-31 VSYNC Delta Difference Result Register

Bit	Access	Symbol	Description
[7:0]	R/W	VSYNC_DLT[7:0]	

3.1.32 HSYNC Delta Difference Result Register

Address Offset: 3Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-32 HSYNC Delta Difference Result Register

Bit	Access	Symbol	Description
[7:0]	R/W	HSYNC_DLT[7:0]	

3.1.33 Input Sync Signal Detection Register

Address Offset: 3Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-33 Input Sync Signal Detection Register

Bit	Access	Symbol	Description
[7]	R/W	HSTLSPVS	1:use trailing edge of hsync to sample 0:use leading edge of hsync to sample
[6]	R/W	AUTOVSD6	When the edges of vsync and hsync are too close, input detection circuit can delay vsync 6 cycle of XCLK to avoid unstable detection 1:Automatically delay 6 cycles of XCLK if CFSEEDGE is true. 0:Dealy 6 cycles of XCLK if FCVSD6 is true
[5]	R/W	FCVSD6	AUTOVSD6 FCSVSD6T 1 x Auomatically delay VSync 6 XCLK if CFSEEDGE is true 0 1 Force to delay VSync 6 XCLK 0 0 No Vsync Dealy
[4]	R	CFSEEDGE	VS and HS edges are to close.

[3:2]	R/W	RESERVED	
[1]	R/W	VsHs_Sync_Edge	1: leading edge of Vsi 0: falling edge of His
[0]	R/W	VsHS_Sync_En	1:leading edge of Vsi starts at leading edge of Hsi 0:leading edge of Vsi starts at mid of Hsi

3.1.34 Left Border Croping

Address Offset: 40h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-34 Left Border Croping

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5:0]	R/W	CROP_LEFTB	Remove noisy pixels appearing on left border. 1LSB =1 pixel

3.1.35 VSYNC Timing Measurement Register

Address Offset: 50h Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-35 VSYNC Timing Measurement Register

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	HSPMD	Register 0x5c and 0x5d can be HS pulse width or hsync period 1:Period in # of pixel clock. 0:Hsync pulse width in # of pixel clock.
[5]	R	DONE_FRMXCLKCNT	When EN_FRAMEXCLKCNT is enabled, a whole frame time can be obtained through XCLK counting. See registers 0x51, 0x52 and 0x53. After this bit read back as 1, then clear EN_FRAMEXCLKCNT first before reading 0x51~0x53 values.
[4]	R/W	EN_FRAMEXCLKCNT	When input VSync changes, enable this bit to start measurement on VSync using XCLK.
[3:0]	R/W	RESERVED	

3.1.36 VSYNC Measurement Counter L Register

Address Offset: 51h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-36 VSYNC Measurement Counter L Register

Bit	Access	Symbol	Description
[7:0]	R/W	FRMXCLK_SUM[7:0]	

3.1.37 VSYNC Measurement Counter M Register

Address Offset: 52h Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-37 VSYNC Measurement Counter M Register

Bit	Access	Symbol	Description
[7:0]	R/W	FRMXCLK_SUM[15:8]	

3.1.38 VSYNC Measurement Counter H Register

Address Offset: 53h Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-38 VSYNC Measurement Counter H Register

Bit	Access	Symbol	Description
[7:0]	R/W	FRMXCLK_SUM[23:16]	

3.1.39 Hsize

Address Offset: 54h Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-39 Hsize

Bit	Access	Symbol	Description
[7:0]	R	HSIZE[7:0]	

3.1.40 Hsize

Address Offset: 55h Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-40 Hsize

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R	HSIZE[11:8]	

3.1.41 Vsize

Address Offset: 56h Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-41 Vsize

Bit	Access	Symbol	Description
[7:0]	R	VSIZE[7:0]	

3.1.42 Vsize

Address Offset: 57h Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-42 Vsize

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R	VSIZE[11:8]	

3.1.43 HSYNC Period LSB Register

Address Offset: 58h Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-43 HSYNC Period LSB Register

Bit	Access	Symbol	Description
[7:0]	R	HS_PERIOD[7:0]	HSYNC period counted by XCLK

3.1.44 HSYNC Period MSB Register

Address Offset: 59h Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-44 HSYNC Period MSB Register

Bit	Access	Symbol	Description
[7:0]	R	HS_PERIOD[15:8]	HSYNC period counted by XCLK

3.1.45 VSYNC Period LSB Register

Address Offset: 5Ah Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-45 VSYNC Period LSB Register

Bit	Access	Symbol	Description
[7:0]	R	VS_PERIOD[7:0]	VSYNC period counted by input HSYNC

3.1.46 VSYNC Period MSB Register

Address Offset: 5Bh Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-46 VSYNC Period MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R	VS_PERIOD[11:8]	VSYNC period counted by input HSYNC

3.1.47 HSYNC Pulse Width LSB Register

Address Offset: 5Ch Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-47 HSYNC Pulse Width LSB Register

Bit	Access	Symbol	Description
[7:0]	R	HS_WIDTH[7:0]	HSYNC pulse width or period counted by dot clock See HSPMD for detail. Note: dot clock speed is in 1-pixel-per-clock mode

3.1.48 HSYNC Pulse Width MSB Register

Address Offset: 5Dh Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-48 HSYNC Pulse Width MSB Register

Bit	Access	Symbol	Description
[7:4]	R	RESERVED	
[3:0]	R	HS_WIDTH[11:8]	HSYNC pulse width or period counted by dot clock

3.1.49 VSYNC Pulse Width LSB Register

Address Offset: 5Eh Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-49 VSYNC Pulse Width LSB Register

Bit	Access	Symbol	Description
[7:0]	R	VS_WIDTH[7:0]	VSYNC pulse width counted by input HSYNC

3.1.50 VSYNC Pulse Width MSB Register

Address Offset: 5Fh Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-50 VSYNC Pulse Width MSB Register

Bit	Access	Symbol	Description
[7:4]	R	RESERVED	
[3:0]	R	VS_WIDTH[11:8]	VSYNC pulse width counted by input HSYNC

3.2 Picture Enhancement Register Set

3.2.1 Bandwidth of Digital Color Transient Improvement

Address Offset: 60h Access:
Default Value: 02h Size: 8 bits

Table 3-51 Bandwidth of Digital Color Transient Improvement

Bit	Access	Symbol	Description
[7:1]	R/W	RESERVED	
[0]	R/W	DCTI_BW	0: high bandwidth 1: low bandwidth

3.2.2 Luma Peaking Control

Address Offset: 61h Access:
Default Value: 08h Size: 8 bits

Table 3-52 Luma Peaking Control

Bit	Access	Symbol	Description
[7]	R/W	PeakingEN	
[6]	R/W	RESERVED	
[5:0]	R/W	PeakingCo	

3.2.3 Bandpass Peaking Coef

Address Offset: 62h Access:
Default Value: 04h Size: 8 bits

Table 3-53 Bandpass Peaking Coef

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[4:0]	R/W	BP_COEF	

3.2.4 Highpass Peaking Coef

Address Offset: 63h Access:
Default Value: 04h Size: 8 bits

Table 3-54 Highpass Peaking Coef

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[4:0]	R/W	HP_COEF	

3.2.5 Lowpass Peaking Coef

Address Offset: 64h Access:
Default Value: 02h Size: 8 bits

Table 3-55 Lowpass Peaking Coef

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2:0]	R/W	LP_COEF	

3.2.6 Gain and Coring of DLTI

Address Offset: 65h Access:
Default Value: 08h Size: 8 bits

Table 3-56 Gain and Coring of DLTI

Bit	Access	Symbol	Description
[7:5]	R/W	DLTI_GAIN	
[4:0]	R/W	DLTI_CO	

3.2.7 Gain and Coring of DCTI

Address Offset: 66h Access:
Default Value: 08h Size: 8 bits

Table 3-57 Gain and Coring of DCTI

Bit	Access	Symbol	Description
[7:5]	R/W	DCTI_GAIN	
[4:0]	R/W	DCTI_CO	

3.2.8 Contrast Adjust

Address Offset: 68h Access:
Default Value: 80h Size: 8 bits

Table 3-58 Contrast Adjust

Bit	Access	Symbol	Description
[7:0]	R/W	LumaCON	

3.2.9 Brightness Adjust

Address Offset: 69h Access:
Default Value: 80h Size: 8 bits

Table 3-59 Brightness Adjust

Bit	Access	Symbol	Description
[7:0]	R/W	LumaBRI	

3.2.10 Hue Sin Adjust

Address Offset: 6Ah Access:
Default Value: 00h Size: 8 bits

Table 3-60 Hue Sin Adjust

Bit	Access	Symbol	Description
[7:0]	R/W	HueSin	

3.2.11 Hue Cos Adjust

Address Offset: 6Bh Access:
Default Value: 7Fh Size: 8 bits

Table 3-61 Hue Cos Adjust

Bit	Access	Symbol	Description
[7:0]	R/W	HueCos	

3.2.12 Chroma Saturation Adjust

Address Offset: 6Ch Access:
Default Value: 80h Size: 8 bits

Table 3-62 Chroma Saturation Adjust

Bit	Access	Symbol	Description
[7:0]	R/W	ChromSat	

3.3 Scaling Register Set

3.3.1 Scaling General Control Register

Address Offset: 70h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-63 Scaling General Control Register

Bit	Access	Symbol	Description
[7:6]	R/W	InpClk_Phase	It might exist setup or hold time violation between ADC and input capture block. Usually, a 4-step delay unit can be applied to move pixel clock up to 4 steps to avoid timing violation.
[5]	R/W	Inv_VideoF	Inv_VideoF: Reverse input odd field control for intrafield scaling, only take action when ITLCPRO set to 1.
[4]	R/W	Dclki_is_Faster	Software need to turn this bit on when the freq of input pixel clock is higher than output pixel clock.
[3]	R/W	RME2	Remove 2D Scaling for 2 pixels width chess board boundary effect.
[2]	R/W	Scale_2D_En	Enable 2-D Scaler
[1:0]	R/W	C16_Pointer_RST	Reset coef table. 01b: Reset write pointer to 0x00. 10b: Reset write pointer to 0x80.

3.3.2 Scaling Coefficient Data Port Register

Address Offset: 71h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-64 Scaling Coefficient Data Port Register

Bit	Access	Symbol	Description
[7:0]	R/W	Coef_Data_Port	

3.3.3 Horizontal Scale Step LSB Register

Address Offset: 72h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-65 Horizontal Scale Step LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	H_Scale_Step [7:0]	

3.3.4 Horizontal Scale Step MSB Register

Address Offset: 73h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-66 Horizontal Scale Step MSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	H_Scale_Step [15:8]	

3.3.5 Vertical Scale Step LSB Register

Address Offset: 74h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-67 Vertical Scale Step LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	V_Scale_Step [7:0]	

3.3.6 Vertical Scale Step MSB Register

Address Offset: 75h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-68 Vertical Scale Step MSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	V_Scale_Step [15:8]	

3.3.7 Horizontal Aspect Ratio Register

Address Offset: 76h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-69 Horizontal Aspect Ratio Register

Bit	Access	Symbol	Description
[7:0]	R/W	HASPR[7:0]	

3.3.8 Horizontal Aspect Ratio Register

Address Offset: 77h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-70 Horizontal Aspect Ratio Register

Bit	Access	Symbol	Description
[7]	R/W	HASPEN	
[6]	R/W	HASP_C_ELG	
[5:0]	R/W	HASPR[13:8]	

3.3.9 Reserved

Address Offset: 7Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-71 Reserved

Bit	Access	Symbol	Description
[7:0]	R/W		

3.3.10 Reserved

Address Offset: 7Ch Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-72 Reserved

Bit	Access	Symbol	Description
[7:0]	R/W		

3.3.11 Reserved

Address Offset: 7Dh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-73 Reserved

Bit	Access	Symbol	Description
[7:0]	R/W		

3.3.12 Reserved

Address Offset: 7Eh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-74 Reserved

Bit	Access	Symbol	Description
[7:0]	R/W		

3.3.13 2D Scaler Configuration Register

Address Offset: 7Fh Access: Read/Write
Default Value: 04h Size: 8 bits

Table 3-75 2D Scaler Configuration Register

Bit	Access	Symbol	Description
[7:6]	R/W	MASK_2D_SEL	
[5:4]	R/W	FULL_2D_SEL	
[3:0]	R/W	DELTA2D	Color transition threshold for 2D Scaling. Less value for more 2D sensitive.

3.3.14 Reserved

Address Offset: 80h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-76 Reserved

Bit	Access	Symbol	Description
[7:0]	R/W		

3.3.15 Input Vsync Leading Edge to DE Time Counter 1/3 Register

Address Offset: 81h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-77 Input Vsync Leading Edge to DE Time Counter 1/3 Register

Bit	Access	Symbol	Description
[7:0]	R	TVIBLK[7:0]	Timing counter can measure the time interval between leading edge of input vsync and first valid input pixel. This time interval is TVIBLK * (1/XCLK)

3.3.16 Input Vsync Leading Edge to DE Time Counter 2/3 Register

Address Offset: 82h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-78 Input Vsync Leading Edge to DE Time Counter 2/3 Register

Bit	Access	Symbol	Description
[7:0]	R	TVIBLK [15:8]	

3.3.17 Input Vsync Leading Edge to DE Time Counter 3/3 Register

Address Offset: 83h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-79 Input Vsync Leading Edge to DE Time Counter 3/3 Register

Bit	Access	Symbol	Description
[7:0]	R/W	TVIBLK[23:16]	

3.3.18 Line Buffer Configuration LSB Register

Address Offset: 84h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-80 Line Buffer Configuration LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	LBPRFL[7:0]	LBPRFL can cause a time dealy in XCLK count between the leading edge of input Vsync and leading edge of output Vsync.

3.3.19 Line Buffer Configuration MSB Register

Address Offset: 85h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-81 Line Buffer Configuration MSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	LBPRFL[15:8]	

3.3.20 Output Hsync Vibration Step Register

Address Offset: 86h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-82 Output Hsync Vibration Step Register

Bit	Access	Symbol	Description
[7:0]	R/W	HSVIB	Output HSync re-map factor in vertical Active period.

3.3.21 Output Vsync Front Porch Remapping Register

Address Offset: 87h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-83 Output Vsync Front Porch Remapping Register

Bit	Access	Symbol	Description
[7:0]	R/W	VSFPRMP	Output HSync remap amount in vertical front porch period.

3.3.22 Left Display Border Configuration Register

Address Offset: 88h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-84 Left Display Border Configuration Register

Bit	Access	Symbol	Description
[7:0]	R/W	HLDSPLB[7:0]	When Output pixel's index is less than HRDSPLB, output pixel value is assigned as left display border {FMCLRRDE, FMCLRGRN , FMCLRBLU}

3.3.23 Left Display Border Configuration Register

Address Offset: 89h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-85 Left Display Border Configuration Register

Bit	Access	Symbol	Description
[7]	R/W	HDSPLB_INV	Horizontal border is on if HDSPLB_INV is set as follows 1: HLDSPLB < Horizontal border < HRDSPLB 0: Horizontal border < HLDSPLB or HRDSPLB < Horizontal border
[6]	R/w	VDSPLB_INV	Vertical border is on if VDSPLB_INV is set as follows 1: VTDSPLB < < VBDSPLB 0: Vertical border < VTDSPLB or VBDSPLB < Vertical border
[5]	R/W	HDSPLB_STY	Border style 1: mesh 0: solid
[4]	R/W	VDSPLB_STY	Border style 1: mesh 0: solid
[3:0]	R/W	HLDSPLB[11:8]	

3.3.24 Right Display Border Configuration LSB Register

Address Offset: 8Ah Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-86 Right Display Border Configuration LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	HRDSPLB[7:0]	When Output pixel's index is greater than HRDSPLB, output pixel value is assigned as right display border {FMCLRRDE, FMCLRGRN , FMCLRBLU}

3.3.25 Right Display Border Configuration MSB Register

Address Offset: 8Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-87 Right Display Border Configuration MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	HRDSPLB[11:8]	

3.3.26 Top Display Border Configuration LSB Register

Address Offset: 8Ch Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-88 Top Display Border Configuration LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	VTDSPLB[7:0]	

3.3.27 Top Display Border Configuration MSB Register

Address Offset: 8Dh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-89 Top Display Border Configuration MSB Register

Bit	Access	Symbol	Description
[7:6]	R/W	HDSPLB_GRID[1:0]	H grip precision, 00b: 1 pixel 01b: 4 pixels 10b: 16 pixels 11b: 32 pixels
[5:4]	R/W	VDSPLB_GRID[1:0]	V grip precision 00b: 1 line 01b: 4 lines 10b: 16 lines 11b: 32 lines
[3:0]	R/W	VTDSPLB[11:8]	

3.3.28 Bottom Display Border Configuration LSB Register

Address Offset: 8Eh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-90 Bottom Display Border Configuration LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	VBDSPLB[7:0]	

3.3.29 Bottom Display Border Configuration MSB Register

Address Offset: 8Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-91 Bottom Display Border Configuration MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	VBDSPLB[11:8]	

3.4 Color Space Converter Register Set

3.4.1 Image Function Control Register

Address Offset: 90h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-92 Image Function Control Register

Bit	Access	Symbol	Description
[7:6]	R/W	GATS[1:0]	Gamma Table Select. Default=2'b00. GATS[1:0] / Polarity 2'b11 / Gamma Table R 2'b10 / Gamma Table G 2'b01 / Gamma Table B 2'b00 / All 3
[5]	R/W	RESERVED	

Bit	Access	Symbol	Description
[4]	R/W	RESERVED	Reserved
[3]	R/W	RESERVED	Reserved
[2]	R/W	EN_CSC	Enable CSC
[1]	R/W	EN_GAMMA	Enable Gamma.
[0]	R/W	EN_DITHER	Enable Dithering.

3.4.2 Built-in Pattern Generator Control Register

Address Offset: 91h Access: Read/Write
Default Value: 0Ch Size: 8 bits

Table 3-93 Built-in Pattern Generator Control Register

Bit	Access	Symbol	Description
[7]	R/W	EFMCLR	Enable Frame background color Turn on this bit may disable Scaler's color and show user-defined color on LCD panel. See 0x9D, 0x9E and 0x9F for user-defined color.
[6]	R/W	ESLDSW	This bit may enable pattern generator shows 9 patterns sequentially. EFMCLR, ESLDSW — Output 2'b00 — Normal Color 2'b01 — Normal Color 2'b10 — Still pattern 2'b11 — Motion patterns
[5]	R/W	PLBIT	1: indicate 8-bit patterns 0:indicate 6-bit patterns
[4]	R/W	RESERVED	
[3:0]	R/W	PTN	Show nth pattern on LCD panel when EFMCLR is enabled When Both EFMCLR and ESLDSW are enabled, pattern generator may show 0, 1 ,2 ...up to PTNth. There are 12 parrerns we can show on LCD panel.

3.4.3 GAMMA Table Address Port Register

Address Offset: 93h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-94 GAMMA Table Address Port Register

Bit	Access	Symbol	Description
[7:0]	R/W	GAMMA_ADR	Gamma coefficient table address. The Index range is 00h~20h

3.4.4 GAMMA Table Write Data Port Register

Address Offset: 94h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-95 GAMMA Table Write Data Port Register

Bit	Access	Symbol	Description
[7:0]	R/W	GAMMA_WR_D	Gamma coefficient write data port.

3.4.5 Black Level Expansion Threshold

Address Offset: 95h Access: Read/Write
Default Value: 10h Size: 8 bits

Table 3-96 Black Level Expansion Threshold

Bit	Access	Symbol	Description
[7:0]	R/W	BLE_TH	

3.4.6 VIP Black level Expansion Gain / Offset Control Register

Address Offset: 96h Access: Read/Write
DefaultValue: 00h Size: 8 bits

Table 3-97 VIP Black level Expansion Gain / Offset Control Register

Bit	Access	Symbol	Description
[7:4]	R/W	BLE_GAIN	
[3:2]	R/W	RESERVED	
[1:0]	R/W	BLE_OFFSET	

3.4.7 CSC Y Coef

Address Offset: 97h Access: Read/Write
Default Value: 9Ah Size: 8 bits

Table 3-98 CSC Y Coef

Bit	Access	Symbol	Description
[7:0]	R/W	YCoefCSC	1.7-bit fixed point

3.4.8 CSC Red Coef of Cr

Address Offset: 98h Access: Read/Write
Default Value: A6h Size: 8 bits

Table 3-99 CSC Red Coef of Cr

Bit	Access	Symbol	Description
[7:0]	R/W	CrCoef_R	1.7-bit fixed point

3.4.9 CSC Green Coef of Cb

Address Offset: 99h Access: Read/Write
Default Value: 64h Size: 8 bits

Table 3-100 CSC Green Coef of Cb

Bit	Access	Symbol	Description
[7:0]	R/W	CbCoef_G	0.8-bit fixed point

3.4.10 CSC Green Coef of Cr

Address Offset: 9Ah Access: Read/Write
Default Value: D0h Size: 8 bits

Table 3-101 CSC Green Coef of Cr

Bit	Access	Symbol	Description
[7:0]	R/W	CrCoef_G	0.8-bit fixed point

3.4.11 CSC Blue Coef of Cb

Address Offset: 9Bh Access: Read/Write
Default Value: 81h Size: 8 bits

Table 3-102 CSC Blue Coef of Cb

Bit	Access	Symbol	Description
[7:0]	R/W	CbCoef_B	2.6-bit fixed point

3.4.12 Pattern Color Gradient & Dithering Mode Register

Address Offset: 9Ch Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-103 Pattern Color Gradient & Dithering Mode Register

Bit	Access	Symbol	Description
[7:4]	R/W	CLRGRDT[3:0]	When both ESLDSW and EFMCLR are enabled, CLRGRDT may set color gradient at pattern 2, 3 ,4, 5
[3:2]	R/W	RESERVED	
[1:0]	R/W	DITHER_MD	Dithering mode. It is enabled by register 90h.

DITHER_MD	Output
2'b00	4-bit output
2'b01	5-bit output
2'b10	6-bit output
2'b11	7-bit output

3.4.13 Frame Color Red Configuration Register

Address Offset: 9Dh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-104 Frame Color Red Configuration Register

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRRDE	8 bits of red color depth for frame color.

3.4.14 Frame Color Green Configuration Register

Address Offset: 9Eh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-105 Frame Color Green Configuration Register

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRGRN	8 bits of green color depth for frame color.

3.4.15 Frame Color Blue Configuration Register

Address Offset: 9Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-106 Frame Color Blue Configuration Register

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRBLU	8 bits of blue color depth for frame color.

3.5 OSD Register Set

(For detail OSD description, please refer to 2 Theory of Operation--OSD section.)

3.5.1 OSD Configuration Index Port Register

Address Offset: A0h Access: Write Only
Default Value: 00h Size: 8 bits

Table 3-107 OSD Configuration Index Port Register

Bit	Access	Symbol	Description
[7:0]	W	OSD_CFG_INDEX	OSD Configuration Address Port

3.5.2 OSD Configuration Data Port Register

Address Offset: A1h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-108 OSD Configuration Data Port Register

Bit	Access	Symbol	Description
[7:0]	R/W	OSD_CFG_DATA	OSD Configuration Data Port

3.5.3 OSD RAM Address Port LSB Register

Address Offset: A2h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-109 OSD RAM Address Port LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	OSD_RAM_AL	OSD RAM Address Port LSB

3.5.4 OSD RAM Address Port MSB Register

Address Offset: A3h Access: Read/Write
Default Value: 00h Size: 8 bits

Table3-110 OSD RAM Address Port MSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	OSD_RAM_AH	OSD RAM Address Port MSB

3.5.5 OSD RAM Data Port Register

Address Offset: A4h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-111 OSD RAM Data Port Register

Bit	Access	Symbol	Description
[7:0]	R/W	OSD_RAM_D	OSD RAM Data Port

3.5.6 Reserved

Address Offset: A5h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-112 Reserved

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	

3.6 LCD Output Control Register Set

3.6.1 Display Window Horizontal Start LSB Register

Address Offset: B0h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-113 Display Window Horizontal Start LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	DWHS_L	Horizontal back porch.

3.6.2 Display Window Horizontal Start MSB Register

Address Offset: B1h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-114 Display Window Horizontal Start MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	DWHS_H	Horizontal back porch

3.6.3 Display Window Vertical Start LSB Register

Address Offset: B2h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-115 Display Window Vertical Start LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	DWVS_L	Vertical back porch. When PAUTO_SYNC is enabled, DWVS_L is set by auto-detection. Writing this register does not affect panel timing control if PAUTO_SYNC is enabled.

3.6.4 Display Window Vertical Start MSB Register

Address Offset: B3h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-116 Display Window Vertical Start MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	DWVS_H	Vertical back porch. When PAUTO_SYNC is enabled, DWVS_H is set by auto-detection. Writing this register does not affect panel timing control if PAUTO_SYNC is enabled.

3.6.5 Display Window Horizontal Width LSB Register

Address Offset: B4h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-117 Display Window Horizontal Width LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	DWHSZ_L	Horizontal Active.

3.6.6 Display Window Horizontal Width MSB Register

Address Offset: B5h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-118 Display Window Horizontal Width MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	DWHSZ_H	Horizontal Active.

3.6.7 Display Window Vertical Width LSB Register

Address Offset: B6h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-119 Display Window Vertical Width LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	DWVSZ_L	Vertical Active.

3.6.8 Display Window Vertical Width MSB Register

Address Offset: B7h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-120 Display Window Vertical Width MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	DWVSZ_H	

3.6.9 Display Panel Horizontal Total Dots per Scan Line LSB Register

Address Offset: B8h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-121 Display Panel Horizontal Total Dots per Scan Line LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	PH_TOT_L	Output horizontal total dots

3.6.10 Display Panel Horizontal Total Dots per Scan Line MSB Register

Address Offset: B9h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-122 Display Panel Horizontal Total Dots per Scan Line MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	PH_TOT_H	

3.6.11 Display Panel Vertical Total Lines per Frame LSB Register

Address Offset: BAh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-123 Display Panel Vertical Total Lines per Frame LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	PV_TOT_L	Output vertical total lines

3.6.12 Display Panel Vertical Total Lines per Frame MSB Register

Address Offset: BBh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-124 Display Panel Vertical Total Lines per Frame MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	PV_TOT_H	

3.6.13 Display Panel HSYNC Width LSB Register

Address Offset: BCh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-125 Display Panel HSYNC Width LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	PH_PW_L	

3.6.14 Display Panel HSYNC Width MSB Register

Address Offset: BDh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-126 Display Panel HSYNC Width MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	PH_PW_H	

3.6.15 Display Panel VSYNC Width LSB Register

Address Offset: BEh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-127 Display Panel VSYNC Width LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	PV_PW_L	

3.6.16 Display Panel VSYNC Width MSB Register

Address Offset: BFh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-128 Display Panel VSYNC Width MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	PV_PW_H	

3.6.17 Panel Output Signal Control 1 Register

Address Offset: C0h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-129 Panel Output Signal Control 1 Register

Bit	Access	Symbol	Description
[7:6]	R/W	OUTFMT	
[5:3]	R/W	RESERVED	
[2]	R/W	POUT_CTL1[2]	PHSYNC Polarity. Default=0. POUT_CTL1[2] = 0: ACTIVE LOW POUT_CTL1[2] = 1: ACTIVE HIGH
[1]	R/W	POUT_CTL1[1]	PVSYNC Polarity. Default=0. POUT_CTL1[1] = 0: ACTIVE LOW POUT_CTL1[1] = 1: ACTIVE HIGH
[0]	R/W	POUT_CTL1[0]	PDE polarity. Default=0. POUT_CTL1[0] = 0: ACTIVE LOW POUT_CTL1[0] = 1: ACTIVE HIGH

3.6.18 Panel Output Signal Control 3 Register

Address Offset: C1h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-130 Panel Output Signal Control 3 Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3]	R/W	DCLK_INV	DCLK Polarity. Default=0. DCLK_INV = 0: Normal DCLK_INV = 1: Inverted
[2]	R/W	LVDS_MD	ODCK Internal Delay. Default=0. LVDS_MD = 0: Natinal standard LVDS_MD = 1: Korean/Non-standard

Bit	Access	Symbol	Description
[1:0]	R/W	Reserved	

3.6.19 Panel VSYNC Frame Delay Control Register

Address Offset: C2h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-131 Panel VSYNC Frame Delay Control Register

Bit	Access	Symbol	Description
[7]	R/W	VO_INTERLACE	Convert interlaced input timing for Output timing generation.
[6:5]	R/W	Reserved	
[4]	R/W	PSYNC_STR	1:Block input vsync triggering on output vsync 0: Allow input vsync to trigger output vsync
[3]	R/W	ELASTPHS	0= Short line, i.e., last hsync is less than 1.0 line 1= Long line , i.e.,last hsync is greater than 1.0 line
[2]	R/W	EN_SAVE_REC	Save recovery mode
[1]	R/W	IGNORE_VSYNC	Ignore the input VSYNC. This can be used for output free run when input VSYN is not available
[0]	R/W	Reserved	

3.6.20 Panel VSYNC Frame Delay Line Count LSB Register

Address Offset: C3h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-132 Panel VSYNC Frame Delay Line Count LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	PV_DELAY_L	

3.6.21 Panel VSYNC Frame Delay Line Count MSB Register

Address Offset: C4h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-133 Panel VSYNC Frame Delay Line Count MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	PV_DELAY_H	Delay last stage VSync output, in the unit of output HSync leading edge.

3.6.22 Output RGB Reordering Register

Address Offset: C7h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-134 Output RGB Reordering Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3]	R/W	BIGENDIANE	Reverse bit [7:0] of RGB on even channel
[2:0]	R/W	RGBSWAPE	See diagram

3.6.23 Output PLL Divider 1 Register

Address Offset: C8h Access: Read/Write
Default Value: 7Ch Size: 8 bits

Table 3-135 Output PLL Divider 1 Register

Bit	Access	Symbol	Description
[7]	R/W	Reserved	
[6:0]	R/W	PLLDIV_F	PLL feedback divider. Default=124.

3.6.24 Output PLL Divider 2 Register

Address Offset: C9h Access: Read/Write
Default Value: 1Bh Size: 8 bits

Table 3-136 Output PLL Divider 2 Register

Bit	Access	Symbol	Description
[7:5]	R/W	Reserved	
[4:0]	R/W	PLLDIV_I	PLL Input Divider. Default=27.

3.6.25 Output PLL Divider 3 Register

Address Offset: CAh Access: Read/Write
Default Value: 01h Size: 8 bits

Table 3-137 Output PLL Divider 3 Register

Bit	Access	Symbol	Description
[7:6]	R/W	PLLMX	PLL MUX Function Select PLLMX: Mode 2'b00: PLLCLK 2'b01: Bypass PLL 2'b10: Keep High 2'b11: Keep High
[5]	R/W	Reserved	1-bit register exists, but R/W doesn't affect T702
[4]	R/W	Reserved	1-bit register exists, but R/W doesn't affect T702
[3:2]	R/W	Reserved	
[1:0]	R/W	PLLDIV_O	PLL Output Divider. Default=1.

3.6.26 Reserved

Address Offset: CBh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-138 Reserved

Bit	Access	Symbol	Description
[7:0]	R/W	Reserved	PLL Configuration Register. For test mode only. Set 00h forever

3.6.27 Horizontal Main Display Start

Address Offset: D8h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-139 Horizontal Main Display Start

Bit	Access	Symbol	Description
[7:0]	R/W	HMDISP_STR	

3.6.28 Horizontal Main Display Start

Address Offset: D9h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-140 Horizontal Main Display Start

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	HMDISP_STR	

3.6.29 Vertical Main Display Start

Address Offset: DAh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-141 Vertical Main Display Start

Bit	Access	Symbol	Description
[7:0]	R/W	VMDISP_STR	

3.6.30 Vertical Main Display Start

Address Offset: DBh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-142 Vertical Main Display Start

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	VMDISP_STR	

3.6.31 Horizontal Main Display Size

Address Offset: DCh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-143 Horizontal Main Display Size

Bit	Access	Symbol	Description
[7:0]	R/W	HMDISP_SIZE	

3.6.32 Horizontal Main Display Size

Address Offset: DDh Access: Read/Write
Default Value: 05h Size: 8 bits

Table 3-144 Horizontal Main Display Size

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	HMDISP_SIZE	

3.6.33 Vertical Main Display Size

Address Offset: DEh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-145 Vertical Main Display Size

Bit	Access	Symbol	Description
[7:0]	R/W	VMDISP_SIZE	

3.6.34 Vertical Main Display Size

Address Offset: DFh Access: Read/Write
Default Value: 04h Size: 8 bits

Table 3-146 Vertical Main Display Size

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	VMDISP_SIZE	

3.6.35 Power Management Control Register

Address Offset: E0h Access: Read/Write
Default Value: 0Ah Size: 8 bits

Table 3-147 Power Management Control Register

Bit	Access	Symbol	Description
[7]	R/W	TPDB	Default=1. When writing 0 to this bit, power down whole chip/pull down pads.
[6]	R/W	PDMD	Power Down Mode. 1:Whole chip power down 0:Output pads pull down
[5]	R/W	PDADC_B	Power Down ADC. Low active.
[4]	R/W	PDC_B	Power Down Comb Video Decoder. For internal software test. Low active.
[3]	R/W	PDVPLL	Power down DisplayPLL
[2]	R/W	PDMPLL	Power down MPLL
[1]	R/W	RESERVED	
[0]	R/W	PWDNTC	Power down TC interface. Low active

3.6.36 Output Pin Configuration

Address Offset: E1h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-148 Output Pin Configuration

Bit	Access	Symbol	Description
[7:6]	R/W	RowSTV_Sel	RowSTV_Sel / Mode 2'b00 / Output both 2'b01 / Output both 2'b10 / Output STV1 2'b11 / Output STV2

Bit	Access	Symbol	Description
[5:4]	R/W	ColSTH_Sel	ColSTH_Sel / Mode 2'b00 / Output both 2'b01 / Output both 2'b10 / Output STH1 2'b11 / Output STH2
[3]	R/W	UD_SEL	
[2]	R/W	LR_SEL	
[1:0]	R/W	RESERVED	

3.6.37 DAC Power Management

Address Offset: E3h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-149 DAC Power Management

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3]	R/W	SL	
[2]	R/W	SLR	
[1]	R/W	SLG	
[0]	R/W	SLB	

3.6.38 PWM General Control Register

Address Offset: E8h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-150 PWM General Control Register

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[4]	R/W	VPWME	Enable Volume PWM
[3]	R/W	RESERVED	
[2:0]	R/W	VPWM_FREQ_SEL	This register allow base clock has 7 types of clock freqs divided from XCLK . 000 = XCLK 001 = XCLK/2^5 010 = XCLK/2^7 011 =XCLK/2^9 100 =XCLK/2^11 101= XCLK/2^13 110=XCLK/2^15 111=XCLK/2^17

3.6.39 PWM Active High Time Counter Register

Address Offset: E9h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-151 PWM Active High Time Counter Register

Bit	Access	Symbol	Description
[7:0]	R/W	VPWM_HIGH	This register may allow volume PWM high time counted by base clock The based clock is divide from XCLK , see 0xE8[2:0]

3.6.40 Serial Bus Slave Device Address Register

Address Offset: F0h Access: Read/Write
Default Value: 40h Size: 8 bits

Table 3-152 Serial Bus Slave Device Address Register

Bit	Access	Symbol	Description
[7:4]	R/W	SDADDR	
[3:0]	R/W	Reserved	

3.6.41 2-wire/4-wire Serial Bus Select Register

Address Offset: F1h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-153 2-wire/4-wire Serial Bus Select Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3]	R/w	XBUS_EN	Enable XBUS for purpose of test moe.
[2]	R/W	I2CATINCADR	Enable 2-wire serial bus automatic address increment in multiple R/W Access mode. Default=1'b1. Mode: INC 1'b0: STOP INC 1'b1: Auto INC
[1:0]	R/W	Reserved	

3.6.42 Reserved

Address Offset: F2h Access: Read Only
Default Value: 00h Size: 8 bits

Table 3-154 Reserved

Bit	Access	Symbol	Description
[7:0]	R	Reserved	

3.6.43 Vendor ID 1 Register

Address Offset: F3h Access: Read Only
Default Value: 54h Size: 8 bits

Table 3-155 Vendor ID 1 Register

Bit	Access	Symbol	Description
[7:0]	R	VID_L	Reading this register obtains ASCII code “T”. Hex value is 54h

3.6.44 Vendor ID 2 Register

Address Offset: F4h Access: Read Only
Default Value: 57h Size: 8 bits

Table 3-156 Vendor ID 2 Register

Bit	Access	Symbol	Description
[7:0]	R	VID_H	Reading this register obtains ASCII code “W”.

3.6.45 Device ID Register

Address Offset: F5h Access: Read Only
Default Value: C1h Size: 8 bits

Table 3-157 Device ID Register

Bit	Access	Symbol	Description
[7:0]	R	DID	This field puts a part number in Hex “C1”.

3.6.46 Revision ID Register

Address Offset: F6h Access: Read Only
Default Value: A1h Size: 8 bits

Table 3-158 Revision ID Register

Bit	Access	Symbol	Description
[7:0]	R	RID	This field puts a revision number in Hex “A1”.

3.6.47 Page Select Register

Address Offset: FFh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-159 Page Select Register

Bit	Access	Symbol	Description
[7:3]	R/W	RESERVED	
[2:0]	R/W	PAGE[2:0]	

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3.7 TCON Register Set

3.7.1 Timing Controller (TCON) Control Register

Address Offset: 20h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-160 Timing Controller (TCON) Control Register

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	RESERVED	
[5]	R/W	GTOE	Enable gate driver output Mode Type 0 Shutdown output 1 Enable
[4]	R/W	RESERVED	
[3]	R/W	RESERVED	
[2]	R/W	RESERVED	
[1]	R/W	RESERVED	
[0]	R/W	PNINV	Enable line-inverted function.

3.7.2 Timing Protocol & Polarity Control Register

Address Offset: 21h Access: Read/Write
Default Value: 7Fh Size: 8 bits

Table 3-161 Timing Protocol & Polarity Control Register

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	GTOEPL	This bit may control GOE polarity Mode Type 0 Low-active 1 Highactive
[5]	R/W	STVPL	Row Driver start pulse polarity Mode Type 0 Negative 1 Positive
[4]	R/W	CLKVPL	Data Inversion Polarity Mode Type 0 Negative 1 Positive
[3]	R/W	INVOPL	Data Inversion Polarity Mode Type 0 Negative 1 Positive

[2]	R/W	POLPL	Column Driver POL inversion polarity Mode Type 0 Negative 1 Positive
[1]	R/W	LPPL	Column Driver Latch Pulse polarity Mode Type 0 Negative 1 Positive
[0]	R/W	STHPL	Column Driver Start Pulse polarity Mode Type 0 Negative 1 Positive

3.7.3 Column Driver Latch Pulse Placement LSB Register

Address Offset: 22h Access: Read/Write
Default Value: 03h Size: 8 bits

Table 3-162 Column Driver Latch Pulse Placement LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	CDLPPLM[7:0]	This register allows LP to place between 2 DE pulses counted by LLCK dot clock The reference point is the rising edge of DE.

3.7.4 Column Driver Latch Pulse Placement MSB Register

Address Offset: 23h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-163 Column Driver Latch Pulse Placement MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	CDLPPLM[11:8]	This register allows LP to place between 2 DE pulses counted by LLCK dot clock The reference point is the rising edge of DE.

3.7.5 Column Driver Latch Pulse Duration Control Register

Address Offset: 24h Access: Read/Write
Default Value: 21h Size: 8 bits

Table 3-164 Column Driver Latch Pulse Duration Control Register

Bit	Access	Symbol	Description
[7:0]	R/W	CDLPDU[7:0]	This register allows LP duration programmable. counted by LLCK dot clock.

3.7.6 POL Placement LSB Register

Address Offset: 25h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-165 POL Placement LSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	POLPLM[7:0]	The reference point is the leading edge of DE.

3.7.7 POL Placement MSB Register

Address Offset: 26h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-166 POL Placement MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	POLPLM[11:8]	The reference point is the leading edge of DE.

3.7.8 CLKV Placement LSB Register

Address Offset: 27h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-167 CLKV Placement LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	CLKVPLM[7:0]	The reference point is the leading edge of DE

3.7.9 CLKV Placement MSB Register

Address Offset: 28h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-168 CLKV Placement MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	CLKVPLM[11:8]	The reference point is the leading edge of DE

3.7.10 CLKV Duration LSB Register

Address Offset: 29h Access: Read/Write
Default Value: 0Fh Size: 8 bits

Table 3-169 CLKV Duration LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	CLKVDU[7:0]	The reference point is leading edge of DE

3.7.11 CLKV Duration MSB Register

Address Offset: 2Ah Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-170 CLKV Duration MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	CLKVDU[11:8]	The reference point is the leading edge of DE

3.7.12 STH Position Placement Register

Address Offset: 2Bh Access: Read/Write
Default Value: 01h Size: 8 bits

Table 3-171 STH Position Placement Register

Bit	Access	Symbol	Description
[7:2]	R/W	RESERVED	
[1:0]	R/W	STHPLM[1:0]	This register allows STH lead DE 0, 1 or 2 CLKHs Mode Type 2'b00 0 CLKH 2'b01 1 CLKH 2'b1x 2 CLKHs

3.7.13 Reserved

Address Offset: 2Ch Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-172 Reserved

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	

3.7.14 Gate Driver Predriving

Address Offset: 2Dh Access: Read/Write
Default Value: 05h Size: 8 bits

Table 3-173 Gate Driver Predriving

Bit	Access	Symbol	Description
[7:0]	R/W	GDPreDu	

3.7.15 Reserved

Address Offset: 2Eh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-174 Reserved

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	

3.7.16 Reserved

Address Offset: 2Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-175 Reserved

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	

3.7.17 Row Driver Configuration Register

Address Offset: 30h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-176 Row Driver Configuration Register

Bit	Access	Symbol	Description
[7:1]	R/W	RESERVED	
[0]	R/W	ESTVOFFSET	

3.7.18 Gate Driver OE Pulse Position Placement LSB Register

Address Offset: 31h Access: Read/Write
Default Value: 0Fh Size: 8 bits

Table 3-177 Gate Driver OE Pulse Position Placement LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	GOEPL[7:0]	

3.7.19 Gate Driver OE Pulse Position Placement MSB Register

Address Offset: 32h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-178 Gate Driver OE Pulse Position Placement MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	GOEPL[11:8]	

3.7.20 Gate Driver OE Pulse Duration LSB Register

Address Offset: 33h Access: Read/Write
Default Value: 0Fh Size: 8 bits

Table 3-179 Gate Driver OE Pulse Duration LSB Register

Bit	Access	Symbol	Description
[7:0]	R/W	GOEDU[7:0]	

3.7.21 Gate Driver OE Pulse Duration MSB Register

Address Offset: 34h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-180 Gate Driver OE Pulse Duration MSB Register

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	GOEDU[11:8]	

3.7.22 STV Offset Register

Address Offset: 35h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-181 STV Offset Register

Bit	Access	Symbol	Description
[7:0]	R/W	STVOFF[7:0]	

3.8 ITU - 656 Decoder Register Set

3.8.1 ITU-656 Decoder HS Delay

Address Offset: D0h Access: Read/Write
Default Value: 30h Size: 8 bits

Table 3-182 ITU-656 Decoder HS Delay

Bit	Access	Symbol	Description
[7:0]	R/W	HS_DELAY656[7:0]	Unit: Cycles of Half VCLK

3.8.2 ITU-656 Decoder HS Delay

Address Offset: D1h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-183 ITU-656 Decoder HS Delay

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	
[3:0]	R/W	HS_DELAY656[11:8]	

3.8.3 ITU-656 Decoder HS Pulse Width

Address Offset: D2h Access: Read/Write
Default Value: 20h Size: 8 bits

Table 3-184 ITU-656 Decoder HS Pulse Width

Bit	Access	Symbol	Description
[7:0]	R/W	HS_WIDTH656[7:0]	Unit: Cycles of Half VCLK

3.8.4 ITU-656 Decoder VS Delay

Address Offset: D3h Access: Read/Write
Default Value: 01h Size: 8 bits

Table 3-185 ITU-656 Decoder VS Delay

Bit	Access	Symbol	Description
[7:0]	R/W	VS_DELAY656[7:0]	Unit: HS

3.8.5 ITU-656 Decoder VS Pulse Width

Address Offset: D4h Access: Read/Write
Default Value: 01h Size: 8 bits

Table 3-186 ITU-656 Decoder VS Pulse Width

Bit	Access	Symbol	Description
[7:0]	R/W	RESERVED	
[3:0]	R/W	VS_WIDTH656[3:0]	Unit: HS

3.8.6 ITU-656 Decoder HDE Start

Address Offset: D5h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-187 ITU-656 Decoder HDE Start

Bit	Access	Symbol	Description
[7:0]	R/W	HSTART656[7:0]	Unit: Pixel

3.8.7 ITU-656 Decoder HDE Start

Address Offset: D6h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-188 ITU-656 Decoder HDE Start

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	HSTART656[11:8]	Unit: Pixel

3.8.8 ITU-656 Decoder HDE Size

Address Offset: D7h Access: Read/Write
Default Value: D0h Size: 8 bits

Table 3-189 ITU-656 Decoder HDE Size

Bit	Access	Symbol	Description
[7:0]	R/W	HSIZE656[7:0]	Unit: Pixel

3.8.9 ITU-656 Decoder HDE Size

Address Offset: D8h Access: Read/Write
Default Value: 02h Size: 8 bits

Table 3-190 ITU-656 Decoder HDE Size

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/w	HSIZE656[11:8]	Unit: Pixel

3.8.10 ITU-656 Decoder Odd Field VDE Start

Address Offset: D9h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-191 ITU-656 Decoder Odd Field VDE Start

Bit	Access	Symbol	Description
[7:0]	R/W	OVSTART656[7:0]	Unit: HS

3.8.11 ITU-656 Decoder Odd/Even Field VDE Start

Address Offset: DAh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-192 ITU-656 Decoder Odd/Even Field VDE Start

Bit	Access	Symbol	Description
[7]	R/W	EVPluse1	Even Filed VDE Start 1: EVSTART656=OVSTART + 1 0: EVSTART656=OVSTART
[6:4]	R/W	RESERVED	
[3:0]	R/W	OVSTART656[11:8]	Odd Filed VDE Start Unit: HS

3.8.12 ITU-656 Decoder VDE Size

Address Offset: DBh Access: Read/Write
Default Value: F0h Size: 8 bits

Table 3-193 ITU-656 Decoder VDE Size

Bit	Access	Symbol	Description
[7:0]	R/W	VSIZE656[7:0]	Unit: HS

3.8.13 ITU-656 Decoder VDE Size

Address Offset: DCh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-194 ITU-656 Decoder VDE Size

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3:0]	R/W	VSIZE656[11:8]	Unit: HS

3.8.14 ITU-656 Decoder VCLK Tuning

Address Offset: DEh Access: Read/Write
Default Value: 02h Size: 8 bits

Table 3-195 ITU-656 Decoder VCLK Tuning

Bit	Access	Symbol	Description
[7:2]	R/W	RESERVED	
[1]	R/W	VCLK_INV	
[0]	R/W	VCLK_DLY	Unit: 2ns

3.8.15 ITU-656 Decoder Format Control

Address Offset: DFh Access: Read/Write
Default Value: 4Ch Size: 8 bits

Table 3-196 ITU-656 Decoder Format Control

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6]	R/W	ODDF_INV	Filed flag indicator 0: 1st field =0, 2nd field=1 1: 1st filed =1, 2nd field=0
[5:4]	R/W	RESERVED	
[3]	R/W	UV_ALN	UV Align

[2]	R/W	UV_INTPL	422-444 UV Interpolation
[1]	R/W	SIZE_DET	Read back Size of HDE and VDE 1:Enable 0:Disable
[0]	R/W	URBK_DET	1:Keep previous detection 0:Update current detection

3.9 Y/C Separation and Chroma Decoder Register Set

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3.9.1 Video Source Selection of Comb Filter

Address Offset: 00h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-197 Video Source Selection of Comb Filter

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6:5]	R/W	HPIX	These bits select the number of pixel per scan line. Standard / pixels/line / HPIX NTSC, PAL(M) / 858 / 00 PAL(B,D,G,H,I,N,CN),SECAM / 864 / 01 NTSC Square Pixel, PAL(M) Square Pixel / 780 / 10 PAL(B,D,G,H,I,N) Square Pixel / 944 / 11
[4]	R/W	VSLine_625	This bit selects the number of scan lines per frame. 0 = 525 (default) 1 = 625
[3:1]	R/W	STD_MD	These bits select Standard Definition TV video mode. 000 = NTSC (default) 001 = PAL (I,B,G,H,D,N) 010 = PAL (M) 011 = PAL (CN) 100 = SECAM
[0]	R/W	YC_SEL	This selects input video format. 0 = CVBS composite (default) 1 = S-Video (separated Y/C)

3.9.2 Bandwidth Control

Address Offset: 01h Access: Read/Write
Default Value: 01h Size: 8 bits

Table 3-198 Bandwidth Control

Bit	Access	Symbol	Description
[7]	R/W	CMPV_INV	This bit inverts the select signal for the analog input multiplexer during component video mode. 0 = not inverted (default) 1 = inverted
[6]	R/W	CMPV_SEL	0= S-video or CVBS 1 =YPbPr compoent video input

Bit	Access	Symbol	Description
[5:4]	R/W	LUMA_NOTCH_BW	These bits select luma notch width 00 = none (default) 01 = narrow 10 = medium 11 = wide
[3:2]	R/W	CHROMA_LP_BW	This bit set the chroma low pass filter to wide or narrow 0 = narrow (default) 1 = wide 2 = extra wide 3 = extra wide
[1]	R/W	CHROMA_BST5OR10	This bit selects the burst gate width 0 = 5 subcarrier clock cycles (default) 1 = 10 subcarrier clock cycles
[0]	R/W	PedBlk	This bit enables black level correction for 7.5 blank-to-black pedestal. 0 = no pedestal subtraction 1 = pedestal subtraction (default)

3.9.3 Y/C AGC Enable

Address Offset: 02h
Default Value: 4Fh
Access: Read/Write
Size: 8 bits

Table 3-199 Y/C AGC Enable

Bit	Access	Symbol	Description
[7]	R/W	Hagc_field_mode	When this bit is “0” (the default), then the gain is updated once per line, after DC clamping. When this bit is set, then the gain is only updated once per field, at the start of vertical blank. 0 = off (default) 1 = on
[6]	R/W	MV_hagc_mode	Set 1 to automatically reduce the gain (set in register P2_04) by 25% when macro-vision encoded signals are detected 0 = off 1 = on (default)
[5:4]	R/W	DC_clamp_mode	Analog front end DC clamping 00 = auto (default) 01 = backporch only 10 = synctip only 11 = off
[3]	R/W	Dagc_en	Set 1 to enable the digital AGC. The digital AGC is used in series with the analog gain. 0 = off 1 = on (default)
[2]	R/W	RESERVED	
[1]	R/W	Cagc_en	Set 1 to enable the chroma AGC. If disabled, then the AGC target is used to drive directly the AGC gain. 0 = off 1 = on (default)
[0]	R/W	Hagc_en	Set 1 to enable the luma/composite AGC. If disabled, then the AGC target (P2_04h) is used to drive directly the AGC gain. 0 = off 1 = on (default)

3.9.4 Comb Filtering Mode

Address Offset: 03h Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-200 Comb Filtering Mode

Bit	Access	Symbol	Description
[7:4]	R/W	RESERVED	
[3]	R/W	Color_trap	This bit enables the notch-filter at the luma path after the comb filter. This filter can be turned on or off irrespective of the adaptive mode setting. 0 = Disabled (default) 1 = Enabled
[2:0]	R/W	Adaptive_mode	These bits select modes for the composite signal's luma (Y) and chroma (C) separation before color demodulation. 000 = fully adaptive comb (2-D adaptive comb) (default) 001 = vertical adaptive comb (1-D adaptive comb, vertical comb only) 010 = 5-tap adaptive comb filter (PAL mode only) 011 = basic luma notch filter mode (for very noisy and unstable pictures) 100 = simple 2-tap comb 101 = simple 3-tap comb 110 = 5-tap hybrid adaptive comb filter (PAL mode only)

3.9.5 Luma AGC Target Value

Address Offset: 04h Access: Read/Write
Default Value: DDh Size: 8 bits

Table 3-201 Luma AGC Target Value

Bit	Access	Symbol	Description
[7:0]	R/W	Hagc	These bits specify the luma AGC target value. The gain of the AGC is modified until the horizontal sync height is equal to this value. Note that if a MacroVision signal is detected and "MV_hagc_mode" (P2_02[6]) is set, then this value is automatically reduced by 25%. Standard / Programming Value: NTSC M: DDh (221d) (default) NTSC J: CDh (205d) PAL B,D,G,H,I, COMB N, SECAM: DCh (220d) PAL M,N: DDh (221d) NTSC M (MACROVISIOIN): A6h (166d) PAL B,D,G,H,I, COMB N (MACROVISION): AEh (174d) If "Hagc_en" (P2_02[0]) is "0", then "Hagc" is used to directly drive the analog gain. In this case, a value of 64 represents a unity gain, 32 represents a one-half gain, and 128 denotes a double gain.

3.9.6 Noise Threshold

Address Offset: 05h Access: Read/Write
Default Value: 32h Size: 8 bits

Table 3-202 Noise Threshold

Bit	Access	Symbol	Description
[7:0]	R/W	noise_thresh	This value sets the noise value at which the circuit considers a signal noisy. The detected noise value may be read back through register P2_7Fh (“status_noise”). If the detected noise value is greater than “noise_thresh”, then register P2_3C[3] (“noisy”) is set. Larger values of “status_noise” indicate noisier signals, so larger values of “noise_thresh” decreases the likelihood of “noisy” being set while smaller values of “noise_thresh” increases the likelihood of “noisy” being set. Default = 50.

3.9.7 Y/C Output Control

Address Offset: 07h Access: Read/Write
Default Value: 20h Size: 8 bits

Table 3-203 Y/C Output Control

Bit	Access	Symbol	Description
[7:5]	R/W	RESERVED	
[6]	R/W	cbcr_swap	This bit swaps Cb/Cr outputs. 0 = don’t swap Cb/Cr (default) 1 = swap Cb/Cr
[5:4]	R/W	blue_mode	This bit controls the blue screen mode. 00 = Disabled 01 = Enabled 10 = Auto (Default) 11 = reserved
[3:0]	R/W	yc_delay	This 2’s complement number controls the output delay between luma and chroma. Negative values shift luma outputs to the left while positive values shift luma values to the right. The range is [-5,7]. Default = 0.

3.9.8 Luma Contrast

Address Offset: 08h Access: Read/Write
Default Value: 80h Size: 8 bits

Table 3-204 Luma Contrast

Bit	Access	Symbol	Description
[7:0]	R/W	contrast	These bits control the adjustable gain to the luma output path. Default = 128.

3.9.9 Luma Brightness

Address Offset: 09h Access: Read/Write
Default Value: 20h Size: 8 bits

Table 3-205 Luma Brightness

Bit	Access	Symbol	Description
[7:0]	R/W	brightness	These bits control the adjustable brightness level to the luma output path. This value is offset by -32, i.e., a value of 32 (the default) implies a brightness level of 0, and a value of 0 implies a brightness level of -32.

3.9.10 Chroma Saturation

Address Offset: 0Ah Access: Read/Write
Default Value: 80h Size: 8 bits

Table 3-206 Chroma Saturation

Bit	Access	Symbol	Description
[7:0]	R/W	saturation	These bits adjust the color saturation. Default = 128.

3.9.11 Chroma Hue Phase

Address Offset: 0Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-207 Chroma Hue Phase

Bit	Access	Symbol	Description
[7:0]	R/W	hue	This 2's complement number adjusts the hue phase offset. Default = 0.

3.9.12 Chroma AGC

Address Offset: 0Ch Access: Read/Write
Default Value: 8Ah Size: 8 bits

Table 3-208 Chroma AGC

Bit	Access	Symbol	Description
[7:0]	R/W	cage	These bits set the chroma AGC target. Default = 138.

3.9.13 Chroma Kill

Address Offset: 0Dh Access: Read/Write
Default Value: 07h Size: 8 bits

Table 3-209 Chroma Kill

Bit	Access	Symbol	Description
[7]		RESREVED	
[6]	R/W	user_ckill_mode	0: uses auto hardware chroma kill. 1: forces chroma kill on Default=0.
[5]	R/W	vbi_ckill	When set, chroma is killed during VBI. Default = 0.
[4]	R/W	hlock_ckill	When set, chroma is killed whenever horizontal lock is lost. Default = 0.
[3:0]	R/W	ckill	These bits set the chroma kill level. Default = 7.

3.9.14 Chroma Auto-Position

Address Offset: 0Fh Access: Read/Write
Default Value: 0Ch Size: 8 bits

Table 3-210 Chroma Auto-Position

Bit	Access	Symbol	Description
[7:6]	R/W	RESERVED	
[5]	R/W	fixed_burstgate	When set, this bit disables the burst gate autoposition. The manual burstgate window position is defined by the burst_gate_start(P2_2C) and burst_gate_end (P2_2D) register. Default = 0.
[4:0]	R/W	cautopos	These bits set the chroma burst gate position relative to the auto centre position. Default = 12.

3.9.15 AGC Peak Nomial

Address Offset: 10h Access: Read/Write
Default Value: 0Ah Size: 8 bits

Table 3-211 AGC Peak Nomial

Bit	Access	Symbol	Description
[7]	R/W	RESERVED	
[6:0]	R/W	Agc_peak_nominal	These bits set the luma peak white detection's AGC nominal peak white value. This value is added to 128 and then the result is multiplied by 4. Default = 10.

3.9.16 AGC Peak and Gate Control

Address Offset: 11h Access: Read/Write
Default Value: A9h Size: 8 bits

Table 3-212 AGC Peak and Gate Control

Bit	Access	Symbol	Description
[7]	R/W	Agc_gate_vsync_coarse	This bit forces coarse sync-tip and backporch gates to be used during vsync when VCRs are detected Default = 1.
[6]	R/W	Agc_gate_vsync_stip	This bit forces sync-tip clamping during vsync. Default = 0.
[5:4]	R/W	Agc_gate_kill_mode	These bits determine the method that sync-tip and backporch gates are suppressed: 00 = off 01 = enabled – if sync-tip gate is killed, kill backporch gate 10 = enabled – if sync-tip gate is killed, kill backporch gate, except during vsync 11 = enabled – if sync-tip gate is killed, do not kill backporch gate (default)
[3]	R/W	Agc_peak_en	This bit enables the AGC peak white detector. Default = 1.
[2:0]	R/W	Agc_peak_cntl	These bits set the time constant for the AGC peak white detector. Default = 1.

3.9.17 Lock Count

Address Offset: 16h Access: Read/Write
Default Value: 74h Size: 8 bits

Table 3-213 Lock Count

Bit	Access	Symbol	Description
[7:4]	R/W	locked_cnt_noisy_max	These bits set the max value of the hlock sensor for noisy signals. 8 is added to this value. Default = 7 stands for 15.
[3:0]	R/W	locked_cnt_clean_max	These bits set the max value of the hlock sensor for clean signals. 8 is added to this value. Default = 4 stands for 12.

3.9.18 H Loop Max State

Address Offset: 17h Access: Read/Write
Default Value: CBh Size: 8 bits

Table 3-214 H Loop Max State

Bit	Access	Symbol	Description
[7:6]	R/W	hlock_vsync_mode	These bits control hsync locking during vsync: 00 = disabled 01 = enabled 10 = enabled except for noisy signals 11 = enabled only for VCR signals (default)
[5]	R/W	hstate_fixed	This bit when set forces the state machine to remain in the state set in “hstate_max”. Default = 0.
[4]	R/W	disable_hfine	This bit, when set, disables the fine mode of the HPLL phase comparator. Default = 0.
[3]	R/W	hstate_unlocked	This bit sets the state when unlocked. default = 1.
[2:0]	R/W	hstate_max	These bits set the maximum state for the horizontal PLL state machine. The range of this register is 0 to 5, inclusive. Higher states have a finer PLL control. Values of “0” and “1” should not programmed into this register. If “hstate_fixed” is set, then this register is used to force the state. Default = 3.

3.9.19 Chroma DTO Incremental 0

Address Offset: 18h Access: Read/Write
Default Value: 21h Size: 8 bits

Table 3-215 Chroma DTO Incremental 0

Bit	Access	Symbol	Description
[7]	R/W	cdto_fix	1: Fix Chroma DTO at center frequency 0: Chroma DTO assigned by registers
[6]		RESERVED	
[5:0]	R/W	cdto_inc[29:24]	These bits contain bits 29:24 of the 30-bit-wide chroma DTO increment.

3.9.20 Chroma DTO Incremental 1

Address Offset: 19h Access: Read/Write
Default Value: F0h Size: 8 bits

Table 3-216 Chroma DTO Incremental 1

Bit	Access	Symbol	Description
[7:0]	R/W	cdto_inc[23:16]	These bits contain bits 23:16 of the 30-bit-wide chroma DTO increment.

3.9.21 Chroma DTO Incremental 2

Address Offset: 1Ah Access: Read/Write
Default Value: 7Ch Size: 8 bits

Table 3-217 Chroma DTO Incremental 2

Bit	Access	Symbol	Description
[7:0]	R/W	cdto_inc[15:8]	These bits contain bits 15:8 of the 30-bit-wide chroma DTO increment.

3.9.22 Chroma DTO Incremental 3

Address Offset: 1Bh Access: Read/Write
Default Value: 0Fh Size: 8 bits

Table 3-218 Chroma DTO Incremental 3

Bit	Access	Symbol	Description
[7:0]	R/W	cdto_inc[7:0]	These bits contain bits 7:0 of the 30-bit-wide chroma DTO increment.

3.9.23 Horizontal Sync DTO Incremental 0

Address Offset: 1Ch Access: Read/Write
Default Value: 20h Size: 8 bits

Table 3-219 Horizontal Sync DTO Incremental 0

Bit	Access	Symbol	Description
[7]	R/W	hdto_fix	1: Fix Hsync DTO at center frequency 0: Hsync DTO assigned by registers
[6]		RESRVED	
[5:0]	R/W	hdto_inc[29:24]	These bits contain bits 29:24 value of the 30-bit-wide horizontal sync DTO increment.

3.9.24 Horizontal Sync DTO Incremental 1

Address Offset: 1Dh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-220 Horizontal Sync DTO Incremental 1

Bit	Access	Symbol	Description
[7:0]	R/W	hdto_inc[23:16]	These bits contain bits 23:16 value of the 30-bit-wide horizontal sync DTO increment.

3.9.25 Horizontal Sync DTO Incremental 2

Address Offset: 1Eh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-221 Horizontal Sync DTO Incremental 2

Bit	Access	Symbol	Description
[7:0]	R/W	hdto_inc[15:8]	These bits contain bits 15:8 value of the 30-bit-wide horizontal sync DTO increment.

3.9.26 Horizontal Sync DTO Incremental 3

Address Offset: 1Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-222 Horizontal Sync DTO Incremental 3

Bit	Access	Symbol	Description
[7:0]	R/W	hdto_inc[7:0]	These bits contain bits 7:0 value of the 30-bit-wide horizontal sync DTO increment.

3.9.27 Horizontal Sync Rising Edge Occurrence Time

Address Offset: 20h Access: Read/Write
Default Value: 3Eh Size: 8 bits

Table 3-223 Horizontal Sync Rising Edge Occurrence Time

Bit	Access	Symbol	Description
[7:0]	R/W	hsync_rising	These bits set the position of the expected hsync rising edge. It is used by the fine hsync detector. The fine detector uses this time position to sample the video signal for the rising edge of the hsync. Default = 62

3.9.28 Chroma Burst Gate Start Time

Address Offset: 2Ch Access: Read/Write
Default Value: 23h Size: 8 bits

Table 3-224 Chroma Burst Gate Start Time

Bit	Access	Symbol	Description
[7:0]	R/W	burst_gate_start	This specifies the beginning of the burst gate window. Note that this window is set to be bigger than the burst. The automatic burst position tracker finds the burst within this window. Default = 35

3.9.29 Chroma Burst Gate End Time

Address Offset: 2Dh Access: Read/Write
Default Value: 64h Size: 8 bits

Table 3-225 Chroma Burst Gate End Time

Bit	Access	Symbol	Description
[7:0]	R/W	burst_gate_end	These bits specifies the end of the burst gate window Default = 100

3.9.30 Active Video Horizontal Start Time

Address Offset: 2Eh Access: Read/Write
Default Value: 82h Size: 8 bits

Table 3-226 Active Video Horizontal Start Time

Bit	Access	Symbol	Description
[7:0]	R/W	hactive_start	These bits control the active video line time interval. This specifies the beginning of active line. This register is used to centre the horizontal position, and can be used to crop the image to a smaller size. Default = 130.

3.9.31 Active Video Horizontal Width

Address Offset: 2fh Access: Read/Write
Default Value: 50h Size: 8 bits

Table 3-227 Active Video Horizontal Width

Bit	Access	Symbol	Description
[7:0]	R/W	hactive_width	These bits control the active video line time interval. This register specifies the width of the active line, and can be used to crop the image to a smaller size. The value 640 is added to this register. Default = 80 stands for 640+80 = 720

3.9.32 Active Video Vertical Start

Address Offset: 30h Access: Read/Write
Default Value: 22h Size: 8 bits

Table 3-228 Active Video Vertical Start

Bit	Access	Symbol	Description
[7:0]	R/W	vactive_start	These bits control the first active video line in a field. This specifies the number of half lines from the start of a field. Default = 34.

3.9.33 Active Video Vertical Height

Address Offset: 31h Access: Read/Write
Default Value: 61h Size: 8 bits

Table 3-229 Active Video Vertical Height

Bit	Access	Symbol	Description
[7:0]	R/W	vactive_height	These bits control the active video height. This specifies the height by the number of half lines. The value 384 is added to this register. Default = 97 stands for 394+97 = 481 half lines

3.9.34 Vsync Time Constant

Address Offset: 39h Access: Read/Write
Default Value: 0Ah Size: 8 bits

Table 3-230 Vsync Time Constant

Bit	Access	Symbol	Description
[7]	R/W	field_polarity	This bit sets the output field polarity. 0 : field=1 for odd fields, field=0 for even fields (default) 1 : field=0 for odd fields, field=1 for even fields
[6]	R/W	flip_field	This bit flips even/odd fields
[5]	R/W	veven_delayed	This bit delays detection of even fields by 1 vertical line Default = 0.
[4]	R/W	vodd_delayed	This bit delays detection of odd fields by 1 vertical line Default = 0.
[3:2]	R/W	field_detect_mode	These bits control the field detection logic. Default = 2.
[1:0]	R/W	vloop_tc	These bits set the vertical PLL time constant 0 = fast. Only useful if the vloop_cntl register is not 11. Internal values are 2 and 1. 1 = moderate. Internal values are 1 and ¼. 2 = slow. Internal values are ½ and 1/16 (default) 3 = very slow. Most useful for noisy signals. Internal values are ¼ and ½

3.9.35 Comb Video Status Register 1

Address Offset: 3Ah Access: Read only
Default Value: 00h Size: 8 bits

Table 3-231 Comb Video Status Register 1

Bit	Access	Symbol	Description
[7:5]	R	mv_colourstripes	Macrovision color stripes detected. The number indicates the number of colour stripe lines in each group

[4]	R	mv_vbi_detected	MacroVision VBI pseudo-sync pulses detection 1 = Detected 0 = Undetected
[3]	R	chromalock	Chroma PLL locked to color burst 1 = Locked 0 = Unlocked
[2]	R	vlock	Vertical lock 1 = Locked 0 = Unlocked
[1]	R	hlock	Horizontal line locked 1 = Locked 0 = Unlocked
[0]	R	no_signal	No signal detection 1 = No Signal Detected 0 = Signal Detected

3.9.36 Comb Video Status Register 2

Address Offset: 3Bh Access: Read only
Default Value: 00h Size: 8 bits

Table 3-232 Comb Video Status Register 2

Bit	Access	Symbol	Description
[7:1]		RESERVED	
[0]	R	Proscan_detected	Progressive Scan Video Detected

3.9.37 Comb Video Status Register 3

Address Offset: 3Ch Access: Read only
Default Value: 00h Size: 8 bits

Table 3-233 Comb Video Status Register 3

Bit	Access	Symbol	Description
[7]	R	vcr_rew	VCR Rewind Detected
[6]	R	vcr_ff	VCR Fast-Forward Detected
[5]	R	vcr_trick	VCR Trick-Mode Detected
[4]	R	vcr	VCR Detected
[3]	R	noisy	Noisy Signal Detected. This bit is set when the detected noise value (status register P2_7Fh) is greater than the value programmed into the “noise_thresh” register (P2_05h).
[2]	R	vline_625_detected	625 Scan Lines Detected
[1]	R	secam_detected	SECAM Color Mode Detected
[0]	R	pal_detected	PAL Color Mode Detected

3.9.38 Soft Reset

Address Offset: 3Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Table 3-234 Soft Reset

Bit	Access	Symbol	Description
[7:1]		RESERVED	
[0]	R/W	soft_reset	Soft Reset: Write 1 to reset initial values for comb filter

3.9.39 Luminance Peaking Control

Address Offset: 80h Access: Read/Write
Default Value: 04h Size: 8 bits

Table 3-235 Luminance Peaking Control

Bit	Access	Symbol	Description
[7:6]		RESERVED	
[5:4]	R/W	peak_range	These bits set the range of peak_gain. Setting peak_range value 00 1 (default) 01 2 10 4 11 8 Ypeak = Y + YH *(peak_gain/peak_range) where Y is the luma and YH is the high frequency luma only
[3:1]	R/W	peak_gain	These bits set the gain for the luma horizontal peaking control. This allows adjustable gain to the luma around the colour subcarrier frequency. Default = 2.
[0]	R/W	peak_en	This bit enables the luma horizontal peaking control around the colour subcarrier frequency 0 = Disabled (default) 1 = Enabled

3.9.40 Comb Filter Configuration

Address Offset: 82h Access: Read/Write
Default Value: 04h Size: 8 bits

Table 3-236 Comb Filter Configuration

Bit	Access	Symbol	Description
[7]		RESERVED	
[6]	R/W	pal_perr	This bit is used to reduce phase-error artifacts in the comb filter's luma-path. It should be set for VCR signals Default = 1.
[5]	R/W	pal_perr_auto_en	When set, this will turn on the pal_perr when VCR signals is detected. Default = 0.
[4]	R/W	comb_wide_band	This bit is used to select the bandpass filter used in the comb-filter. This should be set to 1 for PAL mode. Default = 0.
[3:2]		RESERVED	
[1:0]	R/W	palsw_level	This bit is used to determine how many incorrect lines are used for the pal switch circuit before switching. Use a higher level for noisy signals. Default = 2.

3.9.41 Chroma Lock Configuration

Address Offset: 83h Access: Read/Write
Default Value: 6Fh Size: 8 bits

Table 3-237 Chroma Lock Configuration

Bit	Access	Symbol	Description
[7:4]	R/W	lose_chromalock_count	This register is used to tune the chromakill, higher values are more sensitive to losing lock Default = 6.
[3:1]	R/W	lose_chromalock_level	Set the level for chromakill. Default = 7.
[0]	R/W	lose_chromalock_ckill	When set, chroma is killed whenever chromlock is lost. Default = 1.

4 Electrical Characteristics

4.1 Digital I/O Pad Operation Condition

Table 4-1 Operation Condition

	Parameter	Min	Typ	Max
VDD25	Digital Core Power Supply	2.25V	2.50V	2.75V
VD33	Digital I/O Power Supply	3.0V	3.3V	3.6V
VIL	Input Low Voltage	0.3V		0.8V
VIH	Input High Voltage	2.0V		5.0V
VT+	Schmitt Trigger Low-to-High Threshold	1.44V	1.58V	1.71V
VT+	Schmitt Trigger High-to-Low Threshold	1.09V	1.19V	1.31V
II	Input Leakage Current@ VI=3.3V or 0V			±1μA
IOZ	Tri-state Output Leakage Current@ Vo=3.3V or 0V			±1μA
IOL	Low level Output Current@ VOL=0.4V			
	2mA	2.1mA	3.4mA	4.2mA
	4mA	4.2mA	6.9mA	8.6mA
	8mA	8.4mA	13.9mA	17.2mA
	12mA	12.5mA	20.8mA	25.8mA
IOH	High level Output Current@ VOH=2.4V			
	2mA	3.0mA	6.2mA	10.0mA
	4mA	5.7mA	11.6mA	18.6mA
	8mA	9.5mA	19.4mA	30.9mA
	12mA	13.3mA	27.1mA	43.3mA
RPD	Pull-up resistor	74KΩ	104KΩ	177KΩ
RPD	Pull-down resistor	62KΩ	90KΩ	176KΩ

Note: R_{PD} and R_{PD} are always present no matter normal operation or power down mode is enabled. A typical 30~40μA false leakage current which is resulted from R_{PD} and R_{PD} when a tester forces I/O to 3.3V or 0.0 V.

4.2 DC Characteristics

(DVDD=AVDD=2.5V; AVD33R=AVD33G=AVD33B=3.3V; VREFIN=1.235V; RL=37.5ohm, CL=10pF; RSET=386ohm; Temp=75oC, unless otherwise noted)

Table 4-2

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating voltage range	AVD33R AVD33G AVD33B	3.0	3.3	3.6	V	
Operating voltage range	AVDD	2.25	2.5	2.75	V	
Operating voltage range	DVDD	2.25	2.5	2.75	V	
AVD33R supply current	IAVD33R	--	35	--	mA	SL=0, SLR=0
AVD33G supply current	IAVD33G	--	35	--	mA	SL=0, SLG=0
AVD33B supply current	IAVD33B	--	35	--	mA	SL=0, SLB=0
AVDD supply current	IAVD33	--	1	--	mA	SL=0
VDD supply current	IDVDD	--	TBD	--	mA	
Full scale current	IOFS	2.00	34.08	--	mA	Full-Scale adjust resistor. A resistor should be connected between this pin and AVS33 to control the magnitude of the full-scale video signal. RSET(ohm)=VREFIN(V)*10.66/IOFS(A) ,where IOFS is full-scale output current.
Output voltage range	V(IO)	--	1.28	--	V	.
DAC resolution	--	--	10	--	bits	.
Integral non-linearity error	INL	--	0.5	+-2	LSB	.
Differential non-linearity error	DNL	--	0.5	+-1	LSB	.
Gain error	--	--	--	TBD	%	.
DAC to DAC matching	--	--	TBD	TBD	%	.

4.3 AC Characteristics

(DVDD=AVDD=2.5V; AVD33R=AVD33G=AVD33B=3.3V; VREFIN=1.235V; RL=37.5ohm; CL=10pF; RSET=386ohm; Temp=75oC, unless otherwise noted)

Table 4-3

Parameter	Sym	Min	Typ	Max	Unit	Condition
CK period	Tck	5	--	--	Ns	
CK to valid output	Tdelay	--	--	0.5*Tck+2	Ns	
Output rise time	Tr	--	--	4	Ns	10% to 90% IOFS; assume no package inductance.
Output fall time	Tf	--	--	4	Ns	90% to 10% IOFS; assume no package inductance.
Output settling time	Tsettle	--	--	TBD	Ns	assume no package inductance
Glitch energy	--	--	--	--	pvs	assume no package inductance
DAC to DAC crosstalk	--	--	TBD	--	Db	.

4.4 Analog Processing and A/D Converters

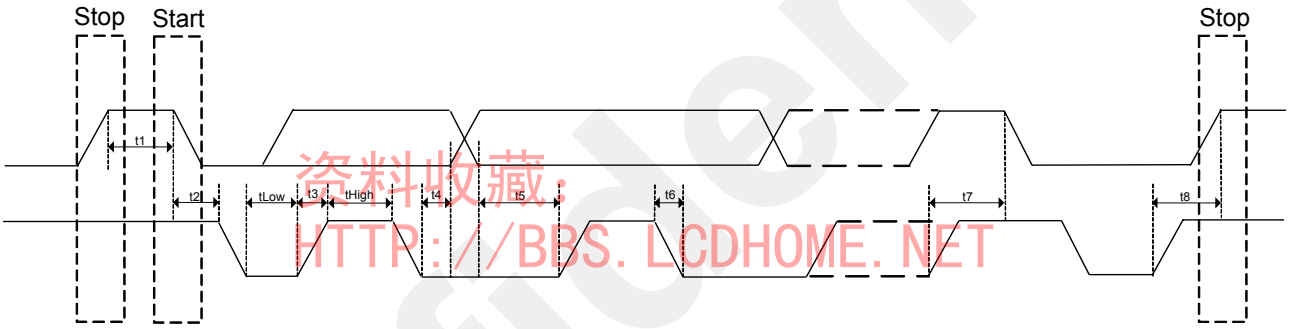
Table 4-4

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zi	Input impedance, analog video inputs	By design		500		kΩ
Ci	Input capacitance, analog video inputs	By design		10		pF
Vi(pp)	Input voltage range†	Ccoupling = 0.1µF	0		0.75	V
△G	Gain control range		0		12	dB
DNL	DC differential nonlinearity	A/D only		±0.5		LSB
INL	DC integral nonlinearity	A/D only		±1		LSB
Fr	Frequency response	6 MHz		−0.9	−3	dB
SNR	Signal-to-noise ratio	6 MHz, 1.0 Vp-p		50		dB
NS	Noise spectrum	50% flat field		50		dB
DP	Differential phase			1.5		
DG	Differential gain			0.5%		

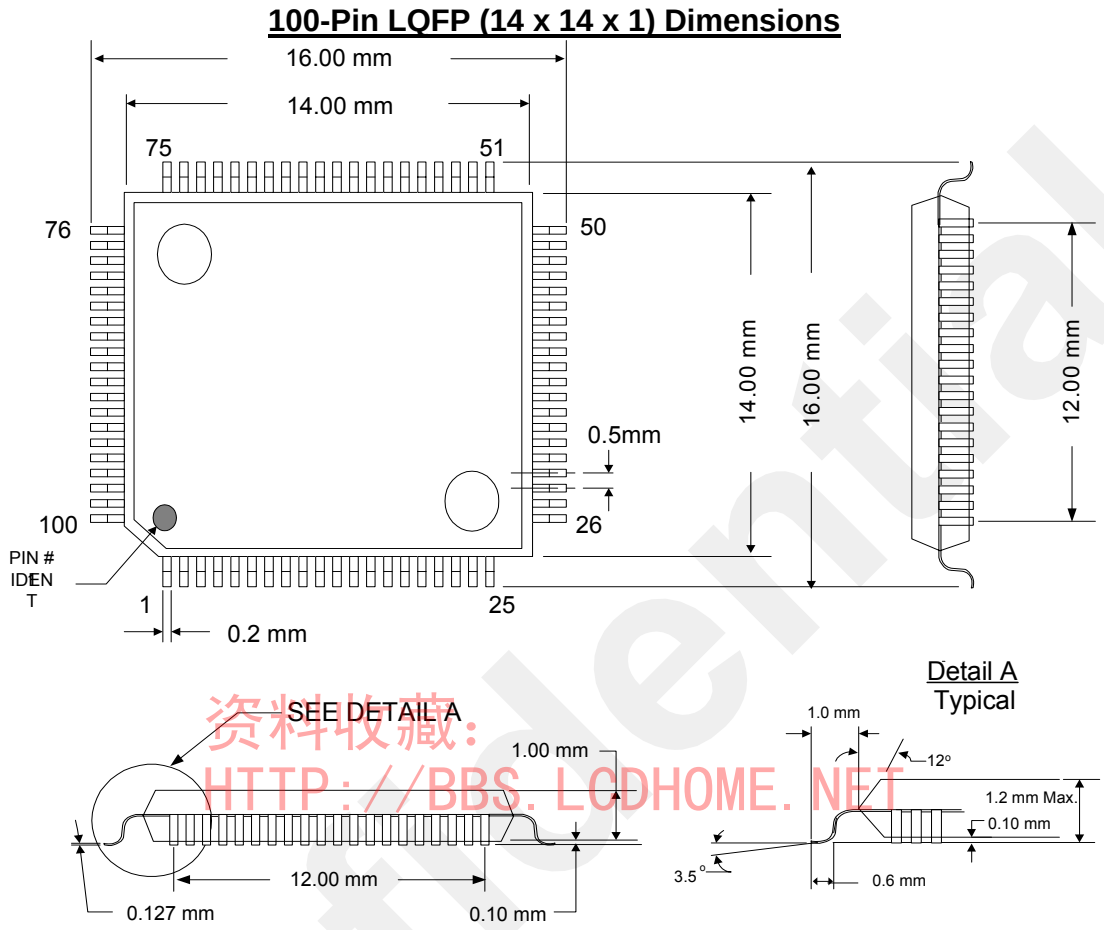
4.5 I²C Host Interface Timing

Table 4-5

	Parameter	Min	Typ	Max
t1	Bus free time between a Stop and Start condition	4.7ns		
t2	Hold time (repeated) Start condition	4.0us		
t3	Rise time of both SDA and SCL			1000ns
t4	Data hold time	5.0us		
t5	Data setup time	250ns		
t6	Fall time of both SDA and SCL			300ns
t7	Setup time for a repeated Start condition	4.7us		
t8	Setup time for Stop condition	4.0us		
tLow	Low period of the SCL	4.7us		
tHigh	High period of the SCL	4.0us		
fSCL	SCL clock frequency			1Mhz
Cb	Capacitive load for each bus line			400pF



5 Package Dimensions



[100 LQFP 14 X 14 X 1.4 mm]

Figure 5-1

6 Ordering Information

Table 6-1

Part No.	Package
T100	100 LQFP

7 Revisions Note

Table 7-1

Revisions	Description of changes	Date	Note
0.1	First draft	Sep 25, 2003	
0.2	Complete Block Diagram	Nov. 17, 2003	

8 General Disclaimer

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Life Support Policy

Terawins' products are not authorized for use within Life Support Systems without the specific written consent of Terawins, Inc.
Life support systems are systems which are intended for support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user. A critical component in any component of a life support system whose failure to perform can be reasonably expected to cause the failure of the life support system, or to affect its safety or effectiveness.

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