

Layer Name	Type	Material	Thickness (mm)	Color	Epsilon R	Loss Tangent
F.Silkscreen	Top Silk Screen	Not specified	0 mm	White	1	0
F.Paste	Top Solder Paste		0 mm		1	0
F.Mask	Top Solder Mask	Not specified	0.01 mm	Green	3.3	0
F.Cu	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.35 mm	FR4 natural	4.5	0.02
In1.Cu	copper		0.035 mm		1	0
Dielectric	core	FR4	0.7 mm	FR4 natural	4.5	0.02
In2.Cu	copper		0.035 mm		1	0
Dielectric	prepreg	FR4	0.35 mm	FR4 natural	4.5	0.02
B.Cu	copper		0.035 mm		1	0
B.Mask	Bottom Solder Mask	Not specified	0.01 mm	Green	3.3	0
B.Paste	Bottom Solder Paste		0 mm		1	0
B.Silkscreen	Bottom Silk Screen	Not specified	0 mm	White	1	0

Manufacturability/DFM

- Edge clearance:
- Copper: 0.6 mm (humidity), at break-out tabs: 1.5 mm
 - Parts: 3 mm, 1 mm with edge rails (line transport de-panelization, pick & place)
 - Test points: 2.5 mm
 - Fiducials: 4 mm

- Edge clearance for assembly:
- 1.5 mm distance from mounting hole screw head area to control board edge (assembly).

- PTH:
- FR-4: Ø ≥0.2 mm, distance: 0.5 mm (= 0.7 mm center/center)

- NPTH:
- FR-4: Ø ≥0.6 mm, distance: 0.5 mm (= 1.1 mm center/center)
 - Al, 1 layer: Ø ≥1 mm, distance: 0.5 mm (= 1.5 mm center/center)

- Depanelization:
- Board edge mill: Ø 2 mm
 - Edge rail: ≥5 mm (incl. milling, if break-away tabs are used)
 - Break-away tab width: ≥2 mm
 - Mouse bite: see NPTH

- Isolation:
- Int. & ext. layers ≤30 V: 0.2 mm (manufacturability, IPC2221: 0.1 mm)
 - Int. layers ≤100 V: 0.2 mm (manufacturability, IPC2221: 0.1 mm)
 - Ext. layers ≤100 V: 0.6 mm (altitude ≤3 km MSL)
 - Ext. layers. 1.8 mm clearance from mounting hole screw head area (IEC 60664-1: OVC III, 100 V, PD2, mat. IIIa, alt. 3 km).

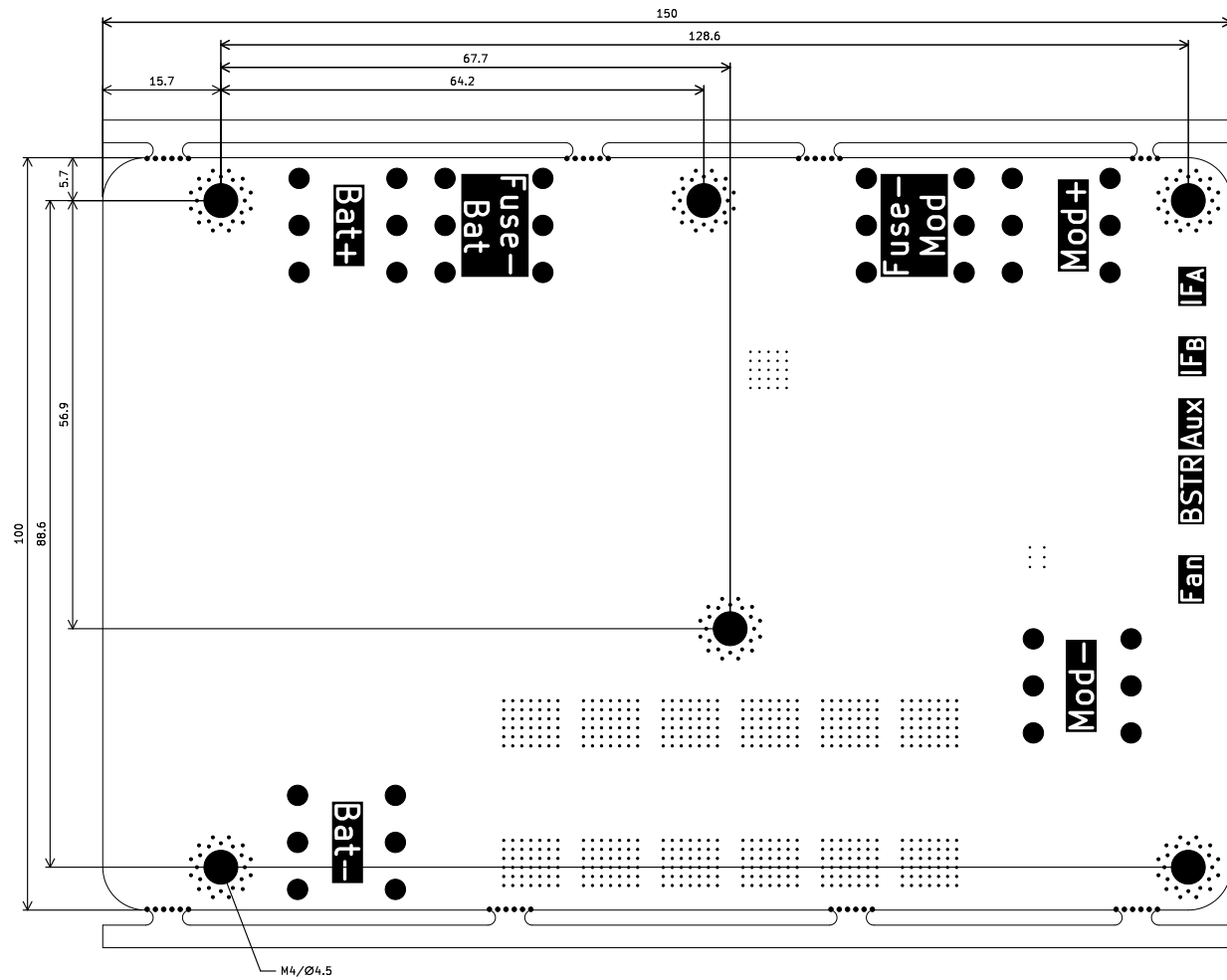
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Frank Bättermann (frank /at/ ich-war-hier.de)

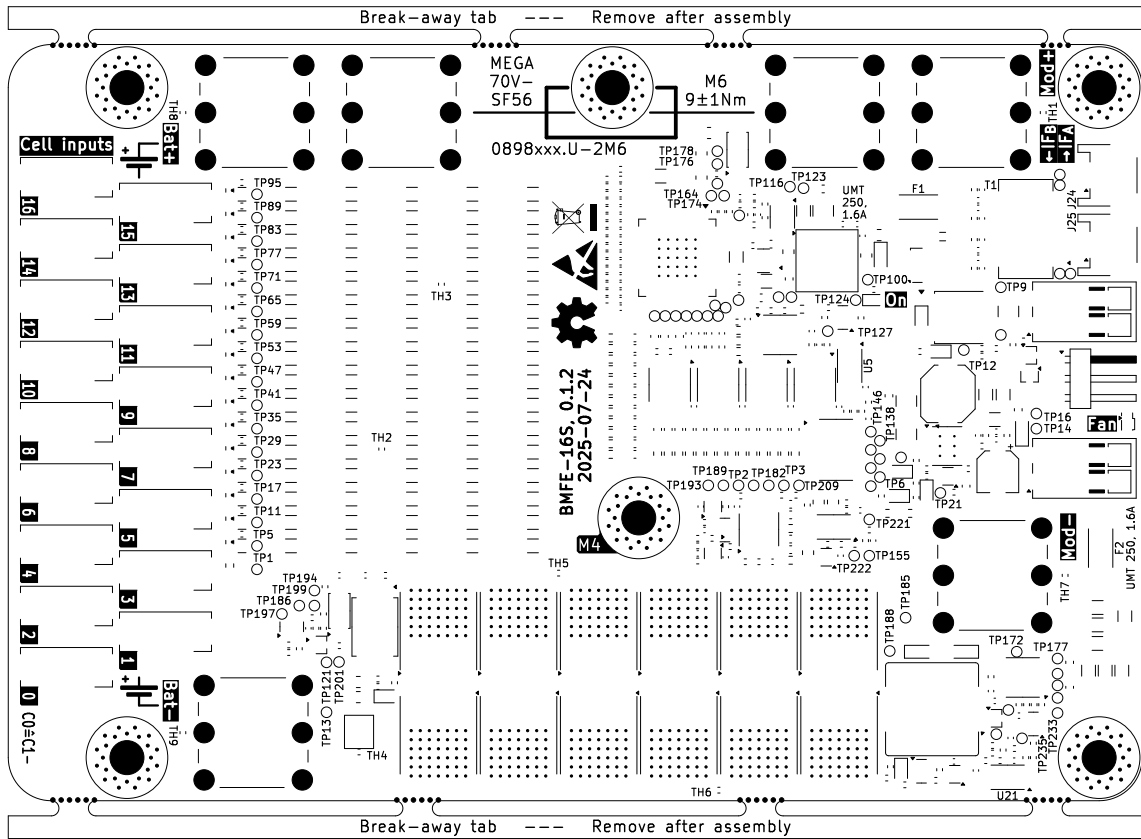
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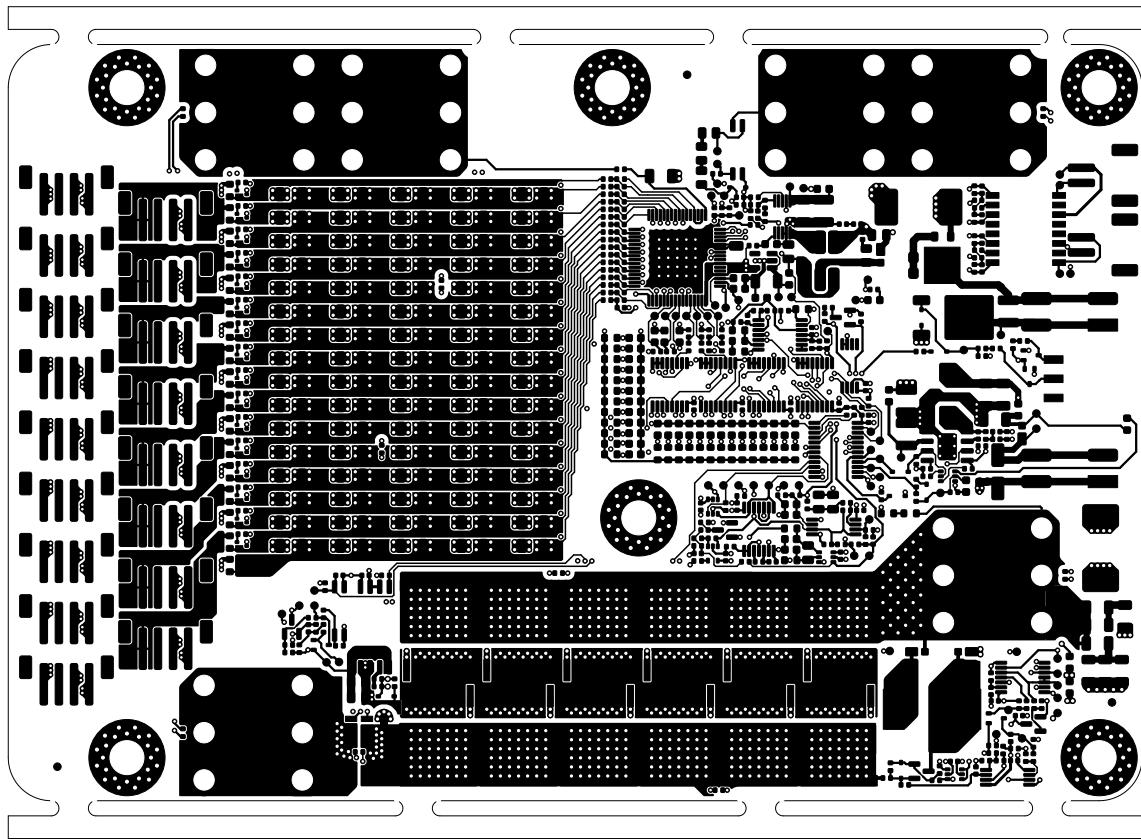
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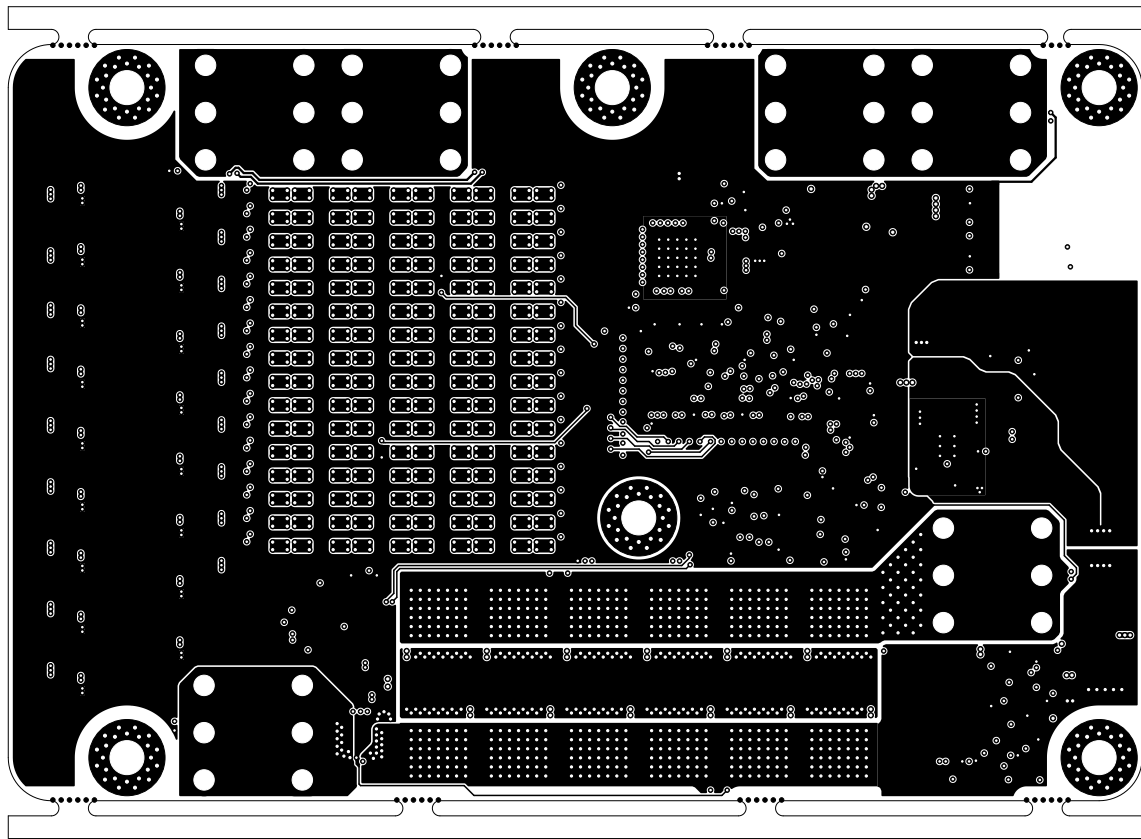
Size: A3	Date: 2025-07-24	Rev: 0.1.2
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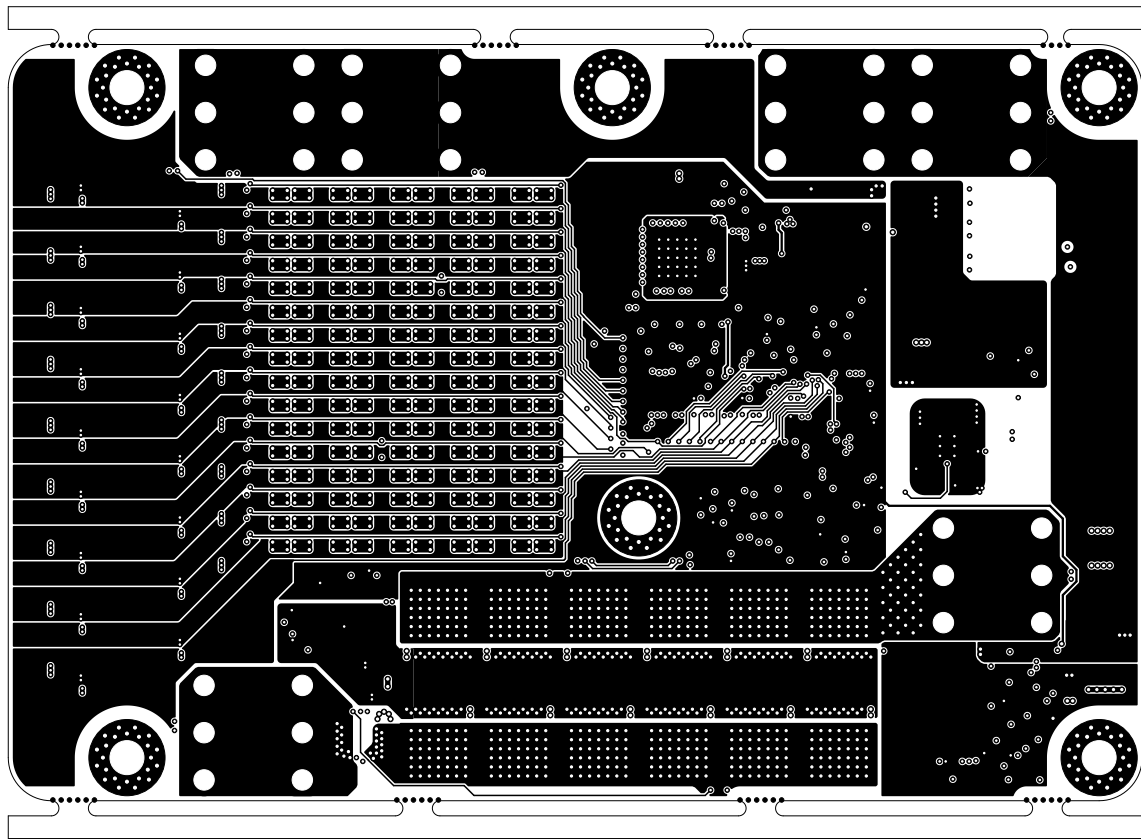


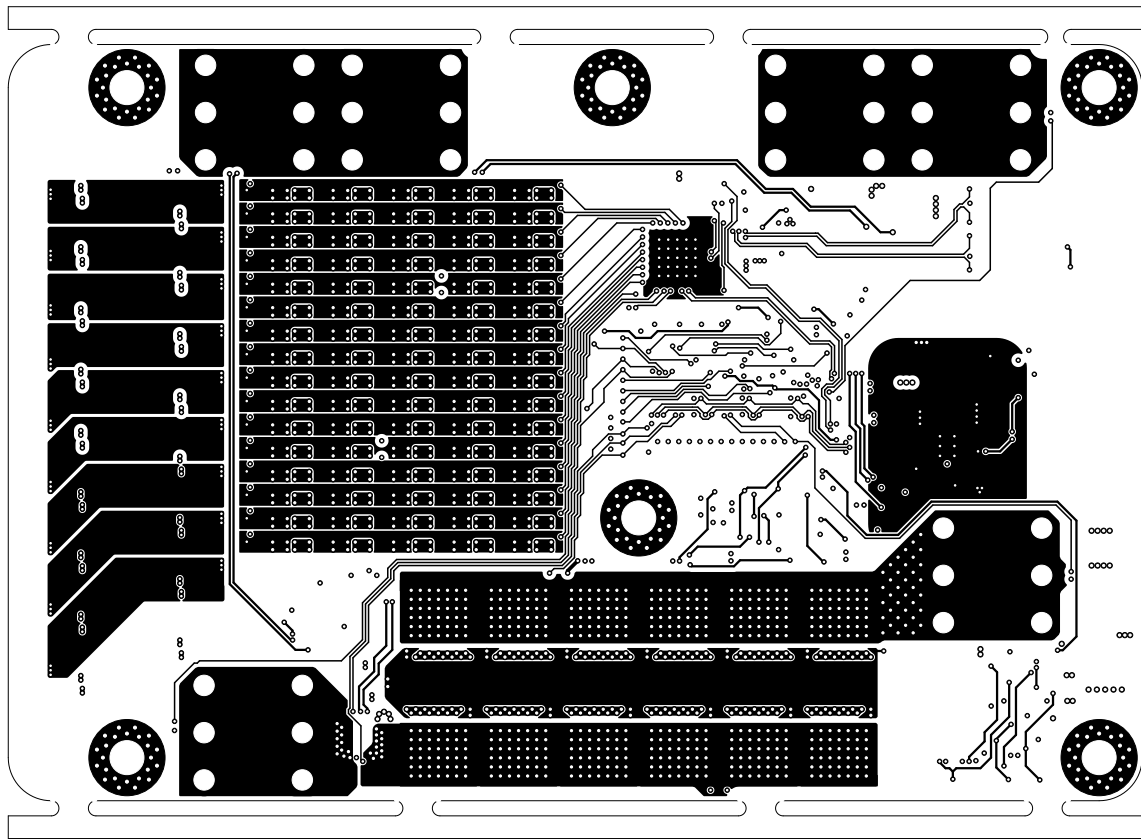




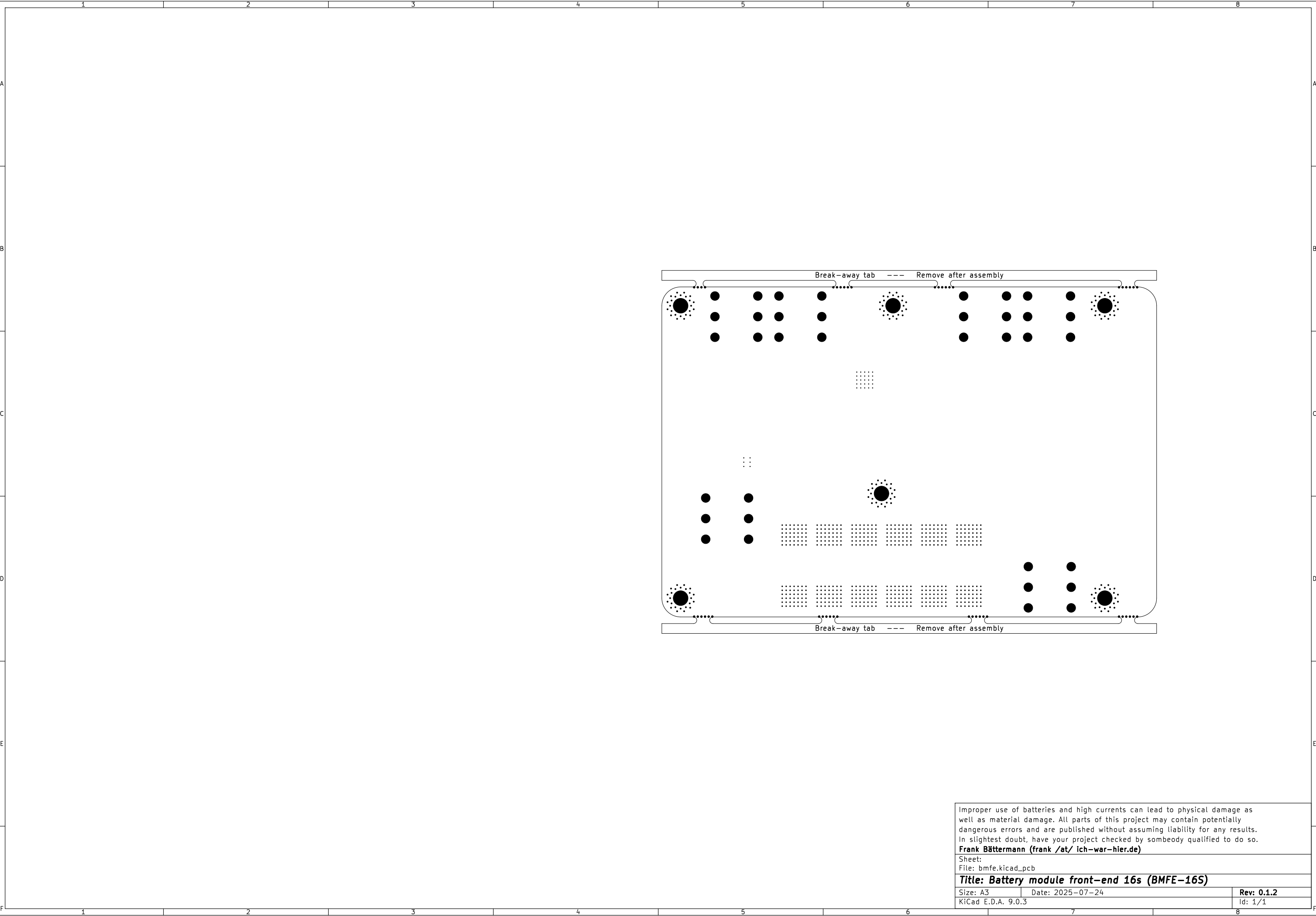
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	1	2	3	4	5	6	7	8
A								
B								
C								
D								
E								
F								

Revision history

- 0.1.2 (2025-07-24)
- Updated to KiCad9
 - Switch power-good
 - Lowered R248 to 16kΩ (make sure optocoupler U14 turns off with low V_{GS(th)} transistor)
 - Lowered R247 with 16kΩ (adjustment of PG-threshold)
 - Replaced R249 with 100kΩ.
 - Removed R252 (wrong connection).
 - Connect R245 from SwPg/TP199 to U13 pin 1 (to generate hysteresis).
 - Connected R250 from U14 pin 1 (anode) to GND1.
 - Supply
 - Removed R132 (set U3 to forced PWM-mode; higher efficiency in majority of situations.)
 - Replaced R191 with 200kΩ (U3 f_{sw}: 210kHz; higher efficiency, less effect of leakage on secondary side regulation)
 - Added 15pF in parallel to R128/R192 (TP122 to U3-5)
 - Replaced L1 with 220μH (higher SRF and less leakage inductance).
 - Increased C53 to 4.7μF (was 2.2μF)
 - Secondary side snubber across L4-1/4 (R_{Snub}: 1kΩ, C_{Snub}: 100pF)
 - Lowered R93 to 1k (increase LED visibility)
 - isoSPI interface
 - Replaced R183, R184 and R310 with 1.3kΩ (increases signal level, harmonize with BMM).
 - I2C
 - Lowered R208/R209 to 2.2kΩ (I2C pullups for 400kHz)
 - Fan output
 - Added missing testpoint to Fan+ (TP14).
 - Added diodes D9/D7 (protect controlling IO expander if Bat~-fused~ fuse blows).
 - Pre-charge
 - Tie pins 4 and 6 of U20 together.
 - Increased R308 to 220k (Ip_k: 475mA)
 - Replace Q31A/B (dual FET) with BSS123 (single FET), connect R299 to GND

- 0.1.1 (22024-04-21)
- Exchanged U14, U23 to ACPL-217-56CE to fit smaller footprint
 - Updated PCB stackup to more common one

- 0.1.0 (22024-03-08)
- First revision

Version number: X.Y.Z

X+1: Changes on interfaces, downwards compatibility is not ensured, changes on provisions
Y+1: Changes without impact on interfaces, downwards compatibility is ensured, improvements
Z+1: Formal changes, spelling mistakes, corrections

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Date: 2025-07-24

Rev: **0.1.2**

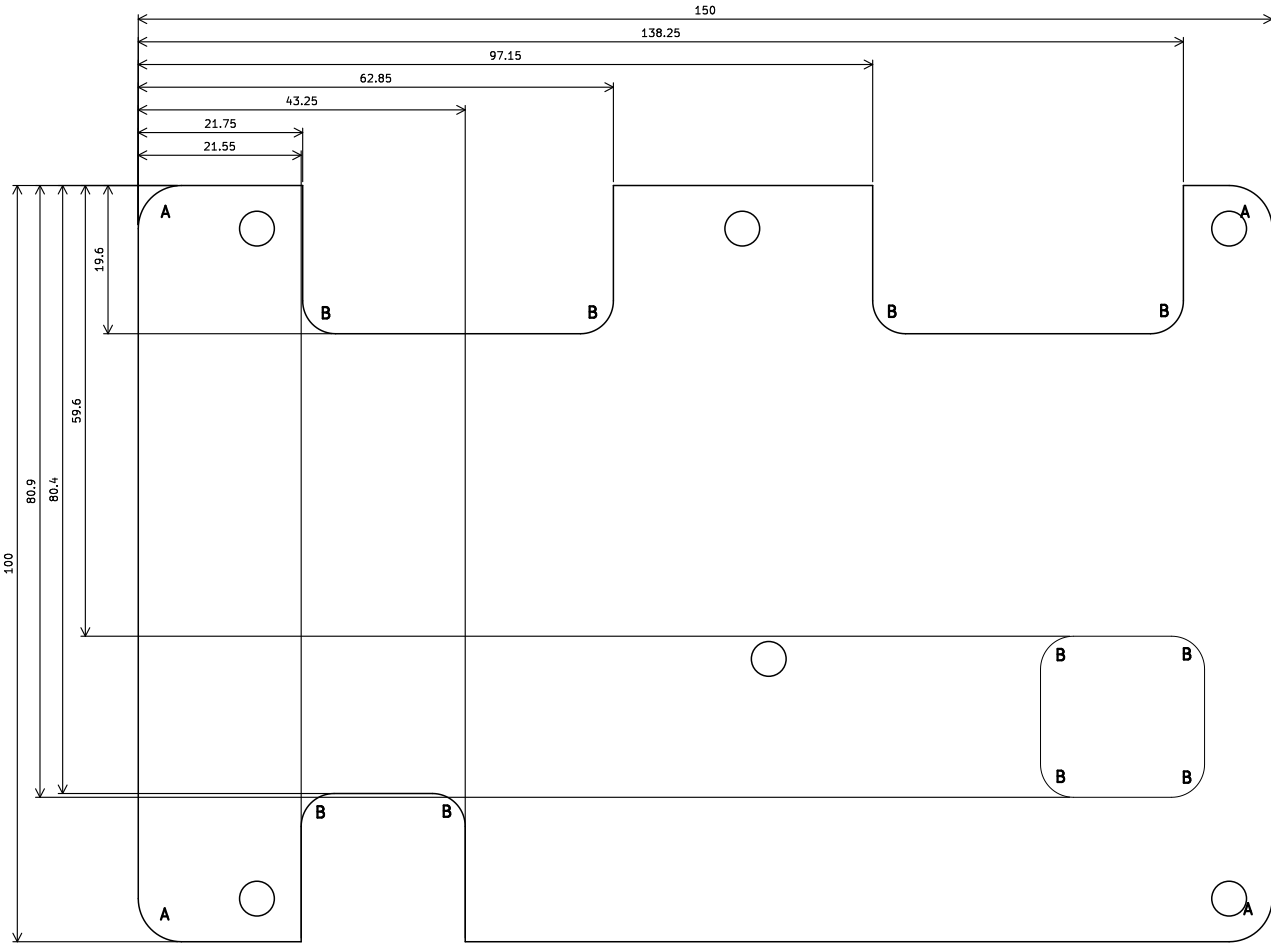
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Metal heatsink mounting plate

Material: Aluminium (6063, 6061 or similar)
Thickness: 5 mm
Tolerance: ISO 2768–1 medium
Roughness: Ra 3.2 µm (tbd)
Surface: no treatment

All dimensions in mm



A: r5.7
B: r4.35

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