

Layer Name	Type	Material	Thickness (mm)	Color	Epsilon R	Loss Tangent
F.Silkscreen	Top Silk Screen	Not specified	0 mm	White	1	0
F.Paste	Top Solder Paste		0 mm		1	0
F.Mask	Top Solder Mask	Not specified	0.01 mm	Green	3.3	0
F.Cu	copper		0.035 mm		1	0
Dielectric 1	core	FR4	1.47 mm	FR4 natural	4.5	0.02
B.Cu	copper		0.035 mm		1	0
B.Mask	Bottom Solder Mask	Not specified	0.01 mm	Green	3.3	0
B.Paste	Bottom Solder Paste		0 mm		1	0
B.Silkscreen	Bottom Silk Screen	Not specified	0 mm	White	1	0

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Sheet:
File: cpbnk-25x18-60.kicad_pcb

Title: Capacitor bank (25x18mm, 60V) (CPBNK-25x18-60)

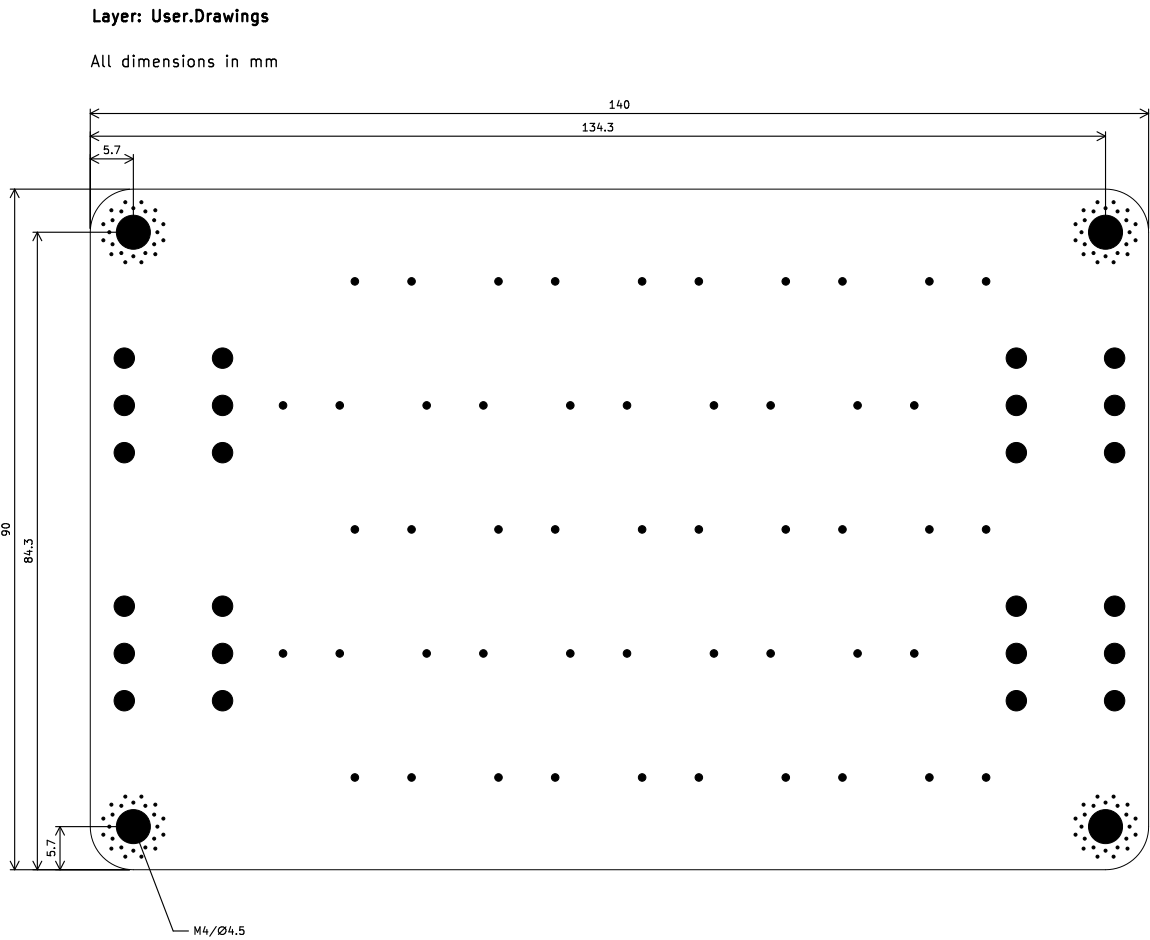
Size: A3

Date: 2025-07-29

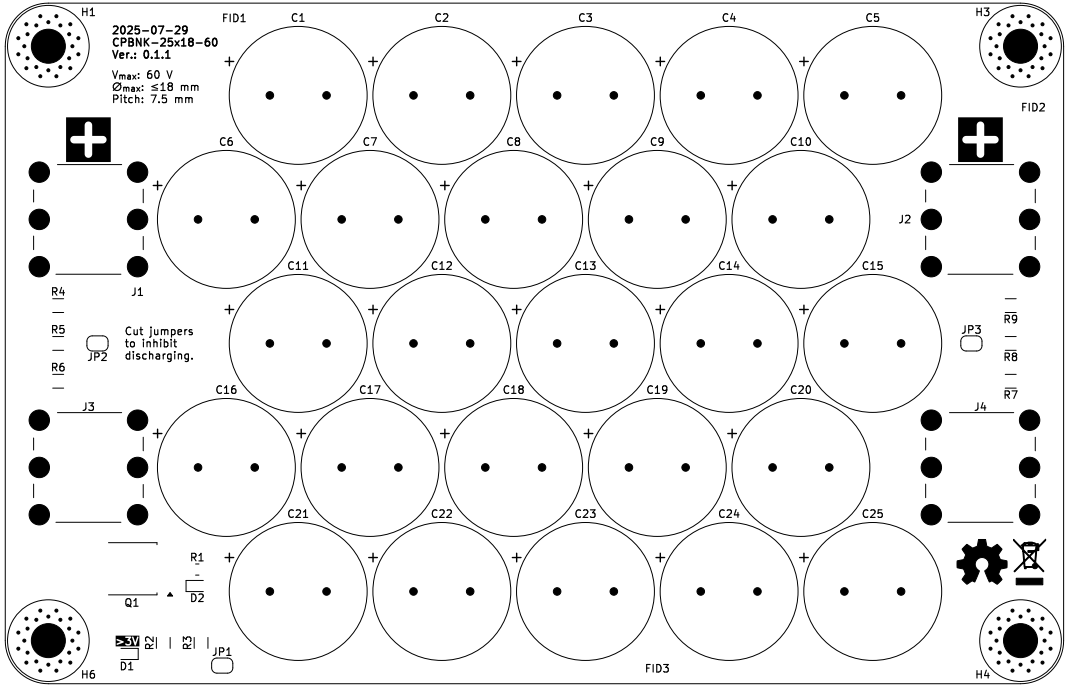
Rev: 0.1.1

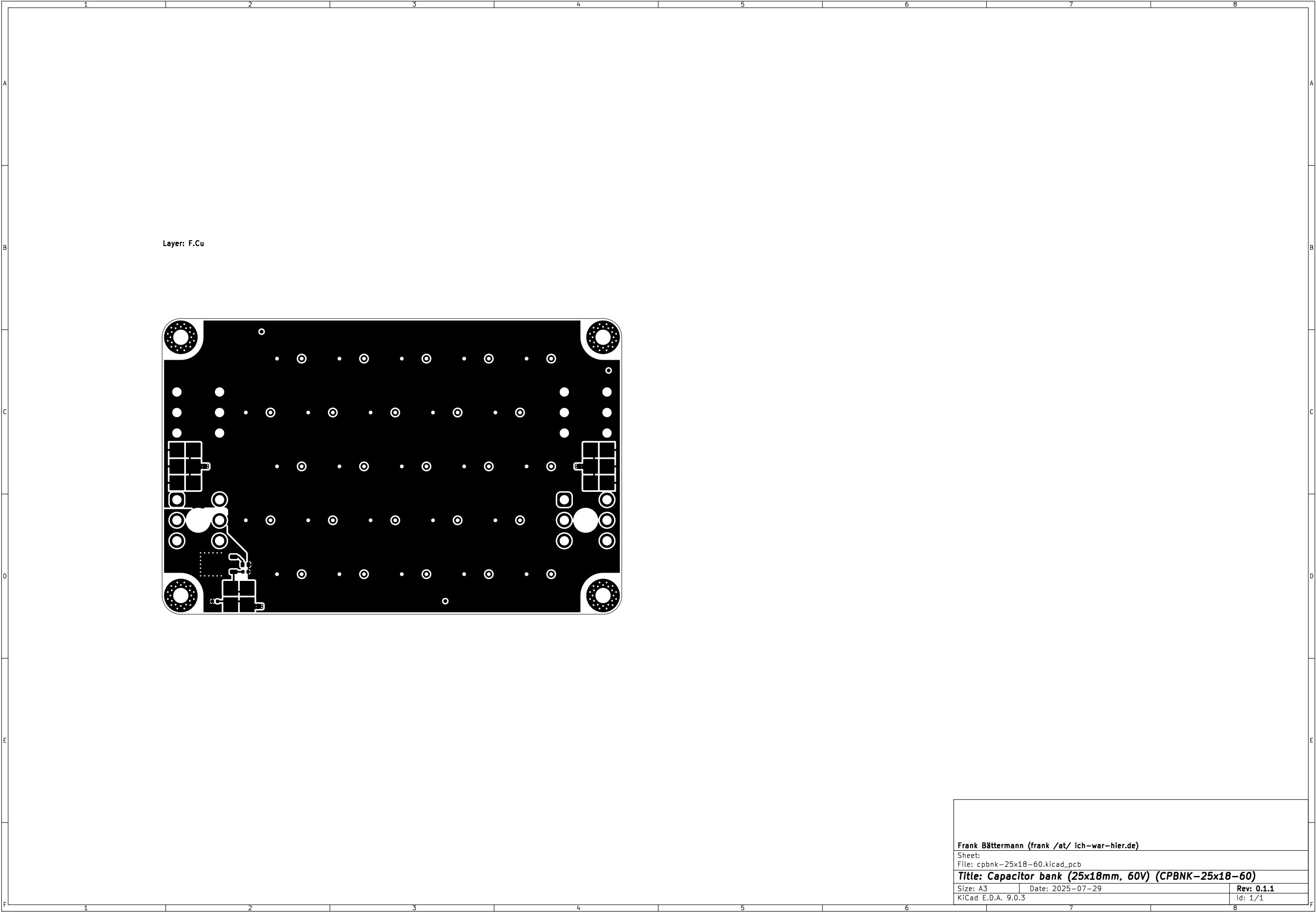
KiCad E.D.A. 9.0.3

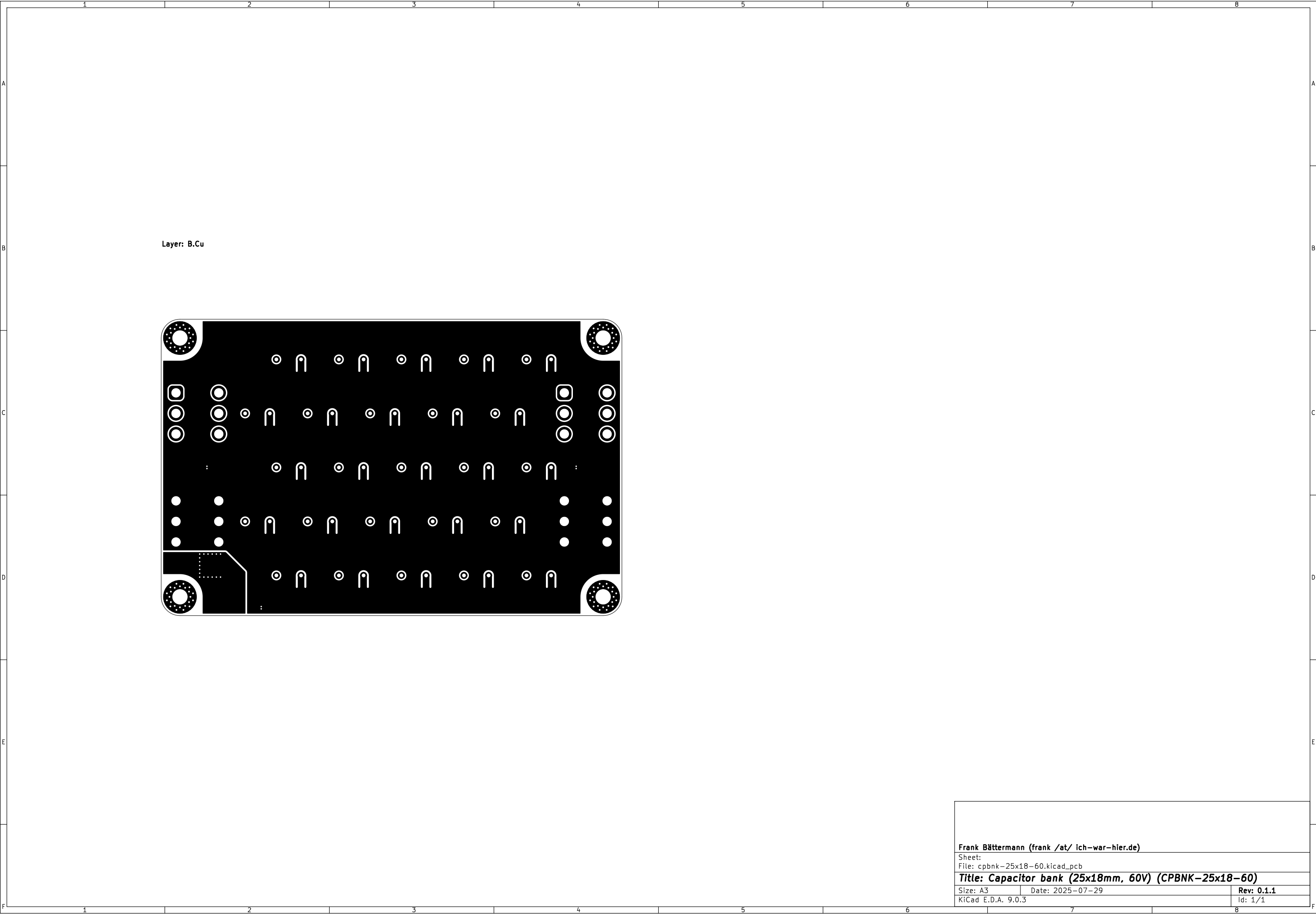
Id: 1/1



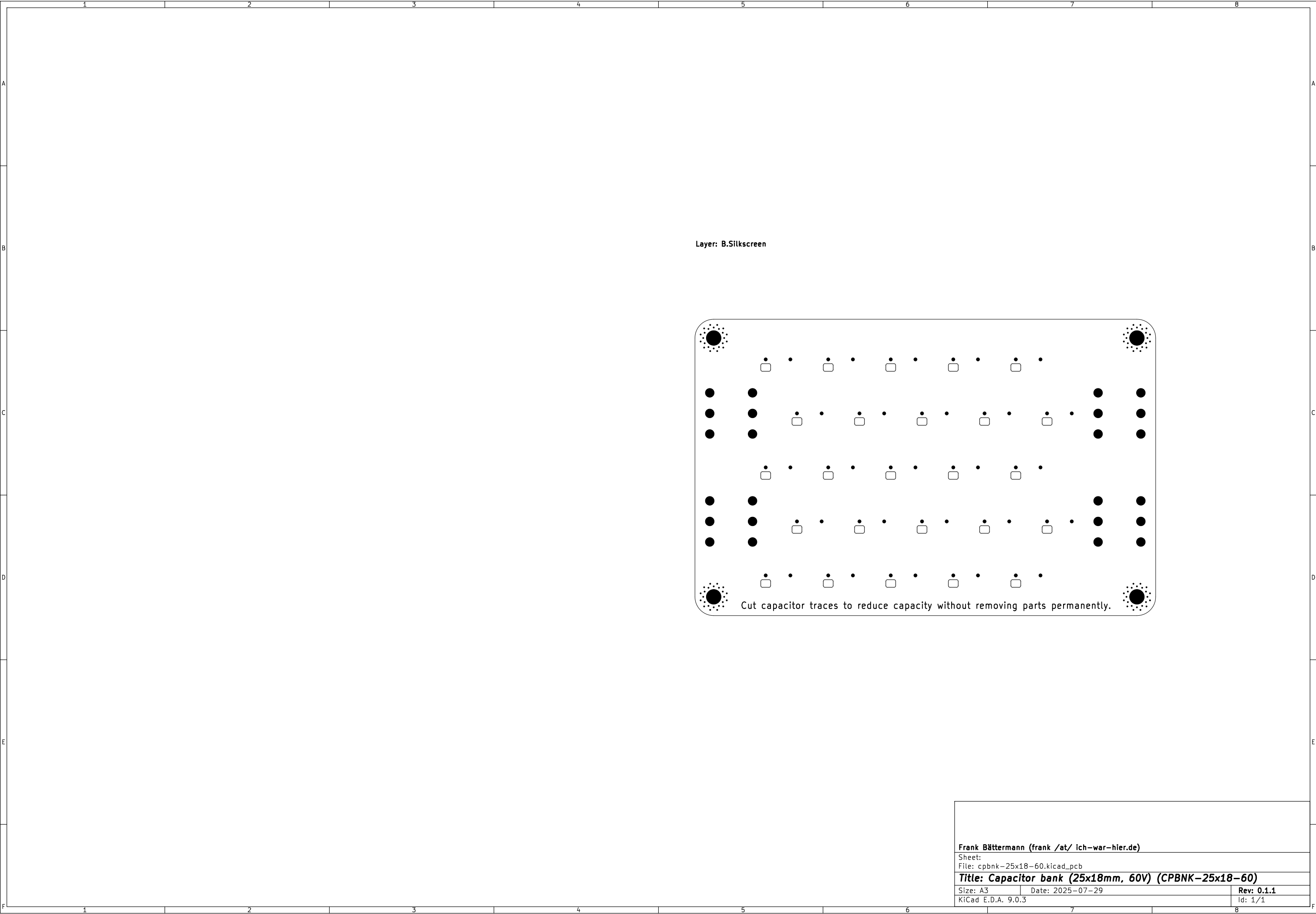
Layer: F.Silkscreen







Layer: B.Cu



	1	2	3	4	5	6	7	8
A								
B								
C								
D								
E								
F	1	2	3	4	5	6	7	8

Revision history

- 0.1.1 (2025-07-29)
- Added keep-outs underneath the neg. screw terminals to avoid potential short-circuit using too long screws
 - Bump to KiCad 9
- 0.1.0 (2024-03-21)
- First revision

Version number: X.Y.Z

X+1: Changes on interfaces, downwards compatibility is not ensured, changes on provisions
Y+1: Changes without impact on interfaces, downwards compatibility is ensured, improvements
Z+1: Formal changes, spelling mistakes, corrections

	1	2	3	4	5	6	7	8
A								
B								
C								
D								
E								
F	1	2	3	4	5	6	7	8

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