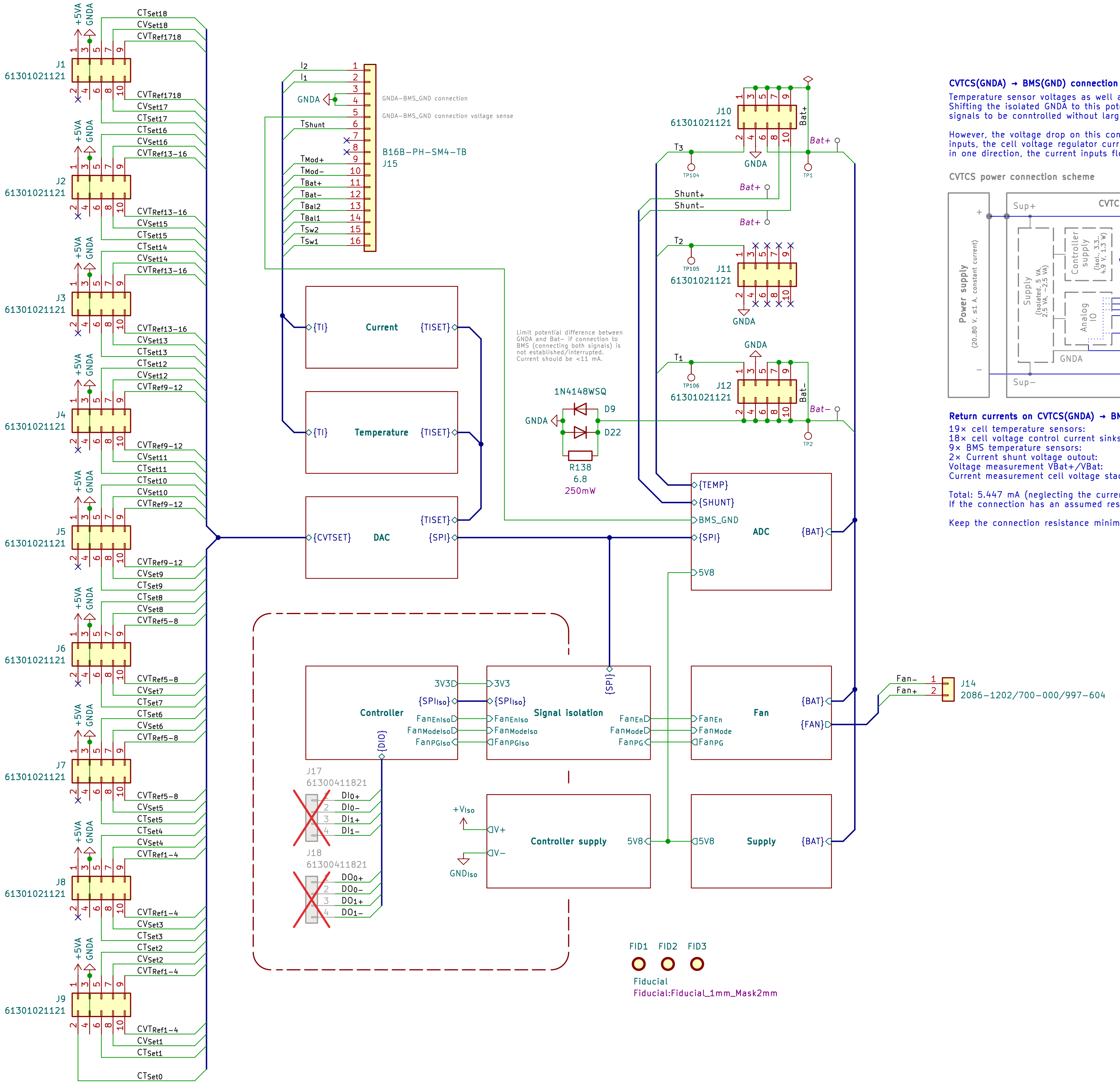
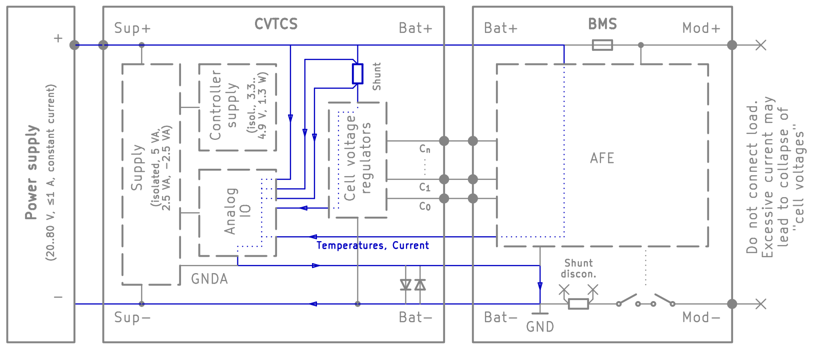


CVTCS(GNDA) → BMS(GND) connection

Temperature sensor voltages as well as current sense resistor voltages are referenced to the local GND of the connected BMS. Shifting the isolated GNDA to this potential (or at least very close) by directly connecting to it, allows the aforementioned signals to be conntrolled without large errors due to common-mode voltages on then Bat- supply connection.

However, the voltage drop on this connection will also not be absolute zero. The return currents of the BMS's temperature inputs, the cell voltage regulator current as well as then current sourced from Bat+ for the measurement of Bat+/Bat- flow in one direction, the current inputs flow either in the same or/opposite direction.

CVTCS power connection scheme



Return currents on CVTCS(GNDA) → BMS(GND) connection

19× cell temperature sensors:	19× 3 V/47 kΩ clamped to 0 V = 1.213 mA	(BMS(V_{Bias}) → CVTCS(GNDA) → BMS(GND) → CVTCS(Bat-))
18× cell voltage control current sinks:	18× 1.8055 V/10 kΩ clamped to 0 V = 3.25 mA	(CVTCS(Bat+) → CVTCS(GNDA) → BMS(GND) → CVTCS(Bat-))
9× BMS temperature sensors:	9× 3 V/47 kΩ clamped to 0 V = 574.5 µA	(BMS(V_{Bias}) → CVTCS(GNDA) → BMS(GND) → CVTCS(Bat-))
2× Current shunt voltage outout:	2× 33.7 mV/10 kΩ = 6.8 µA	(BMS(V_{Bias}) → CVTCS(GNDA) → BMS(GND) → CVTCS(Bat-))
Voltage measurement VBat+/VBat:	2.048 V/10 kΩ = 204.8 µA	(CVTCS(Bat+) → CVTCS(GNDA) → BMS(GND) → CVTCS(Bat-))
Current measurement cell voltage stack:	2.048 V/10 kΩ = 204.8 µA	(CVTCS(Bat+) → CVTCS(GNDA) → BMS(GND) → CVTCS(Bat-))

Total: 5.447 mA (neglecting the current shunt outputs), adding 100% headroom the total current is <11 mA.
If the connection has an assumed restistance of 100 mΩ this amounts to 1.1 mV - which is significant to at least for the current sensor output.

Keep the connection resistance minimal. To enable an assessment of the errors that occur, a measurement of the voltage drop is provided.

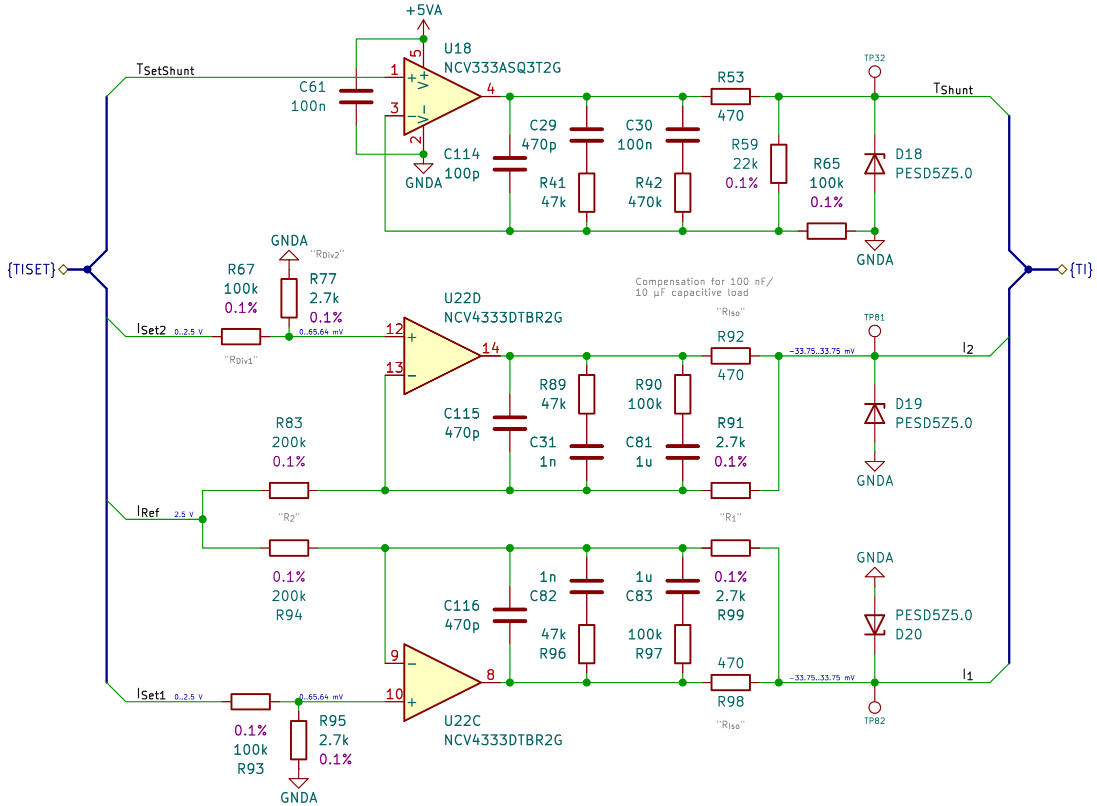
Frank Bättermann (frank /at/ ich-war-hier.de)

Sheet: /
File: cvtcs-c.kicad_sch

Title: Cell voltage, temp. and current sim. (control) (CVTCS-C)

Size: A3 | Date: 2025-07-30 | Rev: 0.2.1
KiCad E.D.A. 9.0.3 | Id: 1/12

Current output



For each current output:
$V_{Out} = V_{Set} \times R_{Div1} / R_{Div2} - V_{Ref} \times R_1 / R_2$

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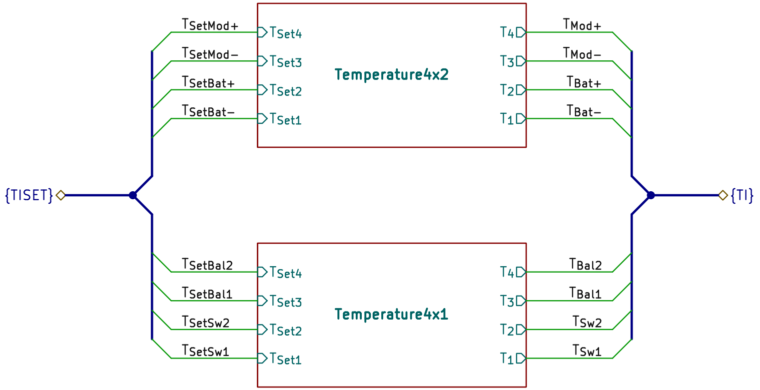
Sheet: /Current/
File: current.kicad_sch

Title: Cell voltage, temp. and current sim. (control) (CVTCS-C)

Size: A4 | Date: 2025-07-30 | Rev: 0.2.1
KiCad E.D.A. 9.0.3 | Id: 11/12



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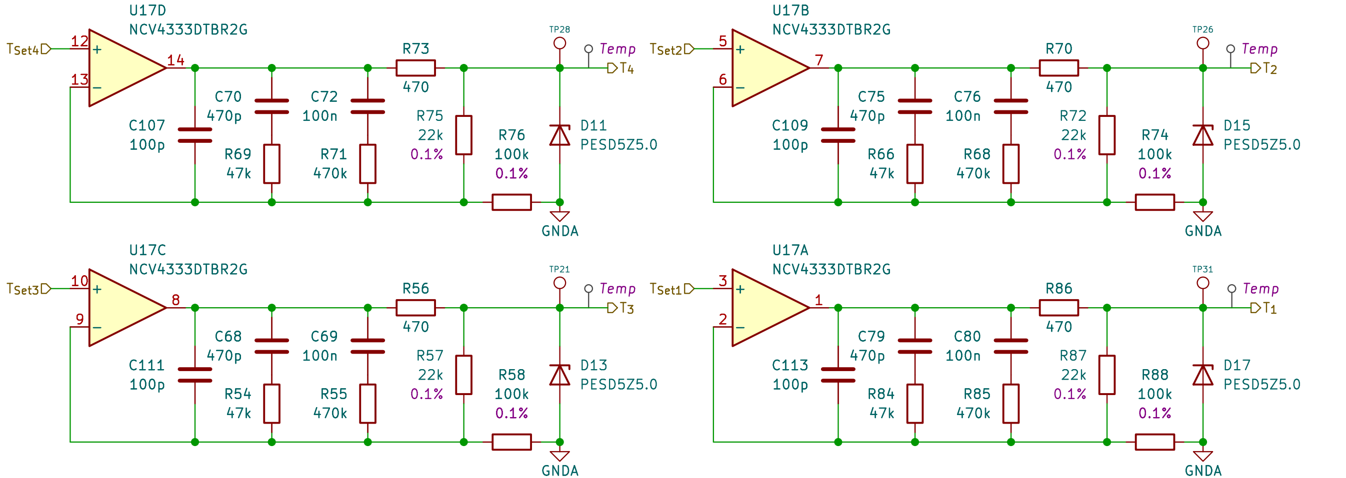
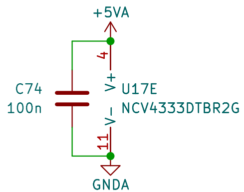
Sheet: /Temperature/
File: temperature.kicad_sch

Title: Cell voltage, temp. and current sim. (control) (CVTCS-C)

Size: A5	Date: 2025-07-30	**Rev: 0.2.1**
KiCad E.D.A. 9.0.3		Id: 8/12



For notes and comments refer to CVTCS-P schematic.



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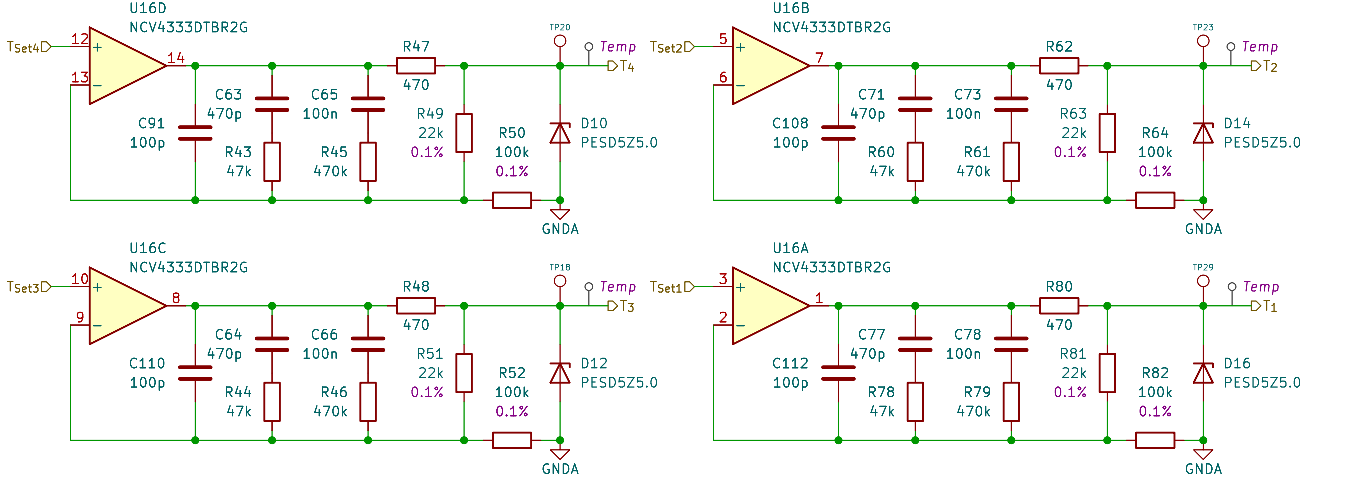
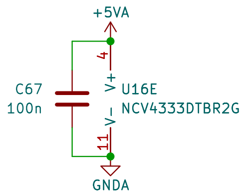
Sheet: /Temperature/Temperature4x2/
File: temperature_4ch.kicad_sch

Title: Cell voltage, temp. and current sim. (control) (CVTCS-C)

Size: A5	Date: 2025-07-30	**Rev: 0.2.1**
KiCad E.D.A. 9.0.3		Id: 10/12



For notes and comments refer to CVTCS–P schematic.



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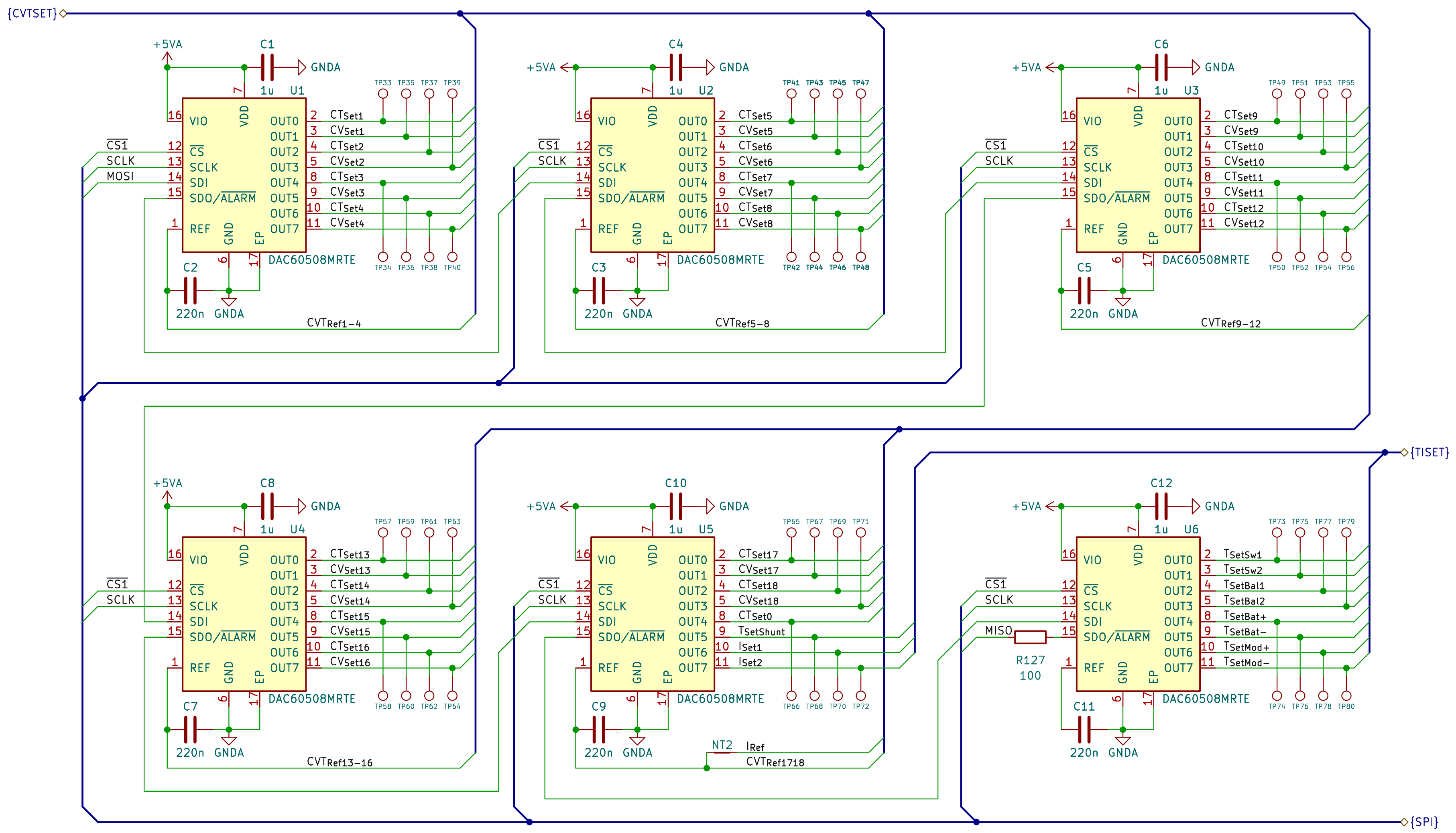
Sheet: /Temperature/Temperature4x1/
File: temperature_4ch.kicad_sch

Title: Cell voltage, temp. and current sim. (control) (CVTCS–C)

Size: A5 | Date: 2025-07-30 | **Rev: 0.2.1**
KiCad E.D.A. 9.0.3 | Id: 9/12



- DACs are in daisy chain configuration
- DAC60508 (12 bit) can be replaced by DAC70508/DAC80508 (14/16 bit) to improve resolution.

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Sheet: /DAC/
File: dac.kicad_sch

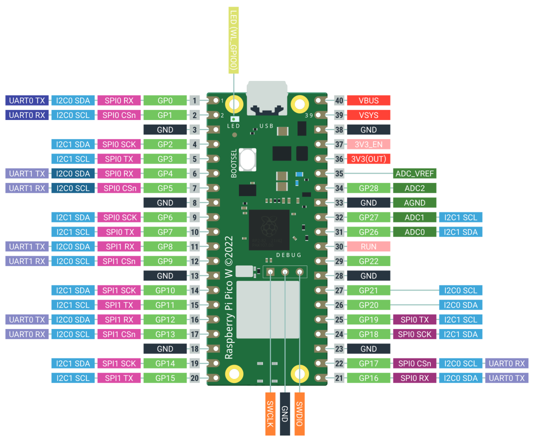
Title: Cell voltage, temp. and current sim. (control) (CVTCS-C)

Size: A4	Date: 2025-07-30	Rev: 0.2.1
KiCad E.D.A. 9.0.3		Id: 6/12

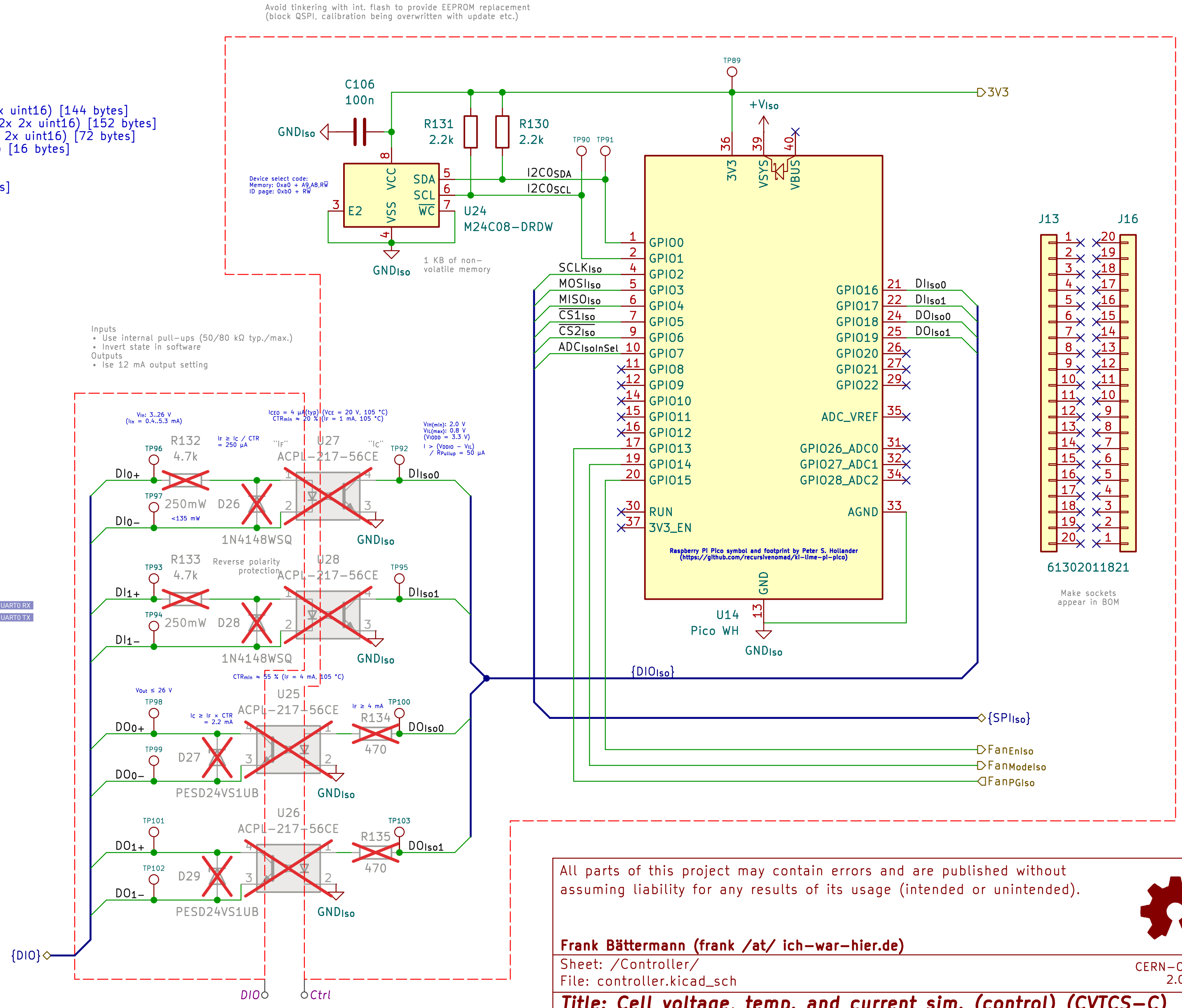
Controller

Memory contents (0.2.1, 2025–07–30):

- CRC32 on all floowing data [4 bytes]
- Configuration version (2× uint8: major, minor) [2 bytes]
- Calibration data (2 point calibration)
  - Calibration date: timestamp (uint32) [4 bytes]
  - Cell voltage: 18× 2× DAC value/voltage pairs (18x 2x 2x uint16) [144 bytes]
  - Cell temperature: 19× 2× DAC value/voltage pairs (19x 2x 2x uint16) [152 bytes]
  - BMS temperature: 9× 2× DAC value/voltage pairs (9x 2x 2x uint16) [72 bytes]
  - Current: 2× 2× DAC value/voltage pairs (2x 2x 2x int16) [16 bytes]
- Start–up values
  - Cell voltage: 18× voltage (18x uint16) [36 bytes]
  - Cell temperature: 19× temperature (19x uint16) [38 bytes]
  - BMS temperature: 9× temperature (9x uint16) [18 bytes]
  - Current: 2× voltage (2x int16) [4 bytes]
- Connectivity
  - WLAN SSID [32 Bytes]
  - WLAN PSK [32 Bytes]
  - WLAN reserved (reserved) [32 bytes]
  - BT configuration (reserved) [96 bytes]



Source: https://datasheets.raspberrypi.com/picow/PicoW-A4-Pinout.pdf



SPI1 is used for CYW43439

Pin	Function
GP23	Wireless Power On
GP24	Wireless SPI Data
GP25	Wireless SPI Chip–Select
GP29/A3	Wireless SPI Clock / VSYS Sense
A4	Temperature
WL_GPIO0	User LED
WL_GPIO1	RT6150B–33GQW Power–Select
WL_GPIO2	VBUS Sense

Source: https://picow.pinout.xyz

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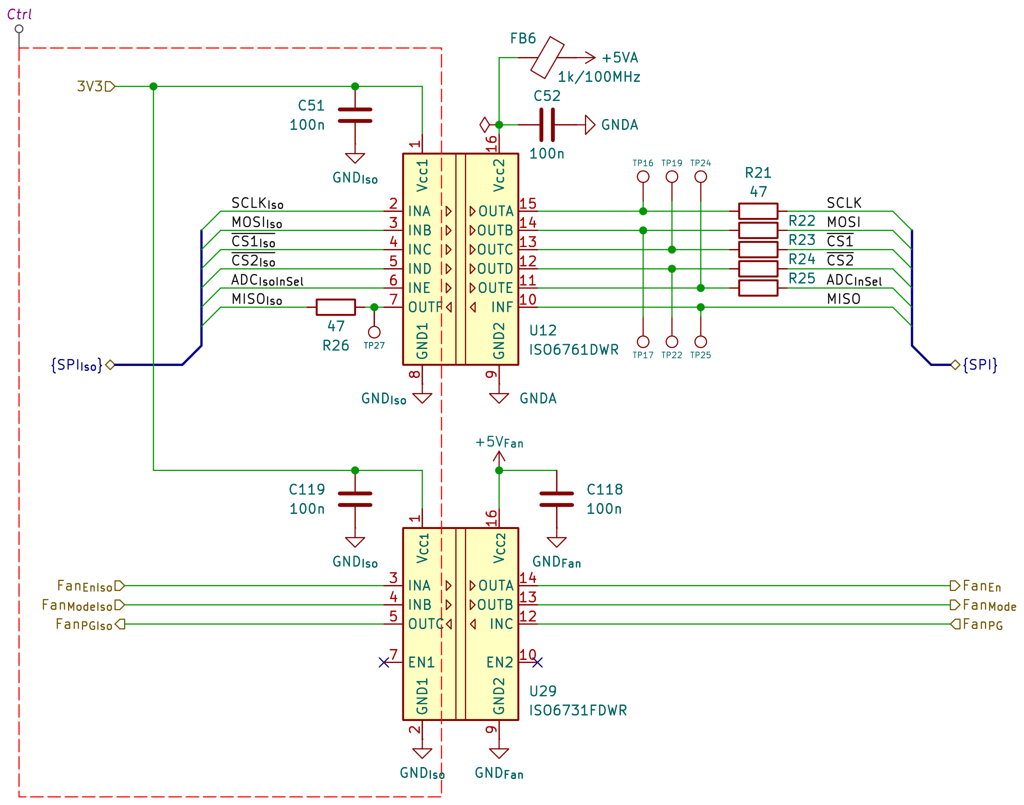
Sheet: /Controller/
File: controller.kicad_sch

Title: Cell voltage, temp. and current sim. (control) (CVTCS–C)

Size: A4 | Date: 2025–07–30 | **Rev: 0.2.1**
KiCad E.D.A. 9.0.3 | Id: 4/12

Signal isolation

Controller ↔ Analog



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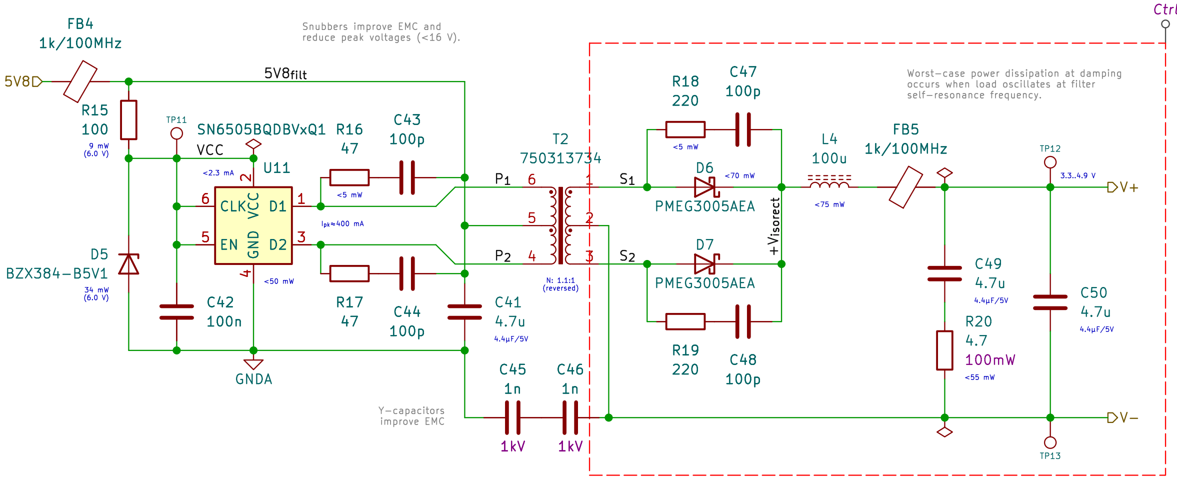
Sheet: /Signal isolation/
File: signal_isolation.kicad_sch

Title: Cell voltage, temp. and current sim. (control) (CVTCS-C)

Size: A4	Date: 2025-07-30	**Rev: 0.2.1**
KiCad E.D.A. 9.0.3		Id: 5/12

Controller supply

The controller supply is galvanically isolated from the cell voltage to prevent ground loops when multiple CVTCSs are in use.
Tight ouput regulation is not required as the Raspberry Pi Pico (W) has an step-up/step-down regulator built-in. Output voltage must be 1.8..5.5 V at all input voltages and all output load conditions. The transformer is used in reversed to step down from 5.8V.



The output must be able to deliver 1.3 W:
- Pi Pico (W) is assumed to require 50 mA/3.3 V (165 mW) under "computation load".
- CYW43439 takes up to 320 mA/3.6 V (1.15 W) at "full WiFi-load".

V_{out}/efficiency (V_{in}: 5.4 V/6.2 V)
- 4.2 V/4.9 V, 88/89 % at 150 mW
- 3.3 V/4.1 V, 80/84 % at 1.3 W

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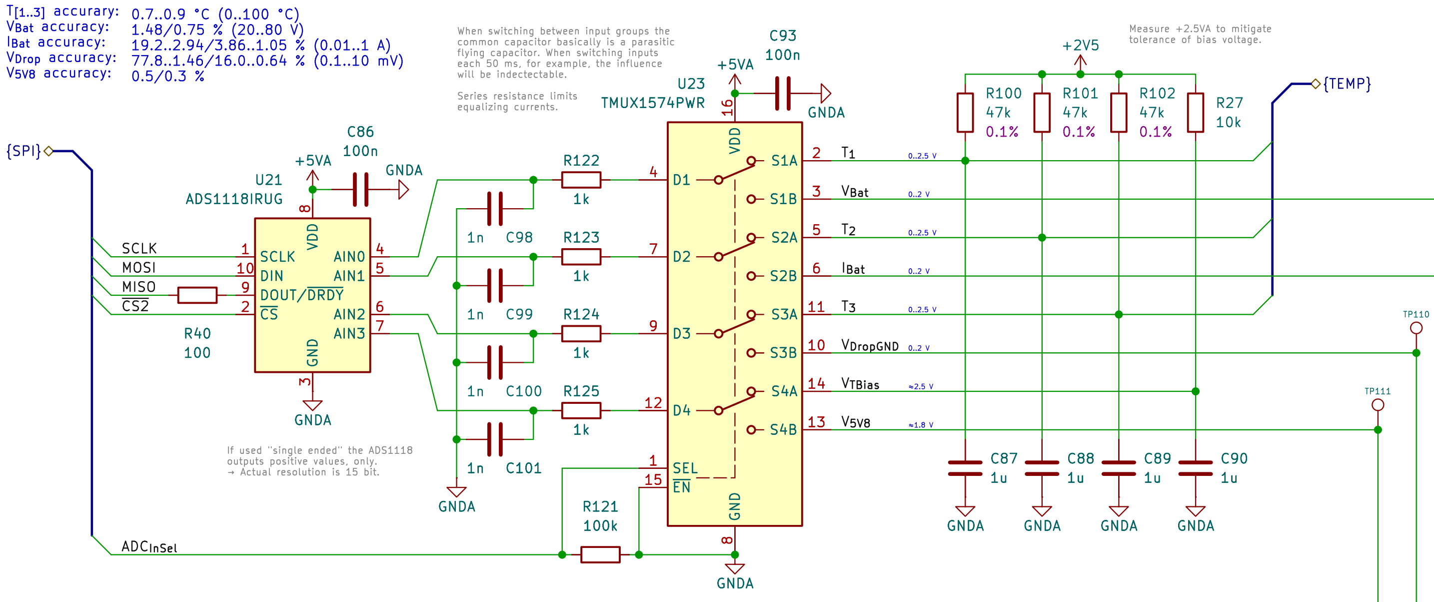
Sheet: /Controller supply/
File: ctrl-supply.kicad_sch

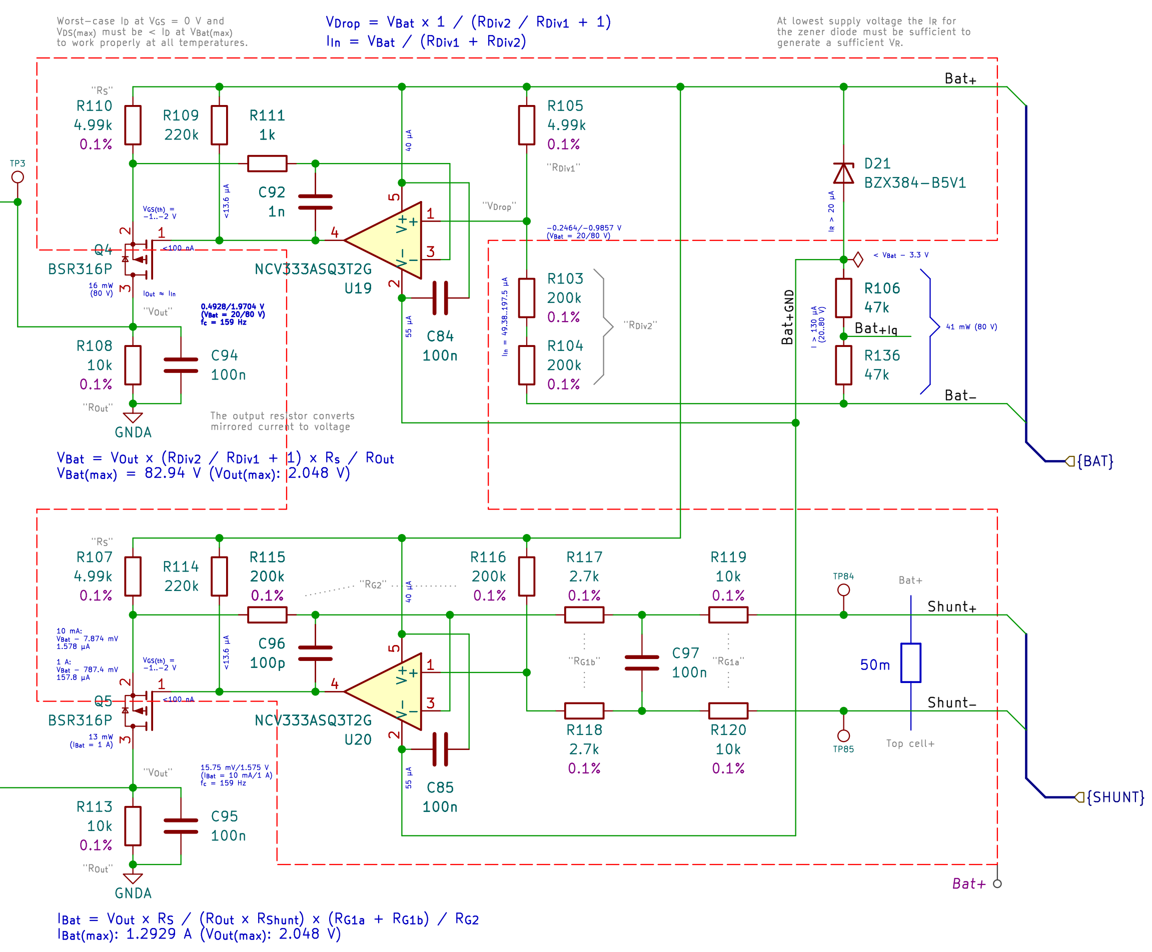
Title: Cell voltage, temp. and current sim. (control) (CVTCS-C)

Size: A5	Date: 2025-07-30	Rev: 0.2.1
KiCad E.D.A. 9.0.3		Id: 3/12

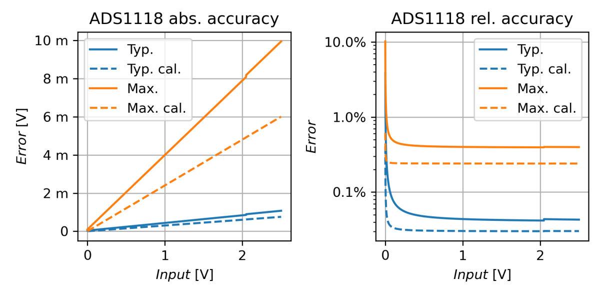
Masurement tolerances (incl. ADC(max), uncalibrated/calibrated)

$T_{[1..3]}$ accurary:	0.7..0.9 °C (0..100 °C)
V_{Bat} accuracy:	1.48/0.75 % (20..80 V)
I_{Bat} accuracy:	19.2..2.94/3.86..1.05 % (0.01..1 A)
V_{Drop} accuracy:	77.8..1.46/16.0..0.64 % (0.1..10 mV)
V_{5V8} accuracy:	0.5/0.3 %

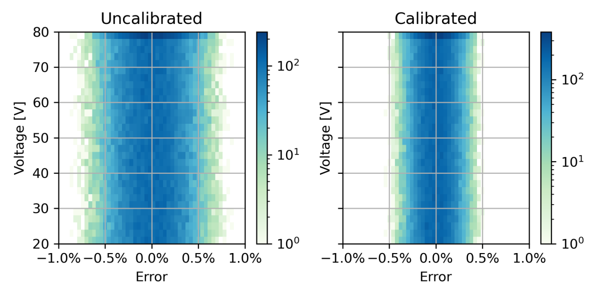




ADC accuracy (max.): Uncalibrated: 1.37 %/0.40 % (10 mV/1 V)
Calibrated: 0.28 %/0.24 %

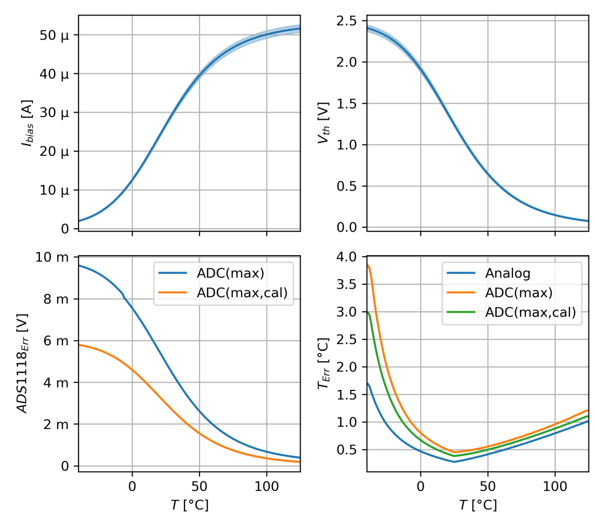


Voltage analog tolerance: Uncalibrated: 0.81 %
Calibrated: 0.50 %

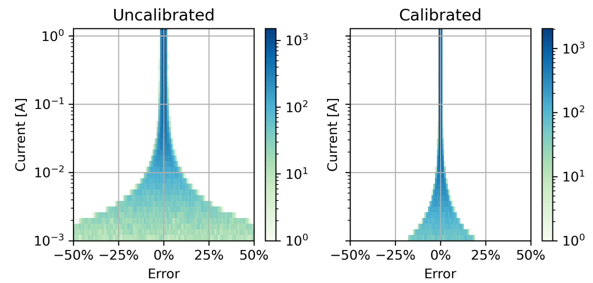


Temperature tolerance:

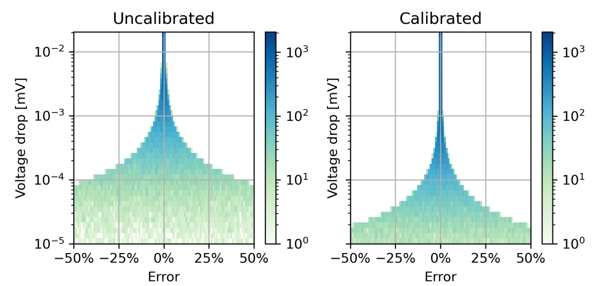
The temperarture measurement uses +2.5 V as sensor supply and the PGA=1 (2.048 V FSR) setting as well as the PGA=2 (4.096 V FSR) at temperatures below 0 °C.



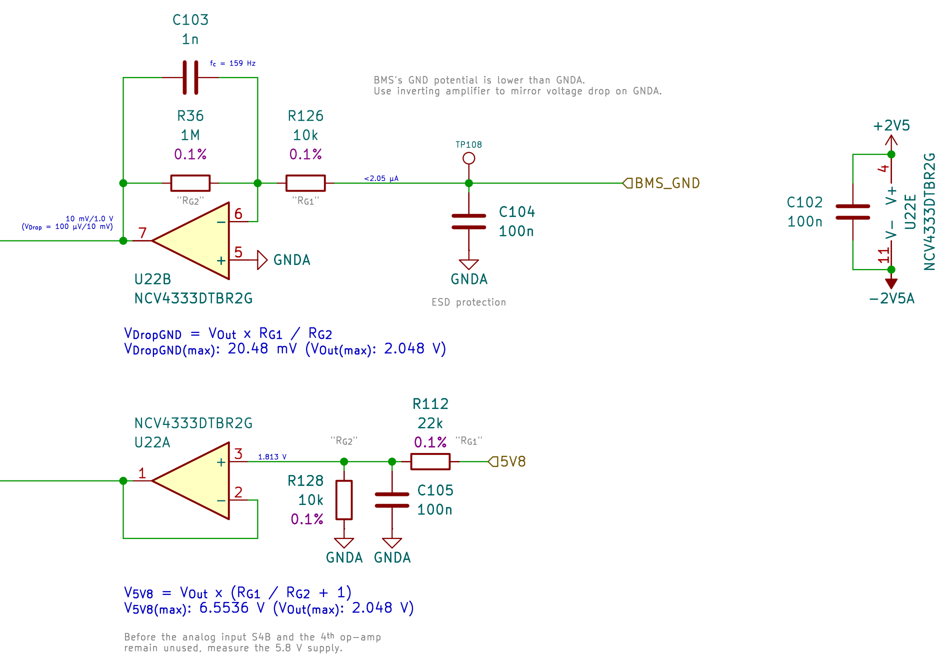
Current analog tolerance: Uncalibrated: 14.4 %/2.4 % (10 mA/1 A)
Calibrated: 3.2 %/0.8 %



GNDA–BMSGND–offset tolerance: Uncalibrated: 67.9 %/0.91 % (100 µV/10 mV)
Calibrated: 15.0 %/0.39 %



Assumptions for "uncalibrated": 30 µV op-amp offset (+140 nV/°C), 0.1 % resistors (+25 ppm/°C), 60 °C temperature rise
Assumptions for "calibrated": 140 nV/°C offset drift, 25 ppm/°C resistor drift, 60 °C temperature rise



T [°C]	T_{Err} [°C]	V_{Th} [V]
−40	3.02	2.410
−20	1.31	2.257
0	0.68	1.913
10	0.53	1.663
20	0.43	1.385
30	0.40	1.107
40	0.44	0.856
50	0.50	0.646
60	0.57	0.481
80	0.72	0.264
100	0.90	0.147
125	1.13	0.074

Frank Bättermann (frank /at/ ich-war-hier.de)

Sheet: /ADC/
File: adc.kicad_sch

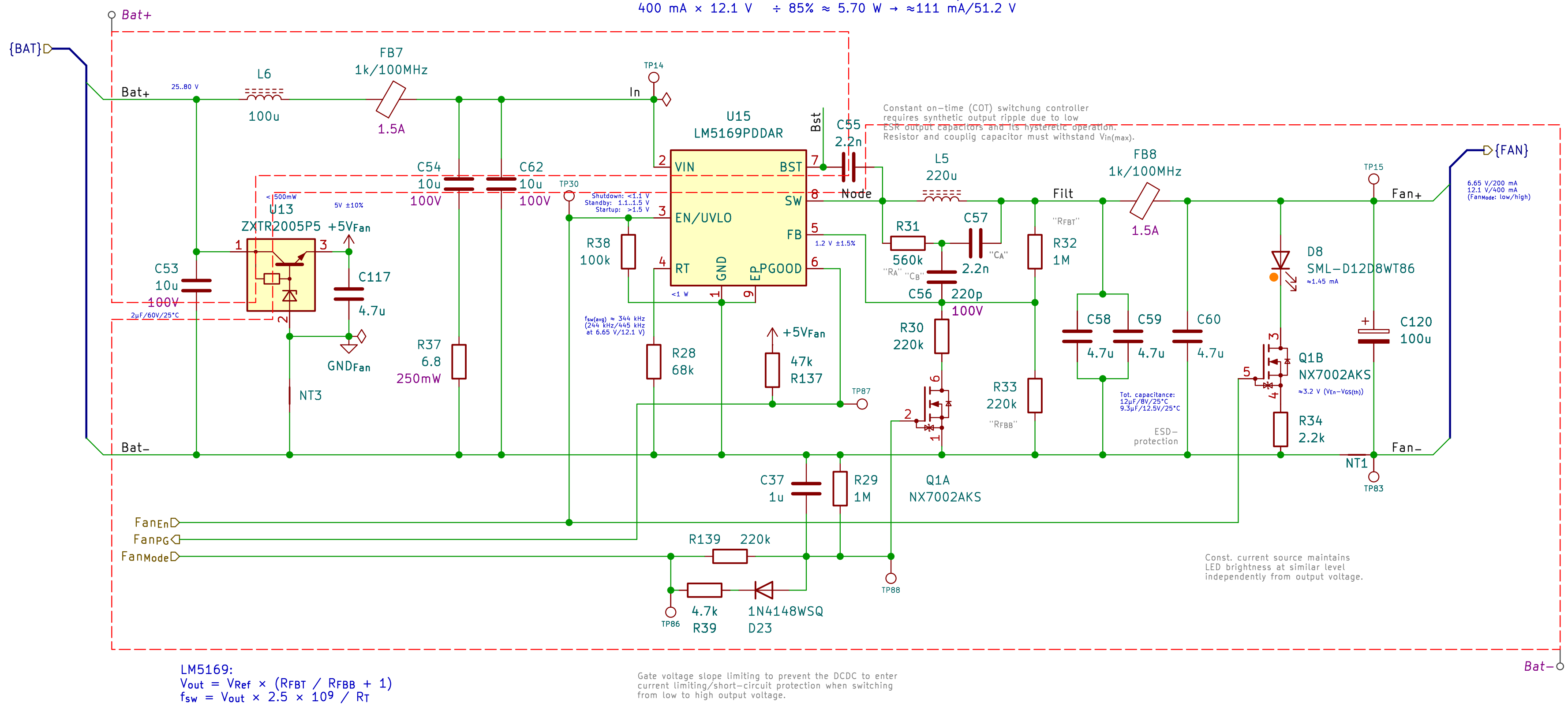
Title: Cell voltage, temp. and current sim. (control) (CVTCS-C)

Size: A3 | Date: 2025-07-30 | Rev: 0.2.1

KiCad E.D.A. 9.0.3

Fan output (non-isolated)

Battery current (examples):
200 mA × 6.65 V ÷ 75% ≈ 1.77 W → ≈35 mA/51.2 V
400 mA × 12.1 V ÷ 85% ≈ 5.70 W → ≈111 mA/51.2 V



LM5169:
$V_{out} = V_{Ref} \times (R_{FBT} / R_{FBB} + 1)$
$f_{sw} = V_{out} \times 2.5 \times 10^9 / R_T$

Inductor calculation:
Assume $\Delta I_L = I \times 40\ \% \approx 80$ mA/160 mA, $V_{in} = 65$ V
$L = V_{out} / (f_{sw} \times \Delta I_L) \times (1 - V_{out}/V_{in}) \approx 302$ µH/137 µH → 220 µH (compromise)
$\Delta I_L = V_{out} / (f_{sw} \times L) \times (1 - V_{out}/V_{in}) \approx 110$ mA/100 mA
$I_{L(pk)} = I_{out} + \Delta I_L / 2 \approx 255$ mA/450 mA

Output capacitor calculation:
Assume $\Delta V_{out} = 144$ mV/253 mV (2 % V_{out} drop on current transient)
$C_{out} > L \times (I_{out} + \Delta I_L / 2)^2 \div (2 \times \Delta V_{out} \times V_{out}) \approx 6.9$ µF/ 7.0 µF
$V_r \approx \Delta I_L \div (8 \times f_{sw} \times C_{out}) \approx 43$ mV/30 mV

Ripple network calculation (type-3):
Assume $V_{in(min)} = 40$ V
$C_A > 10 \div (f_{sw} \times R_{FBB} \,||\, R_{FBT}) \approx 373$ pF/204 pF → 2.2 nF (already used elsewhere)
$R_A \approx (V_{in} - V_{out}) \times V_{out} \div (20\ \text{mV} \times V_{in} \times f_{sw} \times C_A) \approx 455$ kΩ/581 kΩ → 560 kΩ
$C_B \geq 50$ µs $\div (3 \times R_{FBT}) \approx 150$ pF → 220 pF (alread used elsewhere)

Simulation shows ≥14.5 mV feedback ripple at $V_{in(min)}$ and $V_{out(max)}$.
According to the datasheet 12 mV shall be the very minimum at $V_{in(min)}$.

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Sheet: /Fan/
File: fan.kicad_sch

Title: Cell voltage, temp. and current sim. (control) (CVTCS-C)

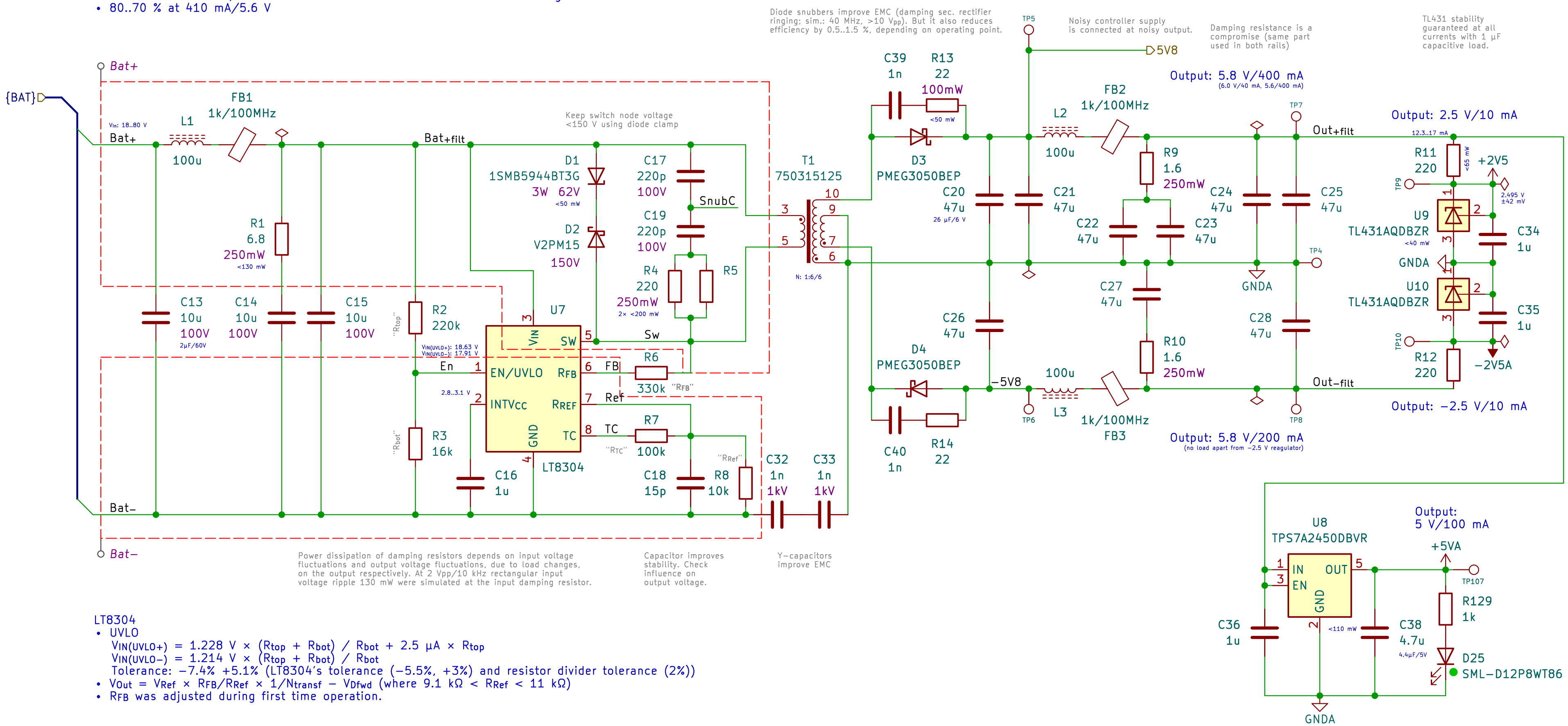
Size: A4	Date: 2025-07-30	**Rev: 0.2.1**
KiCad E.D.A. 9.0.3		Id: 12/12

Main power supply

This supplies the required voltage rails (5V8, +5VA, +2V5A, −2V5A) isolated from $Bat_{+/-}$ to allow GND to move to the potential of the connected BMS.
In this way, a voltage drop on the Bat_--connection does not disturb output signals. Partly, oversized components are used, as they can also be used for 5V supplies with increased output current.

Simulated efficiency (V_{In}: 18..80 V; PMEG3050BEP):
- 79..58 % at 40 mA/6.0 V
- 80..70 % at 410 mA/5.6 V

LT8304 minimum load (≥20 mA) is covered by
2x 2.5 V shunt regulator: ≈2x15 mA



LT8304
- UVLO
  $V_{IN(UVLO+)} = 1.228\ V \times (R_{top} + R_{bot}) / R_{bot} + 2.5\ \mu A \times R_{top}$
  $V_{IN(UVLO-)} = 1.214\ V \times (R_{top} + R_{bot}) / R_{bot}$
  Tolerance: −7.4% +5.1% (LT8304's tolerance (−5.5%, +3%) and resistor divider tolerance (2%))
- $V_{Out} = V_{Ref} \times R_{FB}/R_{Ref} \times 1/N_{transf} - V_{Dfwd}$ (where 9.1 kΩ < R_{Ref} < 11 kΩ)
- R_{FB} was adjusted during first time operation.

Parallel LC-filter dampening:
$C_{damp} = 4 \times C_{filt}$ (opt. case)
$R_{damp} = 1/(2 \times \zeta) \times \sqrt{L_{filt}/C_{filt}}$ where $\zeta = 0..1$ (1: critically damped)

Frank Bättermann (frank /at/ ich-war-hier.de)

Sheet: /Supply/
File: supply.kicad_sch

Title: Cell voltage, temp. and current sim. (control) (CVTCS-C)

Size: A4 | Date: 2025-07-30 | Rev: 0.2.1
KiCad E.D.A. 9.0.3 | Id: 2/12