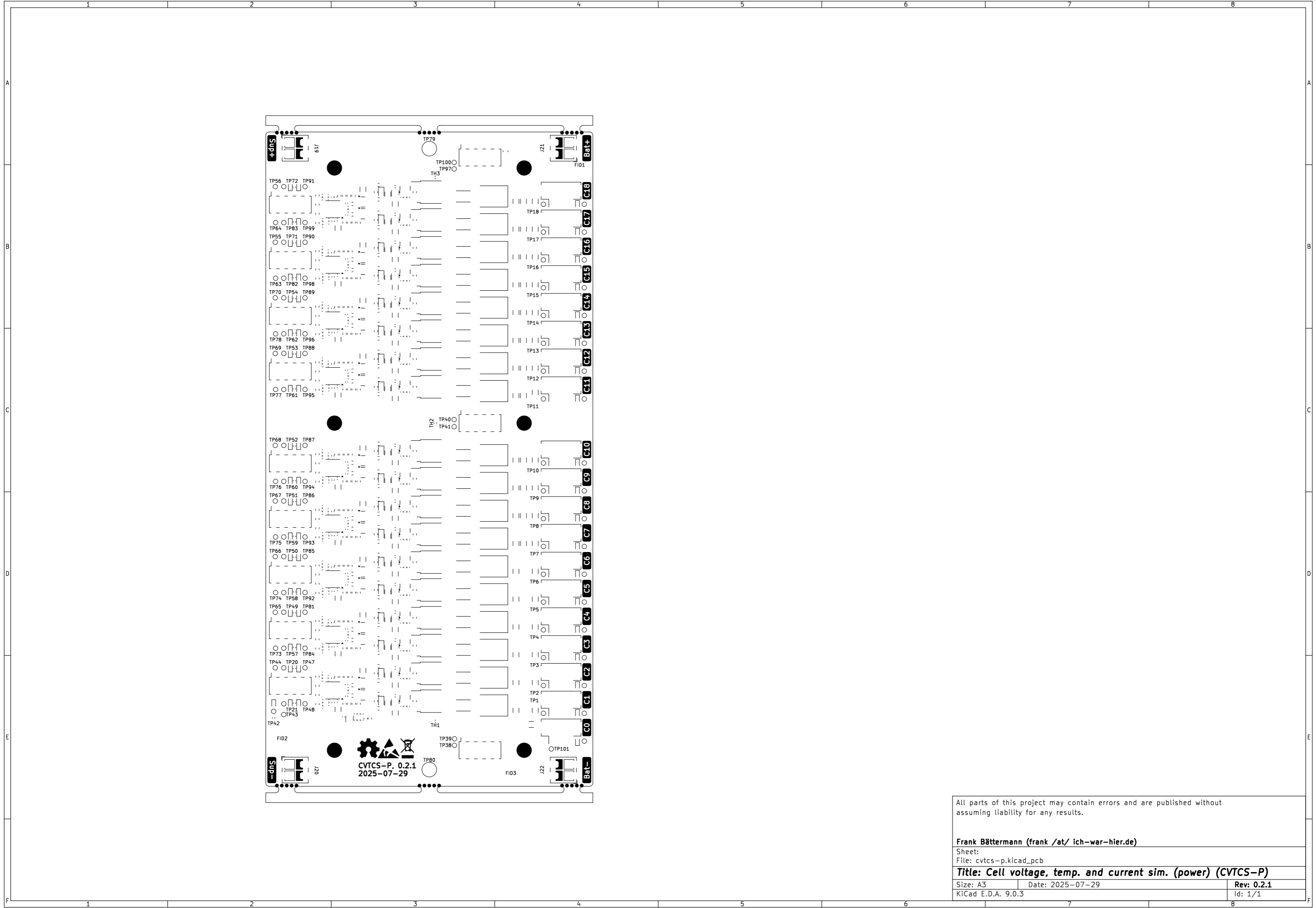
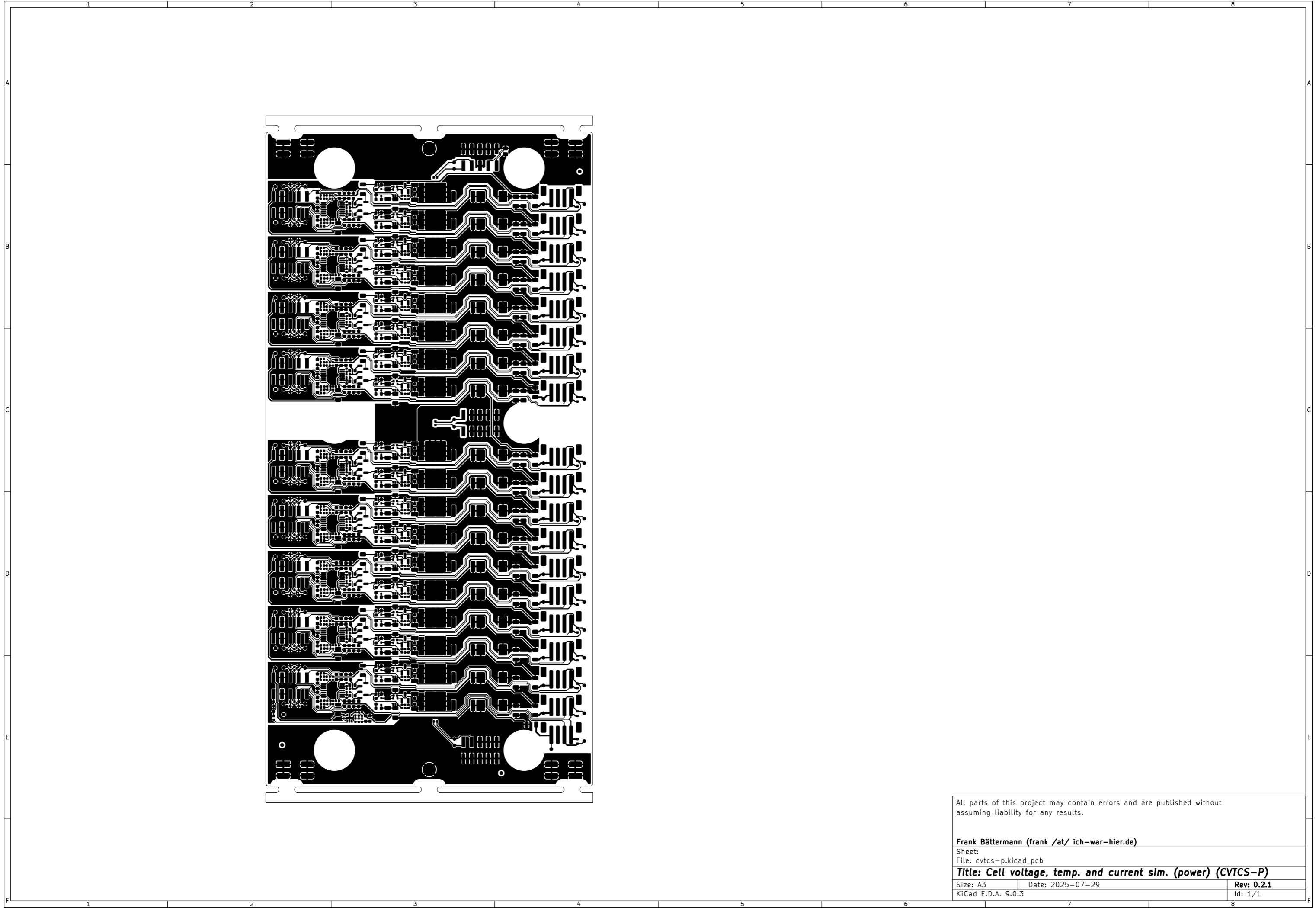


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| All parts of this project may contain errors and are published without assuming liability for any results. | | |
| Frank Bättermann (frank /at/ ich-war-hier.de) | | |
| Sheet: File: cvtcs-p.kicad_pcb | | |
| Title: Cell voltage, temp. and current sim. (power) (CVTCS-P) | | |
| Size: A3 | Date: 2025-07-29 | Rev: 0.2.1 |
| KiCad E.D.A. 9.0.3 | Id: 1/1 | |





Revision history

- 0.2.1 (2025-07-29)
- Bump to KiCad 9
 - Cleaned up F.Bat/B.Fab layers
- 0.2.0 (2024-01-12)
- Corrected C9, C15, C16, C22, C23, C29, C30, C36, C37, C43, C44, C50, C51, C57, C58, C64, C65, C120 part-numbers (correct package 0201 → 0402): GRM0335C2A101JA01? → GRM1555C2A101JA01?
 - Added 100pF in parallel to existing temperature outputs compensation (against potentially very low capacitive load, 1..10nF).
 - Corrected Silkscreen "Bat+" to "Bat-" on the negative supply.
 - Updated manufacturability/DFM info
 - Corrected typos
- 0.1.0 (2023-09-29)
- First feature complete revision
- Ideas:
- Replace channel shorting jumpers by low-resistance dip-switches or similar.
(Changing the number of cells by soldering on assembled and cooled metal-PCBs is very difficult).

Version number: X.Y.Z

X+1: Changes on interfaces, downwards compatibility is not ensured, changes on provisions
Y+1: Changes without impact on interfaces, downwards compatibility is ensured, improvements
Z+1: Formal changes, spelling mistakes, corrections

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| A | | | | | | | | |
| B | | | | | | | | |
| C | | | | | | | | |
| D | | | | | | | | |
| E | | | | | | | | |
| F | | | | | | | | |

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Frank Bättermann (frank /at/ ich-war-hier.de)

Sheet:
File: cvtcs-p.kicad_pcb

Title: **Cell voltage, temp. and current sim. (power) (CVTCS-P)**

Size: A3

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