Quartus II Device Support Release Notes

May 2008 **Quartus II version 8.0**

This document provides late-breaking information about device support in this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your **\altera\quartus<*version number*>** directory. For information about New Features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

Device Support & Pin-Out Status 3
- Full Device Support 3
- Advance Device Support 4

Timing Models 4
- Preliminary Timing Models 4
- Final Timing Models 5

Power Models 6
- Preliminary Power Models 6
- Final Power Models 6

Changes in Device Support 7

Changes to Cyclone III Final Timing Models 7
The DPA lock signal does not work in Stratix III devices 7
Default drive strength assignments for the 3.3-V LVTTL I/O Standard 8
Cyclone III RAM f_{MAX} specification changed..... 8
Stratix IV HSSI channel maximum data rate not restricted for -4 speed grade 8
Removal of 25 row DPA placement restriction..... 9
High bandwidth setting is not supported for Stratix III PLLs in External Feedback mode..... 9
M9K memory block issue in SDP x36 mode 9
Improved static power and new I/O transfer protocol support for Arria GX devices 9
Soft-CDR block simulation model issue 10
Interface issues with LVDS circuits 10
Stratix III and Stratix IV LVDS Data Rate specification 10
Stratix IV LAB counts incorrect in the Quartus II Software Version 8.0 10
Stratix III DSP Block shiftouta signal restriction 11
Stratix III pseudo LVDS standards should show slower output toggling rate 11
I/O Placement Error for External Memory Interfaces 11
M144K RAM block preliminary timing model change..... 11
MLAB RAM block size changed from 64x10 or 32x20 (640 bits) to 16x20 (320 bits)..... 12
Changed Transceiver PLL Settings for Stratix II GX and Arria GX Devices..... 12
Device Specification Change for EP3SL200 Devices..... 12
Incorrect Delay Chain Setting for Cyclone III Devices with DQS Interface 13
Incorrect f_{MAX} Reporting for Some Stratix II GX Designs 13
User Pin Assignments to PGM Pins Do Not Function Correctly Under Some Circumstances..... 13
Change in Clock Management Unit PLL Multiplication Factors.... 13
Memory Block Power Optimization Change..... 14

Revision History 15

Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the devices listed.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
MAX® IIZ	EPM240ZM100	EPM240ZM68
	EPM570ZM100	EPM570ZM144
	EPM570ZM256	
Cyclone® II	EP2C5AT144	EP2C5AF256
Cyclone III	EP3C5M164	EP3C10M164
	EP3C16M164	
	EP3C16E144	EP3C16F256
	EP3C16U256	EP3C16F484
	EP3C16U484	EP3C40Q240
	EP3C40F324	EP3C40F484
	EP3C40U484	EP3C40F780
	EP3C80F484	EP3C80U484
	EP3C80F780	
Stratix® III	EP3SL50F780	EP3SL50F484
	EP3SL70F780	EP3SL70F484
	EP3SL110F1152	EP3SL110F780
	EP3SL150ESF780	EP3SL150ESF1152
	EP3SL150F1152	EP3SL150F780
	EP3SL200F1152	EP3SL200F1517
	EP3SL200H780	EP3SL340F1517
	EP3SE50F780	EP3SE50F484
	EP3SE80F780	EP3SE110F780
	EP3SE80F1152	EP3SE110F1152
	EP3SL340H1152	
	EP3SL340F1760	EP3SE260F1152
	EP3SE260F1517	EP3SE260H780

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. The Compiler generates neither pin-out information nor programming files for these devices in this release.

Devices with Advance Support

Device Family	Devices	
Stratix IV	EP4SGX70	EP4SGX110
	EP4SGX230	EP4SGX290
	EP4SGX360	EP4SGX530
	EP4SE530	

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device	
Cyclone III	EP3C10	EP3C16
MAX II	EPM240Z	EPM570Z
Stratix III	EP3SE50	EP3SL50
	EP3SL70	EP3SE80
	EP3SE110	EP3SL110
	EP3SL150	EP3SL200
	EP3SE260	EP3SL340
Stratix IV	EP4SGX70	EP4SGX110
	EP4SGX230	EP4SGX290
	EP4SGX360	EP4SGX530
	EP4SE530	

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
Arria® GX	EP1AGX20	7.2
	EP1AGX35	7.2
	EP1AGX50	7.2
	EP1AGX60	7.2
	EP1AGX90	7.2
Cyclone II(1)	EP2C5	6.0
	EP2C8	5.1 SP2
	EP2C15	6.0
	EP2C20	5.1 SP2
	EP2C35	5.1 SP2
	EP2C50	6.0
	EP2C70	5.1 SP2
Cyclone III	EP3C40	8.0
	EP3C55	8.0
	EP3C80	8.0
	EP3C25	7.2 SP1
	EP3C120	7.2 SP1
HardCopy® II(2)	HC210	HC210W
	HC220	HC230
	HC240	
Stratix II	EP2S15	5.0 SP1
	EP2S30	5.0
	EP2S60	5.0
	EP2S90	5.0 SP1
	EP2S130	5.0 SP1
	EP2S180	5.1
Stratix II GX	EP2SGX30	7.0
	EP2SGX60	7.0
	EP2SGX90	6.1
	EP2SGX130	6.1

(1) Automotive (“A”) temperature grade EP2C15 device timing models were preliminary in the Quartus II software version 7.2 SP1.

(2) HardCopy II timing models are fully correlated to silicon in this release.

The current version of the Quartus II software also includes final timing models for the ACEX® 1K, APEX® 20K, APEX 20KE, APEX 20KC, APEX II, Cyclone, FLEX® 6000, FLEX 10K, FLEX 10KA, FLEX 10KE, MAX II, MAX 7000S, Stratix, and Stratix GX device families. Timing models for these device families became final in versions 5.0 and earlier.

Power Models

Preliminary Power Models

The following table shows the devices with preliminary power model status in the current version of the Quartus II software:

Devices with Preliminary Power Models

Device Family	Power Model Status
Cyclone III	Preliminary – 8.0
MAX IIZ	Preliminary – 8.0
Stratix III	Preliminary – 8.0
Stratix IV	Preliminary – 8.0

Final Power Models

The following table shows the devices with final power model status in the current version of the Quartus II software:

Devices with Final Power Models

Device Family	Power Model Status
Arria GX	Final – 7.2
Cyclone	Final – 5.1
Cyclone II	Final – 6.0
HardCopy II	Correlated(1) – 7.2
MAX 3000A	Final – 5.1
MAX 7000AE	Final – 5.1
MAX 7000B	Final – 5.1
MAX II	Final – 5.0 SP1
Stratix	Final – 5.1
Stratix GX	Final – 5.1
Stratix II	Final – 6.0
Stratix II GX	Final – 7.1

(1) HardCopy II power models are fully correlated to silicon in this release.

Changes in Device Support

Changes to Cyclone III Final Timing Models

Issues in the Quartus II software version 7.2 SP2 Cyclone III timing models were discovered through the characterization of follow-on devices; these issues are addressed in all Cyclone III devices in the Quartus II software version 8.0 release. Here is a summary of the fixed issues:

Description	Timing Impact	Type of Design Impacted
Modeled on-die variations of clock delays with minimum/maximum delay windows	Downside (-1.1% f_{MAX})	All designs
Reduced clock uncertainty guard bands based on silicon characterization	Upside	High performance clocks when **derive_clock_uncertainty** is used
M4K t_{CO} reduction by 10%	Upside	Designs with not fully registered M4K memory blocks
M4K f_{MAX} upgraded (up to 315MHz)	Upside	High performance designs with M4K memory blocks
DSP f_{MAX} upgraded (up to 340MHz)	Upside	High performance designs with DSP blocks
Updated DDR macro timing model with characterized data	DDR specific	DDR designs should be re–timing analyzed
Corrected (swapped) I/O timing models rise/fall delays	I/O specific	Designs with tight I/O timing constraints
Routing delays may change slightly due to round-off/ compiler changes	Negligible	All designs

The DPA lock signal does not work in Stratix III devices

The DPA lock signal does not function correctly for all situations in Stratix III devices. It has been replaced with soft logic inside the altlvds megafunction itself. If you are using the altlvds megafunction with DPA, recompile your design in the Quartus II software version 8.0.

Most designs should not require modification. For details on the soft-logic implementation, refer to the Stratix III Device Family Errata Sheet.

The megafunction simulation model has not been updated and so will still reflect the old DPA lock behavior, which is functionally similar to the soft logic implementation.

External PLL mode is not supported in the MegaWizard Plug-In Manager when using DPA lock because two extra ports on the altlvds megafunction are now required (core clock and PLL reset). These ports can be manually added in the altlvds MegaWizard-generated wrapper file. The altlvds megafunction will give an error if the DPA lock is used and these ports are not connected in external PLL mode. The error indicates how to manually fix the wrapper.

The altlvds MegaWizard will show some DPA lock options that will not work.

Additionally, if the `rx_dpa_locked` output port is used for Stratix III devices, the formal verification model does not match the Quartus II-generated megafunction; however, this error message can be safely ignored.

Applies to: Stratix III devices

Default drive strength assignments for the 3.3-V LVTTL I/O Standard

If you do not make any specific drive-strength assignments for the 3.3-V LVTTL I/O standard when targeting a Cyclone III device, the default drive-strength is correctly set at 8mA in the Quartus II software version 8.0. However, for the Quartus II software version 7.2, the default drive-strength was incorrectly changed to 4mA for 3.3-V LVTTL I/O standard.

- Quartus II 7.2 SP1, 7.2 SP2, 7.2 SP3 - 3.3-V LVTTL default drive-strength is 4mA.
- Quartus II 8.0 - 3.3-V LVTTL default drive-strength is 8mA.

Applies to: Cyclone III devices

Cyclone III RAM f_{MAX} specification changed

The Cyclone III RAM f_{MAX} specification has changed in Quartus II software version 8.0. The new specification is as follows:

- Cyclone III devices in C6 grades - 315 MHz
- Cyclone III devices in C7/I7/A7 grades - 274 MHz
- Cyclone III devices in C8 grades - 238 MHz

Applies to: Cyclone III devices

Stratix IV HSSI channel maximum data rate not restricted for -4 speed grade

The Quartus II software version 8.0 allows you to run the HSSI channel at 6.375Gbps in the -4 speed grade; however, the maximum data rate should be only 5 Gbps in the -4 speed grade.

Applies to: Stratix IV devices

Removal of 25 row DPA placement restriction

Quartus II software versions earlier than 8.0 enforced a maximum separation of 25 rows between any two DPA channels that were part of the same interface (that is, driven from the same PLL). This restriction was intended to ensure minimum skew between any two channels.

Starting in the Quartus II software version 8.0, this restriction has been removed. To account for skew between any two channels (which can also result from board level skew), use receiver data realignment to ensure alignment across multiple channels. For information on receiver data realignment, refer to the "High-Speed Differential I/O Interfaces and DPA" chapter in the *Stratix III Handbook*, vol. 1.

Applies to: Arria GX,HardCopy II, Stratix II, Stratix II GX, and Stratix III devices

High bandwidth setting is not supported for Stratix III PLLs in External Feedback mode

External Feedback mode for Stratix III PLLs does not support the **High** bandwidth setting. However, the Quartus II software version 8.0 does not generate an error message for this case. In addition, the MegaWizard Plug-In Manager also allows you to select **High** for the bandwidth setting for Stratix III PLLs in External Feedback mode.

If you use the External Feedback mode, always select **Low** or **Medium** for the bandwidth setting while instantiating an altpll megafunction in the MegaWizard. However, if you select the **Auto** bandwidth setting, the MegaWizard could still generate a PLL with a **High** bandwidth setting, and so you should avoid the **Auto** bandwidth setting as well.

Applies to: Stratix III devices

M9K memory block issue in SDP x36 mode

The M9K memory block was configured incorrectly when used in SDP x36 mode using Output Clear latch but not output register in the Quartus II software version 7.2. This issue is resolved in the Quartus II software version 8.0.

Applies to: Stratix III devices

Improved static power and new I/O transfer protocol support for Arria GX devices

Static power specifications of Arria GX devices have been reduced by 20%. This change affects power models that were previously designated as Final. I/O transfer protocol support for Arria GX devices now includes 3G, SDI, XAUI, SGMII, and SRIO. Multiple I/O transfer protocols are now allowed in the same transceiver quad.

Applies to: Arria GX devices

Soft-CDR block simulation model issue

For Quartus II software version 7.2, the Quartus II software incorrectly modeled the recovered clock for the Stratix III Soft-CDR block (that is, LVDS_RX `divfwdclk`) as a positive clock in timing analysis, when in fact the clock was inverted. Starting in the Quartus II software version 8.0, this issue is fixed. Additionally, the altlvds megafunction is fixed so that the inverted recovered clock is a positive clock before being sent to the core (that is, altlvds `rx_div_fwdclk` is a positive clock).

Applies to: Stratix III devices

Interface issues with LVDS circuits

The Quartus II software version 7.2 (including all 7.2 service packs) incorrectly modeled the timing of the interface from LVDS RX register to LE register for Stratix III devices, with the result that the interface could malfunction. This issue is fixed in the Quartus II software version 8.0. Stratix III designs with LVDS should be recompiled with version 8.0 or later.

Applies to: Stratix III devices

Stratix III and Stratix IV LVDS Data Rate specification

The Quartus II software version 8.0 has incorrect -4 LVDS data rate specifications for Stratix III and Stratix IV devices that use C4 grades, Stratix III industrial -4 devices, and Stratix III devices that use C4L speed grades (high and low core voltage). These specifications should be 1040 Mbps, not 1250 Mbps.

Applies to: Stratix III and Stratix IV devices

Stratix IV LAB counts incorrect in the Quartus II Software Version 8.0

The Quartus II software version 8.0 shows incorrect LAB counts for Stratix IV devices. The data should be the following:

Stratix IV device	Number of LABs shown in the software	Final number of LABs
EP4SGX70	2816	2904
EP4SGX110	3960	4224
EP4SGX230	8550	9120
EP4SGX290	12208	11648
EP4SGX360	13936	14144
EP4SGX530	21248	21248

Applies to: Stratix IV devices

Stratix III DSP Block shiftouta signal restriction

The DSP block `shiftouta` signal can drive logic only if the option **Register shifouta output** is **Off**. If that option is **On**, the `shiftouta` signal may drive the `chainin` signal of an adjacent DSP block using only a direct routing connection.

Applies to: Stratix III devices

Stratix III pseudo LVDS standards should show slower output toggling rate

The Stratix III Row I/O output toggling rate of pseudo LVDS standards (**LVDS 1R and 3R**, **RSDS 1R and 3R**, **mini-LVDS 1R and 3R**) shows the same as the True-LVDS counterpart standard and is too fast. Pseudo LVDS standards should have slower output toggling rate. Please refer to the *Stratix III Device Handbook* for the correct numbers.

Applies to: Stratix III devices

I/O Placement Error for External Memory Interfaces

Stratix III designs using external memory interfaces may cause a compilation error if the data pins of your external memory interface use I/O pins on more than one side of the device. External memory interfaces with DQ pins exclusively bound in top, bottom, left, or right side I/O pins are not affected. The error message is "`Error: Cannot place DQ I/O "mem_dq[nn]" to I/O location Pin_Nn since its memory interface I/O group cannot be placed.`" Altera recommends that data groups for external memory interfaces be grouped on a single side of your Stratix III FPGA. If you cannot group your DQ pins on a single side or if you want more information on this issue, contact Altera Technical Support at **www.altera.com/mysupport** and provide the reference number **rd05232008_407**.

Applies to: Stratix III devices

M144K RAM block preliminary timing model change

The Stratix III M144K RAM block timing performance has changed for memory blocks using fast write mode. Fast write mode is used for M144K memories when the Read-During-Write option is set to "Don't Care" or "New Data". The timing model change does not affect memories using ECC mode or ROM mode or for which the Read-During-Write option is set to "Old Data" or "Old memory contents appear". To apply the updated timing model for M144K RAM blocks, recompile the design with the Quartus II software version 7.2 SP3 or later.

Applies to: Stratix III ES devices

MLAB RAM block size changed from 64x10 or 32x20 (640 bits) to 16x20 (320 bits)

The Stratix III MLAB RAM block size has changed from 64x10 or 32x20 (640 bits) to 16x20 (320 bits) and no longer has native byte enable signals. The MLAB block in ROM mode is not affected and remains at 64x10 or 32x20 (640 bits).

If your design uses MLAB blocks, you must recompile your design with the Quartus II software version 7.2 SP3 or later to implement the changes to the MLAB blocks as well as automatic fixes to ensure device functionality when targeting MLAB blocks. To determine whether your design uses MLAB blocks, check the Quartus II Fitter Report.

There are two reasons your design may contain MLAB blocks. The first reason is due to an explicit (hard) assignment to the MLAB block type. This assignment is made either through an EDA synthesis tool or through the Quartus II RAM MegaWizard by setting the block type to MLAB. The second reason your design may contain MLAB blocks is due to a determination that is made at the discretion of the Quartus II software synthesizer or Fitter during compilation. The current Quartus II software version will automatically use MLAB blocks in the new configuration when appropriate as well as promote larger RAM blocks to M9K blocks where necessary.

Recompile your design with the Quartus II software version 7.2 SP3 or later.

Applies to: Stratix III devices

Changed Transceiver PLL Settings for Stratix II GX and Arria GX Devices

The Quartus II software has updated the CMU PLL loop filter resistor control and charge pump settings used for 3G and 6G basic modes in Stratix II GX devices and 3G basic modes in Arria GX devices. This change improves the CMU PLL performance for some configurations. No design change is needed; the Quartus II software will apply the updated settings during compilation.

Applies to: Stratix II GX and Arria GX devices

Device Specification Change for EP3SL200 Devices

The device specifications for EP3SL200 devices have changed, including resource counts, pin-outs, speed grades and package options. Projects that use EP3SL200 devices should be compiled with the Quartus II software version 7.2 SP1 or later. Updated device specifications are provided in the *Stratix III Device Handbook*.

Applies to: Stratix III EP3SL200 devices

Incorrect Delay Chain Setting for Cyclone III Devices with DQS Interface

Device characterization has determined that the correct delay chain value for hybrid memory interfaces (i.e., those with multiple DQS pins placed on adjacent sides of the device) should be 0. The Quartus II software version 7.2 and earlier incorrectly set the value to 1. The incorrect setting causes a performance decrease. To correct the setting, recompile your design using the Quartus II software version 7.2 SP1 or later.

Applies to: Cyclone III devices

Incorrect f_{MAX} Reporting for Some Stratix II GX Designs

Designs that target the Stratix II GX C5 speed grade, and use the DSP block in 36x36-bit multiply mode and use dynamic control of the signed / unsigned behavior of the multiplier have an overly low f_{MAX} limit in the Quartus II software version 7.2 (197 MHz). The Quartus II software versions 7.2 SP1 and later correct the f_{MAX} limit for this mode to 305 MHz, which matches the limit in the Quartus II software releases earlier than 7.2.

No design that closed timing in the Quartus II software version 7.2 will be affected by this change, because it can only increase the operating speed of a design. If your design matches the case listed above, and your operating frequency was limited by the DSP block, you should re-run timing analysis in the Quartus II software version 7.2 SP1 or later to obtain a corrected and less conservative timing report.

Applies to: Stratix II GX devices in C5 grades

User Pin Assignments to PGM Pins Do Not Function Correctly Under Some Circumstances

Programming pins do not function correctly as user I/O pins when remote update is enabled in an Active Serial Configuration scheme. No Compiler warning is issued by the Quartus II software version 7.2 SP1 and earlier.

Applies to: Arria GX, Stratix II, and Stratix II GX device families

Change in Clock Management Unit PLL Multiplication Factors

This change affects the (OIF) CEI PHY interface protocol for Stratix II GX instantiations of the alt2gxb megafunction. In the Quartus II software version 7.2 and earlier, you could specify a data rate to input clock frequency ratio of 10, 20,

or 40 when operating in the 4.7–5.7 Gbps range. Beginning in version 7.2 SP1, that ratio can be only 10 or 20.

Applies to: Stratix II GX

Memory Block Power Optimization Change

The ability to use separate clock enable signals for the input clock and the core clock to save power on Stratix III M9K and M144K memory blocks has been temporarily disabled in the Quartus II software version 7.2 SP2, 7.2 SP3, and 8.0. If you are using Quartus II native synthesis, this change is transparent. If you are using a 3rd party EDA synthesis tool, the Quartus II software may generate an error during compilation. Use the MegaWizard Plug-In Manager or your 3rd-party tool to regenerate the netlist and recompile the design in the latest version of the Quartus II software. This change results in an average core dynamic power increase of 1% for designs that use embedded memory.

Applies to: Stratix III

Revision History

Revision	Description
1.0	Initial Release