APPENDIX D - SETUP FOR DIFFERENT MCU's

Using JBug11 with different members of the 68HC11 family.

Talker, Map and Overlay Files:

Chip	**Default CONFIG register**	**Suitable RAM talker**	**Map file for RAM talker**	**EEPROM and EPROM programming overlay files**
A0, A1, A8	$0C, $0D, $0F	Talk_A.BOO or Talk_A.XOO	Talk_A.MAP	Ovly_Eeprom_A.rec *OTP Eprom is not available in 'A' chips*
D	N/A	Talk1_D.BOO **and** Talk2_D.rec *See note 1 below*	Talk_D.MAP	
E0, E1, E9	$0C, $0D, $0F	Talk_E.BOO or Talk_E.XOO	Talk_E.MAP	Ovly_Eeprom_E.rec Ovly_Eprom_E.rec
811E2	$FF	Talk_E2.BOO or Talk_E2.XOO	Talk_E2.MAP *If using Al Williams Talkeree:* Talk.AW.MAP	Ovly_Eeprom_E.rec
E20	$0F ?	Talk_E.BOO or Talk_E.XOO	Talk_A.MAP	Ovly_Eeprom_E.rec Ovly_Eprom_E20.rec
F1	$FF	Talk_F1.BOO	Talk_F1.MAP	Ovly_Eeprom_F1.rec
K series		Talk_K.BOO or Talk_K.XOO *See note 2 below*	Talk_K.MAP	Ovly_Eeprom_K.rec Ovly_Eprom_K4.rec

Notes:

1. The D series chips present something of a challenge to JBug11 because of the limited RAM available for the talker. I have experimentally overcome this limitation, but only for chips able to access external RAM memory, such as the MicroStamp11 development boards by Technological Arts. The talker is split into two parts: the first is loaded by the normal bootstrap loading operation; it contains the basic memory read and write routines. The first part is then able to load the second part, which has the inherent register and SWI service routines, as an S19 into any convenient bit of external RAM. Anyone proposing to use these talkers must study the assembly file listings, as they will probably need to re-assemble both parts to suit the available on-board memory.

2. The K series talkers should be treated as experimental at this stage, although from user feedback, they appear to be satisfactory.