FD6287T

Three-phase 250V gate driver

Overview

The FD6287T is a device that integrates three independent half-bridges. Gate driver integrated circuit chip, specially designed for high voltage and high speed driving The active MOSFET design allows it to operate at voltages up to +250V.

FD6287T has built-in VCC/VBS undervoltage (UVLO) protection. Protection function to prevent the power transistor from operating at excessively low voltage.

The FD6287T features built-in pass-through prevention and dead time protection. Prevents shoot-through of driven high-side and low-side MOSFETs , effectively protecting them. Power devices.

The FD6287T has a built-in input signal filter to prevent input signal interference. Noise interference.

Features

ÿ Floating absolute voltage +250V

ÿ Power supply operating voltage range: 7~20V

ÿ Integrates three independent half-bridge drives

Output current +1.5A/-1.8A

ÿ 3.3V/5V input logic compatible

ÿ VCC/VBS undervoltage protection (UVLO)

Built-in pass-through prevention function

Built-in 200ns dead time

Built-in input filtering function

High-end and low-end channel matching

• High-side outputs are in phase with inputs, low-side outputs are in phase with inputs. Inverted

Packaging

TSSOP-20

application

Three-phase motor drive

1. Absolute maximum ratings (unless otherwise specified, all pins are referenced to COM).

parameter		symbol	scope	unit
High-side floating absolute voltage		VB1,2,3	-0.3ÿ275	In
High-side floating offset voltage,		VS1,2,3	VB1,2,3-25ÿVB1,2,3+0.3	In
high-side output voltage,		VHO1,2,3	VS1,2,3-0.3ÿVB1,2,3+0.3	In
low-side supply voltage,		VCC	-0.3ÿ25	In
low-side output voltage		VLO1,2,3	-0.3ÿVCC+0.3	In
Logic input voltage (HIN, LIN*) Offset		COME	-0.3ÿVCC+0.3	In
voltage Slew rate range Power		dVS/dt	ÿ50	V/ns
dissipation @TAÿ25ÿC TSSOP-20	Junction-to-ambient	PD	ÿ1.25	IN
thermal resistance	TSSOP-20	The Region	ÿ100	ÿC/W
Junction		Tj	ÿ150	ÿC
temperature range Storage		Test	-55ÿ150	ÿC

temperature range Note 1: Under no circumstances should the PD be exceeded.

Note 2: Exceeding the absolute maximum rated voltage may damage the chip.

2. Recommended operating conditions (all voltages are referenced to COM)

parameter	symbol	Minimum value	Maximum value	unit
High-side floating absolute	VB1,2,3	VS1,2,3+7	VS1,2,3+20	In
voltage, static high-side floating offset	VS1,2,3	COM-2 (Note 1) -50	250	In
voltage, dynamic high-side floating offset	VS1,2,3	(Note 2)	250	In
voltage, high-side output voltage	VHO1,2,3	VS1,2,3	VB1,2,3	In
Low-side supply voltage	VCC	7	20	In
Low-side output	VLO1,2,3	0	VCC	In
voltage, logic input voltage (HIN, LIN*),	COME	0	VCC	In
ambient	FACING	-40	125	ÿC

temperature. Note 1: HO operates normally when VS1,2,3 are from (COM-2V) to 250V . When VS1,2,3 are from (COM-2V) to (COM-VBS), HO logic...

The editing status remains unchanged.

Note 2: VS1,2,3 are (COM-50V) and HO works normally when there is a transient negative voltage of 50ns.

Note 3: Operating the chip beyond the recommended operating conditions for extended periods may affect its reliability. It is not recommended to operate the chip beyond the recommended conditions.

Long-term work.

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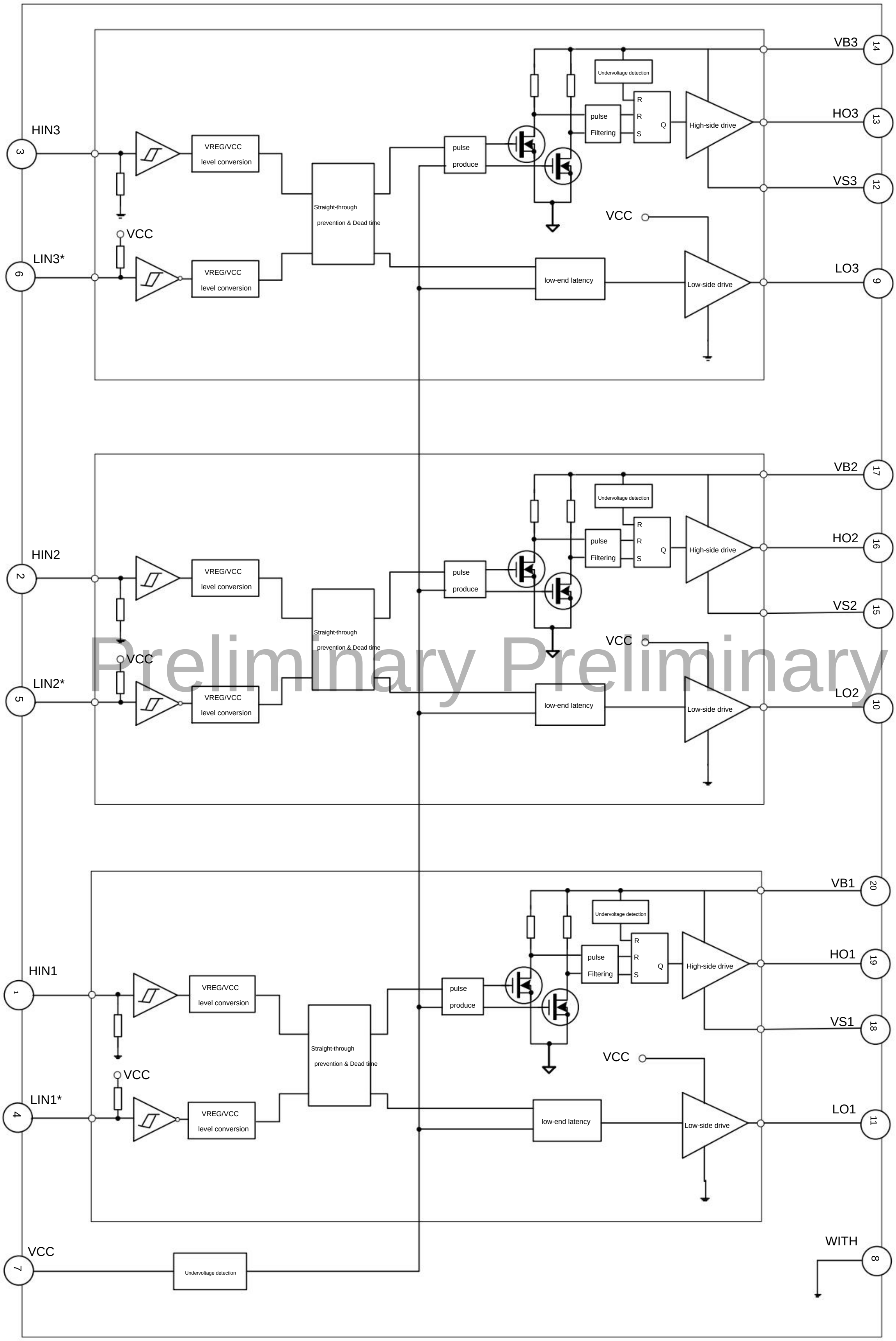
3. Static electrical parameters (unless otherwise specified, TA = 25°C, VCC = VBS1,2,3 = 15V, VS = COM)

parameter	symbol	Test conditions	Minimum va	lue, typical valu	e, maximum v	alue, unit
High-level input threshold voltage; Low-	HIV		2.7	--	--	In
level input threshold voltage; VCC	WILL		--	--	0.8	In
undervoltage protection trip voltage ; VCCUV+ ; VCC undervoltage			5.8	6.4	7.0V	
protection reset voltage; VCCUV-; VCC undervoltage protection			5.4	6.0	6.6V	
hysteresis voltage; VCCUVH ; VBS undervoltage protection trip			0.3	0.4	-- In	
voltage; VBSUV + ; VBS undervoltage protection reset voltage;			5.8	6.4	7.0V	
VBSUV- ; VBS undervoltage protection hysteresis voltage; VBSUVH;			5.4	6.0	6.6V	
Floating power supply leakage current.			0.3	0.4	-- In	
	FIRST	VB1,2,3=VS1,2,3=250V	--	0.1	5.0 ÿA	
VBS static current	IQBS VIN=0V or 5V		--	180	270 ÿA	
VBS dynamic current	IPBS fHIN1,2,3=20kHz		--	180	270 ÿA	
VCC quiescent current	IQCC	VIN = 0V or 5V	--	330	500 uA	
VCC dynamic current	IPCC fLIN1,2,3=20kHz LIN* High-level		--	330	500 uA	
input bias current ILIN+ VLIN=0V LIN* Low-level input bias current ILIN- VLIN=5V HIN High-			--	20	40 ÿA	
level input bias current IHIN+ VHIN =5V HIN Low-level input bias current IHIN- VHIN=0V			--	--	2	ÿA
Input pull-down resistor High-level output voltage Low-level output voltage High-level output			--	20	40 ÿA	
short-circuit pulse current IOH VO=0V, VIN=5V, PWDÿ10ÿs 1.1 Low-level output short-circuit			--	--	2	ÿA
pulse current IOL VO=15V,	ALSO		200	260	320 Kÿ	
VIN=0V, PWDÿ10ÿs 1.3 VS	VOH IO=100mA		--	0.6	0.9V	
Static negative voltage	VOL IO=100mA		--	0.3	0.45V	
				1.5	1.9 A	
				1.8	2.3 A	
	VSN		--	-6.0	-- In	

4. Dynamic electrical parameters (unless otherwise specified, TA = 25°C, VCC = VBS1,2,3 = 15V, VS = COM)

parameter	symbol	Test conditions	Minimum va	lue, typical valu	e, maximum v	alue, unit
Output rising edge propagation	your		--	300	450 ns	
time; Output falling edge	picture		--	100	160	ns
propagation time;	tr	CL=1000pF	--	12	--	ns
Output rise time;	tf	CL=1000pF	--	12	--	ns
Output fall time; High/low	MT		--	--	50	ns
side delay matching; Dead time	DT		100	200	300 ns	

5. Circuit block diagram



6. Chip Pin Configuration

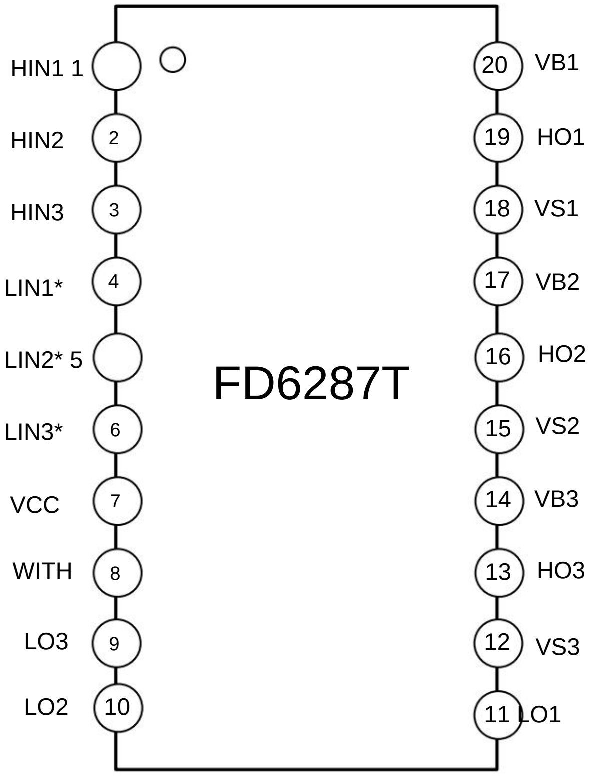
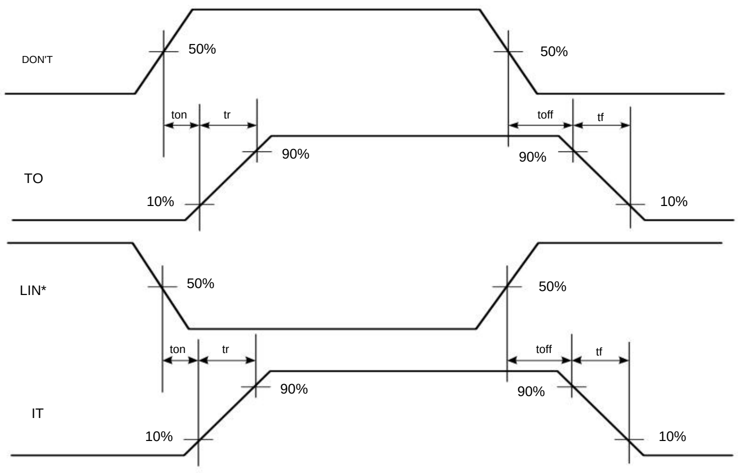


Figure 6-1 Package pin diagram

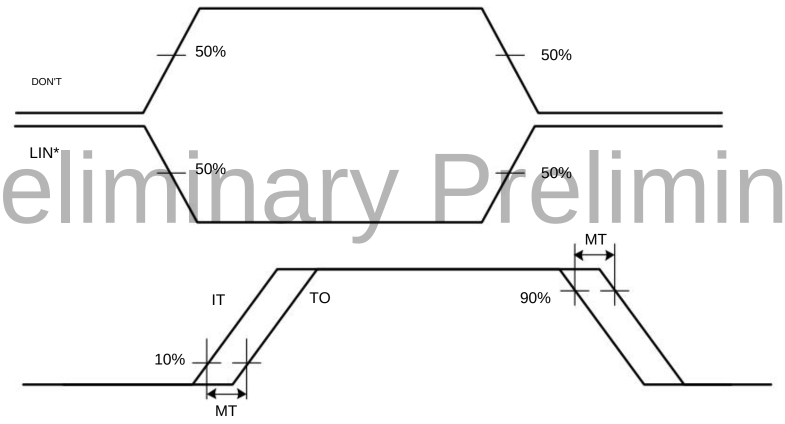
Table 6-1 Pin Description

pin number	Pin name	Pin Description
1,2,3	HIN1, HIN2, HIN3	High-side input
4,5,6	LIN1*, LIN2*, LIN3*	Low-side inputs
7	VCC	Low-side supply voltage
8	WITH	Grounding
9,10,11	LO3, LO2, LO1	Low-side output
12,15,18	VS3, VS2, VS1	High-side floating offset voltage
13,16,19	HO3, HO2, HO1	High-side output
14,17,20	VB3,VB2,VB1	High-side floating absolute voltage

7. Switching Time Test Standard



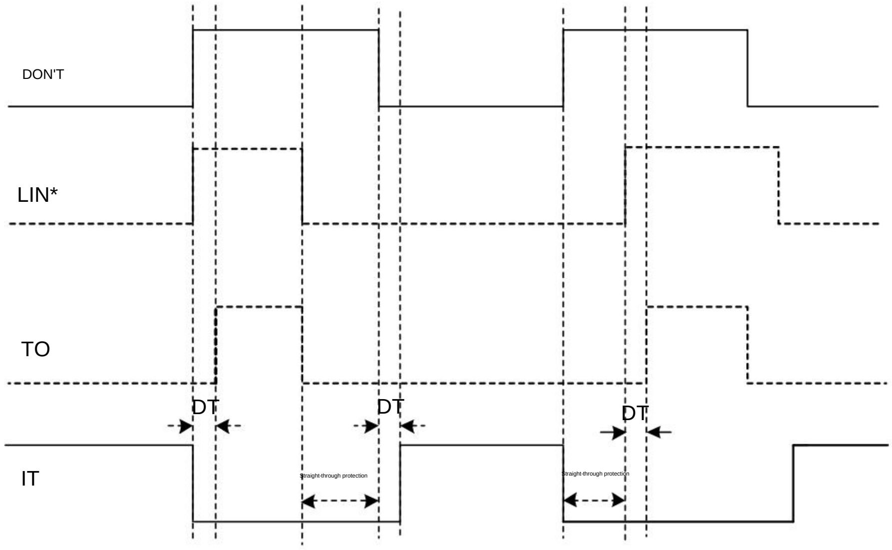
8. Transmission Time Matching Test Standard



9. Straight-through prevention function

The chip's internal design includes a dedicated protection circuit to prevent power transistor shoot-through, effectively preventing interference with high-side and low-side input signals.

Shoot-through damage to the power transistor caused by interference. The diagram below illustrates how a shoot-through prevention circuit protects the power transistor.



10. Dead Zone Function

The chip has a fixed dead-time protection circuit inside. During the dead time, both the high-side and low-side outputs are set to low level.

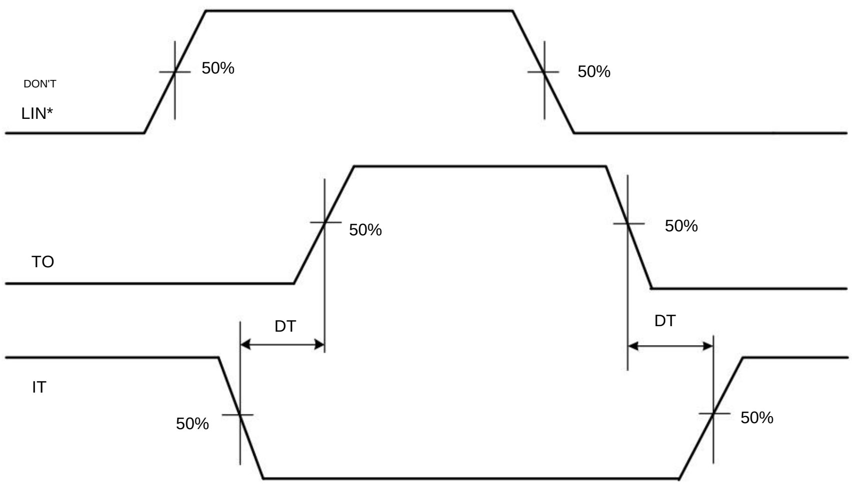
The set dead time must ensure that one power transistor is turned off before another power transistor is turned on, effectively preventing power transistor switching.

Shoot-through phenomenon. If the external dead time set for the logic input is greater than the internal dead time set for the chip, then the dead time set for the logic input will prevail.

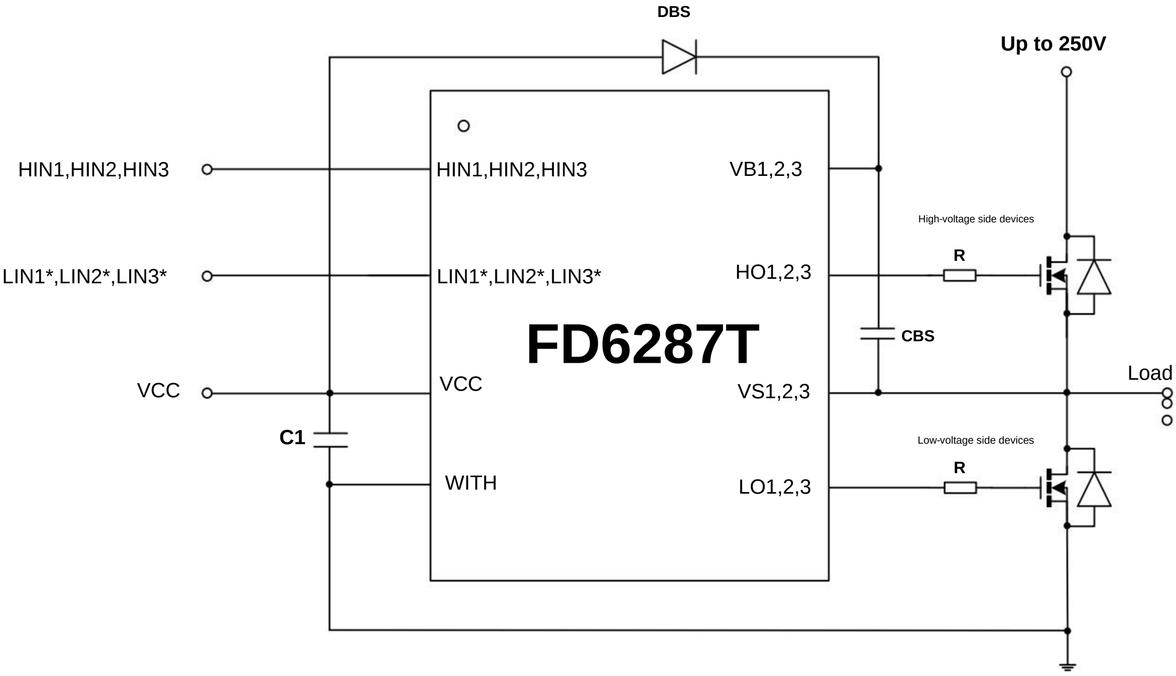
The external dead time is the chip output dead time; if the external dead time set for the logic input is less than the dead time set internally by the chip...

If the dead time is set internally, the output dead time of the chip is the same as the dead time set internally. The following diagram illustrates the dead time, input signal, and driver.

Timing relationship of the output signal.



11. Typical Application Circuits



C1: Power supply filter capacitor, which can be selected from 10ÿF to 100ÿF depending on the circuit requirements, and should be placed as close as possible to the chip pins.

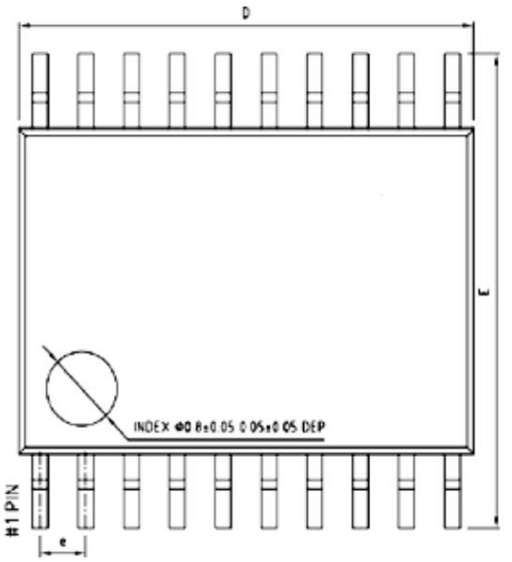
R: Gate drive resistor, the value of which depends on the driven device and the dead time.

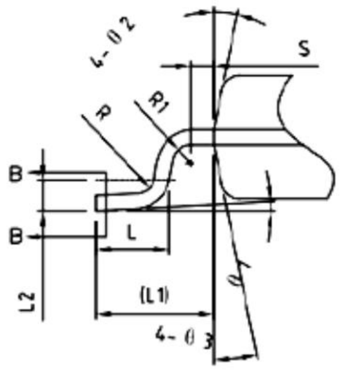
Dbs: Bootstrap diode. A Schottky diode with high reverse breakdown voltage and shortest possible recovery time should be selected.

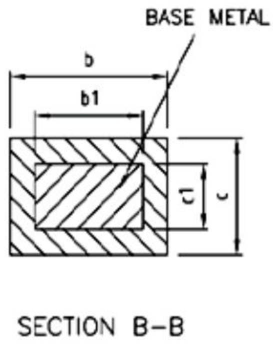
Cbs: Bootstrap capacitors, which should be ceramic or tantalum capacitors, with a range of 1uF to 50ÿF, and should be placed as close as possible to the chip pins.

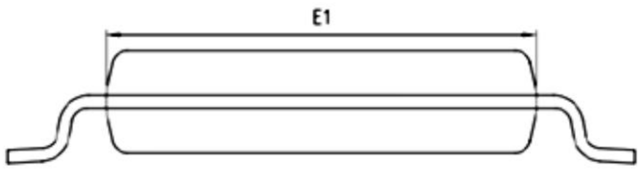
Note: The above circuits and parameters are for reference only. The parameters should be set according to the actual application circuit based on the test results.

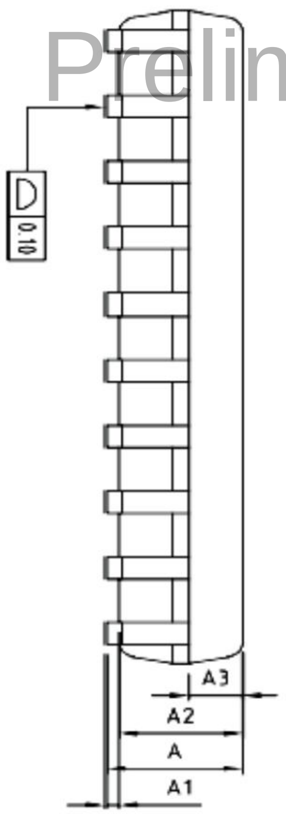
12. Package size (TSSOP-20)











	MIN(mm)	NOM(mm)	MAX(mm)
A	one	one	1.20
A1	0.05	one	0.15
A2	0.80	1.00	1.05
b	0.19	one	0.30
b1	0.19	0.22	0.25
c	0.09	one	0.20
c1	0.09	one	0.16
D	6.40	6.50	6.60
AND	6.20	6.40	6.60
E1	4.30	4.40	4.50
and	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		

Product Model	Packaging	Marking	Packaging	quantity
FD6287T	TSSOP20	FD6287T	Tape&Reel	3000

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