INTRODUCTION TO TERMINATIONS FOR HIGH SPEED BUS APPLICATIONS

Introduction

As microprocessors, memories, and other components increase in speed, the printed circuit board connections which allow these components to communicate with one another begin to behave like transmission lines. These transmission line characteristics were always present, but as edge rates increase and the transmission rates increase, the effective line lengths become longer and the transmission line effects become especially important - important to the degree that if they are not addressed, the system will not work. Reflections in the transmission line cause distortions of the signal at the receiving end of the line. These distortions can cause false triggering in clock lines, can cause erroneous data on data, address and control lines, and contribute significantly to clock and signal jitter.

The phenomenon that causes this is reflections at various points in the transmission line. For digital signals, this can be modeled as an effective rise time which is longer than the rise time of the signal that is launched by the driver. There are several very well done explanations of this. Motorola has several application notes [1,2], which treat reflections very well with clear explanations of what is happening along with graphical techniques for working out the resulting signals. The Cypress Semiconductor Applications Handbook [3,4], has a good explanation of the results especially the effective rise time.

This application note starts from these points and discusses the practical aspects of termination. In today's equipment, meeting the ideal theoretical termination is seldom practical or for other reasons not really desirable. This note will discuss practical terminations and how they are applied.

Review of Termination Basics

The fundamental characteristics of transmission lines tell us that if the transmission line is uniform and reasonably lossless, reflections are eliminated if the transmission line is terminated at the end with a pure resistance which is equal to the characteristic impedance of the transmission line. When terminated in this way, the signal arriving at the end of the transmission line is the same as the signal launched at the source end except of course for the propagation delay and losses and dispersion in the line. This and the analyses in the literature are of course validated experimentally. The need for transmission line uniformity is to make sure that the transmission line impedance is constant down the line. This eliminates reflections from nonuniformities and is the reason printed circuit board layouts daisy chain the connections from device to device.

Real printed circuit board traces (transmission lines), as implied above, usually have devices connected between the source and the receiver. In this implementation reality, the ideal transmission line conditions are violated. However in most cases this can be easily modeled. If the loads on the transmission line are uniformly distributed along the line and if the spacing between the loads is small compared to the signal wavelengths on the line, then the loads can be modeled as simply adding a capacitance to the transmission line's characteristic capacitance per unit length. This effectively lowers the transmission line impedance. (California Micro Devices, Application Note AP-200: GTL + Terminations, Milpitas, CA, 1996) The effective transmission line impedance, Zeff , of the loaded line is

$$Zeff = \frac{Zo}{\sqrt{1+\frac{C1}{dC}}}$$

Z0 is the characteristic impedance of the unloaded line, C is the capacitance per unit length of the unloaded line, C1 is the capacitance of each equally spaced load on the line, and d is the distance between the loads.

In some cases having a resistor termination is not possible. In these applications, diode terminations are used. This will be discussed more later. For the diode termination shown in Figure 1, any voltages at the end of the transmission line that rise above Vcc enough to forward bias the diode will get clamped. This clamping will minimize overshoots caused by reflections. Although with diodes there will be multiple reflections, the amplitude of these reflections is minimized and signal integrity is maintained to a successful degree.

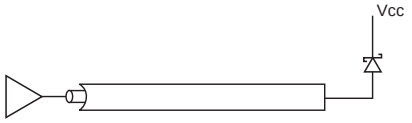

Figure 1. Diode termination

For falling edge signals, a clamp diode to ground effects a similar ideal termination. Note that for diode terminations, there is no match to the characteristic impedance of the transmission line. This characteristic makes the diode termination approach very useful in situations where the line impedance is unknown or can vary. This occurs in memory arrays where the user can add memory components which will alter the effective impedance of the transmission line.

System Timing Aspects

The system designer views termination in terms of both timing and noise budgets. Reflections and cross talk influence both budgets and the objective of the designer is to reduce additions to the budgets to the point where the system will work reliably. The timing budget is concerned with setup, hold, and propagation delays, and the timing relationship of signals with respect to clocks. Any phenomenon that shifts the arrival time of a signal affects the timing budget and must be dealt with successfully to guarantee system operation. Any time the state of the line can be different as a function of data rates or recent events, the timing of new signals will vary, resulting in what is typically referred to as jitter. Take for example a system bus terminated with a resistor to a Thévenin voltage source which is not at the correct voltage. This adds a DC shift to the arriving signal which affects the observed arrival time. Figure 2 illustrates this. Signals A and B are exactly the same shape except shifted by some DC level. With regard to the fixed reference representing a logic threshold, Signal B arrives later than Signal A. While this is a simple example, the level shift can be caused by a complex combination of reflections, termination characteristics, and crosstalk.

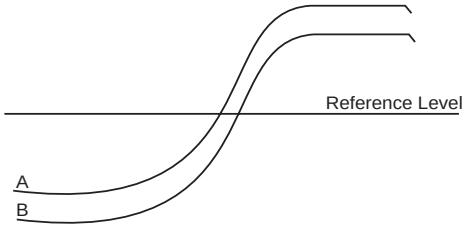

Figure 2. Apparent arrival time differences due to level shift.

Crosstalk is not part of the classic termination theory, but in practice, close spaced lines, non - ideal grounds or termination voltage connections, transmission lines crossing ground gaps, parasitic coupling and integrated circuit ground bounce contribute to components in the desired signal that reduce its integrity. If a signal possesses noise from crosstalk that pushes the signal close to the logic level threshold, a device may clock-in the wrong data. The engineer will normally establish a noise budget to insure that signal levels will not approach logic input thresholds more than some predetermined limit. This limit is determined by experience and is usually established by some authority within the company or design group.

The noise budgets are translated into crosstalk and impedance matching budgets. Generally the impedance of the board traces and the impedance of bus drivers can not be held to close tolerances. For example, board trace impedances can be held to only about plus or minus ten percent of the design center value. The reflection coefficient is then 0.05 with a design center termination resulting in five per cent contribution to the noise on the bus. Similarly, coupling between traces on the board or between termination components contributes to noise. These noise contributions move signals as shown in Figure 2 and contribute to the timing uncertainty of the system.

Practical Terminations

In practice, the pure resistive termination tends to be rare, but its use is reemerging. ECL logic typically uses 50 ohm terminations. More modern systems such as Gunning Transceiver Logic and PECL clock distribution systems use similar pure resistor terminations. In many cases, however, this is not practical. In standard CMOS logic at 5 volts or 3.3 volts, the current in the termination resistor can be large. In other applications, the transmission line impedance may not be well controlled and the designer can not fix a termination resistance value. In these cases designers must abandon the ideal termination concepts and employ compromise solutions which yield a functioning system but achieve other goals as well. In this section, practical termination alternatives will be discussed. Classic parallel, AC, diode, and series terminations will be discussed.

Parallel Terminations

There are several standards which employ direct resistive termination. GTL (Gunning Transceiver Logic, LVDS (Low Voltage Differential Signaling), and ECL and PECL in clock distribution all use this approach. As a detailed example, refer to Intel's Application Note AP-524, Pentium Pro Processor GTL+ Guidelines (Intel Order Number 242765, 1996). The bus uses pull - up terminations on both ends of the bus which terminate signals arriving from sources anywhere along the bus length. This configuration allows relatively undistorted signals to be propagated from any source to any destination along the line since reflections from the ends are eliminated. CMD's PAC RG devices are an example of a highly integrated devices specifically meant for high performance, parallel termination.

In cases where the signaling is more traditional, dual or Thévenin terminations are used. The parallel combination of resistors is matched to the transmission line impedance and the Thévenin voltage is chosen to be the desired center point of the logic swing but possibly modified by any asymmetrical driving characteristics of the signal sources. The disadvantage of this approach is the DC power that is dissipated in the termination. The two design constraints can imply low value resistors for the Thévenin circuit which pass significant amounts of power supply current direct to ground. A more efficient termination which is many times overlooked is the AC termination discussed in the next section.

AC Termination

With standard CMOS or similar logic, the signal levels swing from near ground to near the supply voltage, Vcc. These devices have limited current driving capability and practical printed circuit board traces are seldom higher than about 100 ohms. They are more in the range of 47 to 70 ohms. To terminate a transmission line with a 50 ohm parallel termination or a Thévenin termination in these environments has significant disadvantages. A constant DC current flows through the termination resistor, or a separate power supply level has to be provided. This requires the power supply to provide this current. In large systems, this may mean several watts of power that is essentially wasted, or extra cost is added to the system.

An alternative to the simple resistor termination is the AC termination. This termination is a resistor in series with a capacitor. CMD's PAC AC Series is an example of a highly integrated device specifically meant for AC termination. The resistor provides the termination function and the capacitor blocks the DC average current. As stated before, this termination can save considerable system power and is an extremely attractive termination alternative for system cost reduction. In the application of the AC termination, the resistance is made the same as the transmission line impedance. This termination is particularly useful on clock lines or constant data rate lines. It must be used more carefully on data busses, as the shifting effective DC level of the signal associated with varying data rates could potentially cause DC signal shifts and contribute to the jitter/ timing budget discussed earlier.

The capacitance value is not so easy to determine. When a high edge rate signal arrives at the AC termination, the capacitance voltage does not change instantaneously. The wave front therefore sees the resistive termination. The voltage at the termination end begins to rise as the capacitor charges. This time constant includes the sum of the AC termination resistor plus the transmission line characteristic impedance. The key to this termination is to choose the capacitor value so that the signal integrity is retained until the signal is successfully clocked in. Under the right combinations of signal timing and driver source impedance, the AC termination is very effective. Figure 3A shows a SPICE simulation of an AC terminated 50 ohm transmission line with a propagation delay of 2ns. The source has an internal impedance of 10 ohms, and 600ps rise and fall times. The AC termination uses a 50 ohm resistor and a 200 pF capacitor; a 100 pF capacitor is also satisfactory. Figure 3B shows the same simulation except with a source impedance of 50 ohms. In Figure 3B, note how the low level of the waveform walks up as the capacitor charges and retains this charge over several cycles.

As the simultations show, the simple AC termination is highly effective under the right conditions. Circuit simulations are an easy approach to verifying the choice of an AC termination in a particular system. In cases where it is not necessary to establish a bias level on the signals, the AC termination is probably a better overall choice than a Thévenin termination. It will certainly save considerable DC power.

Diode Termination

Diode clamps at the end of transmission lines minimize the effect of reflections by a clamping operation not a real termination function. This clamping function is not dependent upon any matching to the transmission line characteristic impedance. Systems with unknown or variable impedances are common. This typically occurs in SDRAM or cache memory arrays where the end product allows user upgrades. As memory devices are added or deleted, the characteristic impedance changes making termination based on a resistance impractical suggesting the diode termination as the best alternative.

A real system depends upon many factors. The complete analysis of this environment can be quite complex and is beyond the scope of this introduction. To get some idea of the operation, consider the

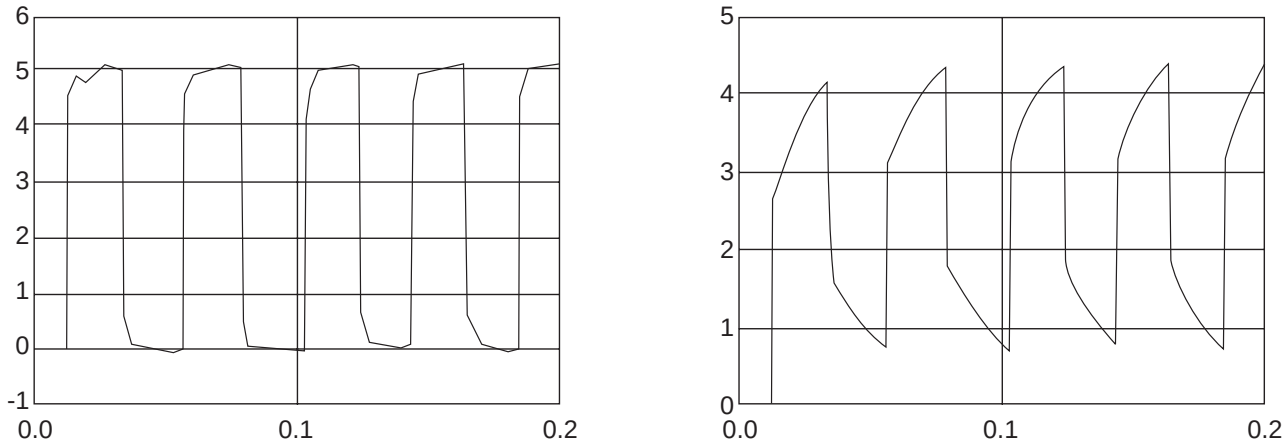

Figure 3. SPICE simulation of an AC terminated signal.

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configuration shown in Figure 4. The driver is represented with a source impedance which is lower that the characteristic impedance of the transmission but drives to the Vcc rail.

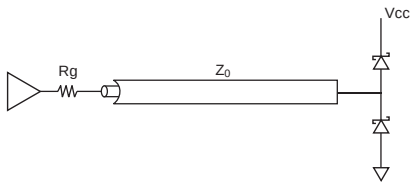

Figure 4. Schottky diode termination

Using the graphical technique described in the Motorola application notes or using SPICE simulation, one finds that the signal at the end of the transmission line is clamped to Vcc plus the forward diode drop and that multiple reflections occur which can last for several round trip delays of the transmission line. The reflections gradually subside principally due to the loss of energy through the diode to the Vcc supply and the internal resistance of the source. The existence of these repeated reflections can affect subsequent signal launches.

To measure the performance of a diode in a termination application, a simple case is set up where only one reflection is involved. This is not typical in practice since the propagation delay of the line is in general short compared to the time between signal transitions. When a signal transition occurs, multiple reflections would have taken place from the previous transition. However, it is quite possible that the diode is still in forward conduction when the new transition arrives. Rather than working with multiple reflections, the simple case sets up conditions where only one reflection is involved. This lets us easily estimate the current in the diode and voltage across in the diode since the results of multiple reflections need not be calculated. Also, the performance of the diode can be measured. Examination of the timing will provide estimates of forward turn on and reverse recovery characteristics of the diode as a termination device. A long transmission line (150 cm, propagation delay, tD) is used as shown in Figure 4. The signal is high for a long time, as shown in Figure 5, in order to let all reflections die away. Without diodes the falling edge of the signal causes a reflection on the open circuited transmission line which results in the under shoot. With no further signal transitions, the first reflection would last for the round trip delay of the transmission line as shown in Figure 5A (The first reflection actually stays there forever, and all future reflections are additive to the original signal plus the first reflection.) If the Schottky diode were present, this reflection would forward bias the diode for the entire time 2tD (and longer as a result of multiple reflec- tions).The arrival of this round trip reflection reduces the undershoot. This setup is made to insure that when a Schottky diode is placed at the end of the transmission line this first reflection will tend to keep the diode forward biased at a known current level calculated from the single reflection that is occuring.

Within a period of time shorter than the round trip delay of the transmission line, a rising edge signal arrives as shown in Figure 5B. With no diode present, the arriving rising edge signal and its reflection cause the response in Figure 5B. The response of this same set of conditions with a Schottky diode present as a terminator is shown in Figure 5C. Expectations are that 1) if the diode is slow to turn on, an undershoot transient would result taking the under-shoot below the forward turn on voltage of the diode, and 2) if the diode has a reverse recovery characteristic which holds the forward voltage, the rising edge of the signal would be delayed. Measure-ment of the zero crossing pulse width (w) with no diode and with the diode present is an indicator of this latter phenomenon.

Note that these are reasons for the choice of Schottky diodes - fast forward turn on characteristics and very low reverse recovery. At the arrival of the rising edge, the diode is still in forward conduction from the reflection of the falling edge signal. The arrival of the rising edge signal is forcing the voltage at the end of the transmission line toward 5 volts. The action is pulling the diode out of conduction. There are two important considerations here.

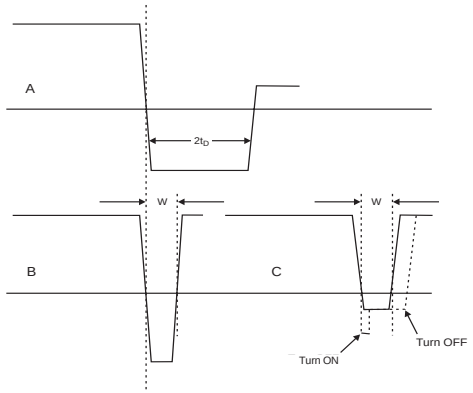

Figure 5. Dynamic response of Schottky diode termination

First, the condition where the diode is in conduction from the reflection of the first signal places a DC bias on the new signal. To reach a fixed logic threshold, the new signal has a longer way to travel as shown in Figure 2. Note the difference in the time of threshold crossing between signal B, biased down by the forward diode drop, in contrast to signal A (Figure 2) where the diode is not in conduction. This indicates that diodes of low forward voltage are highly desirable in this situation. The lower the forward drop, the earlier signal B crosses the logic threshold approaching the ideal of signal A. The low forward voltage drop of Schottky diodes makes this diode highly suited to this application.

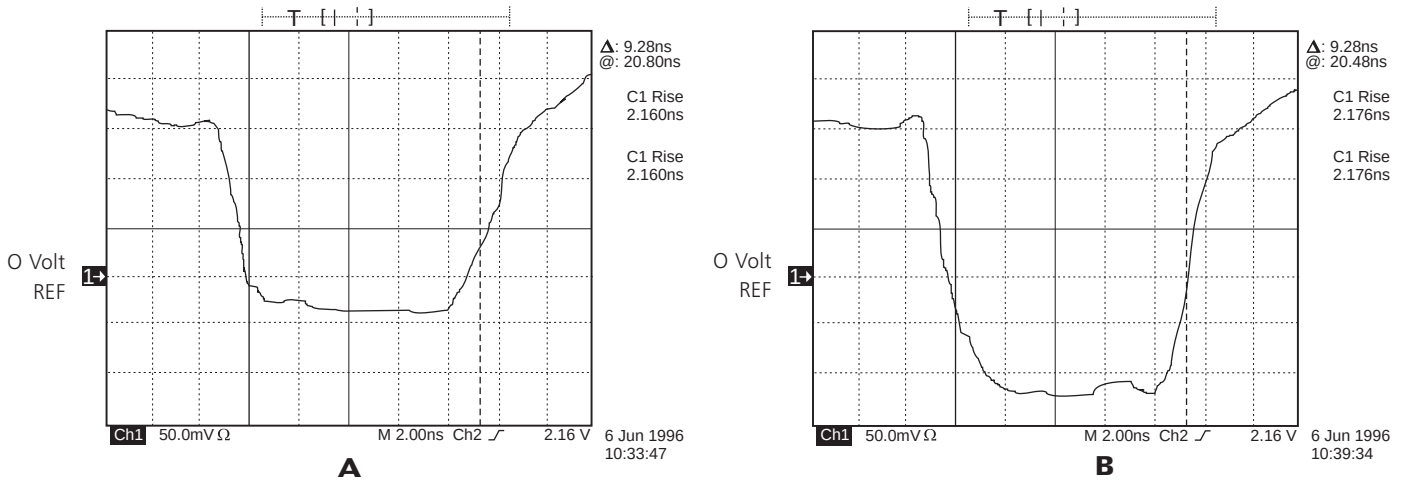

Figure 6. Schottky diode clamp leaving forward conduction.
A diode still in forward conduction, B diode not present

Second, the condition where the diode is in conduction from the reflection of the first signal requires the new signal to pull the diode out of conduction. Diodes which require time to recover from the forward bias condition can delay the movement of the voltage at the diode when a new signal arrives. Schottky diodes have excellent reverse recovery characteristics. Since conduction is based on majority carriers, there is no need to deplete the space charge region of the diode of mobile charge to stop current flow. This is illustrated in Figure 6. This Figure shows oscillograms of a short pulse at the end of a 150 cm transmission line. The timing is set according to the description associated with Figure 5 with the intent to observe the behavior in Figure 5C. Figure 6B shows the waveform with no diode present. Note the undershoot of the low going pulse due to the reflection. Figure 6A shows the waveform with CMD's PAC DN005 Schottky diode present. Note the suppression of the undershoot due to the diode clamp but without any turn - on delay. Comparing the waveforms A and B shows that they are the same width at the zero crossing level indicating that the cessation time of forward conduction is not perceptible in this experiment. If the diode exhibited a characteristic which held the diode voltage at the forward bias level until reverse recovery was completed, a delay in the occurrence of the rising edge would have been expected.

Diode terminations are used very effectively in a variety of situations including those that are fixed impedance environments. They should be included in the designer's solution set as a viable alternative. Integrated diode arrays such as CMD's PAC DN005 make excellent solutions to termination problems. The ability of these arrays to terminate up to eighteen lines in one miniature package makes diode termination practical through manufacturing efficiency and space savings.

Series (Reverse) Termination

The previous termination discussions have focused on terminations at the receiving end of a transmission line. In some cases, this is not always possible. Series terminations take advantage of the fact that there will be reflections by tailoring the first wave down the transmission line to be effectively half of the desired final signal, and relying on the reflection to not increase the signal to the desired level. By adding a suitable resistance in series with the driver, the combined impedance may be brought closer to that of the transmission line. The first wave down the line is equal to 50% of the desired signal. The reflection takes the voltage to the desired level. The resulting reflection is then properly terminated by the driving device so that no further reflections are generated. Since the termination is in series with the signal source, power dissipation is less than an equivalent parallel termination at the end of the transmission line. CMD's PRN 110 Series series is an excellent example of a high performance isolated resistor network specifically designed for series termination. With up to twelve terminations in a miniature package, the PRN 110 Series termination is practical through manufacturing efficiency and space savings.

Performance Considerations

In all of these cases, certain ideals were mentioned. One particular assumption was that termination resistors are pure resistance. Consider for a moment a high speed computer bus operating at 100 MHz or more with signal rise times at 1 ns or less. The spectral components of these signals can be significant to ten times the fundamental clock rate - 1 GHz in the case of the example. If the 100 MHz component is properly terminated and the 300 MHz component is not, then the 300 MHz component will be reflected and its reflection can destroy the signal integrity and the integrity of the bus communication. It is important therefore, that the

termination be "high performance". That is, if a resistor is selected for termination in this environment, than it must look like a resistor up to 1GHz.

Selection of components to this criterion is not a simple matter. Many components turn capacitive or inductive as the frequency increases. A key factor in selecting components for termination is the frequency response characteristics. An example of proper characterization is the PRN 110 Series. In the data sheet for this product, frequency response curves are given which exhibit the characterization results of a series termination product up to 1.8 GHz. The results show the user that this component remains purely resistive with a constant resistance value to over 800 MHz. It is important to seek components which have this type of performance to guarantee that in the application, the device will perform as expected.

Another issue is that, NPO capacitors which might be used in AC termination turn inductive above 300 Mhz, again distorting the higher frequency components and causing spurious reflections. By comparison, the high frequency capaitors used in the CMD's P/Active AC series retain their capacitive characteristics to well over 2 GHz.

Summary

As designers begin to take on the challenges brought about by high speed microprocessors, memories, and other components, they will have to become familiar with the implementation environment and the possible termination solutions available. Many solution possibilities exist and fortunately they exist as easy to use, high performance, small size, highly integrated components.

Table 1 is a guide to the application of the various termination approaches. This is simply a guide; specific design issues will require detailed analysis and possible experimentation.

References

[1] Motorola Application Note AN 1051 "Transmission Line Effects in PCB Applications" 1990
[2] Motorola Application Note AN 1061 "Reflecting on Transmission Line Effects" 1990
[3] Cypress Application Note "System Design Considerations When Using Cypress CMOS Circuits" March 11, 1993
[4] Cypress Application Note "Layout and Termination Techniques for Cypress Clock Generators" July 24,1997

Bus Environment	Termination Type(s)
Variable Impedance: user expandable such as SDRAM arrays, cache systems, peripheral busses	Schottky diode, Series termination, or combination of these two
Fixed impedance, low signal swing (1 volt), high speed microprocessor busses:GTL, ECL, etc.	Parallel termination, Series termination, or combination of these two
Fixed impedance, standard signal swing, medium to high speed microprocessor busses	Thévenin termination, Schottky diode
Fixed impedance, large memory arrays (cache), no combined pull up/down function required, medium and high speed systems/microprocessor busses	AC termination (not recommended in combination with series termination)
Clock distribution: PECL, ECL	Parallel termination, AC termination

Table 1. Selection Guide for Termination Alternatives