Termination Techniques for High Speed Busses

Introduction

As bus speeds continue to increase, serious consideration is being given to the issues of signal propagation and quality. Issues previously restricted to the analog world, such as transmission line effects, are now affecting whether or not a design will work at these high edge rates and/or signal transmission rates. PCB traces behave like transmission lines and reflections occur at all points on the PCB trace where there is an impedance mismatch. In a typical digital system, the output impedance of the driver is less than the characteristic impedance of the PCB trace, which is less than the input impedance of the receiver. Reflections translate into more observable effects such as ringing and stair-stepping. These distortions can cause false triggering in clock lines or erroneous bits on data, address, or control lines; and can contribute significantly to clock and signal jitter. Distortions also increase the total emissions from the PCB. Proper termination of these lines effectively reduces termination line effects in high speed digital systems.

Commonly practiced passive termination techniques include parallel, Thévenin, serial, and AC termination. Schottky diode termination also has merit, although it is not a conventional passive termination technique. This document discusses the relative merits and demerits of these techniques, and provides design solutions for each. Two reference guides complete this application note. The first, Selection Guide for Termination Techniques, provides specific recommendations for various application scenarios. The second, Standards which Require Terminations, identifies various standards specifications and provides recommended termination techniques for each.

Parallel Termination

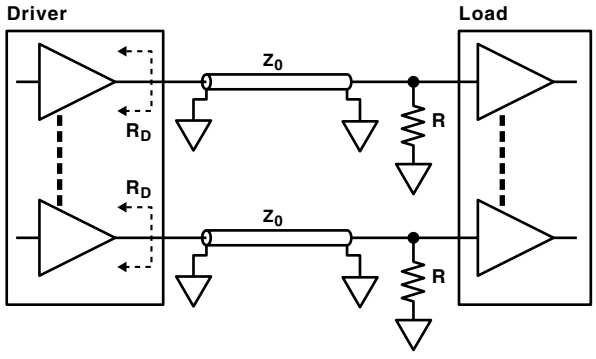


Figure 1. Parallel Termination

Parallel termination is the simplest termination technique, with a resistor connected between the open (load) end of the transmission line and the ground or V_{CC}, as shown in Figure 1. The value of the resistor (R) must match the characteristic impedance (Z_0) of the line in order to eliminate reflection. The energy causing the reflection will now be absorbed in the termination resistor. Typically in digital logic designs, the sinking current is greater than the sourcing current. Terminating to V_{CC} helps the sourcing and terminating to ground helps the sinking capability of the driver. Therefore, terminating to V_{CC} helps with logic families that are weak in pulling up. (See Thévenin Termination.)

Design Equation

$$R = Z_0$$

Note: This is the classic textbook case where no reflections occur when a transmission line is terminated at the end opposite the signal source in its characteristic impedance. For the purposes of this paper, Z_0 refers to the actual time impedance. This impedance can be lowered from the board design center value by the addition of devices or vias placed along the line. The capacitance of these devices adds to the distributed capacitance of the line. If the capacitances are equal and uniformly spaced along the line, the line impedance is abducted according to the formula [14].

$$Z_0' = \frac{Z_0}{\sqrt{1 + C_D/C_0}}$$

Where, C_0 is the intrinsic capacitance per unit length of the trace and C_D is the distributed capacitance of the receiving devices (i.e., total load capacitance per unit trace length). Typically, sockets add 2pF and vias add 0.3 - 0.8pF to C_D. Hence, the effect of distributed capacitive load on a line is its reduced characteristic impedance.

This correction factor for Z_0 applies to all termination schemes depending on the overall system architecture.

Advantages

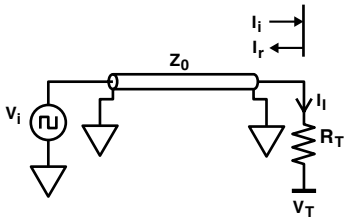
1. Parallel termination offers a simple design solu tion. It is the easiest termination scheme to apply.
2. In most cases, this method requires only one additional component. Two resistors may be required if both ends of the line need to be terminated.

Disadvantages

1. Parallel termination dissipates DC power in the termination resistor (typically of low value between 50-150W).

Lemma

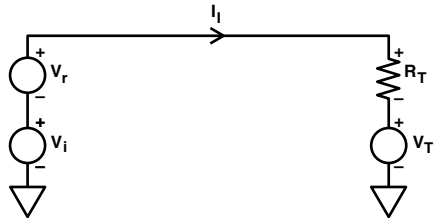
There will exist no reflection on a transmission line provided that the termination resistor connected at the end of the line to an arbitrary termination voltage matches the characteristic impedance of the line, Z_0.



Parallel Termination

Proof

The above circuit can be represented by a Thévenin equivalent circuit as follows:



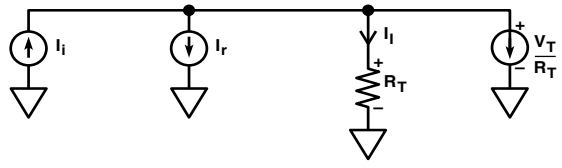
Thévenin Model for Parallel Termination

where, V_i, I_i = Incident voltage and current
V_r, I_r = Reflected voltage and current
V_T = Termination voltage
R_T = Termination resistor
I_l = Current through R_T

From the Thévenin equivalent circuit,

$$V_i + V_r = V_T + I_l R_T \quad (1)$$

The Norton equivalent circuit and the deduced current equation are given as follows:



Norton Model for Parallel Termination

and

$$I_i - I_r - V_T/R_T = I_l \quad (2)$$

$$\frac{V_i}{Z_0} - \frac{V_r}{Z_0} - \frac{V_T}{R_T} = I_l$$

$$V_i - V_r = \frac{Z_0}{R_T} \times V_T + I_l Z_0 \quad (3)$$

adding (1) + (3),

$$2V_i = \left(1 + \frac{Z_0}{R_T}\right) \times V_T + (R_T + Z_0) \times I_l$$

$$I_l = \frac{2V_i - (1 + Z_0/R_T) \times V_T}{R_T + Z_0}$$

$$I_l = \frac{2V_i}{R_T + Z_0} - \frac{V_T}{R_T} \quad (4)$$

subtracting (1) - (3),

$$2V_r = \left(1 + \frac{Z_0}{R_T}\right) \times V_T + (R_T + Z_0) \times I_l \quad (5)$$

substituting (4) in (5),

$$2V_r = \left(1 + \frac{Z_0}{R_T}\right) \times V_T + (R_T + Z_0) \times \left(\frac{2V_i}{R + Z_0} - \frac{V_T}{R_T}\right)$$

$$V_T = \left(\frac{R_T - Z_0}{R_T + Z_0}\right) \times V_i \quad (6)$$

It can be seen from equation (6) that the magnitude of the reflected voltage is independent of the termination voltage.

In addition, if $R_T = Z_0$ (perfectly matched), then $V_r = 0$. Hence, the proof.

2. This method requires constant DC current from the driver at either high or low logic, which adds to the DC load of the driver.
3. Degradation of the high output level of the signal can occur. For example: In a TTL logic design, when the output is terminated to ground, the V_{CH} is lower, and the noise immunity at the receiver input is reduced.
4. With a capacitance load at the end of the line, the slew rate of the arriving edge changes with the termination. When unterminated, the voltage rises to twice the amplitude of the launched signal with time constant Z_0C. This rises more rapidly than when the parallel termination is added.

Applications

The parallel termination has been used with ECL devices and is used with all Pentium and Pentium II processors; these use GTL+ bus styles which have variants GLT and NTL. PECL clock distribution systems also use parallel terminations, some of which take the

form of a T network when differential signaling is used. Most high speed serial communication protocols specify parallel termination.

Caveats

1. As much as 0.25 to 0.5W of power are dissipated, which cannot be accommodated by a CMOS system that consumes only a few milliwatts of power [10].
2. Line impedance of less than 100W when terminated with this scheme will require a DC output current of 24mA for TTL levels ($V_{OH(min)}$=2.4V). For this reason, parallel termination is not advocated for a battery driven system.
3. Power dissipation is dependent on the duty cycle. Connecting the resistor to ground will give the lowest power dissipation for low duty cycles, and terminating to V_{CC} will give the lowest power dissipation for high duty cycles [10].
4. Having a strong pull-down resistor might cause the falling edge to be faster than the rising edge, resulting in the distortion of the duty cycle of the signal [2].

CAMD's Solution

The PACRG family is a highly integrated bus termination network that provides 22 terminations per package. It has low crosstalk voltage of 65mV and meets all of Intel's specifications for Pentium and Pentium II applications. The PACR4G features 1% resistance and 30mV crosstalk for the most critical systems.

Thévenin Termination

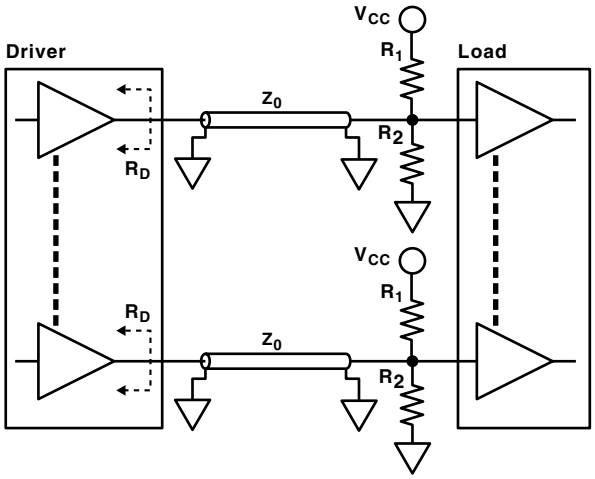
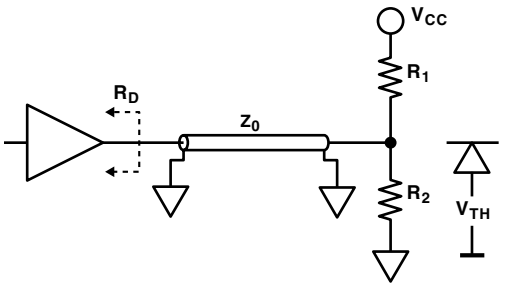


Figure 2. Thévenin Termination

Design Rules for Thévenin Termination

The parallel combination of Thévenin resistors R_1 and R_2 matches the characteristic impedance, Z_0 of the transmission line. The values for R_1 and R_2 are based on the unsymmetric characteristic of the driver during high and low levels of the logic.



Thévenin Termination

given that,

$$Z_0 = \frac{R_1 R_2}{R_1 + R_2} \quad (1)$$

Applying voltage division between R1 and R2 from the above circuit,

$$\frac{V_{TH}}{V_{CC}} = \frac{R_2}{R_1 + R_2} \quad (2)$$

from (1) (2),

$$\frac{V_{TH}}{V_{CC}} = \frac{Z_0}{R_1}$$

$$R_1 = \frac{Z_0 \times V_{CC}}{V_{TH}} \quad (3)$$

from (1),

$$R_2 = \frac{Z_0 \times R_1}{R_1 - Z_0}$$

substituting (3) in the above equation,

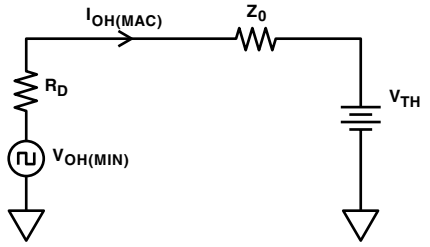
$$R_2 = Z_0 \times \frac{Z_0 \times V_{CC}/V_{TH}}{Z_0 \times V_{CC}/V_{TH} - Z_0}$$

$$R_2 = Z_0 \times \frac{V_{CC}}{V_{CC} - V_{TH}} \quad (4)$$

Equations (3) and (4) give the values of R_1 and R_2. V_{TH} is an unknown in these equations and can be calculated from the driver specifications.

Determining the Thévenin Voltage

The Thévenin termination can be transformed, using Thévenin's theorem, into a single resistor and voltage source. By replacing the driver with its equivalent circuit and eliminating the transmission line for steady state conditions, the following circuit is obtained:



Thévenin Model for Single-Ended Parallel Termination

Where, $I_{OH(MAX)}$ is also the sourcing current

Now,

$$I_{OH(MAX)} = \frac{V_{OH(MAX)} - V_{TH}}{R_D - Z_0}$$

$$V_{TH} = V_{OH(MIN)} - I_{OH(MAX)} (R_D - Z_0) \quad (5)$$

$V_{OH(min)}$ and $I_{OH(max)}$ can be obtained from the data sheet of the driver. It can be inferred that during logic high, the Thévenin resistor R_1 performs pull-up action by supplying current to the load. This current, added with the driver's sourcing current, will be just enough to maintain the voltage at the output of the driver at the minimum threshold logic voltage, $V_{OH(min)}$. A V_{TH} designed this way minimizes power dissipation in R_1 and R_2.

During logic low, R_2 sinks any excess current ($> I_{sink(max)}$ or $I_{OL(max)}$) from the load to the ground.

Since sourcing is a bigger problem than sinking, V_{TH} is designed based on logic high. Hence, R_2 may not be an optimum value for sinking or pull-down action. Nevertheless, R_2 calculated based on the above design equations helps the driver in sinking during logic low.

For digital devices, it is best to center the V_{TH} at a known logic level to avoid holding the input of the receiver at threshold. However, if the driver output is in TRISTATE™ condition, the input will either pull up or pull down, depending on its position relative to V_{TH}, rather than causing oscillations near the threshold and logic uncertainties.

Thévenin or dual termination uses two resistors (R_1 and R_2) as shown in Figure 2. The parallel combination of resistors is matched to the Z_0 of the line. The Thévenin voltage, V_{TH}, is chosen to keep the driver I_{OH} and I_{OL} currents within the specifications of the driver. The resistor R_1 helps the driver pull-up to logic high state easily by sourcing some current to the load, and, similarly, R_2 helps the driver to pull-down to logic low state by sinking some current to the ground. Properly chosen values for R_1 and R_2 enhance the driver's fan-out and smoothes out the power dissipation variations caused by the change in duty cycles.

Design Equations

From the Design Rules for Thévenin Termination,

$$V_{TH} = V_{OH(MIN)} - I_{OH(MAX)} (R_D - Z_0)$$

$$R_1 = \frac{Z_0 V_{CC}}{V_T}$$

$$R_2 = \frac{Z_0 V_{CC}}{V_{CC} - V_{TH}}$$

where, $I_{OH(max)}$ = Maximum output current from the driver when its output voltage is minimum for high level logic, $V_{OH(min)}$

R_D = Output impedance of the driver

V_{CC} = Supply voltage

Advantages

1. The termination resistors also serve as pull-up and pull-down resistors and thereby improve the noise margin of the system.
2. The burden on the driver is reduced by supplying additional current to the load. This is especially helpful in a large voltage swing system like 5V and 3.3V CMOS or BiCMOS based systems.
3. This termination method provides good overshoot suppression.

Disadvantages

1. There is a constant flow of DC current from V_{CC} to ground, irrespective of the logic state, which results in static power dissipation in the termination resistors.
2. This method requires ratio resistors and ground connections.
3. A line voltage (Thévenin voltage on a TRISTATE™ bus) close to the switching thresh old voltage causes greater levels of power dissi pation within CMOS devices. This is because both NMOS and PMOS transistors are conduct ing, resulting in a current path between V_{CC} and ground.

4. Thévenin termination reduces the slew rate of the signal with a capacitive load when compared to an unterminated line. The load capacitance and the resistance (parallel combination of Z_0, R_1 and R_2) add to the RC time constant of the signal, which rises up to the driver's output voltage.

Applications

1. TTL circuits, especially advanced Schottky families such as FAST, often use Thévenin termination [12].
2. Thévenin termination can be used to provide proper ECL termination from the -5.2V supply and for TTL from a 5V supply.

Caveats

CMOS devices switch at 50% threshold. An equal value for resistors R_1 and R_2 results in a line voltage of half the V_{CC} when the line is not driven by a logic device. This causes greater levels of power dissipation within the receiver. In combination with the power dissipation in the termination resistors, the total may be unacceptably high for CMOS logic devices [10].

CAMD's Solution

The PACDT provides matched resistor pairs whose parallel combination matches the specified value to 1% over temperature. (This can be difficult with discrete components.) Using the same technology as the PACRG, the PACDT exhibits excellent impedance match for high performance busses and has very low crosstalk. It is a highly integrated network which provides 18 terminations in a single package.

Series Termination

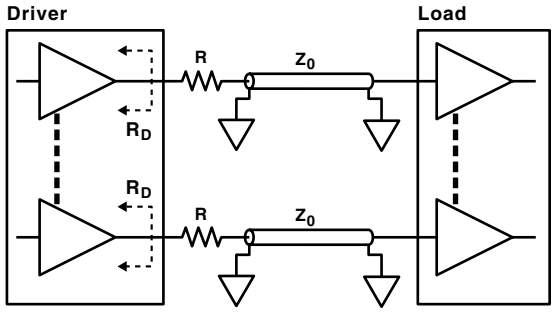


Figure 3. Series Termination

Series termination, or back matching, is a unique source end termination unlike other types. A series termination consists of a resistor connected between the driver output and the line, as shown in Figure 3. The sum of the output impedance of the driver (R_D) and the resistor value (R) must be equal to Z_0. Now, only half the signal value is launched on the line due to the voltage division between the line and combination of the series resistor and the driver impedance. However, at the receiving end, the mismatch between the line impedance and the input impedance of the receiver (typically, very high) will cause a reflection of approximately the same voltage magnitude as the incident signal. The receiving device will immediately see the full voltage (sum of incident and reflected voltages) and the added signal propagates to the driving end. There will be no further reflections as the reflected wave gets terminated at the driving end by the series termination resistor.

Design Equation

$$R = Z_0 - R_D$$

Advantages

1. Series termination adds only one resistor per driver to the system.
2. This method requires the lowest power consumption in the termination resistor when compared to all other resistive types of termination.
3. Series termination adds no DC load.
4. No extra impedance from signal line to ground is introduced by this approach.

Disadvantages

1. Tuning the value of the series resistance after the first reflection to make the received signal amplitude fall within the switching thresh old (noise budget) is difficult. It is further aggra vated by the fact that most drivers are nonlinear; i.e., the output impedance varies with the logic state of the device. Hence, selecting a crisp value for the series resistance for application of the design equation is difficult.
2. The driving end of the transmission line does not see the full reinforced signal amplitude for as long as twice the propagation delay of the line. In a multi-drop situation, the diminished signal ampli tude during this brief period of time reduces some of the receiver's noise immunity.
3. The data setup time for digital signals of the receiver (part of the timing budget) must accommodate the propagation delay mentioned above.
4. Compared to parallel termination, this method reduces the slew rate of the signal with a capacitive load. The load capacitance and the Z_0 of the line add to the RC time constant of the signal, which rises up to half the driver's output voltage.

Applications

Series termination is an easy to apply, low cost approach for medium to low performance environments. The disadvantages listed above tend to make series termination unsuitable for high performance busses. (Although some sophisticated users employ series-parallel termination combinations.) Common applications are in memory arrays and in peripheral busses which use 3.3 or 5V to give logic swings. series termination is commonly used with CMOS devices which do not possess high drive capability. The combined load of the transmission line and the series resistor is something which is in the range that can be successfully driven. When CMOS is mixed with strong drivers, like ABT devices, series termination makes most sense.

CAMD's Solution

The new PACRPI has 11 isolated resistors acting as 11 terminating lines per package, with tight 1% tolerant resistors and very low crosstalk voltage.

AC Termination

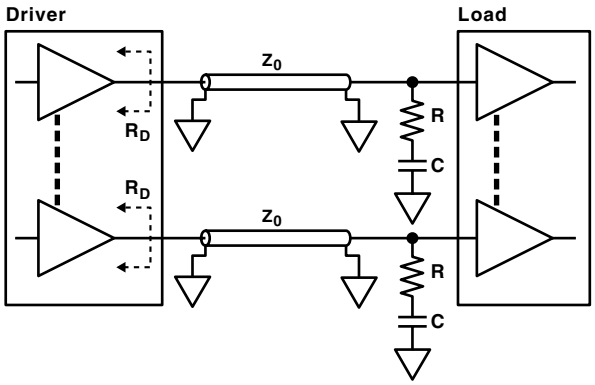


Figure 4. AC Termination

AC termination, also referred to as RC termination, consists of a resistor (R) and a capacitor (C) connected to the load end of the transmission line, as shown in Figure 4. The value of the resistor must match the Z_0 of the line in order to eliminate reflection. Choosing the capacitor's value precisely is crucial. A small capacitor value contributes to a smaller RC time constant and the resulting RC circuit will act as an edge generator, causing overshoot and undershoot. On the other hand, a large capacitor value increases power consumption. As a general rule, the RC time constant must be greater than twice the loaded propagation delay of the line (refer to the design equations given below) [14]. Power dissipation in the termination components is a function of frequency, duty cycle and bit pattern of the previous data. These factors affect the charging and the discharging of the termination capacitor and hence affect power dissipation.

Design Equations

From "The Dynamics of AC Termination" [9],

$$R = Z_0$$

$$C = t_D = \left/ \left(Z_0 \times \ln \left[\frac{Z_0}{Z_0 + R_D} \right] \right) = t_D \right/ \left(Z_0 \times \ln \left[\frac{1 - G}{-2G} \right] \right)$$

$$\tau = RC > 2 \times t_D \times \sqrt{1 + C_D}/C_D$$

where, t_D = Propagation delay of the line

G = Reflection coefficient of the source

C_D = Distributed capacitance of the receiving devices

Advantages

1. The termination capacitor blocks DC, and thus, saves considerable power.
2. If the capacitor's value is designed appropriately, the waveform at the load end will be a near ideal square wave with minimal overshoot or undershoot.

Disadvantages

1. Depending on the previous data pattern, data on the line may exhibit time jitter. For example, this will happen if a long string of like bits causes the line and capacitor to charge to the maximum level of the driver's output voltage. Then a subsequent data bit of the opposite polarity takes longer than normal to cross the receiver threshold because it starts from a greater potential than normal. The timing budget must account for this in order to guarantee system operation [12].
2. Since the AC termination performance is dependent upon the termination line length, the AC Termination may not do well in environments where multiple sources are distributed along the transmission line.

Applications

The AC termination can be used in place of a parallel or Thévenin termination where the termination resistor is not used as a pull-up (i.e., not in GTL, GTL+, or NTL systems). The principal use of the AC termination is to save power, consequently its use is usually indicated where power savings is an overriding concern.

Caveats:

1. Obviously AC termination can not be used where a DC path through the termination is necessary. Some serial communication circuits

employ current mode drivers (but usually use a driver end termination in addition to use at the receive end).

2. AC terminations are less effective in multi-source environments. Simulation should be used to assure suitability.

CAMD's Solution

The PACAC, available in a standard QSOP package, has 18 terminating lines per package. The resistor-capacitor network is highly stable and has excellent high frequency performance. The capacitor also has a 2kV ESD protection across it.

Schottky Diode Termination

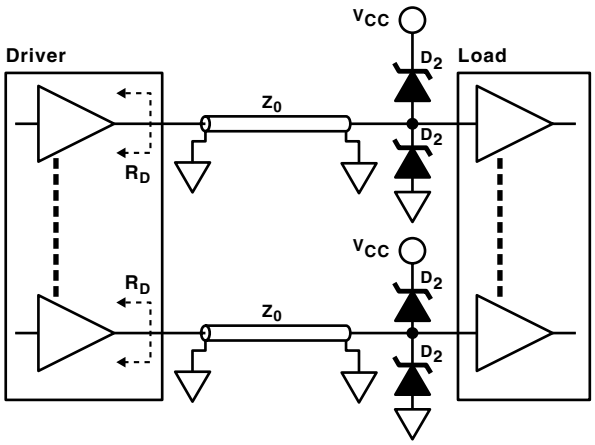


Figure 5. Schottky Diode Termination

Shottky diode transmission, or simply diode termination, consists of two Schottky diodes and their connections, as shown in Figure 5. Any reflection at the end of the transmission line, causing the voltage at the input of the receiver to rise above V_{CC} plus the threshold voltage of the diode (also referred to as the forward bias voltage), will forward bias the diode connected to V_{CC}. The diode turns on and clamps the overshoot to V_{CC} plus threshold voltage. Similarly, the diode connected to the ground limits undershoot to its threshold voltage. However, since energy is not absorbed by the diodes, but is merely diverted to either the power plane or the ground plane, there will be multiple reflections on the line. The reflections gradually subside, due principally to the loss of energy via the diodes to V_{CC} or ground and the resistive losses of the line. The amplitude of these reflections is sufficiently limited that signal integrity is maintained.

Design Considerations

Since there is no impedance matching in the use of Schottky diodes, there are no design equations per se. Key to successful use of this approach is the selection of a diode with the optimum characteristics.

The diode characteristics [8] are denoted as follows:

1. Forward turn-on time, t_{ON}
2. Forward bias voltage, V_F
3. Reverse recovery time, t_{rr} and the rise time of the signal is denoted by t_r.

Effect of Diode Characteristics on Signal Integrity

Diode Characteristics	Effect
Increased t_{ON}	Increased under /overshoot
Increased V_F	larger reflections
Increased t_{rr}	Increasing t_r

As can be seen from this table, signal integrity can be restored by using a diode that has a smaller t_{ON}, V_F and t_{rr}. A Schottky diode possesses these characteristics.

Advantages

1. Unlike classical termination schemes, there is no matching involved in Schottky diode termination. Hence, a line of unknown Z_0 can be terminated using this technique.
2. The load (mostly capacitive) connected to the transmission line effectively reduces Z_0. Schottky diode termination is not affected by the variations in Z_0.
3. Power dissipated in the dynamic-ON resistance of the Schottky diode is extremely small when compared to that of any resistive termination technique.
4. Effects of reflections like overshoot, undershoot, and time jitter are mitigated by good diode characteristics.
5. Schottky diodes can be placed at any point along the line at which reflections may originate.

Disadvantages

1. Diode response at the switching frequency needs to be verified as the existence of multiple reflections can affect subsequent signal launches.
2. The Schottky diode's effectiveness decreases as signaling levels decrease. This is due to the

Selection Guide for Termination Techniques		
No. Scenarios	**Recommended Termination**	**Reason**
1. MECL drivers driving 3 or more lines in the backplane	Series (100Ω)-parallel (600W to –2V) termination (PACRPI)/(PACRG, PACR4G)	Pull-down resistor compensates for the drive current and series termination address parallel fan-out [19].
2. Circuits containing a mixture of bipolar and advanced CMOS devices that are weak drivers	Parallel termination (PACRG, PACR4G)	Reduces overall system power consumption if terminated to ground for low duty cycle and to V_{CC} for high duty cycle [10].
3. Circuits containing a mixture of bipolar and advanced CMOS devices that are weak drivers	Thévenin termination (PACDT)	Provides drive support. Thévenin resitors provide current which helps the driver connected to a long line.
4. CMOS-to-COMOS connections	Series termination (PACRPI)	Adds no extra impedance from signal line to ground [10].
5. FAST (advanced CMOS) devices used for low power applications	Series termination (PACRPI)	Adds no extra impedance of the driver. Hence, driver dissipates less amount of power [10].
6. FAST (advanced Schottky-TTL) devices	Thévenin termination (330Ω pair)	FAST devices have limited current drive capability [12].
7. Switching in/out memory arrays (SDRAM or cache) connected to the backplane	Schottky diode termination/ series termination (10-50Ω) (PACDT)/(PACDN005, DN010)/ (PACRPI)	Memory plug-ins can be perceived as added distributed capacitance on the line which effectively lowers Z_0. There is no impedance matching required with Schottky diode termination [8].
8. Driving a backplane with tri-statable devices	Schottky diode termination (PACDN005, PACDN010)	Shottky diode termination can handle large impedance variations [19].
9. Extensible bus applications (e.g., Scenario 7)	Series termination (PACRPI)	Turning the value of the series resistance limits overshoot and undershoot to predetermined values, typically, 35% and 12% respectively [17].
10. Battery driven systems	Series/AC/Schottky diode termination (PACRPI)/(PACAC)/ (PACDN005, DN010)	Low DC power consumption compared to parallel or Thévenin termination; enhances battery life [10].
11. Drivers with limited current capability driving heavily loaded data lines	Thévenin termination (PACDT)	Sourcing and sinking capabilities of Thévenin termination helps the driver to sustain a crisp logic state at every receiver end.
12. Current source drivers with high output resistance compared to the Z_0 of the line	Parallel termination (PACRG, PACR4G)	Creates matched source [15].

Chart 1.

inherent forward voltage diode drop. Schottky diodes are effective for 3.3V and 5V logic families.

Applications

Shottky diode termination offers an excellent solution for multi-drop situations in which some of the receivers on the line are also capable of driving the line. Application of transmission line theory to provide a conventional termination solution in such situations can become highly complicated. It has been proved through simulations that terminating at multiple points (preferably at points of discontinuity and stubs) yields improved signal integrity uniformly over the entire length of the bus.

Caveats

It is very important to choose a Schottky diode with good

Selection Guide for Termination Techniques		
No. Scenarios	**Recommended Termination**	**Reason**
1. Gunning Transceiver Logic (GTL)	Parallel termination (50Ω to V_{TT} = 1.2V) (PACRG, PACR4G)	GTL (JEDEC) bus uses pull-up termination on both ends of the bus which terminate signals arriving from sources anywhere along the length of the bus [4].
2. GTL + used for boards with Pentium Pro processor.	Parallel termination (PACRG, PACR4G)	Very similar to GTL [11].
3. Backplane Transceiver Logic (BTL)	Thévenin termination (PACDT)	Provides drive support. Thévenin resistors provide current which helps the driver connected to a long line.
4. Futurebus = backplane	Series termination (PACRPI)	Adds no extra impedance from signal line to ground [10].
5. High Speed Transceiver Logic (HSTL)	Series termination (PACRPI)	Adds no extra impedance of the driver. Hence, driver dissipates less amount of power [10].
6. Stub Series Terminated Logic (SSTL)	Thévenin termination (330Ω pair)	FAST devices have limited current drive capability [12].
7. Low Voltage Differential Signaling (LVDS) (e.g., portable computer applications)	Schottky diode termination/ series termination (10-50Ω) (PACDT)/(PACDN005, DN010)/ (PACRPI)	Memory plug-ins can be perceived as added distributed capacitance on the line which effectively lowers Z_0. There is no impedance matching required with Schottky diode termination [8].
8. Universal Serial Bus (USB) (e.g., portable computer applications)	Schottky diode termination (PACDN005, PACDN010)	Shottky diode termination can handle large impedance variations [19].
9. Single-ended Small Computer System Interface (SCSI-I)	Thévenin Termination (R1 = 220Ω and 150Ω between)	Turning the value of the series resistance limits overshoot and undershoot to predetermined values, typically, 35% and 12% respectively [17].
10. Differential SCSI-I	Parallel termination (330Ω to V_T, 150Ω between D+ and D-, and 330Ω to GND. (PACRG, PACR4G)	Low DC power consumption, compared to parallel or Thévenin termination; enhances battery life [10].
11. IEEE 1284 compliant parallel ports in computers, connected to peripherals like printers	Series termination (PACRPI)	Sourcing and sinking capabilities of Thévenin termination helps the driver to sustain a crisp logic state at every receiver end.
12. IEEE-488 bus	Thévenin termination (PACDT)	Creates matched source [15].

Chart 2.

characteristics, especially one designed for termination applications. Most Schottky diodes of this type have no measurable turn-on delay. Forward voltages can vary from about 650mV to over 1 volt. Units intended for high performance applications where dampening reflection quickly is critical should use low V_T diodes. Reverse recovery of the diode will tend to delay signal edge arrival times since the diode, if in forward induction when a new edge arrives, will hold the existing level for its t_{rr}. One needs to include this in the timing budget. Well designed networks will minimize parasitics; 600 pS is achievable.

Any diode must be mounted with low inductance paths to V_{CC} and ground. Parasitic inductance in these paths will diminish the effectiveness of the diode in clamping over/ undershoots.

CAMD's Solution

The PACDN005 offers 18 channel typical termination. The Schottky diode has a low V_F of 0.65V typical and t_{rr} of 600pS. The device itself provides ESD protection and has been tested successfully for 4kV.

Selecting an Appropriate Termination Technique

Several types of termination techniques have been described here as they pertain to high speed digital system design. But, it is not always obvious which technique is the preferred solution to a specific design problem, digital environment, or application. Chart 1 is intended to assist your selection of an optimal solution. Chart 2 summarizes common digital standards and interfaces and recommended termination solutions.

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