Electro-static Discharge Protection of High Performance Integrated Circuits

Introduction to Electrostatic Discharge

We live in an electrified world. Each of us is familiar with the conveniences offered by electrical and electromechanical devices. It is in harnessing the natural properties of electrical particles that such remarkable technologies have changed our lives. But electrical phenomena, improperly controlled, can be the bane of those very same technologies. Integrated circuit and system designers face just such a challenge from the uncontrolled release of electrical charge into their designs. The most familiar example of these discharges is the electrical shock that results from scuffing one's feet on a carpet. This discharge, if the design isn't robust, can result in damage that ultimately causes system failure. While this class of reliability issue has existed for quite some time, the increased sensitivity of ever-shrinking integrated devices, the increased portability of electronic devices, and the multiplication of external interfaces place increasing burdens upon the designer to deal proactively with these serious concerns. Problems of this sort are considered together under a single heading: *Electrostatic Discharge (ESD)*. This article will explore the subject in its many aspects.

The Physical Basis of ESD

Under various conditions, frictional contact between two objects can result in the transport of charged particles from one object to the other. The classic example is the charge that builds up when a glass rod is rubbed with fur. As carriers of charge are transferred from one material to another, the electrostatic potential of one device is increased as that of the other is decreased. Because electrical charge is a conserved property in nature, the total charge of the two materials remains constant through this process. In other words, an increase of charge on the one object by a quantity $+Q$ (measured in Coulombs) results in an equal decrease of $-Q$ on the complementary object. For simplicity's sake, let us consider these two materials to be parallel conductive plates with a capacitance, C, between them. Then the difference in electrostatic potential is given by:

$$V = \Phi_1 - \Phi_2 = Q/C = Qd/\varepsilon A$$

where d is the distance between the plates, A is the area of the plates, and epsilon is the electrical permittivity of the intervening material. This difference in potential is accompanied by an electric field, E. This follows from Gauss' Law, which relates electric field strength to electrical charge density:

$$\nabla \cdot \vec{E} = \frac{\partial E_x}{\partial x} + \frac{\partial E_y}{\partial y} + \frac{\partial E_z}{\partial z} = \frac{\rho}{\varepsilon}$$

For the case of two parallel charged plates, the electric field is proportional to the difference in potential divided by the distance, d, between them:

$$E = V/d = Q/\varepsilon A$$

This electric field operates upon a point charge, q, with a force F according to the following relation:

$$F = qE = qV/d$$

The particle is accelerated toward the charge of opposite polarity. That is to say, a positively charged particle is accelerated toward the lesser of two potentials and the negatively charged particle is accelerated toward the greater of two potentials. From these equations we understand that sharp edges or points on charged objects result in large electric fields.

Frictional forces that generate a difference in potential create a situation in which charged particles would naturally be discharged were there no binding force to the surface of the material. When the electric field becomes too great, this binding force is overcome and electrons are released in a very sudden and non-linear way from their bonds. An arc forms across the ionized dielectric and the natural propensity of the charged carriers (electrons) to flow is given free rein. So if two materials at different potentials are brought within progressively closer proximity, the electric field increases continually, eventuating in the electrical breakdown of the dielectric material (an ESD event). The tendency of materials to accumulate positive or negative charge is given by the triboelectric series, (see Table 1).

++++++	Descending Order ↓		Ascending Order ↑
Asbestos		Hard Rubber	
Rabbit Fur		Nickel, Copper	
Glass		Brass, Silver	
Mica		Gold, Platinum	
Human hair		Sulfur	
Nylon		Acetate, Rayon	
Wool		Polyester	
Fur		Celluloid	
Lead		Orlon	
Silk		Saran	
Aluminum		Polyurethane	
Paper		Polyethylene	
Cotton		Polypropylene	
Steel		PVC (Vinyl)	
Wood		Kelf	
Amber		Silicon	
Sealing Wax		Teflon	
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Table 1: Triboelectric Series

Those materials at the top of the list tend to lose electrons, while those at the bottom tend to pick them up. Therefore, the top materials acquire a positive charge, while the bottom ones acquire a negative charge. And the further their separation in the series, the stronger is the tendency to transfer charge.

One can also get ESD when peripherals are plugged into a system. This can take place during installation or during operation. Portable systems are especially prone to this. A cable can become electrostatically charged simply by its proximity to heavy electrical equipment such as a motor.

The Consequences of ESD

Frictional forces in manufacturing equipment and personnel or in the environment of operation can yield such discharges. The high electrical currents involved can disturb temporarily or destroy permanently the proper operation of the device in question. If the discharge occurs before final product screening, the damage can typically be detected and the affected units scrapped. Clearly, however, this is a costly process that is to be avoided. On the other hand, if the damage occurs after the final product screen, either in the factory, in transport, or in the hands of the customer, the problem is all the more serious. It can result in customer returns of product, expensive yield losses in board manufacture, and disruptions to the predictable flow of product to the end-user. All of these things pose difficulties for both the supplier and customer. As a result of these issues, standards are emerging that specify levels of ESD immunity. Many companies impose these standards on the equipment they purchase.

How can these issues be addressed? To answer this question, we must first distinguish between electrostatic discharge in manufacture and in the field. This is a natural division for four reasons. 1) The manufacturing environment can differ widely from the end-use environment. 2) The means of protection that are available in the two environments can also differ widely. 3) The susceptibility of the finished design may differ from that of its component parts. 4) Temporary dysfunction is a failure criterion only in end-use.

What are the Relevant ESD Models?

Before considering the means that may be taken to protect integrated circuits and printed circuit boards, it is important to understand the various metrics that one seeks to optimize. What is not measurable is not subject to quantitative improvement. Clearly, the test must be repeatable for the results to be meaningful. There are several ESD models that attempt to simulate, under a controlled environment, the nature of an ESD event. As the real environment is variable, different standards have evolved to emulate these environments and provide meaningful correlation between what is measured in the lab and what is seen in the field.

There are three such models in vogue. The first is the most popular and is referred to as the Human Body Model (HBM). It seeks to emulate the conditions of a contact by touch. The second is called the Machine Model (MM). It emulates well the discharge from a machine or cable. The latter method has been particularly popular in Japan, although its popularity is on the wane. The third model is called the Charged Device Model (CDM). In this last model, it is the device, itself, which discharges into a probe.

These standards are not exhaustive, however. There are issues with latch-up, a phenomenon whereby an external electrical stimulus places an integrated circuit into a self-reinforcing state of current conduction. Depending upon the currents involved, the robustness of the device, and the particularities of its function, this latch-up phenomenon can cause either physical damage or temporary dysfunction. There are two models that deal with this contingency: the JEDEC Latch-up (LU) and the Transient Latch-up (TLU) models. These are increasingly important because equipment can be in operation when external connections are made or when an ESD event occurs to some exposed part of the product. All of the models hitherto mentioned are conceived with component

characterization in mind. System-level characterization has resulted in a new specification, IEC 1000-4-2:1995, which will be discussed as well.

The Human Body Model Standard

The traditional standard for ESD testing is MIL-STD-883 (Method 3015). This standard is equivalent to the Human Body Model. It is typically performed upon devices in integrated circuit packages. This has also been formalized as ANSI/EOS/ESD-S5.1-1993 by ANSI and the EOS/ESD Association, Inc. This specification defines the following classes of ESD rating:

MIL-STD-1686 Equivalent Classes	EOS/ESD 5.1 Classes	Voltage Range Minimum	Voltage Range Maxmum
Class 1	Class 0	0 Volts	to 249 Volts
Class 1	Class 1A	250 Volts	to 499 Volts
Class 1	Class 1B	500 Volts	to 999 Volts
Class 1	Class 1C	1000 Volts	to 1999 Volts
Class 2	Class 2	2000 Volts	to 3999 Volts
Class 3	Class 3A	4000 Volts	to 7999 Volts
Class 3	Class 3B	8000 Volts +	

Table 2: Human Body Model ESD Classes

Components must pass all of the ESD stress levels up to and including their classification level.

In essence, a 100 pF capacitor is charged to some test voltage, then discharged into a component pin through a 1.5 Kohm resistor with another pin selected as a return. After three high-going and three low-going pulses across each pin pair, the component is checked for damage. This damage typically takes the form of a leakage current or of an open circuit failure at the pin itself. Testing is to be conducted pin-to-pin. Per the ANSI specification, this is defined as follows:

I. All digital and analog integrated circuit components:
   A. All non-supply pin to all non-supply pin permutations with supply pins floating.
   B. Each supply pin set (defined as only those supply pins which are metallically shorted internally) to every non-supply pin with all other non-supply pins floating.

II. Integrated circuit components with operational amplifier functions: In addition to the above, each non-inverting input to each inverting input.

III. Components with six pins or less: All possible pin pair combinations regardless of their pin function.

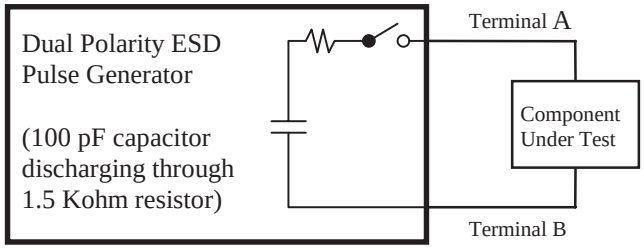

Figure 1: HBM ESD Test configuration

Care should be taken in measuring the ESD rating of an integrated device. It should be kept in mind that ESD damage on one pin may adversely affect the subsequent characterization of other pins. This, again, is due to the manner in which charged particles can be widely dispersed as the discharge arcs across the die. Since the human body model standard specifies pin-to-pin ESD characterization, for a device with N leads, one must perform roughly N(N-1) tests. If one is speaking of an 8-lead package, there are already 56 separate conditions to be evaluated. If one is speaking of a 68-lead package, already one has 4556 combinations to evaluate. A microprocessor in a pin-grid-array (PGA) package yields even more permutations. There are automated testers that can handle permutations, but characterization times can become burdensome. Different ESD tests strive to achieve different current waveforms corresponding to different environmental hazards. The HBM current waveform appears as follows when dissipating into a pure short.

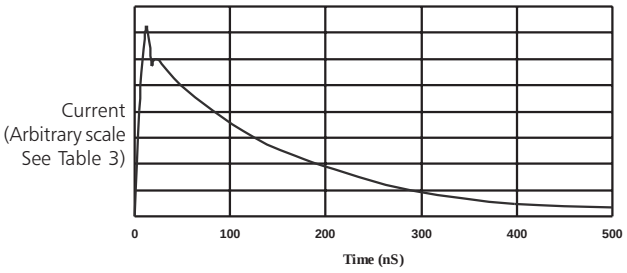

Figure 2: Current Waveform Through a Short - HBM

One ought also to consider the effects of both package and test fixture. Increased lead inductance typically improves ESD results and so variations in fixtures and packages can lead to different ESD ratings. Because inductance naturally resists changes in current flow, the pulse is spread out over a longer time period, the peak currents are reduced, and the threshold of damage is raised. For this reason, it is important to test the device in its true package and to minimize the lengths of fixture leads insofar as this is possible.

Another package-related issue can be arcing across adjacent leads in the package. The threshold of such arcing will clearly depend on the geometry of the package lead-frame. In general, more narrowly spaced leads and sharper edges will lower the potential difference required for arcing by increasing the peak electric fields. All things being equal, one would expect this behavior first in the smaller packages, especially in QSOP, SOT, and MSOP packages, rather than in SOIC or PDIP packages. But this is not typically an issue.

Table 3 indicates the peak currents during ESD stressing according to class ratings. Also included are the peak currents under tester calibration conditions.

Level	Peak current into a short (Ips) (ESD stress current)	Peak current into a 500ohm/0pF load (Ipr) (Calibration)	Peak current into a 500ohm/30pF load (Ipr) (Calibration)	Equivalent peak Voltage (Vp)
1	0.17 A			250 V
2	0.33 A			500 V
3	0.67 A	0.5 A	0.42 A	1000 V
4	1.33 A			2000 V
5	2.67 A			4000 V
6	5.33 A			8000 V

Table 3: Peak Currents during HBM ESD Testing and Tester Calibration

The component is to remain in the temperature range 17°C to 27°C prior to ESD stressing. Test three component samples to all the static and dynamic datasheet parameters. Apply three positive and three negative pulses in series to each component under each specified pin combination. Time between pulses is to be no less than 1 second. Retest the three devices to full static and dynamic datasheet parameters, recording the stress levels and results for each component. Increase the stress level to the next highest rating. (In internal characterization, one may sometimes increment at smaller steps in order to obtain an accurate characterization value. This is typically done in steps of 100 Volts. However, such a procedure can result in *step stress test hardening*. The component, tested under these conditions, may be able to withstand more severe ESD conditions than a fresh component.) As indicated, full static and dynamic testing to datasheet parameters is to be performed prior to and following HBM ESD stress testing to determine if there is failure. Pin leakage current is typically used to determine ESD withstand voltage, but in many cases this is not sufficient as other failure mechanisms may be involved. In some cases, device performance may be degraded but drift back to acceptable levels over time. Therefore, it may be important that static and dynamic testing follow stress testing without significant delay. Consult ANSI/EOS/ESD-S5.1-1993 for details on tester qualification and calibration methods or for further testing details. Alternatively consult the JEDEC standard, EIA/JESD22-A114-A.

The Machine Model Standard

The Machine Model (MM) ESD stressing method is embodied in the specification entitled ANSI/ESD-S5.2-1994 approved by ANSI and the ESD Association. It specifies discharge from a 200 pF capacitor through a nominal 0.75 μH inductor. (What is important is the current profile with time.)

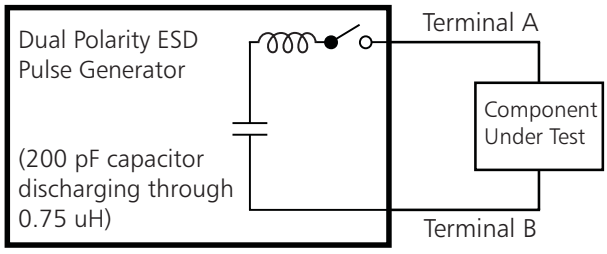

Figure 3: MM ESD Test configuration

The Machine Model differs from the Human Body Model in that the capacitor appears as a voltage source, having no resistor to fix the current level. This was perceived to be a more severe case by the Japanese in the 1970's and so they originated this new model. The name of the test in the English-

speaking world, Machine Model, came from the assumption that the Japanese were using this to emulate their automated assembly and manufacturing environment. While this thinking may or may not have been explicit in Japan, this model does represent many such cases. The Machine Model ratings are at lower voltages than those of the Human Body Model, reflecting the more severe environment. ANSI/ESD-S5.2-1994 specifies the following classes of ESD protection:

Class	Voltage Range Minimum	Voltage Range Maxmum
M0	0 Volts	to 24 Volts
M1	25 Volts	to 99 Volts
M2	100 Volts	to 199 Volts
M3	200 Volts	to 399 Volts
M4	400 Volts	to 799 Volts
M5	800 Volts +	

Table 4: Machine Model ESD Classes (per EOS/ESD S5.2-1994)

Like ANSI/ESD-S5.1-1993, it also specifies the pin combinations that are to be evaluated:

I. All digital and analog integrated circuit components:
- A. All non-supply pin to all non-supply pin permutations with supply pins floating.
- B. Each supply pin set (defined as only those supply pins which are metallically shorted internally) to every non-supply pin with all other non-supply pins floating.

II. Integrated circuit components with operational amplifier functions: In addition to the above, each non-inverting input to each inverting input.

III. Components with six pins or less: All possible pin pair combinations regardless of their pin function.

The peak currents obtained via the Machine Model approach depends upon proper calibration of the system. Whereas in the case of the Human Body Model, the 1.5 Kohm resistor largely limits the peak current, the peak current of the Machine Model depends ultimately on the dynamics of discharge. Therefore the Machine Model can be even more sensitive to parasitic inductance and package variations. The ANSI specification indicates the following peak currents corresponding to the various test levels.

Level	First Peak current into a shorting (Ip1)	Peak current into 500 ohms (Ipr) (Calibration)	Peak current into 500 ohms at 100 ns (Calibration)	Equivalent charging Voltage (Vp)
1	1.75 A			100 V
2	3.5 A			200 V
3	7.0 A	0.85 - 1.2 A	0.29 A	400 V
4	14.0 A			800 V

Table 5: Machine Model ESD Levels and Peak Currents

The Machine Model is also reflected in the JEDEC standard, EIA/JESD22-A115-A, dated October 1997.

The Charged-Device Model

The Charged-Device Model (CDM) is an alternative method of characterization of components. This model does not have the popularity of HBM or MM, but is sometimes used in conjunction with the other methods. JEDEC standard, JESD22-C101, outlines the technique in detail. In many respects it is the most appropriate ESD model for printed circuit board assembly equipment and IC handlers because it most closely emulates that environment. A component may become charged in sliding down a rail to a tester. If this charged device should come into contact with a metallic surface, it will discharge into that surface, potentially damaging the device. One difficulty in creating the CDM standard lies in the rapidity of the ESD event. The current rise-time is often less than 100 psec and the entire discharge may be completed in less that 500 psec. In order to record such a discharge, a transient event recorder with bandwidth of 5 GHz is required.

In the "field-induced method," the Device Under Test (DUT) is placed on the test module and the potential is raised to the voltage indicated by the test. A grounded pogo probe which is connected to a 50 ohm semi-rigid coaxial cable is brought toward the DUT until discharge takes place. The energy which is dissipated in this type of discharge depends upon the capacitance of the device itself and not upon a fixed capacitor as in the HBM and MM. Although the capacitance is much lower in this case, the current peak can be quite severe due to the rapidity of the event. The current waveform is that of a double exponential and damped oscillation. The ESD performance classes for the CDM test method are as follows:

Class	Voltage Range Minimum	Voltage Range Maximum
C0	0 Volts	to 124 Volts
C1	125 Volts	to 249 Volts
C2	250 Volts	to 499 Volts
C3	500 Volts	to 999 Volts
C4	1000 Volts	to 1999 Volts
C5	2000 Volts +	

Table 6: Charged-Device Model ESD Classes (Per EOS/ESD S5.3-1993)

The Charged-Device Model (CDM) has not achieved wide popularity due to some of the difficulties in implementing the test. Because it discharges across an air gap, there is some variability in the results.

The JEDEC Latch-up Standard

Latch-up is a phenomenon in which a parasitic SCR (Silicon Controlled Rectifier) is enabled by an external stimulus. The latch-up state can either enter into thermal run-away, resulting in physical destruction of the component, or it can remain stable and temporarily disable the component until it is powered down. CMOS devices are particularly sensitive to this behavior due to their unique processing and device structures. The JEDEC Latch-up standard, EIA/JESD78, is used to characterize the ruggedness of a component under conditions that tend to produce such failures. Class I specifies latch-up testing at room temperature. Class II specifies testing at the maximum ambient rated temperature for the device. Class I testing is the default.

Six (6) devices are tested using the I-test and the Vsupply Overvoltage test. It is also permitted to use six samples for each of the two tests. In the I-test, each pin under test is subjected to a positive current trigger source while all input pins are tied high. If, in returning the pin to its previous state, the supply current exceeds its previous value, then a latch-up failure has taken place. Similarly, the component is tested with a negative current trigger source. In the Vsupply Overvoltage test, a voltage trigger source is applied to the supply pin. After returning the pin to its normally biased condition, one checks the supply current to see if an increase has taken place. Such an increase indicates a latch-up failure. The details of the test waveforms and biasing conditions can be found in the JEDEC specification. It should be noted, however, that these tests are static tests and that their correlation with the ESD event is inexact.

The Transient Latch-up Standard

Transient latch-up is the phenomenon whereby a very fast current or voltage transient on the supply, input, or output pins couples sufficient energy to an SCR to initiate conduction. These transient events often trigger SCRs that the overstress methods do not. The standard for this type of failure is in committee stage.

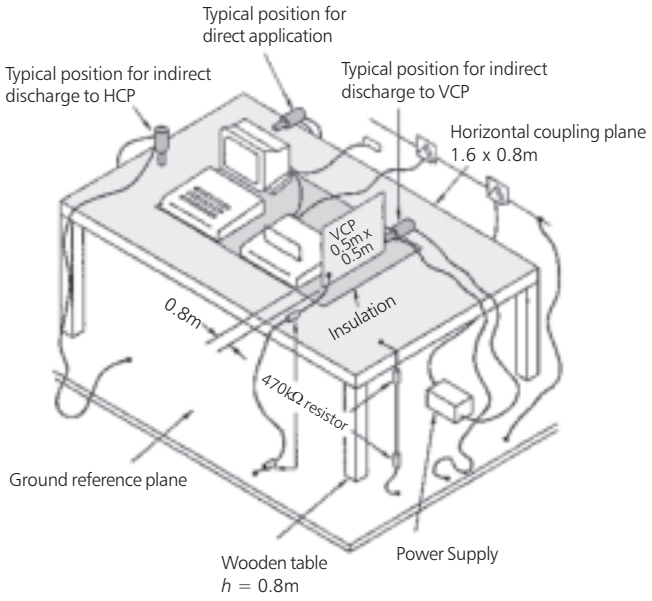

Figure 5: IEC 1000-4-2 Table-top Test Set-up

The IEC 1000-4-2:1995 Standard

IEC 1000-4-2:1995 is an international standard which is gaining acceptance throughout the world. It is not intended for component-level, but rather for system characterization. The standard evolved from IEC 801-2:1984 and IEC 801-2:1991, which it replaces. There are two types of discharge covered by the specification. The first is called "contact discharge" and the second is called "air discharge." Of the two, the air discharge is less reproducible and hence less useful in identifying and correcting ESD problems. A charged probe tip approaches a neutrally charged line or any area on the body of the equipment. As the electric field reaches a critical level, the intervening air gap ionizes, providing a conductive path for an ESD event. The current discharge is a double-exponential function. That is to say, the current rises first by an exponential function and then falls by an exponential function. The fall-time is determined by the discrete resistor (330 ohms), which is in series with the discharging capacitor (150 pF). But the current waveform in the air-gap technique is not well controlled, because the length of the ionized air gap is difficult

to control. One way of minimizing this variation is to move the electrode tip at high speed toward the body. The test configuration is as follows:

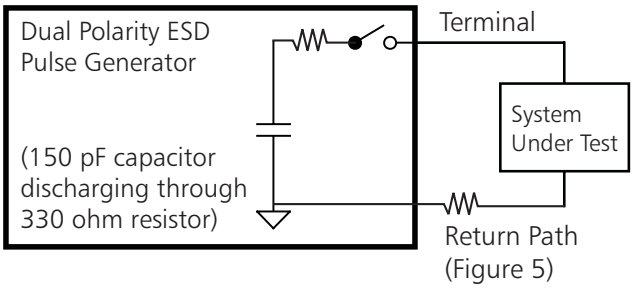

Figure 4: IEC 1000-4-2:1995
Test configuration

Testing should be done in a well-controlled and safe environment. The following test setup for table-top equipment is specified in IEC 1000-4-2. Note that it requires connecting the ground return cable of the ESD gun to the Ground Reference Plane, not the chassis of the equipment under test. Thus the ESD current pulse experienced by the equipment under test would be much smaller if the equipment chassis is electrically isolated from the mains earth-ground. A more detailed illustration of the IEC 1000-4-2 test set-up is shown in Figure 5.

A typical IEC 1000-4-2:1995 current waveform is shown below.

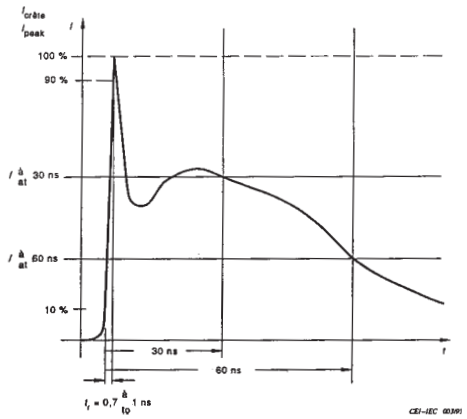

Figure 6: IEC 1000-4-2:1995 ESD Current Characteristics

And the classes of ESD protection are as follows:

Contact Discharge		Air Discharge	
Level	**Test Voltage**	**Level**	**Test Voltage**
1	2 KV	1	2 KV
2	4 KV	2	4 KV
3	6 KV	3	8 KV
4	8 KV	4	15 KV
X	Special	X	Special

Table 7: IEC 1000-4-2:1995 ESD Classes

This table does not imply any equivalency between contact-discharge and air-discharge tests. These two methods are used to characterize the system in very different ways.

There are several difficulties in linking system-level and component-level ESD specifications. First, the system level standard (IEC 1000-4-2) differs from the component-level standard (EIA/JESD22-A114-A or ANSI/EOS/ESD-S5.1-1993). The peak current of IEC 1000-4-2 is 5 times greater. But there can be multiple devices on the same line on a board and each of these may contribute to dissipating the ESD pulse. Moreover, the capacitance and inductance of the line can seriously modify the shape of the pulse. They favor discharge in one path instead of another. The line capacitance reduces the voltage that the devices must withstand. Finally, one must understand the relationship between the ESD protection network and the protected devices. Most ESD protection schemes are based on clamping the maximum voltage downstream from the protection network to a safe level. What downstream voltage is required? This question is very recent. Some corporations have developed their own standards to which suppliers must adhere. Others consider each design as a separate case. The downstream clamp voltage is important to such decisions. It is the bridge between the protection network and the downstream devices.

In validating the design, one must consider several questions. First, one must define the practical limits of failure. These limits include data integrity, recovery time, and other issues. The device should be ESD tested wherever there is the possibility of touch during normal operation. One should use the

"contact discharge" method to test coupling planes, conductive surfaces, I/O ports, flex pads, power supply, and pogo pins. One should use the "air discharge" method to test insulating surfaces, openings at the edge of keys, flex cables, vent areas, seams, slots, and apertures. Some engineers spray the equipment with rapid pulses while the equipment is on. There is a great deal of variability in characterization plans. One ought to refer to IEC 1000-4-2 to formulate such a plan.

It is more difficult to control the path of discharge in the "air discharge" method as compared to the "contact discharge" method. The latter method makes direct contact to the pin or port connector and gates discharge through a switch. The condition is more severe than the air-gap technique, and so whereas the standard target voltage for the air-gap technique is 15 KV, the target for the contact discharge technique is 8 KV. Contact discharge is to be preferred, but sometimes only air-gap discharge is possible.

Since the IEC specification is intended for system ESD characterization, there is confusion on how to design to meet specific IEC immunity levels. A temptation is to employ ESD protection components which guarantee IEC compliance on external ports. The IEC specification would suggest the use of extremely robust protection devices. This can be costly and have significant effect upon signaling capabilities of the ports particularly those that are high performance such as video, SCSI, data communication, etc. Devices that can handle 50 or 100 ESD amperes tend to be discrete, physically large, and have high capacitance (several hundred pF). Several manufacturers seem to be bridging the gap between the IEC system specification and component performance by formulating their own component standards. One approach adopted by a number of manufacturers is a modification of the human body model (component test, contact discharge, etc.) but with the charge capacitor at 150 pF and the series resistor at 330 ohms. These two changes are adopted from the IEC specification. In addition, the desired component level immunity appears to be at 8 KV for contact discharge. Some manufacturers also require 15 KV air discharge to the component although air discharge tends to be an unreliable component test. These criteria imply an IEC Level 4 system ESD immunity when components are used that pass the modified test. This approach seems to be working well in the industry.

ESD failures at the board level can be divided into two categories: radiated upset and conducted upset. Radiated upset occurs when the high current transients during discharge radiate electromagnetic noise, which is then coupled into another part of the system. This coupling can cause either temporary or permanent failure of the system. Protecting against radiated upset is largely a question of proper shielding and cable matching. The former limits the energy that can be radiatively coupled, whereas the latter ensures that whatever noise is coupled, is coupled according to the common mode. But this is beyond the scope of our treatment.

The second mode of failure, conducted upset, is that which most concerns this article. HMB, MM, and CDM all characterize this latter category. The methods used to eliminate such damage are to be considered now.

Limiting ESD in the Manufacturing Environment

While each manufacturing environment may have unique sources of difficulty, there are a number of common procedures around which the industry as a whole has gravitated. As regards manufacturing personnel, adequate grounding via heel and wrist straps, and ESD smocks is a must. Typically, the manufacturing environment is also provided with adequate grounding of tables, floors, and machinery so as to conduct away charged carriers that might otherwise build up over time. Because dry conditions exacerbate the likelihood and severity of discharge, humidity is often maintained at an artificially high level and is closely monitored. Devices are kept in conductive tubes and conductive metallized bags during handling. Automatic handlers are designed in such a way as to minimize the development of static charges during the requisite motions involved in testing devices. These techniques of suppressing the sources of electrostatic discharge have been highly successful in depressing the rate of damage by such events. Many of these devices never see a more severe environment, and so the design of these devices need only meet certain minimal requirements.

Designing for ESD in the Application Environment

The variability of potential environments makes protection more complex. In many cases, the demands are less stringent. If, for example, a device is embedded into a board design, there may be no further issues with ESD that are not accounted for in designing for the manufacturing environment.

Several factors conspire to bring this about. First, many leads to the device may be inaccessible to the end user. This prevents contact with electrical hazards such as statically charged fingers, screw-drivers, or table surfaces. Second, the various leads on the board will have a higher capacitance than the individual pins of a single device. The wire itself has a distributed capacitance and will typically have two or more devices connected to it. This capacitance spreads out the current associated with electrostatic discharge, lowering its peak value. (Total charge dissipation is of course unchanged.) And the multiplicity of devices provides multiple sites for dissipating the current.

However, there are many cases in which the application environment is more demanding than that of the factory. This is generally the case when wires are open to manipulation and contact by the end user, as in peripheral ports. Whereas the sources of ESD can be minimized in the factory by suitable precautions, the user environment is uncontrolled. Hence there are more stringent requirements. These requirements take a number of different forms. The voltage and current limits are typically elevated. The various media through which discharge can be made will vary as will the ways contact can be made, resulting in different models to be used in characterizing reliability. But additionally, there are techniques that may be applied at the board level which are not available at the device package level. These include adding capacitors, spark gaps, discrete diodes, metal oxide varistors (MOVs), and integrated diode networks. The choice of a solution is sensitive to the ESD requirements, cost and performance issues, board space issues, and the signal levels that are being used. The ESD performance of the solution can also be highly dependent on the way both the components and the protection devices are arranged on the board. The relationship between component ESD ratings and those of the board are complex, yet certain design rules can go a long way toward obviating difficulties and optimizing the network performance.

Moreover, there are issues of temporary and non-destructive latch-up of devices, which can disable operation until the system is shut down and restarted. Or devices that are powered during operation may have different sensitivities to ESD strikes than those same devices when they are not powered. These are issues that will rarely, if ever be addressed by evaluating the device only under factory conditions.

Using External Capacitors to Prevent ESD Damage

The total charge that is dissipated into a line is fixed by the test method itself. However, it is not charge *per se* that destroys and disables devices. It is the dissipation of power that is most critical. One measure of interest is the peak current that the device sees during an ESD strike. All other things being equal, a higher peak current is the more demanding case. One of the primary techniques in improving ESD performance is to limit this current by spreading it out over time. How to accomplish this? In some devices there are already internal resistors which serve to limit the current dissipation. For instance, on the RS-232 receiver, a 5 Kohm nominal resistor to ground is part and parcel of the input receiver specification. This limits the current that can be dissipated into the device. But resistors are typically unfeasible at the board level due to the manner in which they reduce output drive. The use of external capacitors is common in some applications. This technique serves as a voltage divider during discharge, and hence reduces the peak current. For example, consider the case of an HBM discharge in a device protected by a 100 pF external capacitor. Recall that the HBM calls for dissipation through a 1.5 Kohm resistor from a charged 100 pF capacitor. Let us ignore the current limitation provided by the HBM resistor itself and consider only the effect of the external capacitor on ESD performance. The HBM capacitor, charged to 8 KV, would, when discharged into the 100 pF external cap, divide its peak voltage to about 4 KV. The device would only see this lower voltage, and so the peak current would be vastly reduced. The analysis with the 1.5 Kohm resistor included is more complex, but the principle is essentially unchanged. But capacitors are not wholly desirable. From a performance point of view, they are often unacceptable because they slow down the signal rates. The driver remains unchanged, but the load it must drive is increased greatly. This increases current consumption according to the $I = fCV$ relation. The performance may also deviate strongly from the ideal case due to parasitic inductance. Since the ESD event takes place so quickly, the inductive contribution to impedance can be quite large. Moreover, the addition of these larger capacitors usually requires the use of discrete devices with the associated penalties of board space, cost, and velocity of the manufacturing line. So capacitors are far from an ideal solution.

Using Spark Gaps in Board Design

The use of spark gaps is a viable technique that can be implemented in many board designs. The principle is to provide a low impedance current path to ground at high voltage levels, while leaving the path open under normal conditions. Typically, one uses interdigitated structures in which one set of fingers is connected to the lead that is to be protected from the strike and the other set of fingers is tied to ground. The fingers are separated, but very close to each other. In the case of an ESD strike, the near proximity of the fingers should ensure that the

electric field is maximized in this locale, so that an electrical breakdown of the intervening dielectric material occurs, thereby shunting current away from the devices to be protected. Under normal operation, there ought to be minimal influence upon signaling, only additional capacitance of the interdigitated structure, which is significantly less than an external capacitor. And, above all, in today's cost-competitive manufacturing environment, it is a low-cost solution. But the use of spark gaps in board designs yields other issues. First, there is the potential degradation of the spark gap with successive ESD strikes. This can widen the gap so that electrical breakdown no longer occurs at this point and the line is no longer protected from ESD pulses. Or there is a potential of shorting across the spark gap, which will effectively destroy the functionality of the board.

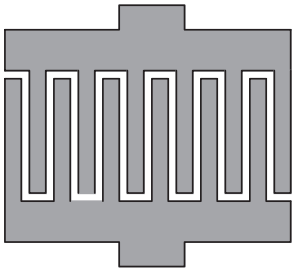

Figure 7: Integrated Spark Gap

The degree of ESD protection which a spark gap will provide depends then on many manufacturing issues: How close can the lines of the spark gap be brought together? How stable is the gap over several ESD strikes? Are the manufacturing tolerances sufficient to guarantee consistent behavior of the spark gap? Does the introduction of the spark gap pose a yield issue in board manufacture? These are all questions that must be posed and answered before this technique can be reliably implemented. Moreover, such structures can sometimes be wasteful of board space. In many respects, these are questions that must be answered in every ESD solution, but this case is different in one important respect:

It requires a higher level of cooperation between board manufacturer and designer to guarantee ESD performance.

Where this level of cooperation is attained, spark gap technology can be an extremely competitive solution.

Metal Oxide Varistors

One popular technique for surge protection, especially for power supplies, is the Metal Oxide Varistor (MOV). The device is connected in parallel to ground with the line that is to be protected. Under normal operating conditions, it is an insulator. But with line surges or ESD events, the device shunts current to ground. Typically, the device consists in a metal oxide insulator (typically zinc oxide) between two conductive metal plates. However, the metal oxide has a breakdown voltage at which it conducts current across the plates, resulting in a short. By this means, the MOV can act as a protection device for sensitive circuitry. MOVs are, by the standards of many other techniques, competitively priced. However, one serious drawback of the MOV is that it degrades with usage. With multiple strikes its capacity to act as an effective ESD guard diminishes. In some cases, the MOV can burn out. MOVs are not useful in protecting signal lines due to their bulkiness and slow response time. Experts in the field typically advise that the Metal Oxide Varistor be used in conjunction with other techniques for effective surge protection.

Connector-Level Solutions to ESD

One recent advance in ESD protection technology is that offered by Bournes with their ChipGuard™ ESD suppressor. This product is a flexible device that press-fits over a D-subminiature connector. The suppressor has an array of stainless-steel spring contacts and a ground plane. The gap between the two is filled by a dielectric. Under normal operating conditions, the connector acts as an insulator. However a transient pulse converts the material into a conductor which shunts current into the ground plane and away from the sensitive port. It has a relatively fast clamping speed of 2 nsec and an off resistance of 500 Kohms at 30 V. Its capacitance is a competitive 3 pF. Additionally, the clamping voltage is typically 100V, permitting wide voltage swings. The primary drawback of the connector is its cost. But it has a unique advantage in that it can be retrofitted onto existing connectors in order to protect existing designs from ESD hazards. Where the cost or time required for board redesign are prohibitive, this technology provides an acceptable solution.

Using Discrete Diodes for ESD Protection

Discrete diodes offer a number of advantages over some of the techniques heretofore discussed. They can offer effective ESD protection without the severe degradation of performance that accompanies the use of capacitors. Essentially, this solution takes advantage of the rectifying characteristics of a diode to provide a current sink during discharge, while minimally loading the line during normal operation. The following figure illustrates two possible solutions. The first is to provide two diodes per line, one to ground and the other to the power rail. Each of these diodes is reverse-biased during normal operation of the system. When there is an ESD pulse from an external source, this drives the line voltage either

above the power rail potential or below the ground potential, resulting in the forward-biasing of one of these diodes. If the diode to the power rail is forward-biased, the diode effectively sinks the external current into the power rail. If, on the other hand, the diode to ground is forward-biased, the diode provides a channel for the sourcing of current from the common ground. In either case, the devices that are connected to the line are protected from the surge. They are forced neither to source nor sink high levels of current and are therefore effectively protected from the strike.

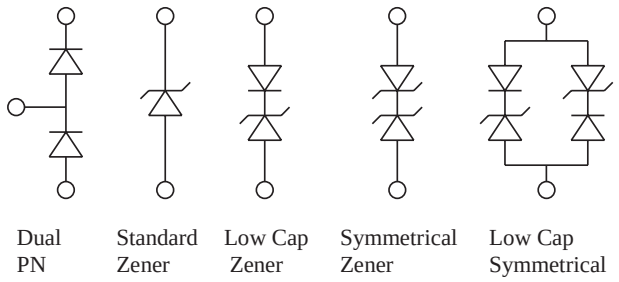

Figure 8: ESD Diode Configuration

Where there is no availability of a power rail, one may implement a similar technique with a Zener diode to ground. The Zener diode offers a well-controlled reverse-bias breakdown, which provides adequate protection when the line is pulsed and the diode driven into Zener breakdown Standard PN diodes are generally deficient in the reverse-bias case. Unfortunately, Zener diodes have high capacitance that can cause line loading and waveform degradation. This can be overcome with some more complex low capacitance versions as shown above. Also, in its simpler configurations, it provides asymmetrical clamping capability with regard to pulse polarity. One advantage of the Zener diode solution is that it offers no issues in power-down because the diode is referenced only to ground and not to the power rail. The dual-PN diode solution, for all its advantages, must be used properly in such situations. This will be discussed more fully under the heading of integrated diode solutions.

These discrete diode techniques are used effectively in many designs to provide dependable protection against ESD damage. Yet they come with several drawbacks. The first is the additional cost of the components, typically two per line. Yet the total cost of implementation can be significantly higher when one factors in the costs of pick and place operations, the impact this has on the velocity of the manufacturing line, and the increased defect and rework rates which accompany the addition of so many components. One may conservatively estimate this additional cost per component at $0.02. Assuming a 17-bit data bus (e.g. the parallel port interface), this implies the incorporation of 17 PN diode pairs and an additional manufacturing cost of $0.34 per board above and beyond the pure component cost. Assuming a single Zener diode per line, the cost would also be about $0.34 per board. So, while the discrete diode solution comes very close to ideal in other respects, the cost is prohibitive in many system level solutions.

The Advantages of Integrated ESD Diode Networks

Integrated solutions can offer the advantages of the PN diode solution at a substantially lower cost. This cost saving derives from two considerations. First, the package cost of multiple discrete diodes is reduced by integration into a single, albeit more expensive, package. Second, the total solution cost is reduced by the reduction of component count. This reduction can have an immediate positive result in increased manufacturing velocity, improved board yields, and reduced board rework. This level of integration can be even more critical in portable applications, when questions of weight and size rule supreme. Three examples of integrated solutions are California Micro Devices' PAC DN006, PAC DN004, and PAC DN007.

Performance Catagory	PAC DN006	PAC DN004	PAC DN007
Number of Lines of ESD Protection	6	2	18
Maximum ESD (HBM)	±15KV	±15KV	±16KV
IEC 1000-4-2 Contact Discharge (100 positive pulses separated by 1 second, 100 negative pulses separated by 1 second)	±8KV	±8KV	±15KV
Downstream Clamping Voltage (@15 KV HBM) Positive Transient Negative Transient	V_P + 13V V_N - 13V	V_P + 13V V_N - 13V	V_P + 13V V_N - 13V
Channel Leakage Current (maximum)	1.0 μA	1.0 μA	1.0 μA
Package Type	8-pin MSOP	SOT-143	24-pin QSOP
Pin Capacitance (typical)	3 pF	3 pF	7 pF

Table 8: Performance of P/Active™ (PAC™) Diode Technologies

An indication of the level of ESD protection afforded by the PAC DN007 or Super 1284 is its performance in conjunction with California Micro Devices' PAC 1284 or Super 1284 parallel printer-port terminations, a standard desk-top and portable solution. The PAC 1284 is already designed for significant ESD robustness. The ESD protection for the Super 1284 is specified at 8 KV HBM in operation and at 4 KV HBM in handling. But there are demands for further protection. Characterization has shown that the Super 1284 readily meets 8 KV contact discharge protection (per IEC-1000-4-2) when used in conjunction with the PAC DN007, offering a complete termination and ESD solution.

The choice of an integrated solution can depend on several board-layout issues. In general, a higher degree of integration yields lower cost and reduces board-space consumption. In many applications, saving board space can be the driving factor, since both discrete diodes and spark gaps can place unreasonable demands on the board designer. However, there is the additional factor of device placement. Routing to a large device can sometimes be difficult if the lines to be protected are widely separated. This situation militates against the use of integrated solutions, or at least the use of lower levels of such integration. In this respect, the PAC DN006, for example, offers advantages over the PAC DN007 because the lower line count permits greater flexibility of placement while the miniature footprint of the MSOP package keeps board space to a minimum. (See Table 8.) But there are cases in which the PAC DN007 is adequate and is the lower cost solution.

Other Considerations in Specifying ESD Diode Networks

As always, capacitance is an important consideration. The PAC DN006 has a typical capacitance of 3 pF measured at 2.5V at the input. This is important for high speed applications which are pressed to minimize signal transition times. In terms of ESD performance, one must distinguish between component-level ESD performance and board-level ESD performance. The relation between the two depends upon both components and effective board design. Nevertheless, one can gauge the relative performance of components not only through the ESD specification, but through downstream clamping voltage. For instance, under conditions of a 15 KV HBM pulse, which results in a peak ESD current of 10 A, the PAC DN006, used correctly, guarantees less than a 13 V pulse downstream from the device. The superior forward voltages on the PAC DN006 account for this excellent clamping characteristic, (see Figure 9).

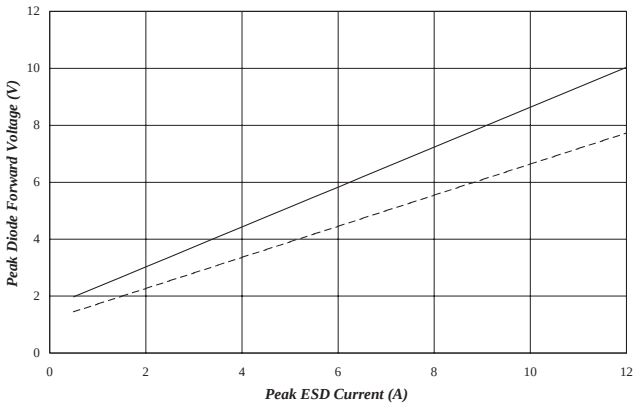

Figure 9: PAC DN006 Diode Forward Voltage @ 25°C

Another issue of interest is the recovery time from an ESD pulse. How much time is required before the system can once again begin signaling? If a non-destructive latch-up occurs, the system may require a complete shutdown and restart. Otherwise, there may be a temporary period during which the device must remain inactive. Clearly, the latter case is a complex one. Recovery time will be sensitive not only to the ESD protection technique, but to the characteristics of the drivers and receivers themselves, and even to the communication protocol. In general, there are no firm answers. However, it stands to reason that better ESD networks will make for improved recovery time, simply on the principle that these devices have better current sinking and sourcing capabilities. The most logical correlate to recovery time would be with the specified downstream protection, as this is an excellent gauge of the disturbance that the system itself sees. Finally, it is important to note that there have been no indications or observations of pin-arcing in the PAC DNXXX family.

Board-Layout Issues Associated With Integrated Diode Networks

The performance of an ESD network in a given application depends upon proper board layout techniques. In order to obtain a good correlation between component-level and board-level ESD performance, it is imperative to adhere to a few basic rules. First, it is important to place the PAC DN004, PAC DN006, or PACDN007 close to the entry point of an ESD pulse. This means, in effect, that the device is placed on the component side of any line inductance. Inductance resists changes in current flow such as that of an ESD pulse. The current will tend to be directed toward the path with the least inductance. As seen in figure 10, if there is a parasitic inductance between the entry point and the device to be protected, the ESD discharge will be largely directed

toward the protected device, making the ESD network less effective. Whereas, if one keeps the ESD network downstream from the parasitic inductance, the network will effectively shunt the pulse away from the device which is to be protected.

Some failure modes, such as latch-up, are current sensitive. While decreasing the downstream voltage will improve the downstream current pulse, it may be desirable to put a precise bound upon the current. For devices such as the PAC DN004, 6, or 7 this is

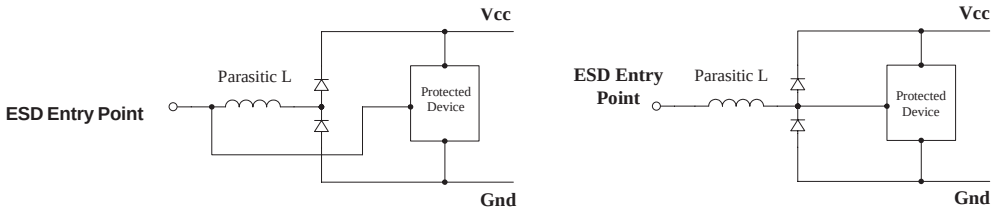

Figure 10: The Need to Keep ESD Diodes Downstream of Line Inductances

A similar issue exists with respect to the ground and power rail connections to the ESD network. A parasitic inductance in the power rail is shown in Figure 11. Because the inductance once again resists rapid changes in current, the power rail shown below will be unable to absorb the currents and these will in turn be shunted into the component itself. For an 8 KV contact discharge per IEC 1000-4-2, the downstream clamping voltage will increase by 30 V for each nH of inductance in the rail discharge path. This makes the use of a bypass capacitor indispensable. Moreover, this capacitor must be rated to high frequencies in order to deal with such rapid transients. It must have a minimum of parasitic inductance in the capacitor itself, and for this reason a larger capacitor may actually degrade performance. A 0.1– 0.2 uF capacitor is sufficient. This capacitor should be placed as close as possible to the power pin on the ESD network. A single capacitor suffices for the network, and so there is no significant cost or board space consumption.

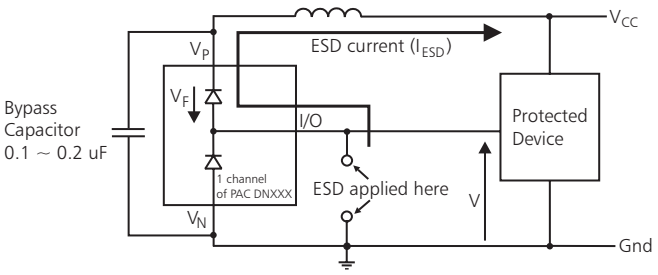

Figure 11: The Need to Minimize Power Rail Inductance

In some respects, it may be desirable to limit not only the downstream voltage that the protected component is to see, but the downstream current as well.

easily accomplished by adding series resistors between the ESD network and the protected device. The downstream current can then be calculated by dividing the diode forward voltage by the series resistance, (see Figure 12). This method is applicable to high impedance CMOS inputs. It cannot be used effectively on driver outputs without resulting in an insertion loss in output levels.

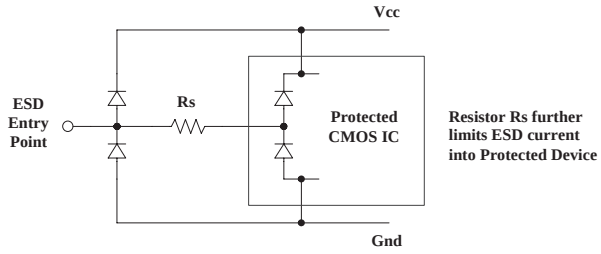

Figure 12: Using a Series Resistor to Limit Downstream Current

Finally, some systems may be powered down. When the power rail is brought to ground, a driver on the other end of the line will simply see a diode to ground. This can result in very high direct current dissipation, which drains batteries and can sometimes cause physical damage to the peripheral device. This issue can be avoided by proper board design. By placing a diode in series on the power rail side of the bypass capacitor, one can eliminate these currents. The power rail, when powered down, will not be able to sink current from the I/O pin. The single diode may be shared among many such clamps, (see Figure 13).

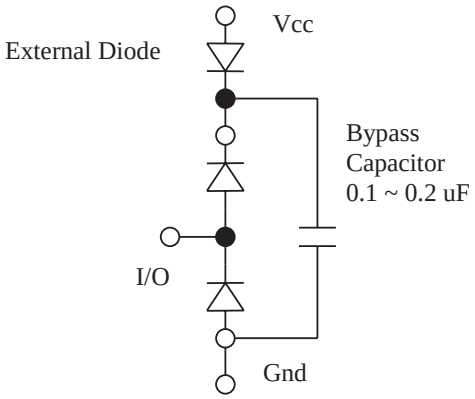

Figure 13: Bypass Capacitor Configuration for Power Down Applications

Questions of Economy in ESD Protection

How great a protection is really required? One typically receives the answer: As much as can be provided. Taken in isolation, this is certainly a valid answer. However, the board designer in practice thinks along the lines of a cost/benefit analysis. The cost-savings of improved ESD protection are real: reduced defect rates, higher reliability, etc. But the marginal benefit, stated in cost terms, is a continually decreasing one. The benefit of reducing rework rates from 5% to 0.5% is very obvious. A little less obvious is the benefit of reducing them from 0.5% to 0.05%. The benefit of reducing them from 0.05% to 0.005% is still less. The point is that ESD damage is a statistical phenomenon and that corresponding increases in ESD protection yield proportionally smaller cost incentives. These costs are represented qualitatively on the following curve, along with the costs inherent in specifying increasing levels of ESD protection. Superimposed upon the graph is the sum of these costs. It is this sum which is to be minimized, and the minimum on this graph does not correspond to maximum ESD protection. While the qualitative features of the curve are retained in every situation, the details depend on the design, the environment in which it must perform, and technology that is available to solve the problem.

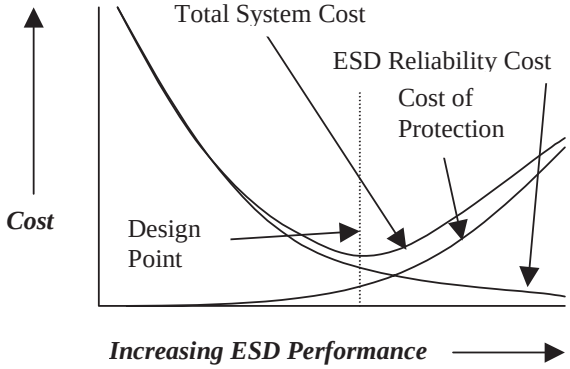

Figure 14: ESD and Total System Cost

ESD Test Equipment

ESD characterization is a method of destructive testing. There is little that can be done about this. And so it is not something that is done in product screening, except as a lot-sampling technique. This is a costly procedure, so it is desirable to design in ESD protection once and for all, characterize it, and be finished with it. The test equipment available to characterize ESD falls under a couple of significant headings. Traditionally, testers were designed for the characterization of devices in semiconductor packages. These testers have become more powerful with improvements in automation, but they remain inapplicable to board-level characterization. For the characterization of the latter, an ESD gun offers advantages over a fixed ESD test box.

One example of an ESD gun is the ESS-200AX from NoiseKen. This system generates discharges of up to 30 KV and has the capability of changing the energy storage capacitor and the discharge resistor. It operates under four different modes: IEC levels, manual, sweep, and programmable. The gun has an external control box which can be interfaced to a personal computer. And it has LCD display of critical parameters. There are other manufacturers of ESD guns. Similar systems are available from Schaffer and Martron.

For component-level testing, there are a number of automated ESD testers available to the reliability engineer. These testers handle much of the repetitive and time-consuming aspects of ESD characterization and are designed to be capable of testing to several different failure models. For example, Oryx Technology's Model 11000 Stress Test System is designed to test to the Human Body Model, the Machine Model, the Charged-Device Model, the Latch-up and Transient Latch-up Models. The test set-up is embodied within the controls of the system for improved productivity. Similar systems are available from KeyTek and other companies. The user should select systems in accordance with their needs.

Conclusion

We have examined the nature of electrostatic discharge (ESD), its causes, and its foundations in electromagnetic theory. We have reviewed the international specifications which apply to both the component and system. We have considered many of the means that are used to eliminate ESD damage and have shown both the advantages and disadvantages of each. We have considered in detail the use of integrated diode networks as the optimal solution for high-performance systems and for systems that require low weight and board space. We have indicated the board-design techniques that optimize ESD performance. And we have considered the economic requirements of an ESD solution. Finally, we have considered the equipment that is available for ESD characterization.

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