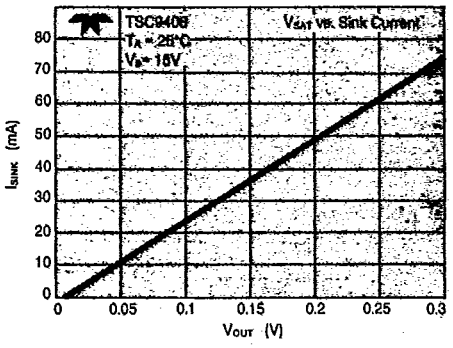
TELEDYNE SEMICONDUCTOR

TSC9405

16-BIT PARALLEL LATCHED OUTPUT PERIPHERAL DRIVER



FEATURES

- High Voltage Outputs 15V
- High Output Current Sink Capability ... 60 mA
- Low Standby Power ..... 1 mW
- High Speed Operation ..... 3.0 MHz
- 16 Latched Parallel Outputs
- Cascading Possible for Longer Data Words
- Dual-Rank Latches and $\overline{\text{STROBE}}$ Input for Ripple-free Data Update
- $\overline{\text{OUTPUT ENABLE}}$ Input Disables Outputs Without Corrupting Data

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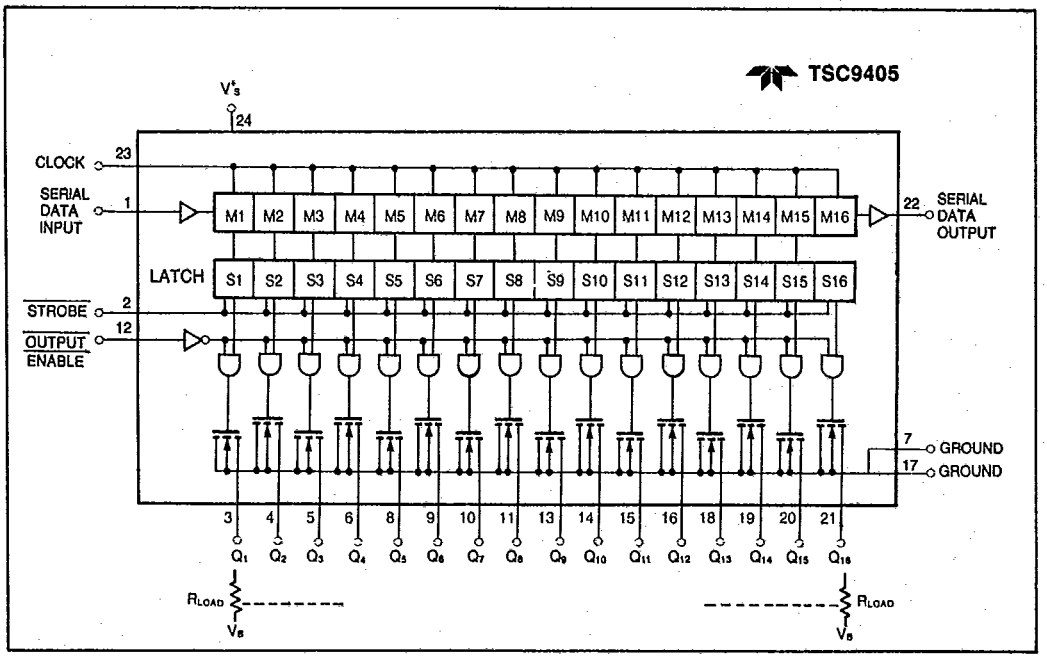
FUNCTIONAL DIAGRAM



NEW PRODUCT INFORMATION

T-52-17

TSC9405

GENERAL DESCRIPTION

The Teledyne Semiconductor TSC9405 is a serial input, 16-bit parallel latched output shift register. Master slave data latches and high output power MOS switching transistors combine to make the TSC9405 an ideal interface circuit between microprocessor I/O ports and high current/voltage peripherals. The CMOS construction limits quiescent power dissipation to 1 mW.

The TSC9405 common source, open drain MOS outputs sustain 15 V in the OFF state and maintain leakage currents under 100 μA. The low output ON resistance allows all 16 channels to simultaneously sink 60 mA with a saturation voltage of 0.5 V maximum and power dissipation of 480 mW. Typical power dissipation of 16 channels sinking 60 mA is only 325 mW.

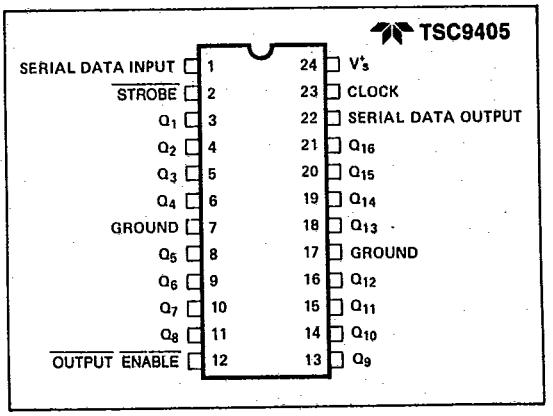
Dual rank latches and a $\overline{\text{STROBE}}$ input permit glitch-free data updating. With the $\overline{\text{STROBE}}$ input high, data is entered into master latches on each rising edge of the CLOCK input. When $\overline{\text{STROBE}}$ is brought low, data is transferred to the slave latches simultaneously. An $\overline{\text{OUTPUT ENABLE}}$ (OE) input is also included, so that all outputs can be turned off. Both $\overline{\text{STROBE}}$ and $\overline{\text{OUTPUT ENABLE}}$ are asynchronous, level-sensitive inputs.

Successive connection of serial data outputs to serial data inputs make longer length serial to parallel conversions possible. Device cascading makes the TSC9405 an ideal thermal printhead, high resolution LED bar graph, or incandescent lamp driver.

Applications

- Incandescent Lamp Driver
- Thermal Printhead Driver
- LED Bar Graph Driver
- High Current, Microprocessor Serial Port Expander
- Relay/Solenoid Driver
- Tungsten Lamp Driver
- SCR Gate Driver

Pin Configuration



ORDERING INFORMATION

Part	Package	Temp. Range	Output Voltage
TSC9405CPG	24-Pin Epoxy Dip	0°C to 70°C	15 V
TSC9405IJG	24-Pin CerDip	-25°C to 85°C	15 V
TSC9405MJG	24-Pin CerDip	-55°C to 125°C	15 V
TSC9405Y	Chip	25°C	15 V
Devices Available with MIL-STD-883 Processing			
TSC9405MJG/883	24-Pin CerDip	-55°C to 125°C	15 V

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Absolute Maximum Ratings

Supply Voltage (V^+_S to Ground) ..... 7.0 V
Digital Logic Input Voltage ..... 5.5 V
Parallel Output Drain Voltage ..... 18 V
Parallel Output Drain Current ..... 80 mA
Package Power Dissipation
CerDIP Package ..... 1 W @ 85°C
CerDIP Package ..... 0.4 W @ 125°C
Epoxy Package ..... 1 W @ 70° C

Operating Temperature
CerDIP Package (IJG) ..... -25°C ≤ T_A ≤ +85°C
CerDIP Package (MJG)..... -55°C ≤ T_A ≤ +125°C
Epoxy Package (CPG) ..... 0°C ≤ T_A ≤ +70°C
Storage Temperature ..... -65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering, 60 Sec) ..... +300°C

Electrical Charateristics

V^+_S = 5.0V, T_A
TSC9405C 0°C to +70°C
TSC9405I -25°C to +85°C
TSC9405M -55°C to +125°C

SYMBOL	PARAMETER	TEST CONDITIONS	TSC9405 MIN	TYP	MAX	UNIT
OUTPUT SECTION						
V_{SAT}	Output ON Voltage	I_O = 60 mA V^+_S = 4.75 V, T_A = 24°C (Note 2)		.25	.4	V
V_{SAT}	Output ON Voltage	I_O = 60 mA V_S = 4.75 V T_A = FULL (Note 2)			0.6	V
V_B	Output OFF Voltage				15	V
I_O	Output Sink Current	V_{SAT} ≤ 0.6 V (Note 1)	60			mA
I_{OX}	Output Leakage Current	V^+_S = 4.75 V V_B = 15 V			100	μA
INPUT SECTION						
V_{INH}	Logic "1" Input Voltage	V^+_S = 5.25 V	2.4			V
V_{INL}	Logic "0" Input Voltage	V^+_S = 5.25 V			0.8	V
I_{INH}	Logic "1" Input Current	V_{INH} = 2.4 V V^+_S = 5.25 V			40	μA
I_{INL}	Logic "0" Input Current	V_{INL} = 0.8 V V^+_S = 5.25 V			40	μA
C_{IN}	Input Capacitance	V_{IN} = 0 V		15		pF
V_{OH}	Serial Output Logic "1" Voltage	I_{OH} = 400 μA I_{OH} = 10 μA	2.4 4.5	4.7 4.98		V V
V_{OL}	Serial Output Logic "0" Voltage	I_{OL} = 3.6 mA			0.4	V

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TSC9405

TIMING SECTION						
SYMBOL	PARAMETER	TEST CONDITIONS	TSC9405 MIN	TYP	MAX	UNIT
t_{DH}	Serial Input Data Hold Time	T_A = 25°C	40	20		ns
t_{DS}	Serial Input Data Set-up Time	T_A = 25°C	50	0		ns
f_C	Clock Frequency	T_A = 25°C	3	5		MHz
t_{PW}	Clock Pulse Width	T_A = 25°C	150	100		ns
t_{PLH1}	Parallel Output Low to High Transition Time	$\overline{STROBE}$ = LOW $\overline{OE}$ = LOW Note 3 and Figure 1			300	ns
t_{PHL1}	Parallel Output High to Low Transition Time	$\overline{STROBE}$ = LOW $\overline{OE}$ = LOW Note 3 and Figure 1			300	ns
t_{PLH2}	Parallel Output Low to High Transition Time	$\overline{STROBE}$ = ↘ $\overline{OE}$ = LOW Note 3 and Figure 1			300	ns
t_{PHL2}	Parallel Output High to Low Transition Time	$\overline{STROBE}$ = ↘ $\overline{OE}$ = LOW Note 3 and Figure 1			300	ns
t_{PLHE}	Parallel Output Low to High Transition Time	$\overline{STROBE}$ = DON'T CARE $\overline{OE}$ = ↗ Note 3 and Figure 1			250	ns
t_{PHLE}	Parallel Output High to Low Transition Time	$\overline{STROBE}$ = DON'T CARE $\overline{OE}$ = ↘ Note 3 and Figure 1			250	ns
t_{SHL}	Serial Output High to Low Transition Time	I_{OL} = 3.6 mA C_L = 25 pF T_A = 25			150	ns
t_{SLH}	Serial Output Low to High Transition Time	I_{OH} = 400 μA C_L = 25 pF T_A = 25			150	ns
t_{SPW}	Strobe Pulse Width	T_A = 25°C	80			ns
SUPPLY SECTION						
V_S	Operating Supply Voltage		+4.75	+5.0	+5.25	V
I_S	Quiescent Power Supply	V^+_S = 5.25 V f_C = 0 Hz V_{INL} = 0V I_O = 0 mA Pin 22 Open		50	200	μA

Notes:
1. Maintain die temperature ≤ 150°C.
2. V_{SAT} increases by 0.1 V when all outputs are sinking 60mA due to internal ground drop and self-heating.
3. V_B = 15 V, R_L = 330 Ω, C_L = 25 pF, T_A = 25°C

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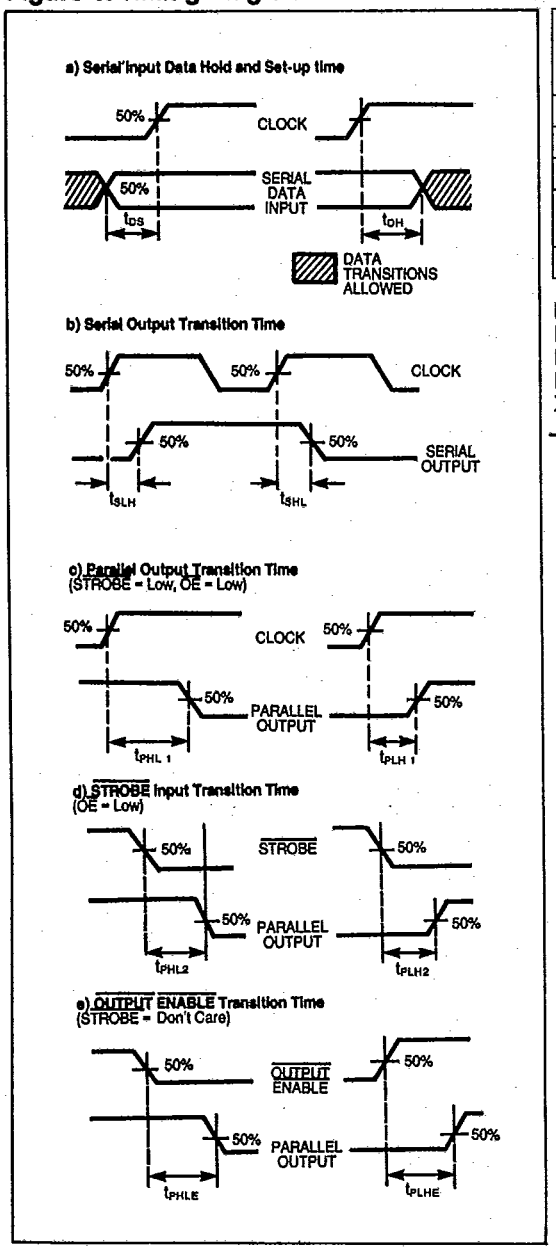
Figure 1. Timing Diagrams



Function Table

$\overline{OE}$	$\overline{STROBE}$	DATA INPUT D_N	CLOCK INPUT	PARALLEL OUTPUTS Q_1 Q_2 Q_3 ...Q_{16}
L	L	X	L	D_1 D_2 D_3 ...D_{16}
L	L	H	↗	L* D_1 D_2 ...D_{15}
L	L	L	↗	H* D_1 D_2 ...D_{15}
L	H	X	X	MAINTAINS LAST VALID STATE
H	X	X	X	H* H* H* H*

L = Logic 0
H = Logic 1
L* = Output NMOS ON
H* = Output NMOS OFF
X = Don't Care
↗ = Transition from Low to High
D_1, D_2, ...D_{16} = Data Outputs before the low-to-high transition of the clock.

NOTE: $\overline{OE}$ and $\overline{STROBE}$ inputs are level sensitive, not edge-triggered.

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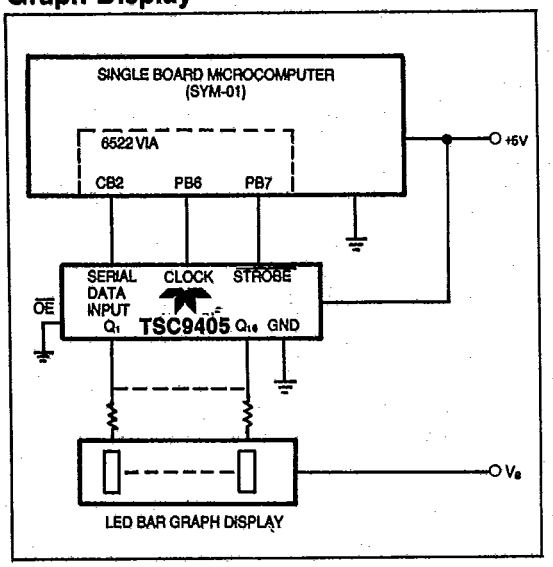
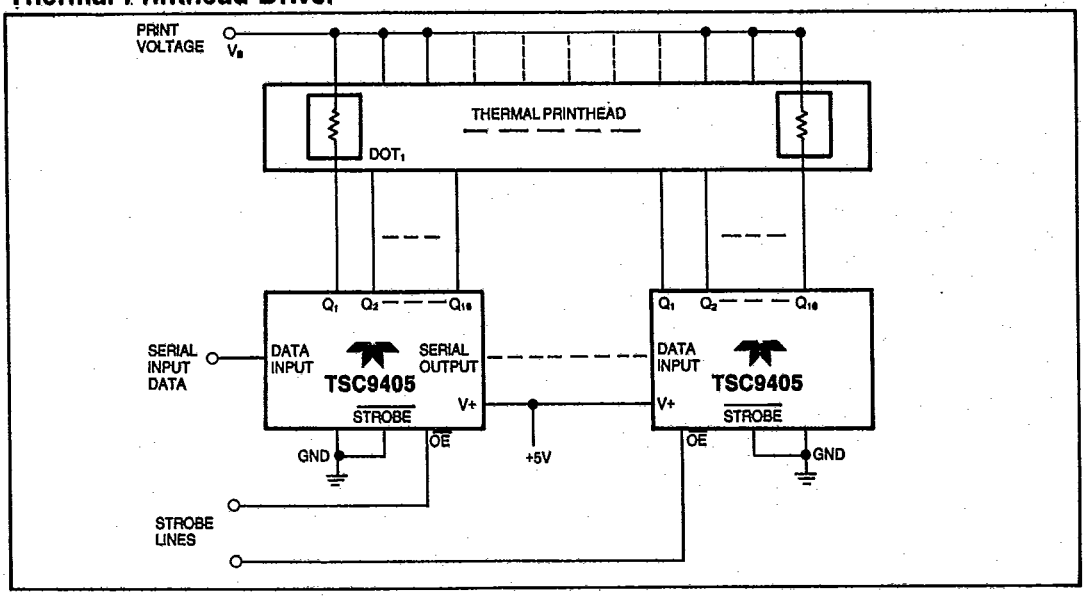
TSC9405

APPLICATIONS

Microprocessor Controlled LED Bar Graph Display



Thermal Printhead Driver



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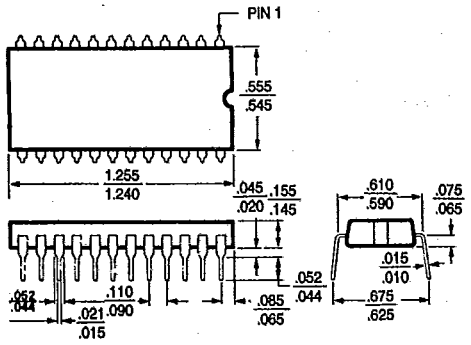
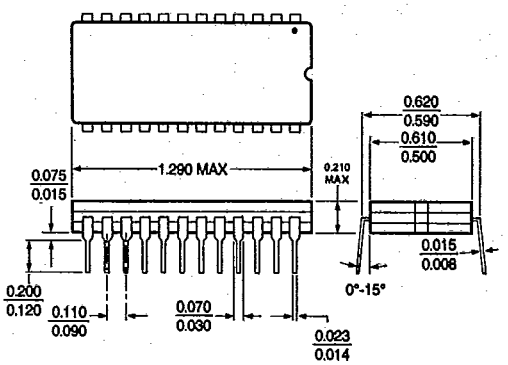
Package Outline

P Package
Plastic Dip
(Package #12)



J Package
CerDIP
(Package #14)



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Bonding Diagram