S5X433CA03-20R0
(1/4” VGA CIS Camera Module)

Preliminary Specification

Revision 2.3.3

Apr. 2003

DOCUMENT TITLE

1/4" Optical Size 640x480 (VGA) CIS Camera Module

REVISION HISTORY

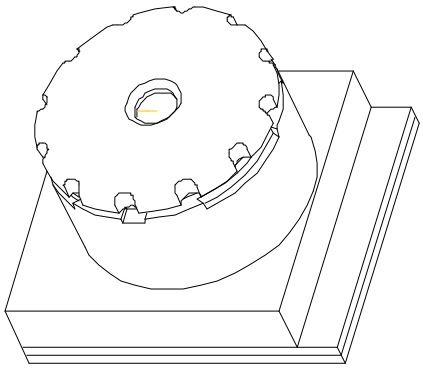
Revision No.	History	Draft Date	Remark
0.0	Initial draft	Sep. 17, 2001	Preliminary
1.0	Changed mechanical dimension	Mar. 25, 2002	Preliminary
2.0	Changed I/O pin diagram and mechanical dimension	Sep. 2, 2002	Preliminary
2.1	Fixed some bugs and changed timing characteristics	Sep. 14, 2002	Preliminary
2.2	Fixed some bugs	Jan. 24, 2003	Preliminary
2.3	Changed optical and timing characteristics	Feb. 19, 2003	Preliminary
2.3.2	Fixed some bugs	Mar. 14, 2003	Preliminary
2.3.3	Fixed some bugs and changed supply current	Apr. 4, 2003	Preliminary

INTRODUCTION

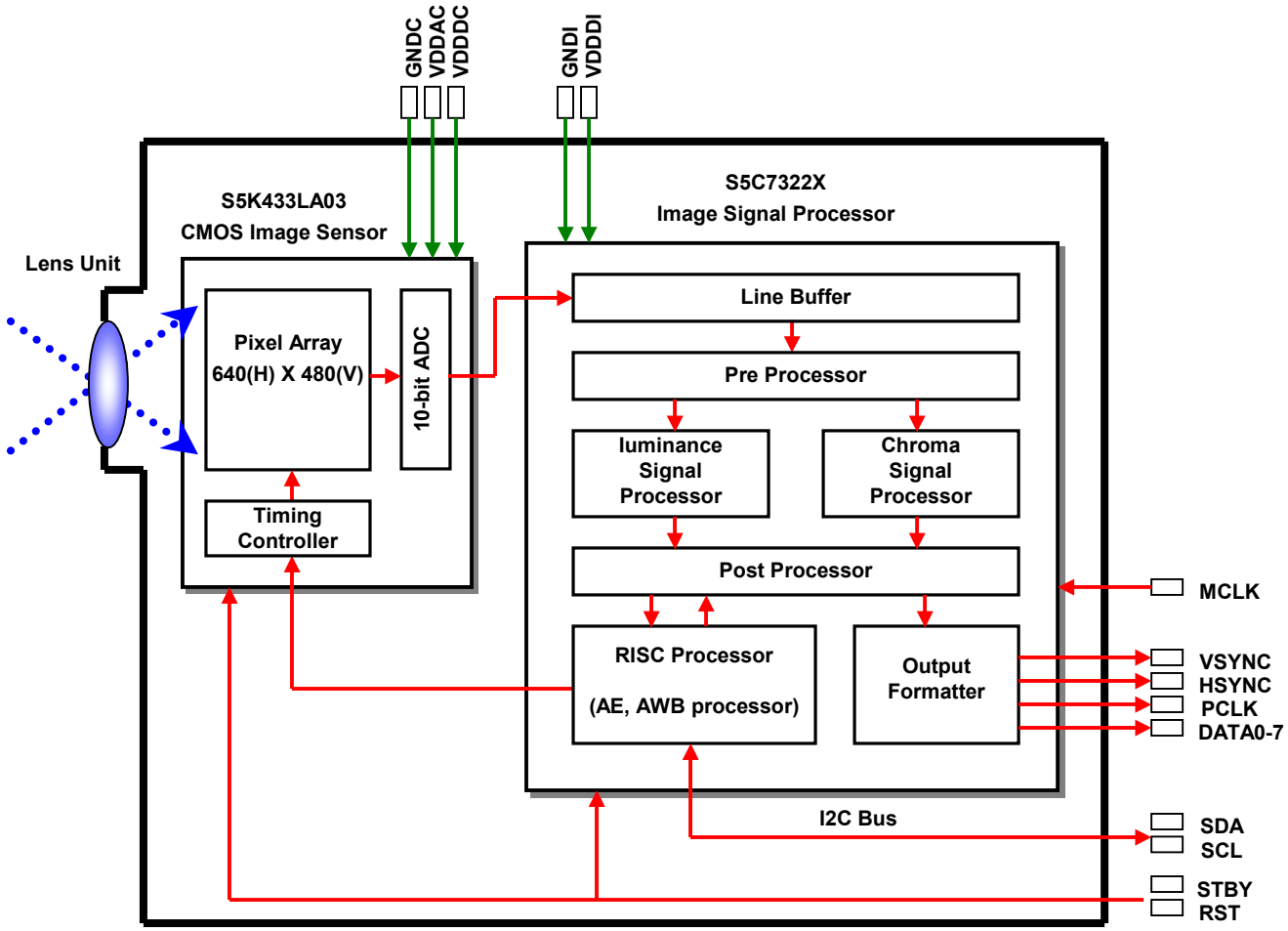
The S5X433CA03-20R0 is fully functional camera module with embedded lens. A low-noise low-power color CMOS image sensor, S5K433LA03 and an image signal processor, S5C7322X produce high-quality digital video output including CCIR656 format with maximum 30 frames per second for full frame readout. The CMOS image sensor, fabricated by SAMSUNG 0.35μm CMOS image sensor process technology which is dedicated to higher-sensitivity and lower-dark level compared to standard CMOS process technology and on-chip CDS and 10-bit column ADC circuit makes high signal-to-noise ratio with low power consumption. The image sensor, signal processor and some passive components are packed with IR-cut filter and lens units to have very small volume of whole camera system. It needs only 2.8V single power supply and a main clock supplied to operate. All the function can be controlled by control register setting through the standard 2-wire serial interface.

FEATURES

- Optical Size: 1/4 inch
- Unit Pixel: 5.6 μm X 5.6 μm
- Effective Resolution: 640X480, VGA
- 8.5mm X 9.5mm X 6.6mm module size
- 8-bit CCIR656 (YCrCb) Video Output
- VGA Output Capability
- Programmable Gamma Correction
- Auto White Balance and Auto Exposure Control
- Horizontal and/or Vertical Mirror Output
- Standby-Mode for Power Saving
- Maximum 30 Frame per Second
- Single Power Supply Voltage: 2.8V
- I^2C Type Control Interface



BLOCK DIAGRAM



OPTICAL CHARACTERISTICS

Characteristic	Value
Optical format	1/4 inch
Effective resolution	640 (H) X 480 (V), VGA
Unit pixel size	5.6μm (H) X 5.6μm (V), square pixel
Minimum object illumination(1)	5 lux
Lens construction	Dual plastic ASP lens
Field of view in horizontal, vertical, and diagonal direction	57° (H), 44° (V), 68° (D)
Effective focal length	f = 3.385mm
Aperture	F = 2.8
TV distortion	-0.32%
Full field distortion	-1.76 %
MTF at center	60% at 80 lp/mm
MTF at 0.7 field	22% at 80 lp/mm
Depth of field	20 cm ~ ∞
Optical track	5.0mm

NOTES:
1. 25 IRE in NTSC converted with white of gray scale chart, 30 FPS @24.54MHz operation.

IO PIN DESCRIPTION

(Connector type and pin numbers can be changed as customer's request.)

Module Pad	Connector Pin	Pin Name	Type	Notation
1	9	VDDDI	Power	Power supply for signal processor (digital)
2	10	GNDI	Power	Ground for signal processor
3	15	SCL	In / Out	I^2C serial communication clock
4	16	SDA	In / Out	I^2C serial communication data
5	11	RST	In	Reset control (active low)
6	12	STBY	In	Standby mode control (active low)
7	20	MCLK	In	Master input clock
8	17	VSYNC	Out	Vertical synchronization clock
9	18	HSYNC	Out	Horizontal synchronization clock
10	19	PCLK	Out	Pixel output clock
11	8	DATA0	Out	8-bit digital video output
12	7	DATA1	Out	
13	6	DATA2	Out	
14	5	DATA3	Out	
15	4	DATA4	Out	
16	3	DATA5	Out	
17	2	DATA6	Out	
18	1	DATA7	Out	
19	13	GNDC	Power	Ground for sensor circuit block
20	14	VDDDC	Power	Power supply for sensor digital circuit block
21	14	VDDAC	Power	Power supply for sensor analog circuit block

MAXIMUM ABSOLUTE RATINGS

Characteristic	Symbol	Rating	Unit
Maximum supply voltage (VDDDI, VDDAC, VDDC supply relative to GNDI, GNDC)	V_{DD}	-0.3 to 3.8	V
DC Input voltage	V_{IN}	-0.3 to V_{DD}+0.3 (Max. 3.8)	
Operating temperature	T_{OPR}	-20 to +60	°C
Storage temperature	T_{STG}	-30 to +85	

ELECTRICAL CHARACTERISTICS

DC Characteristics

(T_A = -20 to +60°C, C_L = 15pF)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Operating voltage	V_{DD}	VDDDI, VDDAC, VDDC	2.55	2.8	3.05	V
Input voltage (1)	V_{IH}	-	2.0	-	-	V
	V_{IL}	-	-	-	0.8	
Input leakage current(1)	I_{IL}	V_{IN} = V_{DD} to V_{SS}	-10	-	10	µA
High Level Output voltage	V_{OH}	I_{OH} = -4mA(2)	0.8V_{DD}	-	-	V
		I_{OH} = -8mA(3)				
Low Level Output voltage	V_{OL}	I_{OL} = 4mA(2)	-	-	0.2V_{DD}	
		I_{OL} = 8mA(3)				
High-Z output leakage current (4)	I_{OZ}	V_{OUT} = V_{DD}	-	-	10	µA
Supply current	I_{STB}	STBYN = Low (active) All input clocks = Low	-	-	TBD	µA
	I_{DD}	f_{MCLK} = 12.0MHz, 15 fps	-	30	TBD	mA

NOTES:

1. MCLK, RST, STBY, SCL, and SDA pin.
2. HSYNC, VSYNC, SCL, and SDA pin
3. PCLK, DATA0 to DATA7 pin
4. SCL and SDA pin when in High-Z output state

Sensor Imaging Characteristics

(Light source with 3200K of color temperature and IR cut filter (CM-500S, 1mm thickness) is used. Electrical operating conditions follow the recommended typical values. The control registers are set to the default values. The ambient temperature, T_A is 25°C if not specified.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Saturation level(1)	V_{SAT}		850	900	-	mV
Sensitivity (G)(2)	S		-	2000	-	mV/lux sec
Dark level(3)	V_{DARK}	T_A = 40°C	-	9	18	mV/sec
		T_A = 60°C	-	50	100	
Dynamic range(4)	DR		-	60	-	dB
Signal to noise ratio(5)	S/N		-	40	-	
Dark signal non-uniformity(6)	DSNU	T_A = 60°C	-	-	100	mV/sec
Photo response non-uniformity(7)	PRNU		-	4	8	%
Vertical fixed pattern noise(8)	VFPN			4	8	%
Horizontal fixed pattern noise(9)	HFPN			4	8	%

NOTES:

1. Measured minimum output level at 100lux illumination for exposure time 1/30 sec. 7X7 rank filter is applied for the whole pixel area to eliminate the values from defective pixels.
2. Measured average output at 25% of saturation level illumination for exposure time 1/30 sec. Green channel output values are used for color version.
3. Measured average output at zero illumination without any offset compensation for exposure time 1/30 sec.
4. 20 log (saturation level/ dark level RMS noise excluding fixed pattern noise). 10-bit ADC limits 60dB.
5. 20 log (average output level/RMS noise excluding fixed pattern noise) at 25% of saturation level illumination for exposure time 1/30 sec.
6. Difference between maximum and minimum pixel output levels at zero illumination for exposure time 1/30 sec. 7X7 median filter is applied for the whole pixel area to eliminate the values from defective pixels.
7, Difference between maximum and minimum pixel output levels divided by average output level at 25% of saturation level illumination for exposure time 1/30 sec. 7X7 median filter is applied for the whole pixel area to eliminate the values from defective pixels.
8. For the column-averaged pixel output values, maximum relative deviation of values from 7-depth median filtered values for neighboring 7 columns at 25% of saturation level illumination for exposure time 1/30 sec.
9. For the row-averaged pixel output values, maximum relative deviation of values from 7-depth median filtered values for neighboring 7 columns at 25% of saturation level illumination for exposure time 1/30 sec.

AC Characteristics

(V_{DD} = 2.55V to 3.05V for S5K433LA, Ta = -20 to + 60 °C, C_L = TBD pF, 15FPS)

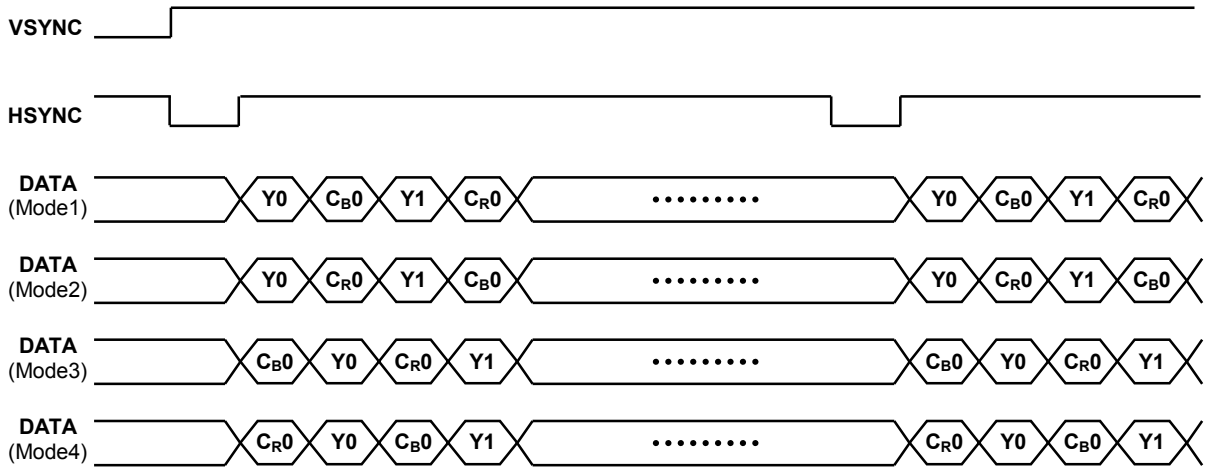
Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Main input clock frequency	f_{MCLK}	Duty = 50%	3	24.54	30	MHz

OUTPUT IMAGE MODE

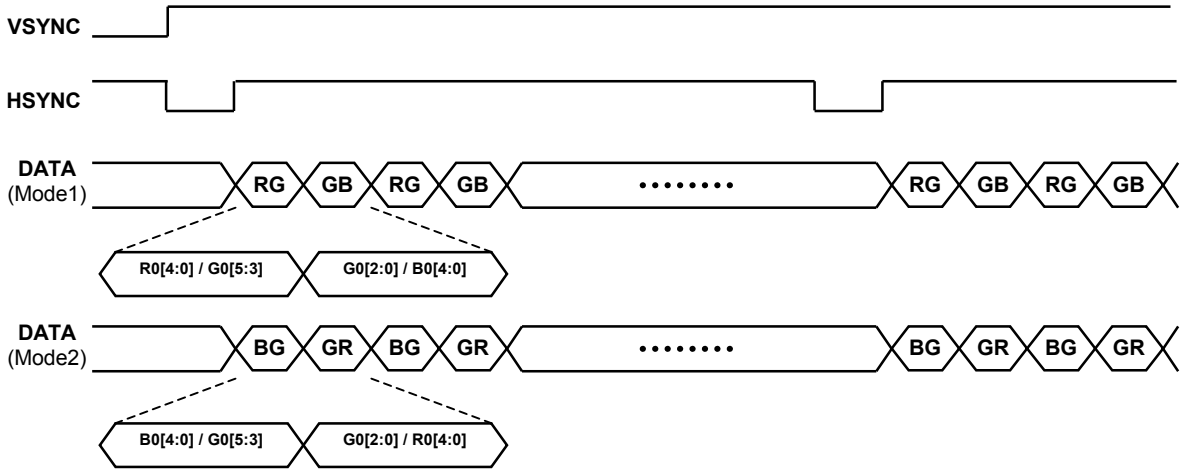
No.	Mode	Resolution (H X V)	Data rate (PCLK)	Zoom	Frame rate with MCLK=24.54MHz
1	VGA	640X480	**MCLK**	-	30 FPS
2	QVGA	320X240	**MCLK**	-	30 FPS

OUTPUT DATA FORMAT

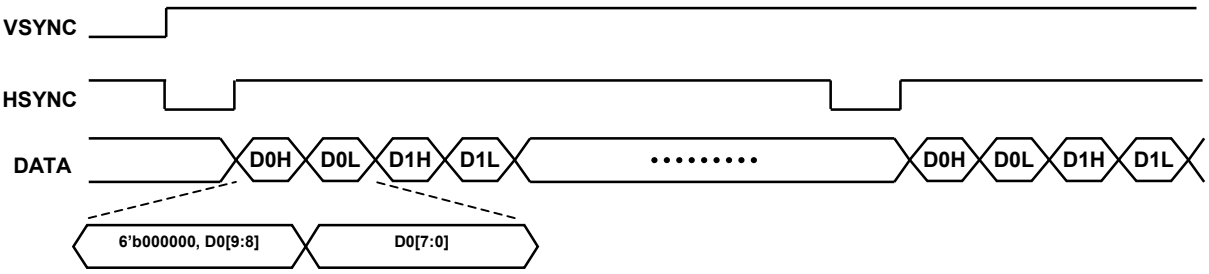
YC_RC_B 4:2:2 FORMAT



RGB565 FORMAT



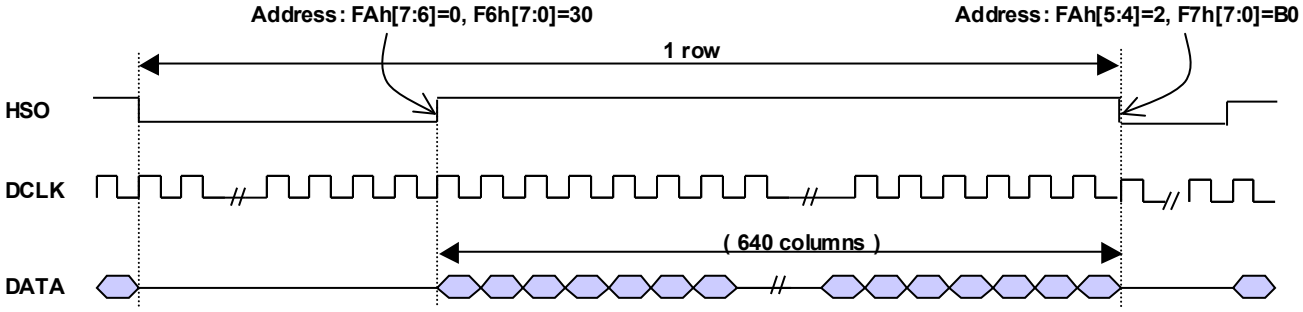
SENSOR RAW IMAGE (BAYER MOSAIC PATTERN) FORMAT



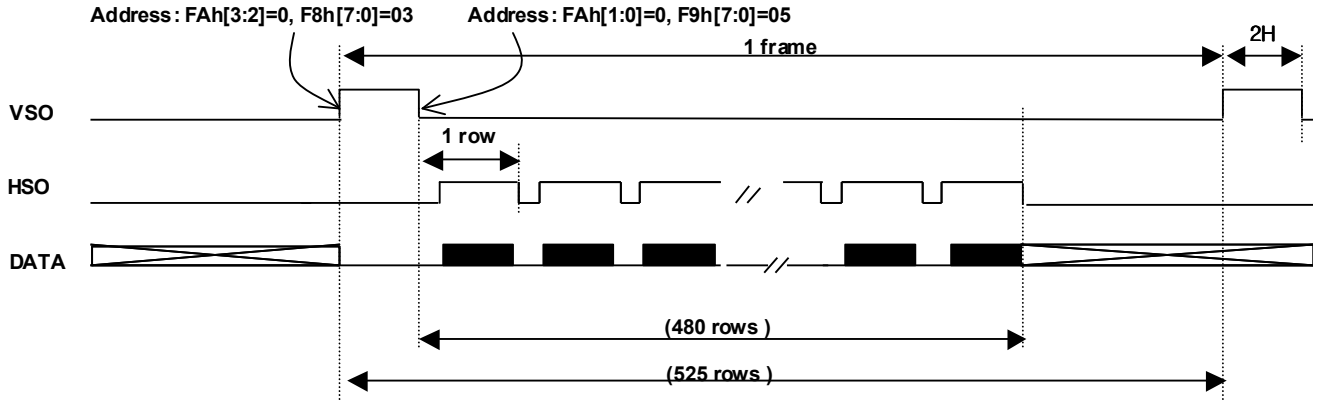
SAMSUNG ELECTRONICS

OUTPUT TIMING DIAGRAMS

HORIZONTAL TIMING



VGA OUTPUT TIMING



NOTES:

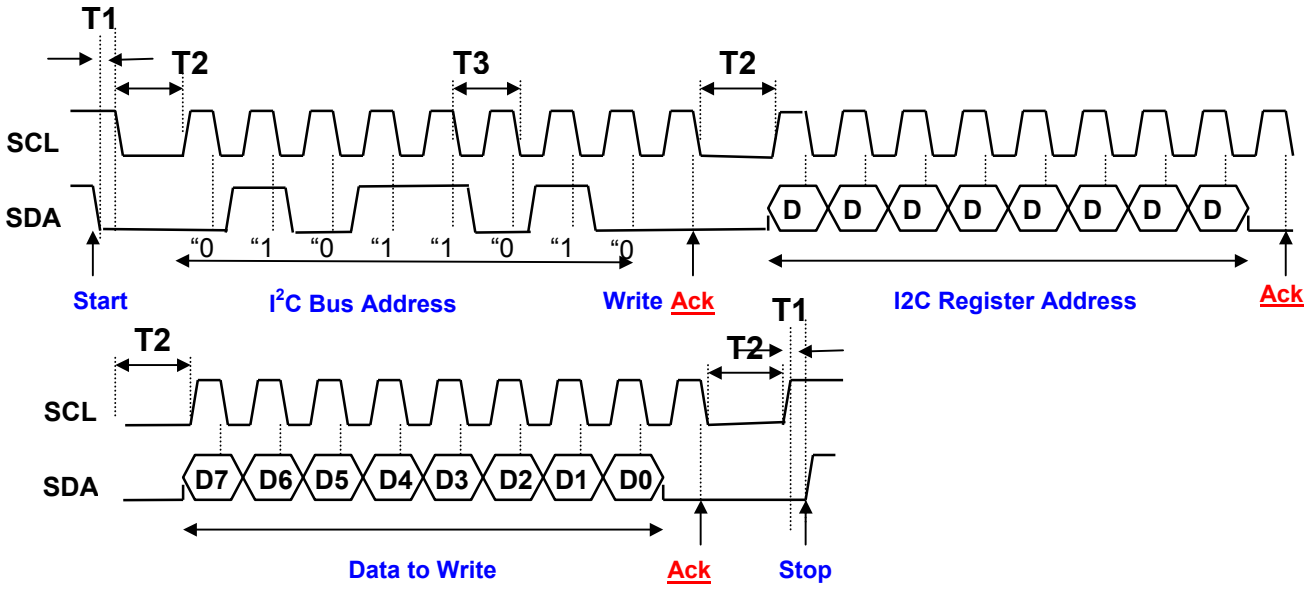
1. Falling and rising time of HSO and VSO can be controlled by register settings.
2. Each default value of rising and falling time control registers is described in the diagram above.

IMAGE PROCESSING FUNCTIONS

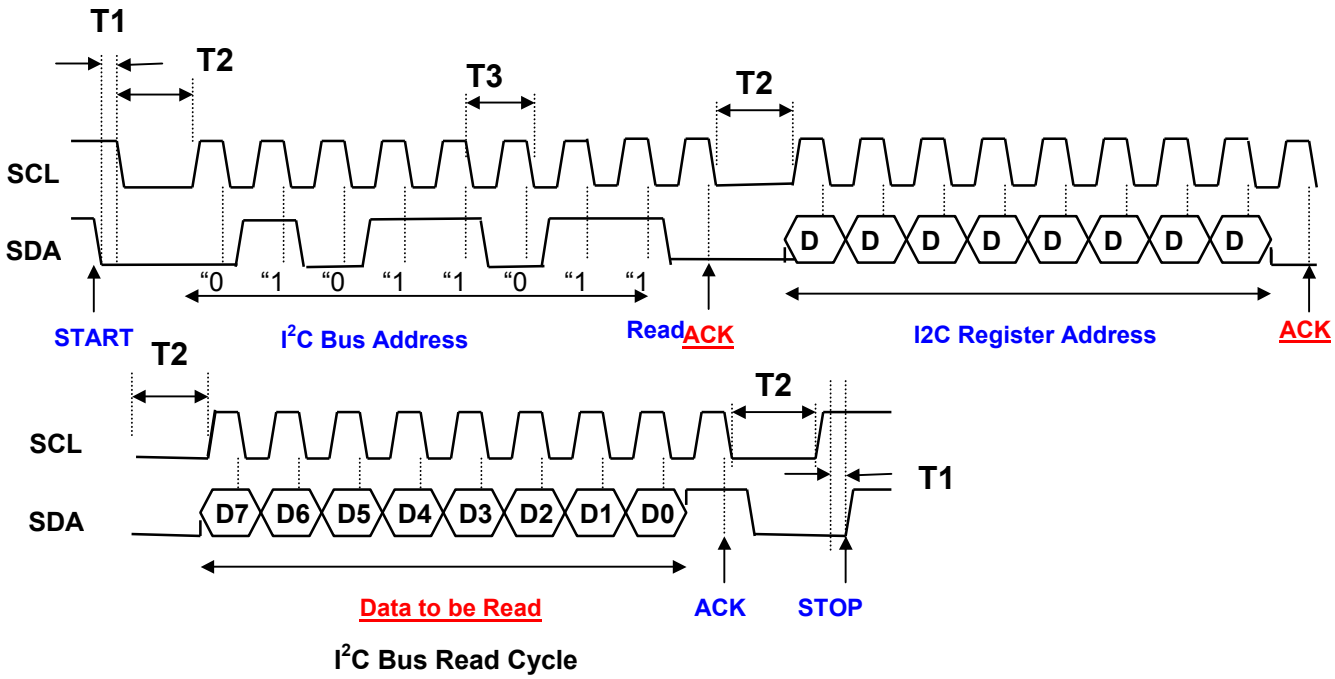
Function	Description	Remarks
Defect detection and correction	If enabled, the defective pixels are detected by comparing its level with horizontally neighboring pixels and replaced by the averaged value of neighboring pixels.	
De-mosaic	The sensor produces one color component from a pixel according to Bayer color filter array. The de-mosaic function performs color interpolation to produce all three-color components at each pixel location.	
Color correction	The spectral response of image sensor is not same to that human eye. To match the spectral response, the sensor output components are pivoted by user programmable 3X3 matrix production.	
Gamma correction	Gamma correction translating the linear response of the sensor into the non-linear characteristics of the display. To make a non-linear conversion, a piecewise linear approximation method based on user programmable lookup table is used.	
Horizontal mirror	The output image can be mirrored in horizontal direction.	
Vertical mirror	The output image can be mirrored in vertical direction.	
Edge enhancement	Enhancing the edge component can attain a clear output image. To perform the edge enhancement function, horizontal and vertical edge detecting and enhancing is processed.	
Auto exposure	According to the incident light level, the auto exposure function controls the sensor gain and effective integration time to maintain the proper output level. Setting the control registers can change the sensing area used in the AE algorithm.	
Auto white balance	The auto white balance function adjusts the gain of the sensor's red and blue channels relative to the green channel to compensate the spectral unbalancing of the light source. Setting the control registers can change the sensing area used in the AWB algorithm.	
Output format conversion	4 types of output format are available. (CCIR656 format, CCIR601 format, RGB format and sensor raw image output format)	
Sub-sampling Control	The user can read out the pixel data in sub-sampling rate in both horizontal and vertical direction. Sub-sampling can be done in two rates: full and 1/2. The user controls the sub-sampling using the Sub-sampling Control Registers, **subsr** and **subsc**. The sub-sampling is performed only in the Bayer space.	

I²C SERIAL INTERFACE

The I²C contains a serial two-wire half duplex interface that features bi-directional operation, master or slave mode. The general **SDA** and **SCL** are the bi -directional data and clock pins, respectively. These pins are open-drain type ports and will require a pull-up resistor to VDD. The image sensor operates in salve mode only and the **SCL** is input only. The I²C bus interface is composed of following parts: START signal, 7-bit slave device address (0101101Xb) transmission followed by a read/write bit, an acknowledgement signal from the slave, 8-bit data transfer followed by an acknowledgement signal and STOP signal. The **SDA** bus line may only be changed while **SCL** is low. The data on the **SDA** bus line is valid on the high-to-low transition of **SCL**



I²C Bus Write Cycle



I²C Bus Read Cycle

Main Clock - 13.5MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Hold time START condition	T1	-	10	32	μsec
Low period of SCL clock	T2	100	110	-	μsec
Clock period	T3	100	110	-	μsec
Bus free time between a STOP and START condition	T_{BUF}	4	6	-	msec

NOTES:

1. The basic frequency of main clock is 13.5MHz for all the followed comments.
2. If you don't have ACK signal on the way of communications through I²C, it means that I²C error is generated.
3. If you have any I²C error, try again after 2VSYNC (The I²C error is reset every 2VSYNC automatically).
4. If any error is not generated till one command is completed, you can transfer another after 4msec
5. The time value of T1, T2, T3, and T_{BUF} is proportional to the change of MCLK.
6. I²C Bus read format is different from I²C standard format.

I²C REGISTER MAP

Address	Chip ID	Item
0x00 - 0x2B	CIS	CIS control register
0x2C - 0x70	CalmRISC	PROGRAM CONSTANT
0x71 - 0x7F		COMMAND LIST
0x80 - 0xFF	ISP	ISP control register

MODULE REGISTER MAP

CIS CONTROL REGISTER MAP

Default Value: Frame size(858x504), Main Clock(19.2MHz), Frame Speed(22fps)					The latest Image tuning
Address	**Control Register**	**Bits**	**Descriptions**	**Default**	**Initial Value**
00h		[5] [4] [3] [2] [1:0]	[5] bprm 0b (disabled) 1b (enabled) [4] dlcm ccsm shutc adcres	06h	
01h		[7] [6] [5:4] [3:2] [1:0]	mircv mirch mcdiv subsr subsc	10h	
02h	wrp_high	[0]	Row start point for window of interest	00h	
03h	wrp_low	[7:0]	Row start point for window of interest	0Eh	
04h	wcp_high	[0]	Column start point for window of interest	00h	
05h	wcp_low	[7:0]	Column start point for window of interest	0Eh	
06h	wrd_high	[0]	Row depth for window of interest	01h	
07h	wrd_low	[7:0]	Row depth for window of interest	E8h	
08h	wcw_high	[1:0]	Column width for window of interest	02h	
09h	wcw_low	[7:0]	Column width for window of interest	90h	
0Ah	offsdef	[7:0]	(Factory use only) Analog offset reference	80h	
0Bh	sfcen	[3]	Single frame capture enable 0b: disabled (default), 1b: enabled	02h	
	sint_high	[2:0]	Integration time in single frame capture mode		
0Ch	sint_low	[7:0]	Integration time in single frame capture mode	0Dh	
0Dh	cintr_high	[3:0]	Row-step integration time in continuous frame capture mode	01h	
0Eh	cintr_low	[7:0]	Row-step integration time in continuous frame capture mode	00h	
0Fh	cintc_high	[4:0]	Column-step integration time in continuous frame capture mode	02h	
10h	cintc_low	[7:0]	Column-step integration time in continuous frame capture mode	92h	
11h	vswd	[7:0]	VSYNC width	02h	
12h	vspolar	[5]	VSYNC polarity 0: active high (default), 1: active low	00h	
	vsdisp	[4]	VSYNC display mode 0: sync mode (default), 1: data valid mode		
	vsstrt_high	[1:0]	VSYNC start position		
13h	vsstrt_low	[7:0]	VSYNC start position	00h	
14h	vblank_high	[3:0]	Vertical blank depth	00h	
15h	vblank_low	[7:0]	Vertical blank depth	10h	
16h	hswd	[7:0]	HSYNC width	20h	
17h	hspolar	[5]	HSYNC polarity 0: active high (default), 1: active low	00h	
	hsdisp	[4]	HSYNC display mode 0: sync mode (default), 1: data valid mode		
	hsstart_high	[1:0]	HSYNC start position		
18h	hsstart_low	[7:0]	HSYNC start position	00h	
19h	hblank_high	[5:0]	Horizontal blank depth	00h	
1Ah	hblank_low	[7:0]	Horizontal blank depth	CAh	
1Bh	sgg1	[3:0]	1st sectional global gain	77h	AAh
	sgg2	[7:4]	2nd sectional global gain		
1Ch	sgg3	[3:0]	3rd sectional global gain	77h	AAh
	sgg4	[7:4]	4th sectional global gain		
1Dh	pgcr	[6:0]	Red channel gain	00h	
1Eh	pgcg1	[6:0]	Green(Red row) channel gain or all channel gain (ccsm=0) pgcg1[6:0] = 0d (default)	00h	
1Fh	pgcg2	[6:0]	Green(Blue row) channel gain	00h	
20h	pgcb	[6:0]	Blue channel gain	00h	
21h	offsr	[7:0]	Red channel analog offset	80h	
22h	offsg1	[7:0]	Green(Red row) channel analog offset or all channel offset (ccsm=	80h	
23h	offsg2	[7:0]	Green(Blue row) channel analog offset	80h	
24h	offsb	[7:0]	Blue channel analog offset	80h	
25h	pthresh	[7:0]	Bad pixel threshold	14h	
26h	adcoffs	[7:0]	ADC offset	06h	19h
2Dh	FrameRate_Start		FrameRate_Start of AgcValue The point of AGC at which Frame Rate AE starts to operate.	5Ah	
2Eh	WB Manual Step		auto mode White Step move 0 : nothing plus : toward 3100 minus : toward 5100	00h	
2Fh	ISP version	[7:0]	isp version (read only)	09h	

CalmRISC CONTROL REGISTER MAP

Address	Control Register	Bits	Descriptions	Default	Initial Value
30h	WBMODE	[7:0]	00h : AWB auto mode 01h : Indoor 3100 mode (Tungsten) 02h : Outdoor 5100 mode (Fluorescent) 03h : Indoor 2000 mode 04h : AE/AWB halt 05h : Cloudy (6000) Rgain_out = WBR5100 + Radj + Cloudy R offset Bgain_out = WBB5100 + Radj - Cloudy B offset 06h : Sunny (8000) Rgain_out = WBR5100 + Radj + Sunny R offset Bgain_out = WBB5100 + Radj - Sunny B offset	00h	
31h	WB_Yellow_tr	[7:0]	Distance Values Of Yellow Decision	20h	
32h	WB_PIXEL_CNT	[7:0]	Pixel Minimum Counter Values Of White Detection	FFh	
33h	WB8000	[7:0]	AWB Tracking Boundary Constant	70h	
34h	Rgain_Max	[7:0]	AWB Tracking Boundary Constant	10h	
35h	Bgain_Max	[7:0]	AWB Tracking Boundary Constant	10h	
36h	R_LimitHigh	[7:0]	AWB Tracking Boundary Constant	05h	
37h	B_LimitHigh	[7:0]	AWB Tracking Boundary Constant	05h	
38h	R_LimitLow	[7:0]	AWB Tracking Boundary Constant	05h	
39h	B_LimitLow	[7:0]	AWB Tracking Boundary Constant	08h	
3Ah	SlopeBottom	[7:0]	AWB Tracking Boundary Constant	08h	
3Bh	SlopeTop	[7:0]	AWB Tracking Boundary Constant	0Ch	
3Ch	Ydepth	[7:0]	Y_Depth Values Of White Detection	18h	
3Dh	Y_Max	[7:0]	Y Max level Limit Values Of White Detection	E0h	
3Eh	Y_Min	[7:0]	Y Min level Limit Values Of White Detection	60h	
3Fh	Shutter_TR	[7:0]	Shutter Values Of AWB Tracking	08h	
40h	WBR2000	[7:0]	Indoor 2000 R	22h	
41h	WBB2000	[7:0]	Indoor 2000 B	3Ah	
42h	WBR3100	[7:0]	Indoor 3100 R	25h	
43h	WBB3100	[7:0]	Indoor 3100 B	35h	
44h	WBR5100	[7:0]	Outdoor 5100 R	2Fh	
45h	WBB5100	[7:0]	Outdoor 5100 B	2Ah	
46h	Cintc_Stable_Area		Cintc_Stable_Area Stable when AE difference is below (N)*2 at the point of Cintc AE.	80h	
47h	OUTDOOR_CINTCAE	[7:0]	BIT0: CINTC Shutter On (1:On 0:Off) BIT1: AWB Tracking Compare with AE (1:On 0:Off) BIT2: Max AE Expand (1:On 0:Off)	07h	
48h	R-Y POSI GAIN(2000)	[7:0]	R-Y Positive Gain Coefficient of R-Y Signal(2000)	A0h	C0h
49h	R-Y NEGA GAIN(2000)	[7:0]	R-Y Negative Gain Coefficient of R-Y Signal(2000)	68h	
4Ah	R-Y HUE POSI GAIN(2000)	[7:0]	R-Y Positive Hue Coefficient of R-Y Signal(2000)	C0h	
4Bh	R-Y HUE NEGA GAIN(2000)	[7:0]	R-Y Negative Hue Coefficient of R-Y Signal(2000)	50h	
4Ch	B-Y POSI GAIN(2000)	[7:0]	B-Y Positive Gain Coefficient of B-Y Signal(2000)	A0h	
4Dh	B-Y NEGA GAIN(2000)	[7:0]	B-Y Negative Gain Coefficient of B-Y Signal(2000)	97h	
4Eh	B-Y HUE POSI GAIN(2000)	[7:0]	B-Y Positive Hue Coefficient of B-Y Signal(2000)	10h	
4Fh	B-Y HUE NEGA GAIN(2000)	[7:0]	B-Y Negative Hue Coefficient of B-Y Signal(2000)	40h	
50h	R-Y POSI GAIN(INDOOR)	[7:0]	R-Y Positive Gain Coefficient of R-Y Signal(INDOOR)	A0h	C0h
51h	R-Y NEGA GAIN(INDOOR)	[7:0]	R-Y Negative Gain Coefficient of R-Y Signal(INDOOR)	68h	
52h	R-Y HUE POSI GAIN(INDOOR)	[7:0]	R-Y Positive Hue Coefficient of R-Y Signal(INDOOR)	D0h	
53h	R-Y HUE NEGA GAIN(INDOOR)	[7:0]	R-Y Negative Hue Coefficient of R-Y Signal(INDOOR)	60h	
54h	B-Y POSI GAIN(INDOOR)	[7:0]	B-Y Positive Gain Coefficient of B-Y Signal(INDOOR)	A0h	
55h	B-Y NEGA GAIN(INDOOR)	[7:0]	B-Y Negative Gain Coefficient of B-Y Signal(INDOOR)	98h	
56h	B-Y HUE POSI GAIN(INDOOR)	[7:0]	B-Y Positive Hue Coefficient of B-Y Signal(INDOOR)	10h	
57h	B-Y HUE NEGA GAIN(INDOOR)	[7:0]	B-Y Negative Hue Coefficient of B-Y Signal(INDOOR)	40h	
58h	R-Y POSI GAIN(OUTDOOR)	[7:0]	R-Y Positive Gain Coefficient of R-Y Signal(OUTDOOR)	A0h	C0h
59h	R-Y NEGA GAIN(OUTDOOR)	[7:0]	R-Y Negative Gain Coefficient of R-Y Signal(OUTDOOR)	68h	
5Ah	R-Y HUE POSI GAIN(OUTDOOR)	[7:0]	R-Y Positive Hue Coefficient of R-Y Signal(OUTDOOR)	F0h	
5Bh	R-Y HUE NEGA GAIN(OUTDOOR)	[7:0]	R-Y Negative Hue Coefficient of R-Y Signal(OUTDOOR)	48h	
5Ch	B-Y POSI GAIN(OUTDOOR)	[7:0]	B-Y Positive Gain Coefficient of B-Y Signal(OUTDOOR)	90h	
5Dh	B-Y NEGA GAIN(OUTDOOR)	[7:0]	B-Y Negative Gain Coefficient of B-Y Signal(OUTDOOR)	A8h	
5Eh	B-Y HUE POSI GAIN(OUTDOOR)	[7:0]	B-Y Positive Hue Coefficient of B-Y Signal(OUTDOOR)	10h	
5Fh	B-Y HUE NEGA GAIN(OUTDOOR)	[7:0]	B-Y Negative Hue Coefficient of B-Y Signal(OUTDOOR)	40h	

Address	Control Register	Bits	Descriptions	Default	Initial Value
60h	Sensor	[7:0]	BIT[2:0]: SENSOR SIZE 0 - VGA (640 x 480) 5 - CIF (352 x 288) BIT3: VCK_INV BIT4: STRB Low	08h	
61h	Alpha_AEWindow	[7:0]	Weighting Values Of AE Center Window	02h	
62h	AESUM_80	[7:0]	YGain Graph constant	50h	
63h	AESUM_50	[7:0]	YGain Graph constant	32h	
64h	AESUM_30	[7:0]	YGain Graph constant	1Eh	
65h	IIC Speed Register	[7:0]	bRegIICPS	80h	04h
66h	AE_Unstable_Count	[7:0]	AE_Unstable_Count Unstable when (N) consecutive AE Unstable values come.	08h	
67h	AE_Agc_Stop_Sub	[7:0]	AE_Agc_Stop_Sub For debugging	10h	
68h	DCLP_1	[7:0]	Output First Values Of DCLMP Function	04h	
69h	DCLP_2	[7:0]	Output Second Values Of DCLMP Function	08h	
6Ah	DCLP_max	[7:0]	Output Third Values Of DCLMP Function	10h	
6Bh	YGAIN_max	[7:0]	Output Max Values Of Y_Gain Function	E0h	
6Ch	AeTarget_Low	[7:0]	AE Target Low	D0h	A0h
6Dh	AeTarget_High	[7:0]	AE Target High	01h	
6Eh	Shutter_Inc	[7:0]	Adaptive Shutter Control Values	10h	
6Fh	Shutter_Stable_Range	[7:0]	Stable Decision Values Of Shutter	15h	
70h	OutDoorInput	[7:0]	AE/AWB Outdoor Initial Setting(00h:SET)	FFh	
71h	Stanby_Mode	[7:0]	AAh :Stand-by Mode On Others : Nothing	00h	
72h	Main Clock	[7:0]	00h : 27Mhz 01h : 13.5Mhz Others : Main Clock integer Ex) 24Mhz 240(dec) => F0h	C0h	
73h	Frame_AE_Mode	[1:0] [7:4]	BIT0 : 0 Frame AE Mode Off 1 Frame AE Mode On BIT1 : 0 30 frame 1 15 frame BIT[7:4] : VBlankMax calculation for Frame AE (N) : VBlankMax = VBlank_init + N * VSize ex) 2 : VBlankMax = VBlank_init + 2 * Vsi	21h	11h
74h	Flicker		BIT2 : 0 - manual 50Hz Off 1 - manual 50Hz On BIT3 : 0 - manual 60Hz Off 1 - manual 60Hz On (prior to BIT2)	01h	
75h	Mirror	[2:0]	01h-Vertical mirror 02h-Horizontal mirror 03h-Symmetric mirror 04h-right_bottom 05h-left_top(default) 06h-left_bottom 07h-right_top	00h	
76h	Brightness	[7:0]	00h~7Fh	40h	58h
77h	Color_Level	[5:0]	00h~64h	20h	28h
78h	AGC_MAX	[7:0]	00h~7Fh	70h	
79h	WhiteBalance R Control	[7:0]	80h~7Fh (-128~127)	02h	
7Ah	WhiteBalance B Control	[7:0]	80h~7Fh (-128~127)	03h	
7Bh	AE,AWB Program Speed	[7:0]	00h(Fastest) ~ FEh(Slowest) FFh : AE, AWB Skip	00h	
7Ch	AWB Tracking Speed	[7:0]	AWB Execution Values Per Vsync	01h	06h
7Dh	AE Tracking SPEED	[7:0]	AE Execution Values Per Vsync	00h	
7Eh	Digital Clamp,Y_gain	[1:0]	bit0 : 0 - Digital Clamp Off 1 - Digital Clamp On bit1 : 0 - Y_gain Off 1 - Y_gain On bit2 : 0 - C_gain Off 1 - C_gain On On/Off of Color Suppress bit3 : 0 - bprm auto function Off 1 - bprm auto function On On/Off of the automatic setting of bprm from the point of 2/3 of AGC_MAX value bit4 : 0 - IIC auto-reset Off 1 - IIC auto-reset O bit5 : 0 - cintc max , cintr max calcurate 1 - cintc max , cintr max rom table from [0x84 - 0x87]	16h	
7Fh	Factory Use	[7:0]	00h : Indoor R,B SAVE 01h : Outdoor R,B SAVE 02h : 2000 R,B SAVE 05h : CIF setting 06h : VGA setting	FFh	

ISP CONTROL REGISTER MAP

Address	Control Register	Bits	Descriptions	Default	Initial Value
80h	Timing Generator Command	[4]	CIS Input Signal Invert('0':Normal'1':Invert)	13h	
		[3]	VSYNC Output Signal Invert('0':Normal'1':Invert)		
		[2]	HSYNC Output Signal Invert('0':Normal'1':Invert)		
		[1]	VSYNC Input Signal Invert('0':Normal'1':Invert)		
		[0]	HSYNC Input Signal Invert('0':Normal'1':Invert)		
81h	PREPROCESS Command	[6:5]	Horizontal Mirror Mode Delay Adjustment Of CIS	00h	
		[4:3]	AD Delay Adjustment		
		[2]	Digital Clamp On('0':OFF,'1':ON)		
		[1]	PREPROCESS Test Mode('0':OFF,'1':ON)		
		[0]	White Defect Correction('0': OFF,'1':ON)		
82h	Digital Clamp Offset	[7:0]	Offset Values	00h	
83h	BLANK			30h	
84h	CintcMax_High	[7:0]	CintcMax_High cintcMax holds true when [7Eh bit5] is On	01h	
85h	CintcMax_Low	[7:0]	CintcMax_Low	FFh	
86h	ShutterMax_High	[7:0]	ShutterMax_High ShutterMax hold true when [7Eh bit5] is On	01h	
87h	ShutterMax_Low	[7:0]	ShutterMax_Low	F7h	
88h	Detection Window Horizontal Start	[7:0]	Horizontal Start Point For Window Of White Defection	14h	
89h	Detection Window Horizontal End	[7:0]	Horizontal End Point For Window Of White Defection	82h	
8Ah	Detection Window Vertical Start	[7:0]	Vertical Start Point For Window Of White Defection	03h	
8Bh	Detection Window Vertical End	[7:0]	Vertical End Point For Window Of White Defection	64h	
8Ch	BLANK			00h	
8Dh	Horizontal Clamp Start	[7:0]	Horizontal Start Point For Window Of Optical Black	00h	
8Eh	Vertical Clamp Start	[7:0]	Vertical Start Point For Window Of Optical	00h	
8Fh	Defect Threshold	[7:0]	Threshold Values For Detection Of White Defect	3Ch	
90h	Formatter Command	[3:2]	00 : ITU.R-656 Format (YCrCb) 01 : ITU.R-601 Format(YCrCb) 10 : R/G/B Data 11 : CIS Raw Data	03h	
		[1]	0 : Y First (Y/Cb/Y/Cr) 1 : C First (Cb/Y/Cr/Y)		
		[0]	0 : Cb or R First (Y/Cb/Y/Cr or R/G/B) 1 : Cr or B First (Y/Cr/Y/Cb or B/G/R)		
91h	RGB Matrix Control	[7]	Black and White CIS Mode 0: Color CIS 1: B/W CIS	09h	
		[6]	Selection of RGB Interpolation 0: Adaptive 1: Linear		
		[5]	Gamma Point Correction 0:16Point 1:8Point		
		[4]	Control of CIS Horizontal Data Arrangement 0: R/G/R/G or G/B/G/B 1: G/R/G/R or B/G/B/G		
		[3]	Control of CIS Vertical Data Arrangement 0: R/G/R/G or G/B/G/B 1: G/R/G/R or B/G/B/G		
		[2:0]	Color Suppress Coefficient Of Delay Adjustment 000: 0CK Delay 001: 1CK Delay 010: 2CK Delay 011: 3CK Delay 100: -4CK Delay 101: -3CK Delay 110: -2CK Delay 111: -1CK Delay		
92h	Horizontal Correlation Threshold	[7:0]	Horizontal Correction Values of Adaptive Interpolation	05h	
93h	Vertical Correlation Threshold	[7:0]	Vertical Correction Values of Adaptive Interpolation	05h	
94h	R Gain for R Color Correction	[7:0]	R Gain Values of R Signal Color Correction	80h	
95h	G Gain for R Color Correction	[7:0]	G Gain Values of R Signal Color Correction	00h	
96h	B Gain for R Color Correction	[7:0]	B Gain Values of R Signal Color Correction	00h	
97h	R Gain for G Color Correction	[7:0]	R Gain Values of G Signal Color Correction	00h	
98h	G Gain for G Color Correction	[7:0]	G Gain Values of G Signal Color Correction	80h	
99h	B Gain for G Color Correction	[7:0]	B Gain Values of G Signal Color Correction	00h	
9Ah	R Gain for B Color Correction	[7:0]	R Gain Values of B Signal Color Correction	00h	
9Bh	G Gain for B Color Correction	[7:0]	G Gain Values of B Signal Color Correction	00h	
9Ch	B Gain for B Color Correction	[7:0]	B Gain Values of B Signal Color Correction	80h	
9Dh	R Coefficient for Y Signal	[7:0]	R Coefficient of Y Signal Generation	4Ch	
9Eh	G Coefficient for Y Signal	[7:0]	G Coefficient of Y Signal Generation	98h	

Address	Control Register	Bits	Descriptions	Default	Initial Value
9Fh	B Coefficient for Y Signal	[7:0]	B Coefficient of Y Signal Generation	1Ch	
A0h	High-Light Color Suppress Reference	[7:0]	High-Light Color Suppress Reference	A0h	
A1h	Edge Color Suppress Reference	[7:0]	Edge Color Suppress Reference	20h	
A2h	High-Light Color Suppress Gain	[5]	High-Light Color Suppress Selection	00h	3Eh
		[4:0]	High-Light Color Suppress Gain		
A3h	Edge Color Suppress Gain	[5]	Edge Color Suppress Selection	28h	
		[4:0]	Edge Color Suppress Gain		
A4h	Gamma Value 1	[7:0]	GM1 Values[7:0]	10h	
A5h	Gamma Value 2	[7:0]	GM2 Values[7:0]	3Ch	4Ch
A6h	Gamma Value 3	[7:0]	GM3 Values[7:0]	65h	75h
A7h	Gamma Value 4	[7:0]	GM4 Values[7:0]	A3h	
A8h	Gamma Value 5	[7:0]	GM5 Values[7:0]	FFh	
A9h	Gamma Value 6	[7:0]	GM6 Values[7:0]	90h	
AAh	Gamma Value 7	[7:0]	GM7 Values[7:0]	87h	
ABh	Gamma Value 8	[7:0]	GM8 Values[7:0]	FFh	D0h
ACh	Gamma Value 1234	[7:6]	GM1 Values[9:8]	00h	
		[5:3]	GM2 Values[9:8]		
		[3:2]	GM3 Values[9:8]		
		[1:0]	GM4 Values[9:8]		
ADh	Gamma Value 5678	[7:6]	GM5 Values[9:8]	1Bh	
		[5:3]	GM6 Values[9:8]		
		[3:2]	GM7 Values[9:8]		
		[1:0]	GM8 Values[9:8]		
AEh	Pattern Selection	[5:4]	00:CIS Pattern 01:Color Bar Pattern 10:Ramp Pattern 11:Blue Screen Pattern	00h	
AFh	BLANK			00h	
B0h	R Dark Slice	[7:0]	Dark Slice Values of R Signal	00h	
B1h	B Dark Slice	[7:0]	Dark Slice Values of B Signal	00h	
B2h	G Dark Slice	[7:0]	Dark Slice Values of G Signal	00h	
B3h	RB White Balance	[3:2]	White Balance Coefficient of R Signal[9:8]	00h	
		[1:0]	White Balance Coefficient of B Signal[9:8]		
B4h	R White Balance	[7:0]	White Balance Coefficient of R Signal[7:0]	20h	
B5h	B White Balance	[7:0]	White Balance Coefficient of B Signal[7:0]	20h	
B6h	G White Balance	[7:0]	White Balance Coefficient of G Signal	48h	
B7h	(R-G) Gain Control for (R-Y)	[7:0]	R-G Signal Coefficient of R-Y Signal Generation	59h	
B8h	(B-G) Gain Control for (R-Y)	[7:0]	B-G Signal Coefficient of R-Y Signal Generation	F2h	
B9h	(R-G) Gain Control for (B-Y)	[7:0]	R-G Signal Coefficient of B-Y Signal Generation	D9h	
BAh	(B-G) Gain Control for (B-Y)	[7:0]	B-G Signal Coefficient of B-Y Signal Generation	72h	
BBh	Horizontal Blank Rising Edge	[7:0]	Horizontal Blank Rising Edge Point Setting[7:0]	30h	
BCh	Horizontal Blank Falling Edge	[7:0]	Horizontal Blank Falling Edge Point Setting[7:0]	b0h	
BDh	Vertical Blank Rising Edge	[7:0]	Vertical Blank Rising Edge Point Setting[7:0]	05h	
BEh	Vertical Blank Falling Edge	[7:0]	Vertical Blank Falling Edge Point Setting[7:0]	E5h	
BFh	H/V Blank Rising/Falling Edge	[7:6]	HBLK_RE[9:8]	21h	
		[5:4]	HBLK_FE[9:8]		
		[3:2]	VBLK_RE[9:8]		
		[1:0]	VBLK_FE[9:8]		
C0h	(R-Y) Positive Gain	[7:0]	R-Y Positive Gain Coefficient of R-Y Signal	6Ch	
C1h	(R-Y) Negative Gain	[7:0]	R-Y Negative Gain Coefficient of R-Y Signal	6Ch	
C2h	(R-Y) Positive Hue Control	[7:0]	R-Y Positive Hue Coefficient of R-Y Signal	0Ch	
C3h	(R-Y) Negative Hue Control	[7:0]	R-Y Negative Hue Coefficient of R-Y Signal	2Ch	
C4h	(B-Y) Positive Gain	[7:0]	B-Y Positive Gain Coefficient of B-Y Signal	55h	
C5h	(B-Y) Negative Gain	[7:0]	B-Y Negative Gain Coefficient of B-Y Signal	5Bh	
C6h	(B-Y) Positive Hue Control	[7:0]	B-Y Positive Hue Coefficient of B-Y Signal	00h	
C7h	(B-Y) Negative Hue Control	[7:0]	B-Y Negative Hue Coefficient of B-Y Signal	00h	
C8h	C Gain	[7:0]	Color Gain	80h	
C9h	Hue Control	[0]	Hue Gain and Control Coefficient	00h	
CAh-CFh	BLANK				
D0h	Edge Enhancement Non-Linear Control	[7:6]	Vertical Edge Enhancement Non-Linear Control Threshold	AAh	
		[5:4]	Vertical Edge Enhancement Non-Linear Control Gain		
		[3:2]	Horizontal Edge Enhancement Non-Linear Control Threshold		
		[1:0]	Vertical Edge Enhancement Non-Linear Control Gain		
D1h	Horizontal Edge Enhancement Control	[6:5]	High Frequency Edge Enhancement Filter Gain	50h	
		[4:0]	Vertical Positive Edge Enhancement Gain		

Address	Control Register	Bits	Descriptions	Default	Initial Value
D2h	Vertical Edge Enhancement Control	[6:5]	Low Frequency Edge Enhancement Filter Gain	50h	
		[4:0]	Vertical Positive Edge Enhancement Gain		
D3h	H Edge Enhancement Negative Gain	[4:0]	Horizontal Negative Edge Enhancement Gain	10h	
D4h	V Edge Enhancement Negative Gain	[4:0]	Vertical Negative Edge Enhancement Gain	10h	
D5h	High-Light Enhancement	[7:0]	High-Light Enhancement Clip Level	0Ah	
D6h	Y Edge Enhancement Clip	[7:0]	Edge Enhancement Clip Level	BFh	
D7h	Y High-Light Enhancement Noise Slice	[5:0]	High-Light Enhancement Noise Slice Level	7Fh	
D8h	Y Edge Enhancement Noise Slice	[4:0]	Edge Enhancement Noise Slice Level	00h	
D9h	Detail Enhancer Threshold & Gain	[5:4]	Detail Enhancer Threshold	00h	
		[1:0]	Detail Enhancer Gain		
DAh	High_Light Enhancement Gain	[4:0]	High_Light Enhancement Gain	10h	
DBh	Y White Clip	[7:0]	Y White Clip Level	FFh	
DCh	Y Gain	[7:0]	Y Gain	80h	
DDh	Y Group Delay	[4]	AE/AWB Window Pulse Enable ('0':OFF,'1':ON)	10h	
		[3]	Vertical Edge Enhancement Selection ('0':OFF,'1':ON)		
		[2:0]	Y/C Group Delay Match Adjust		
Deh	Cloudy R,B offset	[7:0]	[7:4] Cloudy R offset, [3:0] Cloudy B offset	33h	22h
DFh	Sunny R,B offset	[7:0]	[7:4] Sunny R offset, [3:0] Sunny B offset	75h	43h
E0h	AE Window1 Horizontal Start	[7:0]	Horizontal Start Point of AE Window1	05h	
E1h	AE Window1 Horizontal End	[7:0]	Horizontal End Point of AE Window1	CAh	
E2h	AE Window1 Vertical Start	[7:0]	Vertical Start Point of AE Window1	3Ch	
E3h	AE Window1 Vertical End	[7:0]	Vertical End Point of AE Window1	E6h	
E4h	AE Window2 Horizontal Start	[7:0]	Horizontal Start Point of AE Window2	05h	
E5h	AE Window2 Horizontal End	[7:0]	Horizontal End Point of AE Window2	CAh	
E6h	AE Window2 Vertical Start	[7:0]	Vertical Start Point of AE Window2	06h	
E7h	AE Window2 Vertical End	[7:0]	Vertical End Point of AE Window2	E6h	
E8h	AWB Window Horizontal Start	[7:0]	Horizontal Start Point of AWB Window	12h	
E9h	AWB Window Horizontal End	[7:0]	Horizontal End Point of AWB Window	C3h	
EAh	AWB Window Vertical Start	[7:0]	Vertical Start Point of AWB Window	34h	
EBh	AWB Window Vertical End	[7:0]	Vertical End Point of AWB Window	E2h	
ECh~EFh	BLANK	[7:0]			
F0h	AE Y Signal High Threshold	[7:0]	High Threshold Values of Y Signal For AE	FFh	
F1h	AE Y Signal Low Threshold	[7:0]	Low Threshold Values of Y Signal For AE	00h	
F2h	AWB Y Signal High Threshold	[7:0]	High Threshold Values of Y Signal For AWB	F0h	
F3h	AWB Y Signal Low Threshold	[7:0]	Low Threshold Values of Y Signal For AWB	40h	
F4h	AE Clip Counter Threshold	[7:0]	Threshold Values of AE Clip Counter	78h	
F5h	Optical Detector Command	[1:0]	AE/AWB Window Selection 00 : Nothing 01 : AE Window1 10 : AE Window2 11 : AWB Window	00h	
F6h	Horizontal Sync Rising Edge	[7:0]	Horizontal Sync Rising Edge Setting [7:0]	30h	
F7h	Horizontal Sync Falling Edge	[7:0]	Horizontal Sync Falling Edge Setting[7:0]	b0h	
F8h	Vertical Sync Rising Edge	[7:0]	Vertical Sync Rising Edge Setting [7:0]	03h	
F9h	Vertical Sync Falling Edge	[7:0]	Vertical Sync Falling Edge Setting [7:0]	05h	
FAh	H/V Sync Rising/Falling Edge	[7:6]	Horizontal Sync Rising Edge Setting [9:8]	20h	
		[5:4]	Horizontal Sync Falling Edge Setting[9:8]		
		[3:2]	Vertical Sync Rising Edge Setting [9:8]		
		[1:0]	Vertical Sync Falling Edge Setting[9:8]		
FBh	Horizontal Counter End L	[7:0]	1H Sync Value Setting[7:0]	59h	
FCh	Horizontal Counter End H	[1:0]	1H Sync Value Setting[9:8]	03h	
FDh	Line Memory Hold	[7:0]	Line Memory Hold Vertical Position[7:0]	00h	
FEh	Line Memory Hold Enable	[2]	Line Memory Hold Enable(0 : OFF 1 : ON)	00h	
		[1:0]	Line Memory Hold Vertical Position[9:8]		

Mechanical Dimension (unit =mm)