SX5437M21X-X0B0
(1/4” VGA CIS Camera Module)

PRELIMINARY

Preliminary Specification

Revision 1.3

May. 2004

DOCUMENT TITLE

1/4” Optical Size 640x480(VGA) CIS Camera Module

REVISION HISTORY

Revision No.	History	Draft Date	Remark
0.0	Initial draft	Aug 14, 2003	Preliminary
0.1	Added register map and changed timing diagram Added module dimension	Oct. 31, 2003	Preliminary
0.2	Fixed some bugs	Nov. 19, 2003	Preliminary
1.0	Changed I2C timing diagram Changed product code (S5X437CX03-20R0 → SX5437M21X-X0B0)	Dec. 31, 2003	Preliminary
1.1	Changed the register map	Jan. 7, 2004	Preliminary
1.2	Stroke out the register map (published a new document, ‘Register Map for 437’)	Apr.29, 2004	Preliminary
1.3	Modified the optical characteristics	May.4, 2004	Preliminary

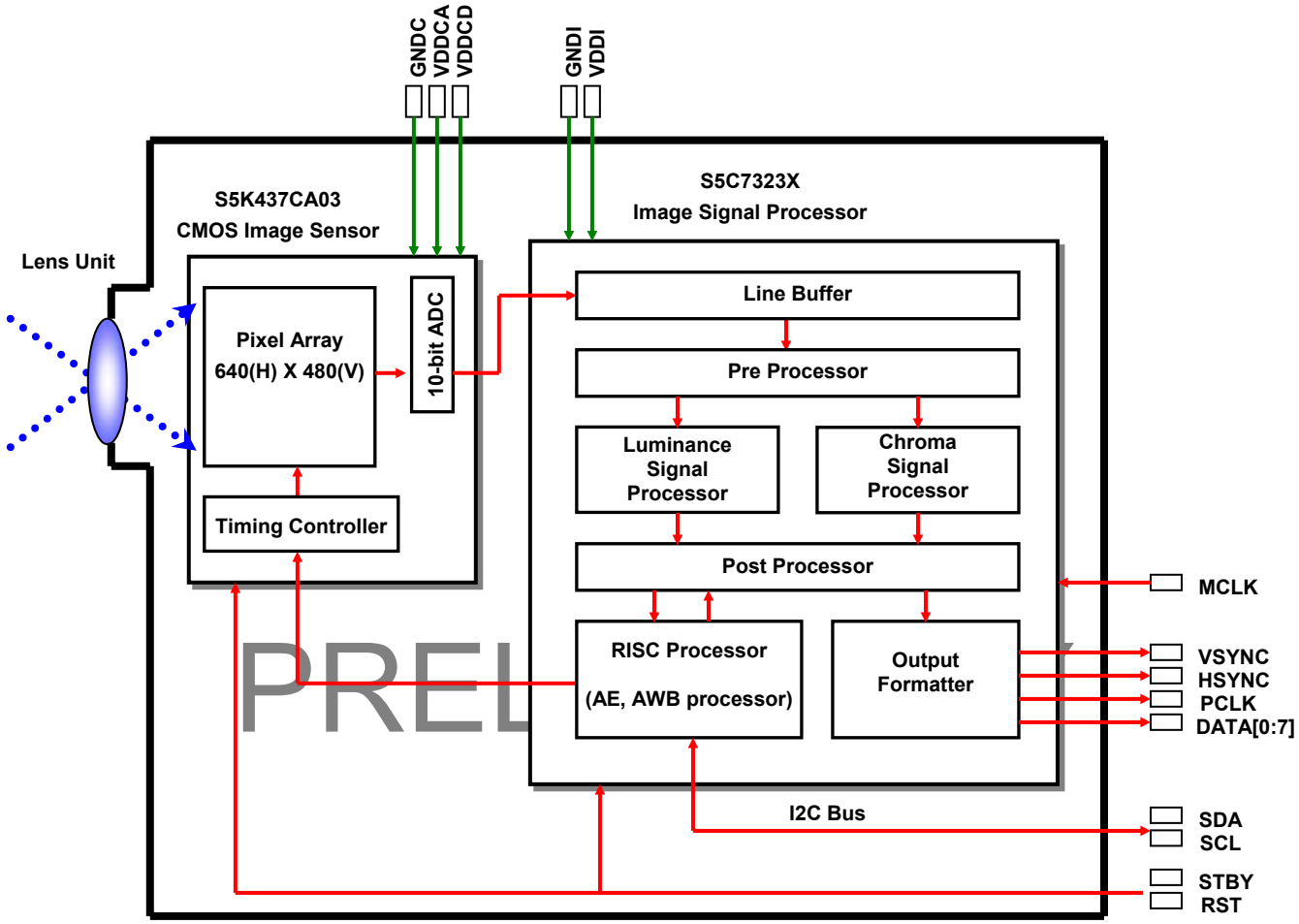
INTRODUCTION

The SX5437M21X-X0B0 is fully functional camera module with a built-in lens. A low-noise low-power color CMOS image sensor, S5K437CX03 and an image signal processor, S5C7323X produce high-quality digital video output including CCIR656 format with maximum 30 frames per second for full frame readout. With SAMSUNG 0.35μm CMOS image sensor process technology which is dedicated to higher sensitivity and lower-dark level compared to standard CMOS process, and on-chip CDS and 10-bit column ADC circuit embedded, the CMOS image sensor provides high signal-to-noise ratio with low power consumption. This compact camera system consists of an image sensor, a signal processor and some passive components packed with IR-cut filter and lens units. The system works with 2.8V single power supply and a clock. All the functions are controlled with control register setting through the standard 2-wire serial interface.

FEATURES

- Optical Size: 1/4 inch format
- Unit Pixel: 5.6 μm X 5.6 μm
- Effective Resolution: 640(H) X 480(V), VGA
- 8.5mm X 9.5mm X 6.6mm module size
- 8-bit ITU.R-656 (YCrCb) Video Output
- Programmable Gamma Correction
- Auto White Balance and Auto Exposure Control
- Horizontal and/or Vertical Mirror Output
- Standby-Mode for Power Saving
- Maximum 30 Frame per Second
- Single Power Supply Voltage: 2.8V
- I^2C Type Control Interface
- Bad Pixel Replacement Function
- Noise Canceling Function
- Shading Correction Function

BLOCK DIAGRAM



OPTICAL CHARACTERISTICS

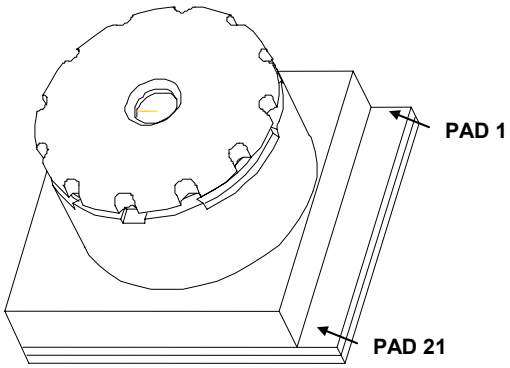
Characteristic		Value
Effective Pixels		640 (H) X 480 (V), VGA
Pixel Size		5.6μm (H) X 5.6μm (V), square pixel
EFL		3.385mm
F/#		2.8
FOV	Diagonal	67.87°
	Horizontal	56.44°
	Vertical	43.59°
TV-Distortion		-0.33%
Relative Illumination		54.40%
MTF	Center	59.90% at 80 lp/mm
		72.60% at 50 lp/mm
	0.7 Field	21.30% at 80 lp/mm
		42.30% at 50 lp/mm
Lens Construction		All Plastic Lens (2P)
Focus Range		22cm ~ ∞

MODULE PAD DESCRIPTION

(Module pad numbers and name can be changed as customer's request.)

Module Pad No.	Name	Connector Pin No. (*)	Type	Description
1	VDDDI	9	Power	Power supply for signal processor (digital)
2	GNDI	10	Ground	Ground for signal processor
3	SCL	15	In/Out	I^2C serial communication clock
4	SDA	16	In/Out	I^2C serial communication data
5	RST	11	In	Reset control (active low)
6	STBY	12	In	Standby control(active low)
7	MCLK	20	In	Master input clock
8	VSYNC	17	Out	Vertical synchronization clock
9	HSYNC	18	Out	Horizontal synchronization clock
10	PCLK	19	Out	Pixel output clock
11	DATA0	8	Out	8-bit digital video output
12	DATA1	7	Out	
13	DATA2	6	Out	
14	DATA3	5	Out	
15	DATA4	4	Out	
16	DATA5	3	Out	
17	DATA6	2	Out	
18	DATA7	1	Out	
19	GNDC	13	Ground	Ground for sensor circuit block
20	VDDDC	9	Power	Power supply for sensor digital circuit block
21	VDDAC	14	Power	Power supply for sensor analog circuit block

NOTES: (*) See [Cf] p. 32.



MAXIMUM ABSOLUTE RATINGS

Characteristic	Symbol	Rating	Unit
Maximum supply voltage (VDDDI, VDDAC, VDDC supply relative to GNDI, GNDC)	V_{DD}	-0.3 to 3.8	V
DC Input voltage	V_{IN}	-0.3 to V_{DD}+0.3 (Max. 3.8)	
*Operating temperature	T_{OPR}	*-20 to +60	°C
*Storage temperature	T_{STG}	*-40 to +85	

NOTES: *Operating temperature and *Storage temperature are not confirmed.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(T_A = -20 to +60°C, C_L = 15pF)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Operating voltage	V_{DD}	VDDCA, VDDCD, VDDI	2.55	2.8	3.1	V
Input voltage (1)	V_{IH}	-	2.05	-	-	V
	V_{IL}	-	-	-	0.8	
Input leakage current(1)	I_{IL}	V_{IN} = V_{DD} to V_{SS}	-10	-	10	µA
High level output voltage	V_{OH}	I_{OH} = -1mA(2)	0.8V_{DD}	-	-	V
		I_{OH} = -4mA(3)				
Low level output voltage	V_{OL}	I_{OL} = 1mA(2)	-	-	0.2V_{DD}	
		I_{OL} = 4mA(3)				
High-Z output leakage current (4)	I_{OZ}	V_{OUT} = V_{DD}	-	-	10	µA
Supply current	I_{STB}	STBY = Low (active) All input clocks = Low	-	-	TBD	µA
	I_{DD}	f_{MCLK} = 12MHz, 15fps	-	TBD	-	mA

NOTES:
1. MCLK, RSTN, STBY, SCL, and SDA pin.
2. HSYNC, VSYNC, SCL, and SDA pin
3. PCLK, YCO0 to YCO7 pin
4. SCL and SDA pin when in High-Z output state

Sensor Imaging Characteristics

(Light source with 3200K of color temperature and IR cut filter (CM-500S, 1mm thickness) is used. Electrical operating conditions follow the recommended typical values. The control registers are set to the default values. The ambient temperature, T_A is 25°C if not specified.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Saturation level(1)	V_{SAT}		850	900	-	mV
Sensitivity (G)(2)	S		-	1500	-	mV/lux sec
Dark level(3)	V_{DARK}	T_A = 40°C	-	9	18	mV/sec
		T_A = 60°C	-	50	100	
Dynamic range(4)	DR		-	60	-	dB
Signal to noise ratio(5)	S/N		-	40	-	
Dark signal non-uniformity(6)	DSNU	T_A = 60°C	-	-	100	mV/sec
Photo response non-uniformity(7)	PRNU		-	4	8	%
Vertical fixed pattern noise(8)	VFPN			4	8	%
Horizontal fixed pattern noise(9)	HFPN			4	8	%

NOTES:

1. Measured minimum output level at 100lux illumination for exposure time 1/30 sec. 7X7 rank filter is applied for the whole pixel area to eliminate the values from defective pixels.
2. Measured average output at 25% of saturation level illumination for exposure time 1/30 sec. Green channel output values are used for color version.
3. Measured average output at zero illumination without any offset compensation for exposure time 1/30 sec.
4. 20 log (saturation level/ dark level RMS noise excluding fixed pattern noise). 10-bit ADC limits 60dB.
5. 20 log (average output level/RMS noise excluding fixed pattern noise) at 25% of saturation level illumination for exposure time 1/30 sec.
6. Difference between maximum and minimum pixel output levels at zero illumination for exposure time 1/30 sec. 7X7 median filter is applied for the whole pixel area to eliminate the values from defective pixels.
7. Difference between maximum and minimum pixel output levels divided by average output level at 25% of saturation level illumination for exposure time 1/30 sec. 7X7 median filter is applied for the whole pixel area to eliminate the values from defective pixels.
8. For the column-averaged pixel output values, maximum relative deviation of values from 7-depth median filtered values for neighboring 7 columns at 25% of saturation level illumination for exposure time 1/30 sec.
9. For the row-averaged pixel output values, maximum relative deviation of values from 7-depth median filtered values for neighboring 7 columns at 25% of saturation level illumination for exposure time 1/30 sec.

AC Characteristics

(V_{DDH} = 2.8V ± 0.25V, V_{DDL} = 1.8V ± 0.15V, T_a = -20 to + 60 °C, C_L = 50pF)

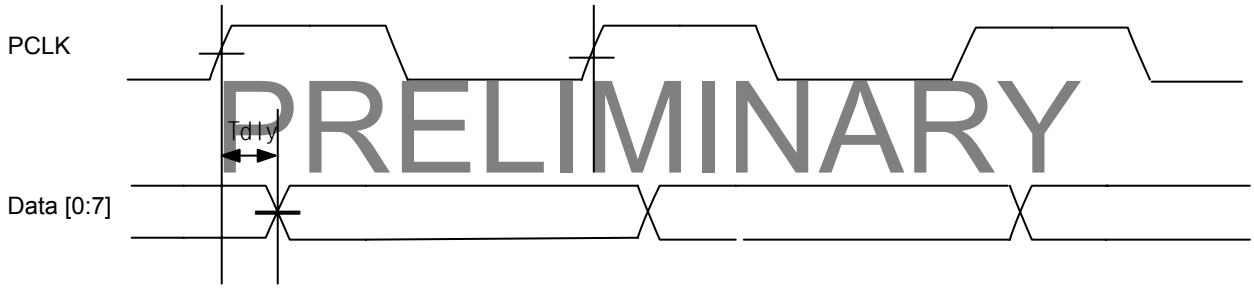
Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Main input clock frequency	f_{MCLK}	Duty = 50%	3(1)	24.54	30	MHz
Output data delay time from PCLK	t_{DLY}	T_a =0~70℃	0.7		3.5	ns
Reset input pulse width	t_{WRST}	RSTN=low(active)	5	-	-	T_{MCLK}(2)
Standby input pulse width	t_{WSTB}	STBYN=low(active)	4	-	-	

NOTES:

1. 8-bit ADC resolution case. If 10-bit ADC resoultion is used, the frequency should be over 12MHz.
2. The period time of main input clock, **MCLK**.

(V_{DDH} = 2.8V ± 0.25, T_a = 0 to + 70 °C)

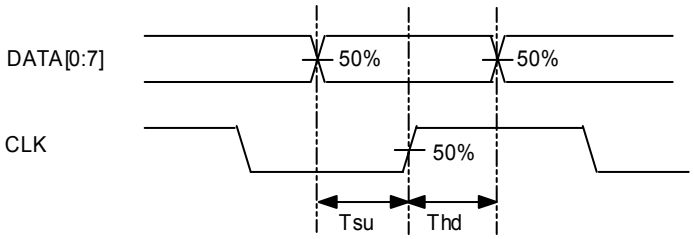
Characteristic	Symbol	Min	Typ	Max	Unit
Output Data Delay Time, Data [0:7]	T_{DLY}	0.7	-	3.5	ns



Setup and Hold Time

(V_{DDL} = 1.8V ± 0.15, T_a = 0 to + 70 °C)

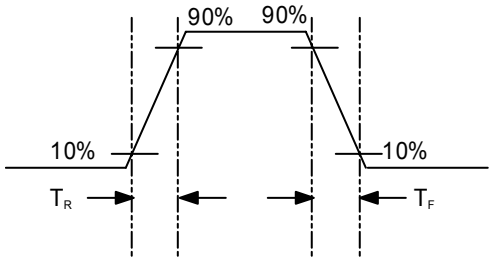
Characteristic	Symbol	Min	Typ	Max	Unit
Output Data Setup Time, Data [0:7]	T_{SU}	0.217	-	-	ns
Output Data Hold Time, Data [0:7]	T_{HD}	0.217	-	-	ns



Rise and Fall Transition Time

(V_{DDL} = 1.8V ± 0.15, T_a = 0 to + 70 °C)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Data, Data [0:7]	T_R	-	-	4.709	ns
	T_F	-	-	4.338	ns

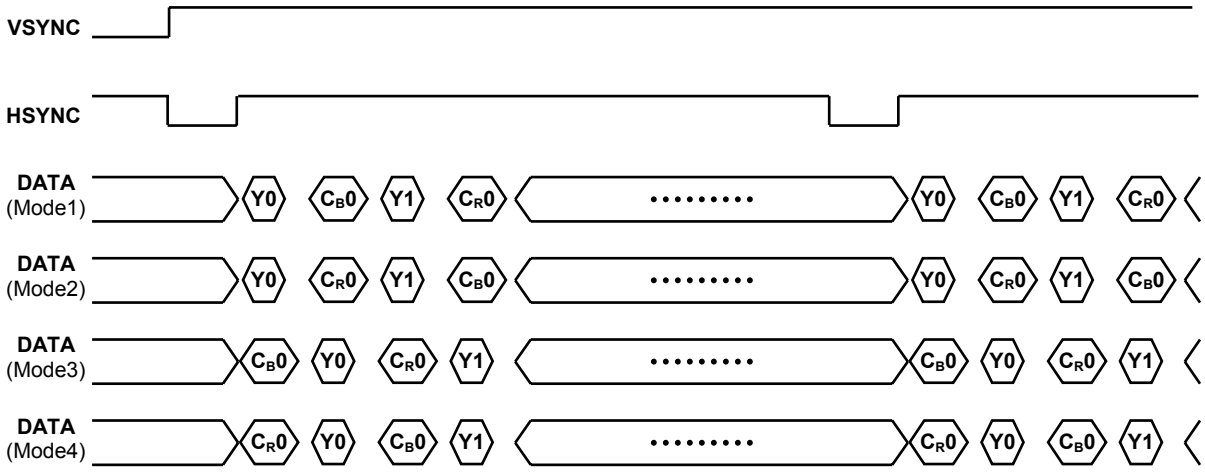


OUTPUT IMAGE MODE

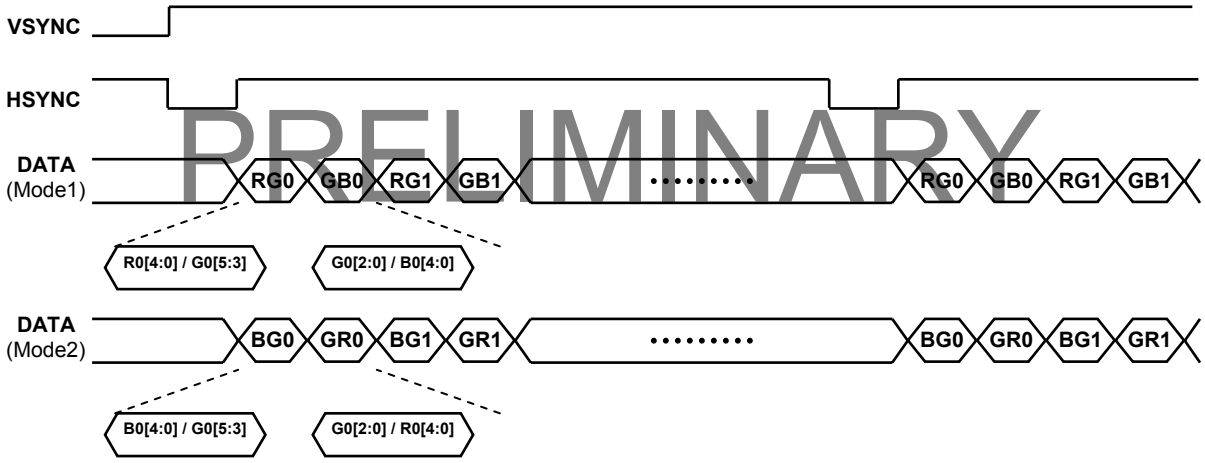
No.	Mode	Resolution (H X V)	Data rate (PCLK)	Zoom	Frame Rate
1	VGA	640 X 480	**MCLK**	-	30 FPS

OUTPUT DATA FORMAT

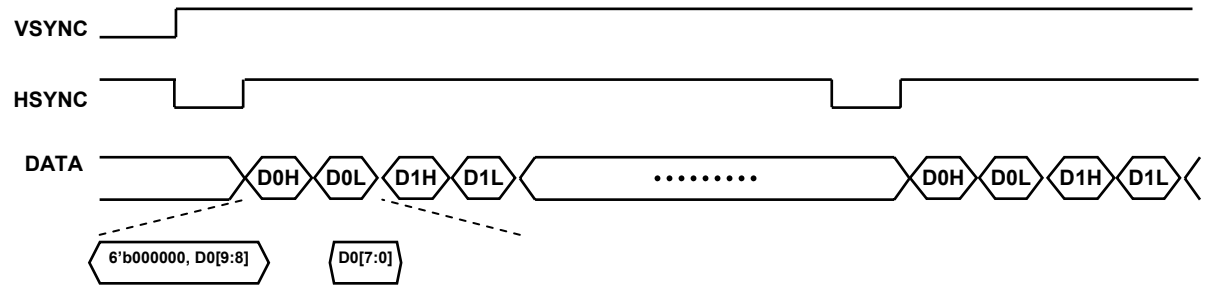
YC_RC_B 4:2:2 FORMAT



RGB565 FORMAT

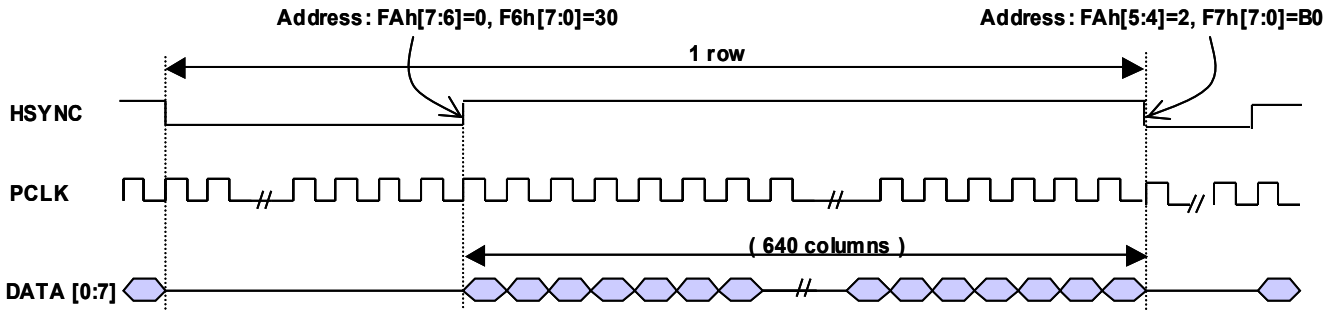


SENSOR RAW IMAGE (BAYER MOSAIC PATTERN) FORMAT

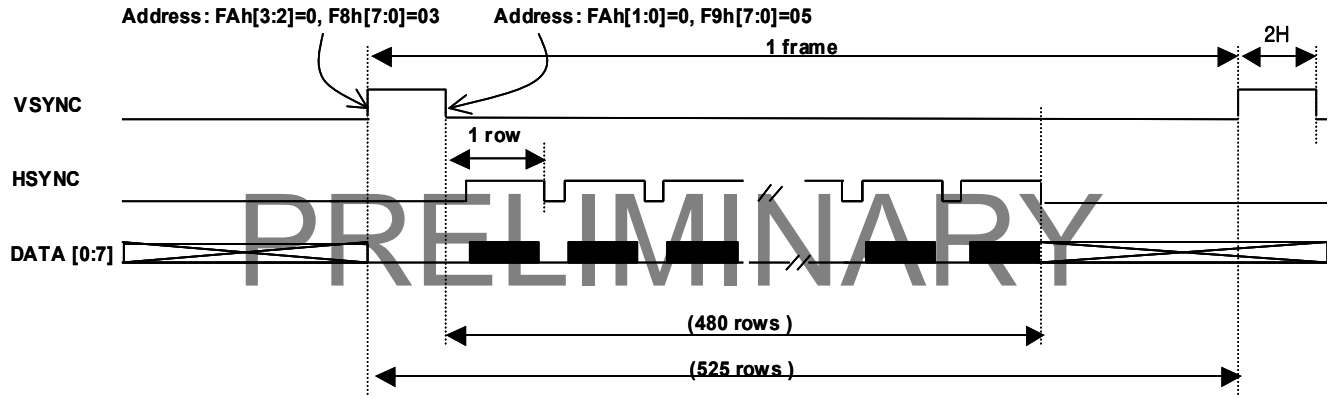


OUTPUT TIMING DIAGRAMS

HORIZONTAL TIMING



VGA OUTPUT TIMING



NOTES:

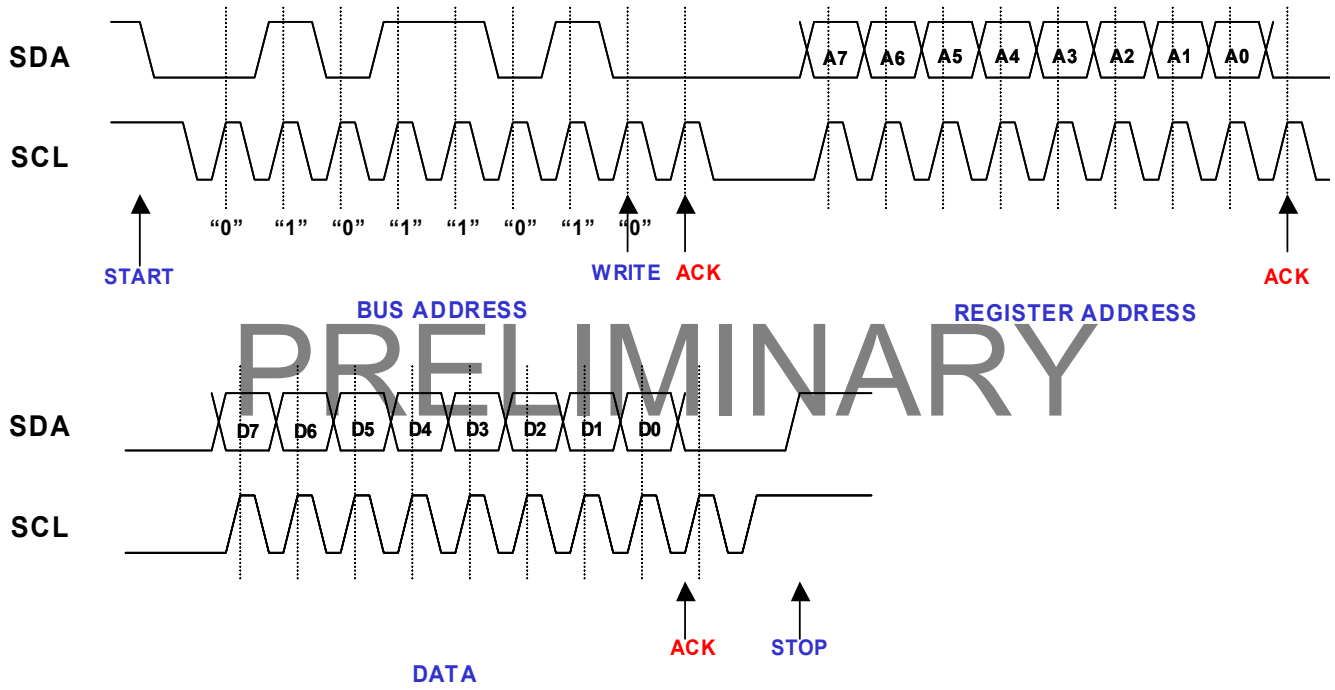
1. Falling and rising time of HSYNC and VSYNC can be controlled by register settings.
2. Each default value of rising and falling time control registers is described in the diagram above.

IMAGE PROCESSING FUNCTIONS

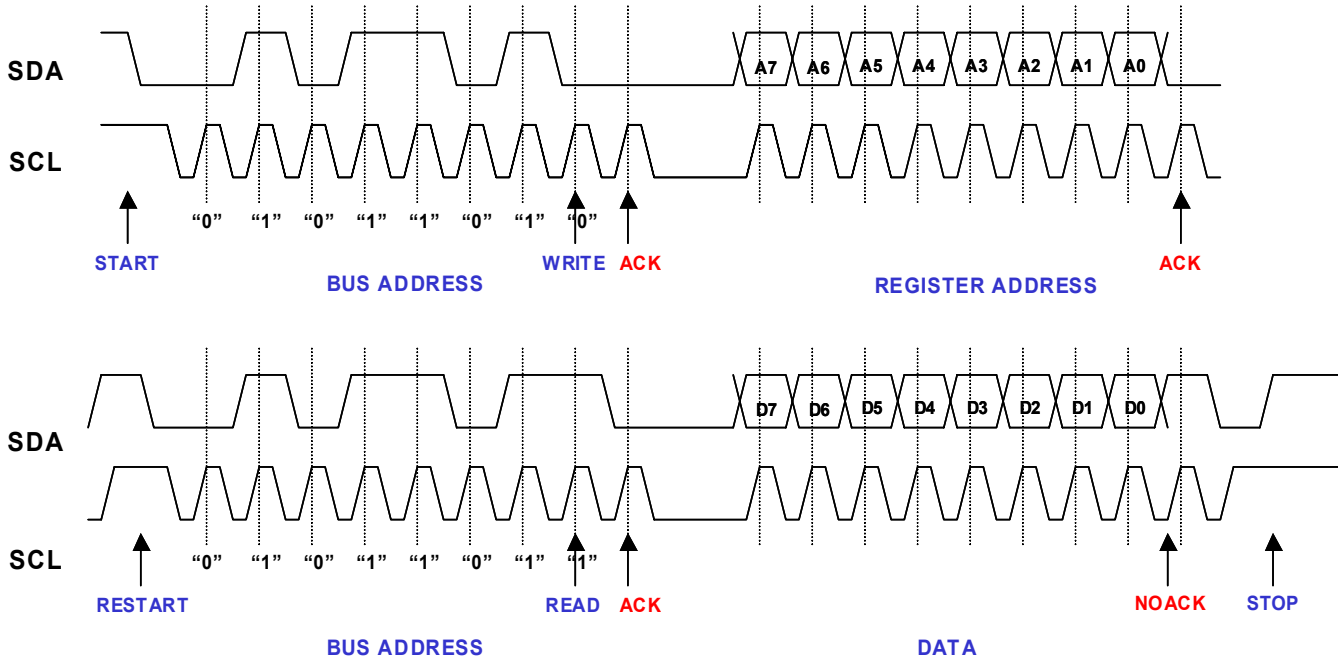
Function	Description	Remarks
Defect detection and correction	If enabled, the function detects the defective pixel by comparing its level with horizontally neighboring pixels, and replaces it with the average value of neighboring pixels.	
De-mosaic	The sensor produces one color component from a pixel according to Bayer color filter array. The de-mosaic function performs color interpolation to produce all three-color components at each pixel location.	
Color correction	The spectral response of image sensor is different from that of human eye. To match the spectral response, the sensor output components are pivoted by user programmable 3X3 matrix production.	
Gamma correction	Gamma correction translating the linear response of the sensor into the non-linear characteristics of the display. Non-linear conversion requires a piecewise linear approximation method based on user programmable lookup table.	
Horizontal mirror	The output image can be mirrored in horizontal direction.	
Vertical mirror	The output image can be mirrored in vertical direction.	
Edge enhancement	Enhancing the edge component provides a clear output image. The edge enhancement function is performed through horizontal and vertical edge detecting and enhancing.	
Auto exposure	According to the incident light level, the auto exposure function controls the sensor gain and effective integration time to maintain the proper output level. Setting the control registers can change the sensing area used in the AE algorithm.	
Auto white balance	The auto white balance function adjusts the gain of the sensor's red and blue channels relative to the green channel, and compensates the spectral unbalancing of the light source. Setting the control registers can change the sensing area used in the AWB algorithm.	
Output format conversion	4 types of output format are available. (CCIR656 format, CCIR601 format, RGB format and sensor raw image output format)	
Sub-sampling Control	The user can read out the pixel data in sub-sampling rate in both horizontal and vertical direction. Sub-sampling can be done in two rates: full and 1/2. The user controls the sub-sampling using the Sub-sampling Control Registers, **subsr** and **subsc**. The sub-sampling is performed only in the Bayer space.	

I²C SERIAL INTERFACE

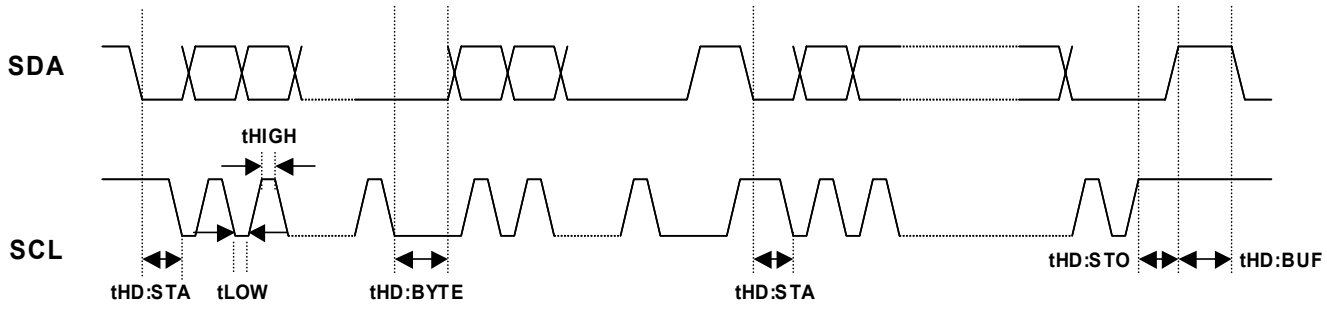
The I²C contains a serial two-wire half duplex interface that features bi-directional operation, master or slave mode. The general **SDA** and **SCL** are the bi-directional data and clock pins, respectively. These pins are open-drain type ports and will require a pull-up resistor to VDD. The image sensor operates in salve mode only and the **SCL** is input only. The I²C bus interface is composed of following parts: START signal, 7-bit slave device address (0101101Xb) transmission followed by a read/write bit, an acknowledgement signal from the slave, 8-bit data transfer followed by an acknowledgement signal and STOP signal. The **SDA** bus line may only be changed while **SCL** is low. The data on the **SDA** bus line is valid on the high-to-low transition of **SCL**.



I²C Bus Write Format



I²C Bus Read Format

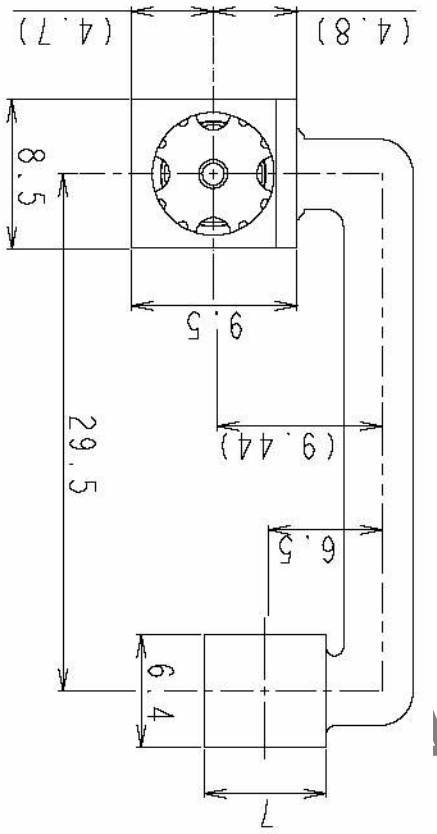


I²C Bus Timing

PARAMETER	Symbol	Min	Max	Unit
SCL clock frequency	fClk		400	kHZ
Low period of the SCL clock	tLOW	1.3		μsec
High period of the SCL clock	tHIGH	0.6		μsec
Hold time START condition	tSTA	0.6		μsec
Hold time STOP condition	tSTO	0.6		μsec
Bus free time between BYTE and BYTE data	tBYTE	130		tMCLK
Bus free time between a STOP and START condition	tBUF	130		tMCLK

NOTES:
1. tMclk : Main clock period

MODULE DIMENSION



PRELIMINARY

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