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AN1543/D

Electronic Lamp Ballast Design

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APPLICATION NOTE

ABSTRACT

With a continuous growth rate of 20% per year, electronic lamp ballasts are widely spread over the world. Even though the light out of a fluorescent tube has a discontinuous spectrum, the higher efficiency brought by the electronic control of these lamps make them the best choice to save the energy absorbed by the lighting systems.

A few years ago, the lack of reliable and efficient power transistors made the design of such circuits difficult! Today, thanks to the technology improvements carried out by ON Semiconductor, design engineers can handle all of the problems linked with the power semiconductors without sacrificing the global efficiency of their circuits.

This Application Note reviews basic electronic lamp ballast concepts and gives the design rules to build industrial circuits.

SUMMARY

ELECTRONIC LAMP BALLAST

Main Purpose

To generate the light out of a low pressure fluorescent lamp, the electronic circuit must perform four main functions:

a. Provide a start−up voltage across the end electrodes of the lamp.
b. Maintain a constant current when the lamp is operating in the steady state.
c. Assure that the circuit will remain stable, even under fault conditions.
d. Comply with the applicable domestic and international regulations (PFC, THD, RFI, and safety).

Obviously, a high end electronic lamp ballast will certainly include other features like dimming capability, lamp wear out monitoring, and remote control, but these are optional and will be analyzed separately.

Fluorescent Lamp Operation

When the lamp is off, no current flows and the apparent impedance is nearly infinite. When the voltage across the electrodes reaches the V_{trig} value, the gas mixture is highly ionized and an arc is generated across the two terminals of the lamp. This behavior is depicted by the typical operating curve shown in Figure 1.

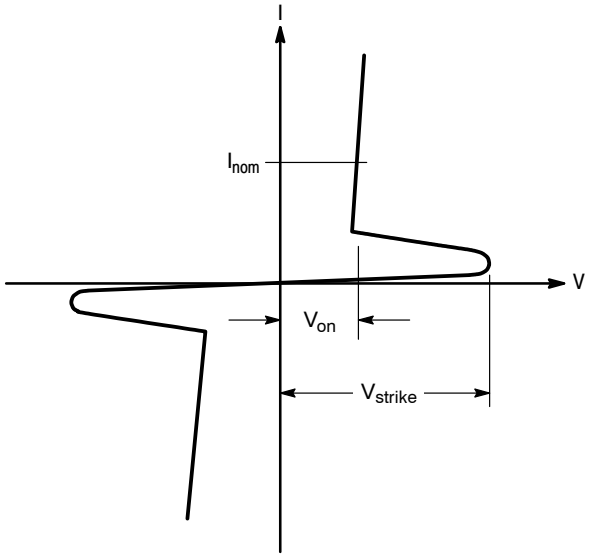


Figure 1. Typical Low Pressure Fluorescent Tube I/V Characteristic

The value of V_{strike} is a function of several parameters:

- gas filling mixture
- gas pressure and temperature
- tube length
- tube diameter
- kind of electrodes: cold or hot

Typical values of V_{strike} range from 500 V to 1200 V.

Once the tube is on, the voltage across it drops to the on−state voltage (V_{on}), its magnitude being dependent upon the characteristics of the tube. Typical V_{on} ranges from 40 V to 110 V.

The value of V_{on} will vary during the operation of the lamp but, in order to simplify the analysis, we will assume, in a first approximation, that the on−state voltage is constant when the tube is running in steady state.

Consequently, the equivalent steady state circuit can be described by two back to back zener diodes as shown in Figure 2, the start−up network being far more complex, particularly during the gas ionization. This is a consequence of the negative impedance exhibited by the lamp when the voltage across its electrodes collapses from V_{strike} to V_{on}.

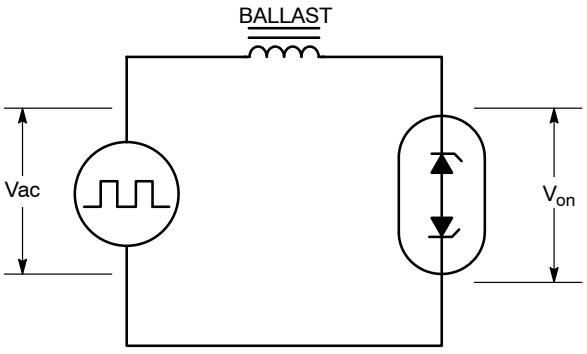


Figure 2. Typical Fluorescent Tube Equivalent Circuit in Steady State

Up to now, there is no model available to describe the start up sequence of these lamps. However, since most of the phenomena are dependent upon the steady state characteristics of the lamp, one can simplify the analysis by assuming that the passive networks control the electrical behavior of the circuit.

Obviously, this assumption is wrong during the time elapsed from V_{strike} to V_{on}, but since this time interval is very short, the results given by the proposed simple model are accurate enough to design the converter.

When a fluorescent tube is aging, its electrical characteristics degrade from the original values, yielding less light for the same input power, and different V_{strike} and V_{on} voltages.

A simple, low cost electronic lamp ballast cannot optimize the overall efficiency along the lifetime of the tube, but the circuit must be designed to guarantee the operation of the lamp even under the worst case “end of life” conditions.

As a consequence, the converter will be slightly oversized to make sure that, after 8000 hours of operation, the system will still drive the fluorescent tube.

Controlling the Fluorescent Lamp

As already stated, both the voltage and the current must be accurately controlled to make sure that a given fluorescent lamp operates within its specifications.

The most commonly used network is built around a large inductor, connected in series with the lamp, and associated with a bi−metallic switch generally named “the starter”. Figure 3 gives the typical electrical schematic diagram for the standard, line operated, fluorescent tube control.

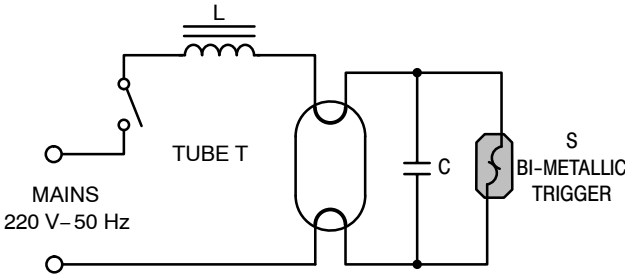


Figure 3. Standard Ballast Circuit for Fluorescent Tube

The operation of a fluorescent tube requires several components around the tube, as shown in Figure 3. The gas mixture enclosed in the tube is ionized by means of a high voltage pulse applied between the two electrodes.

To make this start−up easy, the electrodes are actually made of filaments which are heated during the tube ionization start−up (i.e,. increasing the electron emission), their deconnection being automatic when the tube goes into the steady state mode. At this time, the tube impedance decreases toward its minimum value (depending upon the tube internal characteristics), the current in the circuit being limited by the inductance L in series with the power line.

The starting element, commonly named “starter”, is an essential part to ignite the fluorescent tube. It is made of a bi−metallic contact, enclosed in a glass envelope filled with a neon based gas mixture, and is normally in the OPEN state.

When the line voltage is applied to the circuit, the fluorescent tube exhibits a high impedance, allowing the voltage across the “starter” to be high enough to ionize the neon mixture. The bi−metallic contact gets hot, turning ON the contacts which, in turn, will immediately de−ionize the “starter”. Therefore, the current can flow in the circuit, heating up the two filaments. When the bi−metallic contact cools down, the electrical circuit is rapidly opened, giving a current variation in the inductance L which, in turn, generates an overvoltage according to Lenz’s law.

Since there is no synchronization with the line frequency (the switch operates on a random basis), the circuit opens at a current level anywhere between maximum and zero.

If the voltage pulse is too low, the tube doesn’t turn ON and the start−up sequence is automatically repeated until the fluorescent tube ionizes. At that time, the tube impedance falls to its minimum value, yielding a low voltage drop across its end electrodes and, hence, across the switch. Since the starter can no longer be ionized, the electrical network of the filaments remains open until the next turn−on of the circuit.

We must point out that the fluorescent tube turns off when the current is zero: this is the source of the 50 Hz flickering

in a standard circuit. It's an important problem which can lead to visual problems due to the stroboscopic effect on any rotating machines or computer terminals.

To take care of this phenomena, the fluorescent tubes, at least those used in industrial plants, are always set on a dual basis in a single light spreader, and are fed from two different phases (real or virtual via a capacitor) in order to eliminate the flickering.

The value of the inductor L is a function of the input line frequency (50 Hz or 60 Hz), together with the characteristics of the lamp.

The impedance of L is given by Equation 1:

$$Z_L = L^*\omega \quad (1)$$

with: $\omega = 2^*\pi^*F$

F = in Herz L = in Henry Z = in Ohm

Computing the value of L is straightforward. Assuming a European line (230 V/50 Hz) and a 55 W tube (V_{on} = 100 V, V_{trig} = 800 V), then:

$$I_{RMS} = \frac{P_{tube}}{V_{on}} \quad (2)$$

$$I_{RMS} = 55/100 = 0.55\ A$$

To limit the steady state current, the impedance must be equal to:

$$Z = \frac{Line - V_{on}}{I_{RMS}} \quad (3)$$

$$Z = (230 - 100)/0.55 = 238\ \Omega$$

Therefore, the inductor must have a value of (assuming the pure Ohmic resistance of the total circuit being negligible):

$$L = \frac{Z}{2^*\pi^*F}$$

$$L = 238/(2^*\pi^*50) = 0.75\ H$$

In order to minimize the losses generated into the inductor by Joule's effect, the DC resistance must be kept as low as possible: this is achieved by selecting a current density of 4 A/mm^2 maximum for the copper.

However, the end value of the wire diameter used to manufacture the inductor will be limited by the cost, the size and the weight expected for a given inductor.

The trigger switch S is a standard device.

The electromechanical ballast has two main drawbacks:

a. Ignition of the lamp is not controlled.
b. Light out of the lamp flickers at the same frequency as the AC line voltage.

But, on the other hand, the magnetic ballast provides a very low cost solution for driving a low pressure fluorescent tube.

To overcome the flickering phenomenon and the poor start−up behavior, the engineers have endeavored to design electronic circuits to control the lamp operation at a much higher frequency. The efficiency (Pin/Lux) of the fluorescent lamp increases significantly as shown in Figure 4, as soon as the current through the lamp runs above a few kiloHertz.

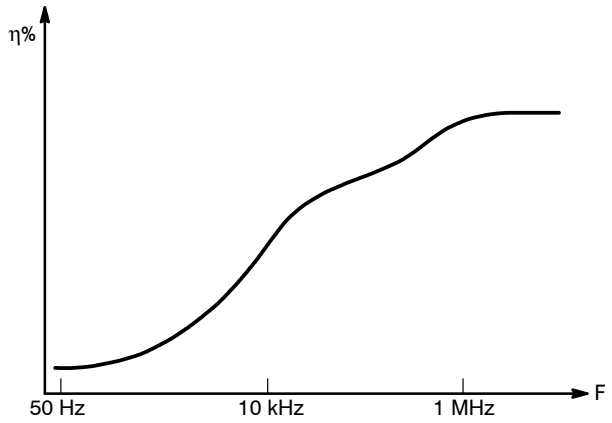


Figure 4. Typical Fluorescent Lamp Efficiency as a Function of the Operating Frequency

The electronic circuit one can use to build a fluorescent lamp controller can be divided into two main groups:

A. Single switch topology, with unipolar AC current, (unless the circuit operates in the parallel resonant mode).
B. Dual switch circuit, with a bipolar AC output current.

The manufacturers of the fluorescent lamps highly recommend operating the tubes with a bipolar AC current. This avoids the constant bias of the electrodes as an Anode−Cathode pair which, in turn, decreases the expected lifetime of the lamp.

In fact, when a unipolar AC current flows into the tube, the electrodes behave like a diode and the material of the cathode side is absorbed by the electron flow, yielding a rapid wear out of the filaments.

As a consequence, all of the line operated electronic lamp ballasts are designed with either a dual switch circuit (the only one used in Europe), or a single switch, parallel resonant configuration (mainly used in countries with 110 V lines), providing an AC current to the tubes.

A few low power, battery operated fluorescent tubes are driven with a single switch flyback topology. But, the output transformer is coupled to the tube by a capacitive network and the current through the lamp is alternating. However, the filaments (if any) cannot be automatically turned off by this simple configuration and the global efficiency is downgraded accordingly.

The dual switch circuits are divided into two main topologies:

A1 Half bridge, series resonant.
A2 Current fed push−pull converter.

The half bridge is, by far, the most widely used in Europe (100% of the so−called Energy Saving Lamps and Industrial applications are based on this topology), while the push−pull

is the preferred solution in the USA with around 80% of the electronic lamp ballasts using this scheme today (see typical schematic diagram Figure 5).

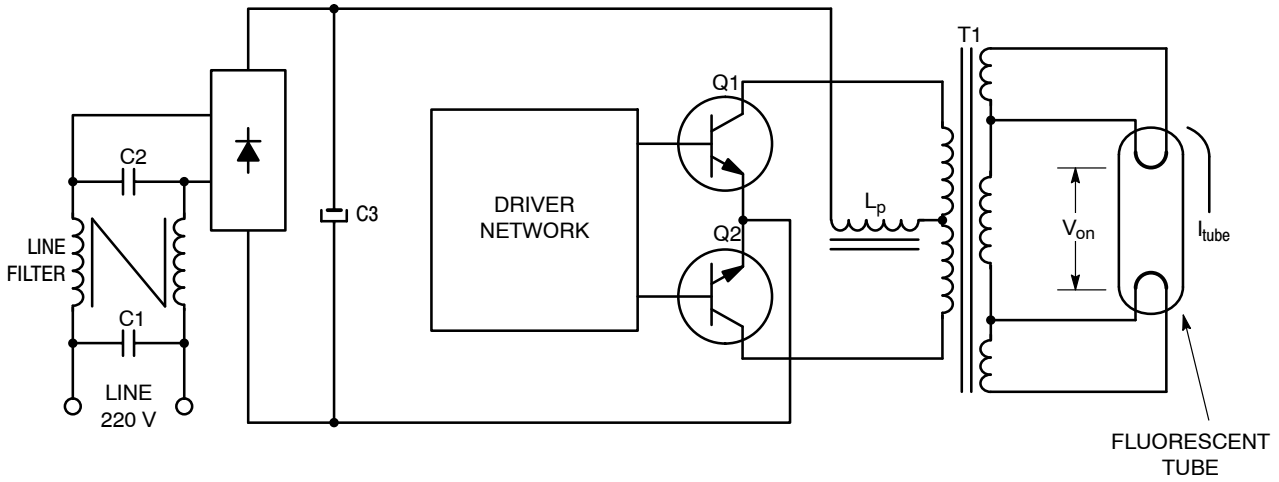


Figure 5. Typical Current Fed, Push−Pull Converter

Both of these topologies have their advantages and drawbacks, the consequence for the associated power transistors being not at all negligible as shown by Table 1.

Table 1.Main Characteristics of the Dual Switches Topologies

Parameters	Half Bridge	Push−Pull
$V_{(BR)CER}$	700 V*	1100 V to 1600 V*
Inrush Current	3 to 4 times I_{nom}**	2 to 3 times I_{nom}**
t_{si} window	2.60 μs−3.60 μs	1.90 μs−2.30 μs
Drive	High & Low side	Low side only
Intrinsic Galvanic Isolation	no	yes

Notes: * numbers are typical for operation on a 230 V line.
** I_{nom}: current into the transistors in steady state.

Push Pull Topology

The main advantage of the current fed push−pull converter, besides the common grounded Emitter structure, is the ruggedness of this topology since it can sustain a short circuit of the load without any damage to the semiconductors (assuming they were sized to cope with the level of current and voltage generated during such a fault condition). This is a direct benefit of the current mode brought by the inductor in series with the V_{CC} line. However, the imbalance in both the power transistors and the magnetic circuit leads to high voltage spikes that make this topology difficult to use for line voltage above 120 V. Additionally, it is not practical to dim the fluorescent tubes when they are driven from a push−pull circuit, the half bridge, series resonant topology being a far better solution.

The push−pull converter can be designed with either one single transformer, as shown in Figure 6, or by using a separate core to build the oscillator (see Figure 7).

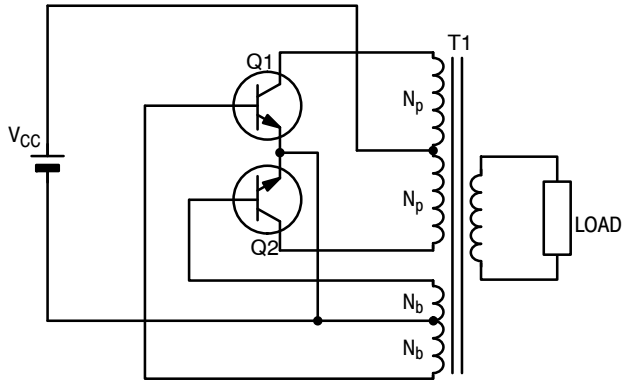


Figure 6. Basic Single Transformer Circuit

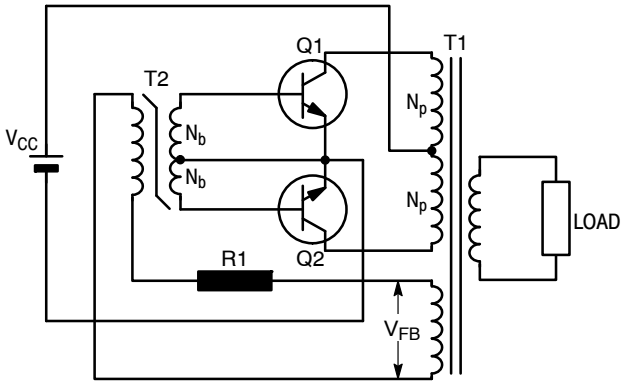


Figure 7. Basic Two Transformer Circuit

Single Transformer Basic Operation

The circuit uses the same core to drive the transistors and to supply the power to the load. Operation is based on the saturation of the core when the magnetic flux exceeds the maximum value the core can sustain. Although this is a very low cost solution, it is not commonly used for power above

a few tens of watts, because the global efficiency is downgraded by the dual mode operation of the output transformer (i.e., saturable and linear). Figure 6 gives the typical schematic diagram.

Two Transformer Operation

At high load currents and high frequency, the transformer requirements for the dual role of frequency control and efficient transformation of output voltage becomes a difficult problem in the single transformer design. For this reason, the two transformer design, depicted in Figure 7, is more advantageous. The operation of this circuit is similar to the one transformer case, except that only the small core T2 need be saturated. Since the magnetization current of T2 is small, high current levels due to transformer saturation magnetic flux are reduced significantly when compared to the one transformer design. Of course, the stresses applied to the power semiconductors are reduced in the same ratio. Another major advantage of the two transformer inverter design is that the operating frequency is determined by V_{FB}, a voltage easily regulated to provide a constant frequency to drive the power transformer.

Starting Circuit

In general, the basic circuits depicted in Figures 6 and 7 will not oscillate readily, unless some means is provided to begin oscillation. This is especially true at full load and low temperature. A simple, commonly used starting circuit is shown in Figure 8 In this design, resistors R1 and R2 form a simple voltage divider to bias the transistors to conduction before the oscillation starts.

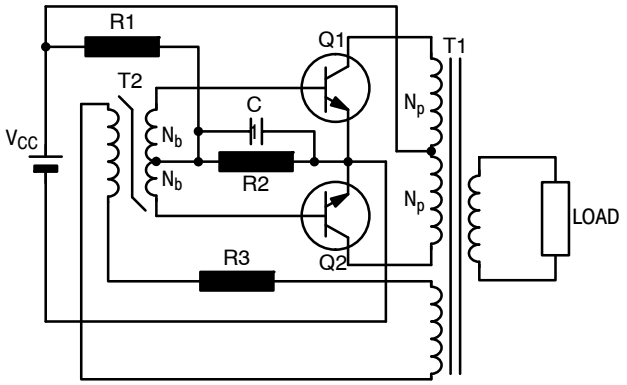


Figure 8. Basic Starting Circuit

Sinusoidal Output Inverter

The basic inverters discussed above have an output frequency and voltage directly proportional to the supply voltage, the output being a square wave. To get a sinusoidal output, or a tightly controlled frequency together with an easily regulated output voltage, the inverter must be modified from the basic circuit. A simple but efficient way, is to use a current fed topology, with an inductor connected between the primary of the output transformer and the supply line as shown in Figure 9. When the circuit is tuned with the capacitors C1 and C2, then the voltage across the switches is sinusoidal, yielding minimum switching losses into the silicon. Typical waveforms are given in Figure 10.

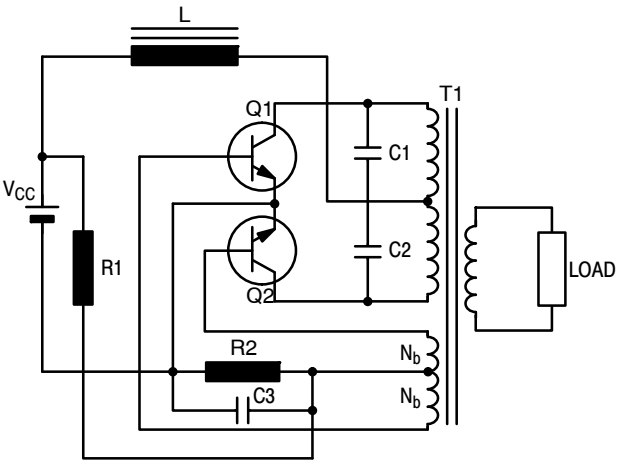
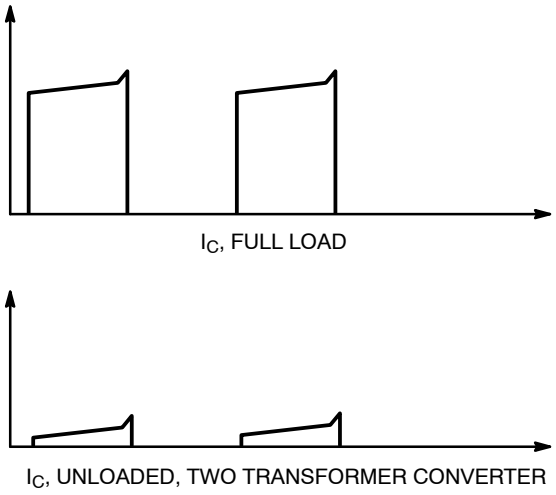


Figure 9. Typical Current Fed, Sinusoidal Output Converter



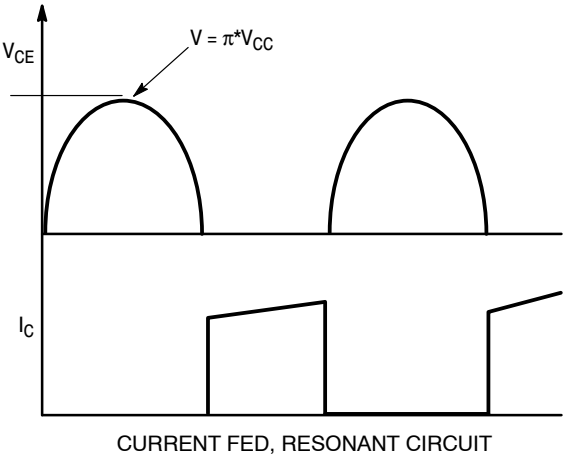


Figure 10. Typical Push−Pull Waveforms

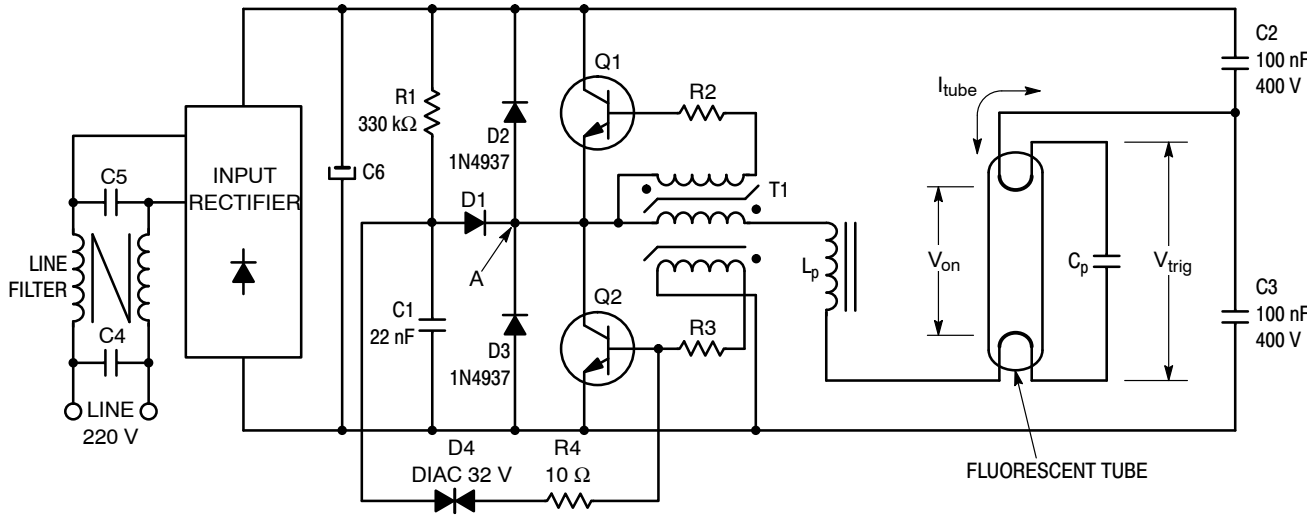


Figure 11. Typical Half Bridge Topology

Transistor selection criteria:

- Select the Collector current capability to sustain the peak value during either the unloaded or short circuit conditions.
- Select the $V_{(BR)CES}$ to avoid avalanche under the worst case conditions (i.e., high line, unloaded operation).
- Define the storage time window to make sure the devices will be tightly matched, thus minimizing the magnetic imbalance into the output transformer.
- Make sure the load line never goes outside either the FBSOA or RBSOA maximum ratings of the selected transistors.

HALF BRIDGE TOPOLOGY ANALYSIS

Basic Circuit

The basic schematic diagram of the half bridge, self oscillant topology is given in Figure 11. The two transistors Q1 & Q2 are the active side of the bridge, capacitors C2 & C3 being the passive arm.

Operation Description

The oscillations are generated by means of the saturable transformer T1. Since the two transistors are biased in the off state via the low Base−Emitter impedance provided by the secondaries of transformer T1, this circuit cannot start by itself, unless there is an imbalance between the high side and the low side of the converter. But, such an imbalance will severely downgrade the operation once the converter begins. Therefore, it is preferable to have a pair of matched transistors and to start the converter with the network built around the Diac D4, capacitor C1 and resistor R1.

When the line voltage is applied, capacitor C1 charges exponentially through resistor R1. When the voltage across C1 reaches the trig value of D4, the diac turns on, discharging C1 into the Base−Emitter network of Q2. This transistor turns on and the change in collector current (dI/dt) through the primary of T1, generates a voltage across each of the secondaries of T1.

By arranging the windings as depicted in Figure 11, the voltage V_{BB} is negative for the upper switch and positive for the lower one. This forward biases Q2 and the Collector current of this transistor keeps rising until the core of T1 saturates .

From electromagnetic circuit theory, the magnitude of the current in the secondaries of T1 is given by Equation 4:

$$I_B = I_C * \frac{N_p}{N_s} \quad (4)$$

Of course, the value of I_B must be large enough to fully saturate the transistor, even under worst case conditions:

$$I_B \geq \frac{I_C}{\beta} \quad (5)$$

with β = intrinsic current gain of the transistor

On the other hand, the V_{BB} voltage developed across the secondaries must be limited to a value lower than the $V_{(BR)EBO}$ of the transistors, otherwise the Base−Emitter junction goes in avalanche and the global efficiency can be downgraded.

Moreover, one must point out that, even if the transistor can sustain a Base−Emitter avalanche (assuming that the associated energy E_j is within the $V_{(BR)EBO}$ maximum rating), such a continuous mode of operation may make the transient and long term behavior of the converter more difficult to predict.

However, there is no problem if the Base−Emitter junction is forced into the avalanche mode during start−up because, under these conditions, the energy dissipated into the junction is very low and can be absorbed by the silicon.

The V_{BB} voltage is given by another electromagnetic equation:

$$V_{BB} = V_B * \frac{N_s}{N_p} \quad (6)$$

As a safety rule of thumb, in steady state $V_{BB} < V_{(BR)EBO}$.

The load being highly inductive,the Collector current will rise with a slope given by Equation 7:

$$\frac{dI_C}{dt} = \frac{V_{CC}}{L} \quad (7)$$

Start−up Sequence

The start−up voltage (V_{strike}) is generated by the series resonant network built with the inductor L and the capacitor C, the behavior of this network being predictable with Equations 8 to 15 given below.

The resonant frequency is:

$$f_o = \frac{1}{2 * \pi * \sqrt{(L * C)}} \quad (8)$$

The Quality Factor Q is given by :

$$Q = \frac{L * \omega}{\Sigma R} \quad (9)$$

with ΣR = sum of the DC resistance in the circuit.

This factor can also be expressed by Equation 10:

$$Q = \frac{1}{\Sigma R} * \sqrt{\frac{L}{C}} \quad (10)$$

Out of resonance, the impedance of the RLC series circuit is given by Equation 11:

$$Z = \sqrt{\left[R^2 + \left(L\omega - \frac{1}{C\omega}\right)^2\right]} \quad (11)$$

At resonance, the Lω term equals the 1/Cω and cancel each other:

$$L\omega = \frac{1}{C\omega} \quad (12)$$

Therefore, the impedance is minimum and equals the DC resistance:

$$Z = \Sigma R \quad (13)$$

At resonance, the current in the circuit is maximum and follows Ohm's law:

$$I = \frac{V_{CC}}{\Sigma R} \quad (14)$$

At the same time, the voltage across the capacitor is maximum as stated by Equation 15:

$$V_C = V_{CC}{}^*Q \quad (15)$$

The behavior of an R/L/C resonant circuit is depicted by Figure 12 Depending upon the L/R ratio, the curve is more or less flattened. This is described as the selectivity of the R/L/C network.

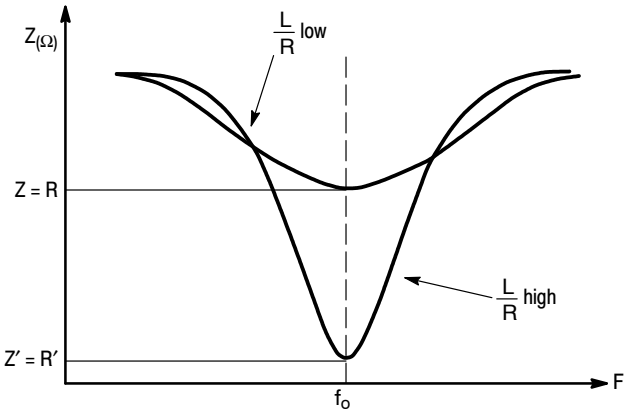


Figure 12. Typical R/L/C Series Network Behavior

The value of Q is dictated by the needs of the application, and the associated components must be sized accordingly. Since the inductor L is a direct function of the output power and operating conditions, the designer has no other choice than to adjust the values of capacitor C and resistor R to set up the Quality factor, keeping in mind the DC resistance of the filaments.

HALF BRIDGE DESIGN

Note: The design proposed herein assumes a 220 V−50 Hz input line voltage together with a single four foot 55 W tube. The V_{on} voltage is 100 V, the V_{trig} being 800 V. Nominal operating frequency: 35 kHz.

Designing a converter for the lamp ballast application is not very difficult, but there are many steps and iterations that must be performed first. Unfortunately, there is no accurate and simple model available, at the time of this publication, to simulate an electronic lamp ballast. However, the simple equivalent circuit given in Figure 13 is helpful to perform the first calculations when designing this kind of circuit.

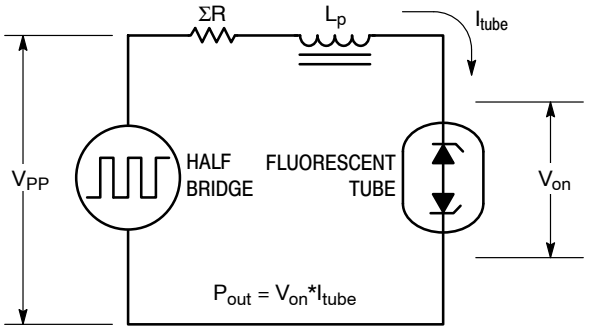


Figure 13. Basic Equivalent Circuit in Steady−State

The first step is to define the chopper frequency, since most of the critical parameters are dependent upon this criteria.

The topology being a self oscillant, Half Bridge will permit the design to make the manufacturing of the electronic circuit as simple as possible.

The selected core used to build the converter must meet the following specifications:

The core must:

a. be saturable
b. exhibit a BH curve as square as possible
c. be available at the lowest possible cost

By re−arranging Ampere's equation, we can compute the operating frequency for a self oscillant converter based on a saturable core:

$$F = \frac{V_P * 10^4}{4 * N_P * B_S * Ae} \quad (16)$$

With: V_P = voltage across the Primary winding
N_P = number of turns of the Primary
B_S = core saturation flux in Tesla
Ae = Core cross section in cm^2
F = frequency in Herz

Care must be taken, not to try to cut cost in the base drive network as the dynamic parameters of the power transistors will likely to not be optimized. In fact, the storage time will probably be greater than the computed operating chopper frequency.

The graph given in Figure 14 gives the typical storage time variation, as a function of the bias conditions, for a bipolar transistor. More detailed information is available from the designer's data sheet provided by ON Semiconductor.

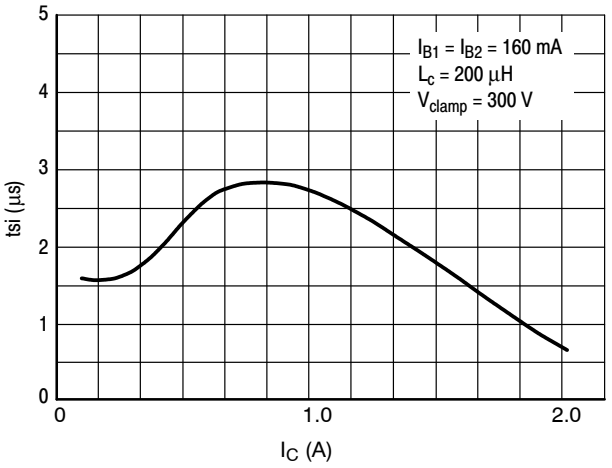


Figure 14. Typical Storage Time Variation as a Function of the Collector Current

The turn−off mechanism of the transistor is twofold:

a. When the current increases in the Primary winding N_P, the magnetic flux increases accordingly, and the operating point of the core moves toward the B_{sat}.

   At this point, the core goes into the saturation area and its relative permeability −mr− collapses from its nominal value down to unity.

   With a typical mr of 6000, this large variation makes the Primary/Secondary coupling nearly negligible and, consequently, the V_{BB} voltage starts to drop, yielding less forward bias to the Base network.

b. As the Collector current increases, the operating point of the transistor moves along its $H_{FE} = f(I_C)$ curve.

   In the meantime, the Base current is limited to the N_S/N_P ratio, as stated by Equation 4.

   One must remember that the V_{BB} voltage is a function of the dI_C/dt, the absolute magnitude of the Collector current I_C being irrelevant.

   When the V_{BB} voltage drops, the available Base drive decreases and the transistor will rapidly leave the saturation region. Consequently, the Collector current decreases and the dI_C/dt reverses from a positive going slope to a negative going slope.

   If the transistor is driven from a current transformer, then the same mechanism applies for the available Base current, as stated by Equation 4.

These two points are cumulative and, as soon as the primary current decreases, the core starts to recover from the flux saturation, the V_{BB} voltage (or the magnetically induced Base current) reverses, and the transistor will rapidly switch off the Collector current.

The oscillograms given in Figures 15 and 16 show the typical Base bias for a standard converter using this technique. Based on these oscillograms, it's clear that the turn−off mechanism, with typical timing values around 4 μs, is not negligible and must be taken into account during the design.

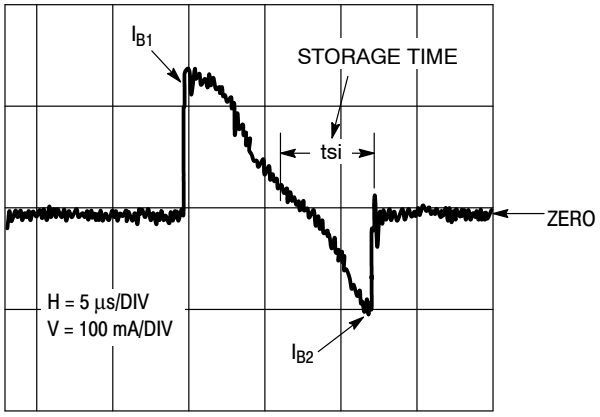


Figure 15. Typical Base Current Waveform

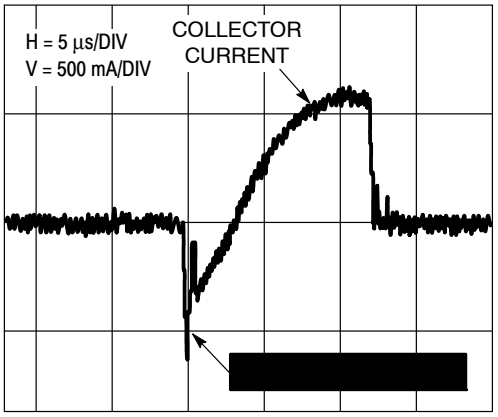


Figure 16. Typical I_C Waveform

Therefore, the practical operating frequency will be dependent upon the core used to build the saturable transformer T1, and the absolute value of the Collector current storage time (t_{si}). This is shown by Equation 17:

$$F = \frac{1}{T} + \frac{1}{2 * t_{si}} \qquad (17)$$

with : T = period depending upon core T1
t_{si} = storage time

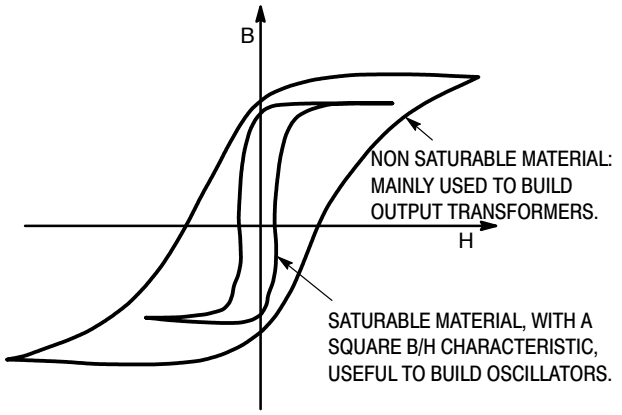
The factor 2 stands for the half bridge topology used.

The design of a saturable transformer is bounded by several parameters:

a. Magnetic material availability
b. Core shapes available (Toroids are preferred because they have the highest μr and square BH characteristic)
c. Manufacturing costs

The typical B/H curves given in Figure 17 are provided by the manufacturers of cores for the different material they may propose in their portfolio of products. Most of the time, the data sheets show the upper side of the curves, the characteristic being absolutely symmetrical on the X axis.

On the other hand, the shape of the curve, i.e. the B_{sat} value, can be controlled by using an air gap to increase the reluctance of the core. Of course, this is not possible for the toroidal cores.



Note: Drawing is not to scale.

Figure 17. Typical B/H Curves

To build the transformer, one can either use the data provided by the manufacturers of the cores, using the B=f(H) curves, or pre−define the type of core that would best fit the application.

This can be derived from Equation 18, which gives the minimum electromagnetic field needed to saturate a given core:

$$H_S = \frac{N_P * I_P}{I_E} \quad (18)$$

with : H_S = saturation field in A/cm
N_P = number of turns on the primary
I_P = current into N_P
I_E = effective core perimeter in cm

Since H_S must be higher than H_O (the intrinsic field sustainable by the material as defined by the data sheet), then one can compute the perimeter of the core, assuming a given number of turns, by rearranging Equation 8:

$$I_E = \frac{N_P * I_P}{H_S} \quad (18a)$$

Of course, in order to end up with lower cost, it's preferable to use a standard core and to run several iterations of the above equation, using N_P as a variable.

Since the current keeps increasing during the storage time of the transistor, one cannot use the calculated I_C peak value to saturate the core because, in this case, the current will be much higher than the expected one. On the other hand, it's not very easy to anticipate all of the tolerance at this point of the design; therefore, as a rule of thumb, the first pass can be made by using $I_P/2$ to compute the oscillator.

From the toroid data book provided by LCC, let us try the FT6.3 toroid (external diameter = 6.30 mm) with I_P = half I_C peak:

$$N_P = \frac{I_E * H_S}{I_P}$$

$$N_P = \frac{1.60 * 0.40}{0.35}$$

$$N_P = 1.82 \text{ turn}$$

Using the next available toroid, a FT10 (external diameter = 10 mm)

$$N_P = \frac{2.50 * 0.40}{0.35}$$

$$N_P = 2.85 \text{ turns}$$

The selection of a core from the 'off the shelf' standard products (see the preferred models given in Table 2, depends upon the expected frequency, the cost, and the availability.

As an example, let us select the T10 toroid with the A4 ferrite material, the μr being higher than 6000. To simplify the manufacture of this transformer we will make a first iteration with N_P = 3 turns, assuming V_P = 1 V across the primary.

The characteristic curves of this core show that the saturation flux is 510 mT at room temperature (T = +25°C), the cross sectional area being 0.08 cm^2.

These parameters yield a theoretical operating frequency of:

$$F = \frac{1 * 10^4}{4 * 3 * 0.51 * 0.08}$$

$$F = 20424 \text{ Hz}$$

Using, as a first analysis, a storage time of 5.5 μs for the power transistors, as given by the data sheet, the practical ON time (t_{on}) per switch will be:

$$t_{on} = \frac{1}{2 * 20424} + 5.5 * 10^{-6}$$

$$t_{on} = 29.98 \text{ μs}$$

yielding a typical operating frequency of:

$$F = 1/(2*t_{on})$$

$$F = 1/(2*29.98*10^{-6}) = 16677 \text{ Hz}$$

This is below the expected operating frequency as specified above.

Performing the same analysis with the FT6.3 toroid yields a typical operating frequency of 53 kHz, with N_P = 2 turns,

a value well within the expected range. This toroid will be the final choice for this design.

Table 2.Popular Available Toroids

Toroid	Ext. Dia. mm	l_E cm	A cm^2
FT6.3	6.30	1.60	0.032
FT10	10.00	2.50	0.08
FT16	16	4.00	0.20

Based on Equation 17, it's clear that the storage time (tsi) of the power transistors plays a significant role in defining the electronic lamp ballast. This dynamic parameter has two main impacts on the design:

a. operating frequency of the converter, hence the power delivered to the load as derived from Equations 1 and 3, will not be constant from one module to another.
b. the output inductor (L) can be driven with other than a 50% Duty Cycle, yielding a risk of saturating the core.

The capacitive side of the half bridge helps to prevent the saturation of the inductor if the D.C. is not 50% (point –b–). The mid point can float around half the V_{CC} value, but cannot compensate for the large variations one will have by using transistors not specifically designed for this circuit.

On the other hand, some low cost designs use a single capacitor to close the loop, yielding a high risk of saturation which, in turn, can lead to the destruction of the power switches by the resulting current under fault conditions.

Point (a) is worse for low power modules, particularly when the line voltage is 120 V, because even a small variation in frequency can either over or under drive the fluorescent lamp.

Consequently, the transistors used in such designs must have a tight dispersion of their dynamic parameters, a specified min/max window of the storage time is mandatory to achieve stable and reliable operation. Of course, this can easily be done by using two MOSFET devices, but the cost increases significantly, keeping the ON losses constant, compared to the BIPOLAR transistors. However, for low power/low line voltage applications, the MOSFET can provide a good alternative to this kind of electronic ballast design.

The next step is the selection of the power semiconductors, the main parameters to take into account are the input line voltage, the output power and the operating chopper frequency.

BREAKDOWN VOLTAGE

Even if the transistors never operate in the $V_{(BR)CEO}$(1) mode, one must select devices with a voltage rating above the rectified line voltage:

$$V_{(BR)CEO} > V_{line_{rms}} * \sqrt{2} \quad (19)$$

For a 220 V nominal line, this yields:

$V_{(BR)CEO} > 230 * 1.15 * \sqrt{2}$ (The 1.15 factor stands for the normalized European line variation).

$V_{(BR)CEO} > 374$ V

Since such a value is not available as a standard device, it is recommended that the designer use a 400 V rated transistor.

It is worthwhile to point out that, assuming the freewheeling diodes are properly selected (fast or ultra–fast type), the voltage across Collector–Emitter junction of each transistor shall not exceed the V_{CC} supply, limiting the RBSOA(2) operation within this voltage limit.

However, a simple low cost converter doesn't provide a well regulated V_{CC} supply and, under transient conditions, the DC voltage can rise well above the expected maximum value. Depending upon the input network, the V_{CC} can be as high as 600 V, yielding unexpected stresses into the semiconductors. Consequently, the power transistors must be sized to sustain the high FBSOA(3) and RBSOA generated by this V_{CC} transient.

Fortunately, as stated above, the Base–Emitter network is not open and, due to its low impedance during these transients, the transistors have a breakdown voltage capability extended to the $V_{(BR)CER}$(4) or $V_{(BR)CES}$(5) region. Figure 18 gives the typical voltage capability of a modern high voltage transistor, as a function of the Base–Emitter impedance.

Curves show the typical values for a BUL44 product at T_{case} = +25°C.

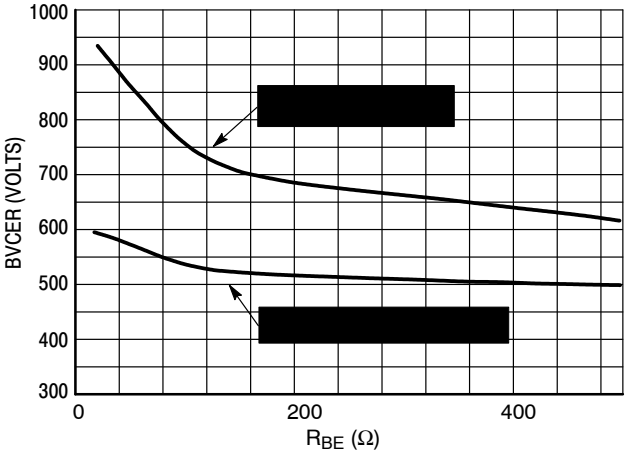


Figure 18. Collector–Emitter Breakdown Voltage as a Function of R_{BE}

COLLECTOR CURRENT RATING

The current capability of the power transistor is defined under two conditions:

a. start up
b. steady state

Since the start up value, together with the Quality factor Q, is dependent upon the steady state conditions, one must first compute the steady state value to derive the start up I_C peak. On the other hand, since the start up sequence lasts a

few hundredths of a millisecond, there is no need to select a transistor with this inrush current value as a nominal I_C capability. The designer will preferably use the steady state condition to define the power semiconductor.

In steady state, the rms current into the lamp will be:

$$I_{rms} = P_{out}/V_{on}$$
$$I_{rms} = 55/100 = 550 \text{ mA}$$

The peak current is:

$$I_P = I_{rms} * \sqrt{2}$$
$$I_P = 550 * \sqrt{2} = 770 \text{ mA}$$

During the start up, the Is current will be (assuming Q = 3):

$$I_S = I_P * Q$$
$$I_S = 0.77 * 3 = 2.31 \text{ A}$$

The selected transistor must have an operating current between 0.80 A and 1.00 A, and must be able to sustain a peak value in the 2.50 A to 3.00 A range, the H_{FE} being high enough to saturate the transistor even during the start up.

To keep the Base drive simple, and to minimize the ON losses, the H_{FE} at 0.80 A must be as high as possible. On the other hand, one must remember the influence of this parameter on the dynamic behavior of any bipolar power transistor, and make compromises accordingly.

As this point, we can make a pre−selection among the lamp ballast dedicated transistors developed by ON Semiconductor. From the preferred devices listed in Table 3, we'll select the BUL44D2, at a 1 A nominal operating current, for this design.

Table 3.Preferred Bipolar Power Devices for Lamp Ballast Applications

Devices	$V_{(BR)CEO}$	$V_{(BR)CES}$	I_C Nom	I_C Peak	Package
BUL35	250 V	400 V	2 A	4 A	TO−220
BUL43B	350 V	650 V	1 A	2 A	TO−220
BUD43B	350 V	650 V	1 A	2 A	TO−220
BUL44	400 V	700 V	1 A	2 A	TO−220
BUL44D2	400 V	700 V	1 A	2 A	TO−220
BUD44D2	400 V	700 V	1 A	2 A	DPAK
BUL45	400 V	700 V	2 A	4 A	TO−220
BUL146	400 V	700 V	3 A	5 A	TO−220
BUL147	400 V	700 V	4 A	6 A	TO−220
MJE18002	450 V	1000 V	1 A	2 A	TO−220
MJE18002D2	450 V	1000 V	1 A	2 A	TO−220
MJE18004	450 V	1000 V	2 A	4 A	TO−220
MJE18004D2	450 V	1000 V	2 A	4 A	TO−220
MJE18006	450 V	1000 V	3 A	5 A	TO−220
MJE18204	500 V	1200 V	2 A	4 A	TO−220
MJE18604D2	800 V	1600 V	1 A	3 A	TO−220
MJE18605D2	800 V	1600 V	2 A	4 A	TO−220

Table 4.Preferred MOSFET Devices for Lamp Ballast Applications

Devices	$V_{(BR)DSS}$	$R_{DS(on)}$	Package
MTD3N25E	250 V	2.00 Ω	DPAK
MTD5N25E	250 V	1.10 Ω	DPAK
MTD1N50E	500 V	8.50 Ω	DPAK
MTD2N60E	600 V	3.80 Ω	DPAK
MTP3N50	500 V	3.00 Ω	TO−220
MTP6N60E	600 V	1.20 Ω	TO−220
MTP8N50	500 V	0.80 Ω	TO−220

Based on the BUL44D2 data sheet, we will set the forced gain (β_f) at 5 as a reference value in steady state. With a collector current of 800 mA, this β_f yields a Base current of 160 mA minimum. The freewheeling diodes will be the MUR150, an UltraFast rectifier.

The Base drive of the transistors can be achieved under one of two modes:

a. current source
b. voltage source

Using a current source is a straightforward solution (Figure 19a): the saturable transformer T1 is designed to yield the Base current, according to Equation 20:

$$N_P * I_P = N_S * I_S \quad (20)$$

Since the values of I_P, I_S and N_P are already defined, one can compute the number of turns for each of the secondaries:

$$N_S = N_P * \frac{I_P}{I_S}$$

$$N_S = 2 * \frac{800}{160} = 10 \text{ turns}$$

It must be pointed out that such a circuit will keep the forced gain at the value defined by the designer (in this case $\beta_f = 5$), whatever the Collector current may be. Therefore, as already stated, one must make sure that the transistor has an intrinsic h_{FE} higher than the β_f, even under the high start−up current condition. On the other hand, it is difficult to improve the dynamic behavior of the transistor when the Base is driven from such a simple current source. A voltage mode will be preferred to improve the global efficiency.

Driving the device from a voltage source is achieved by using a capacitor to load the secondary, the Base having been fed through a series resistor as depicted in Figure 19b.

The windings are derived from the general Equation 21 used for transformers:

$$\frac{V_P}{N_P} = \frac{V_{BB}}{N_S} \quad (21)$$

The value of V_{BB} is bound on the high end by the Base/Emitter breakdown voltage, and by the amount of feedback, associated to the $V_{BE(on)}$, in the Base/Emitter network on the low end.

Assuming a $V_{BE(on)}$ of 1.10 V max and a 1.0 V drop in the Emitter resistor (V_{EE}), the V_{BB} value must be within the limits given here below:

$$R_B{*}I_B + V_{BE(on)} + V_{EE} < V_{BB} < V_{(BR)EBO} \quad (22)$$

The value of R_B must be as small as possible to minimize the losses in the drive network, but must be high enough to provide a feedback for the oscillator. A simple rule for selecting this resistor is to make it higher than the apparent dynamic impedance of the Base input:

$$Z_B = \frac{V_{BE(on)}}{I_B} \quad (23)$$

then: $Z_B = 1.10/0.18 = 6\ \Omega$

Let us select $R_B = 15\ \Omega$, then:

$V_{BB} \geq 15{*}0.18{+}1.10{+}1$

$V_{BB} \geq 4.80$ V

This value is well below the minimum guaranteed $V_{(BR)EBO}$, so we can round it up to 5.0 V to design the transformer:

$$N_B = N_P * \frac{V_{BB}}{V_P}$$

$N_B = 10$ turns

The wire diameter can be derived from the maximum current density of 4.50 A/mm2, or can be selected from the table given in the appendix.

The main advantage associated with voltage mode control is the capability to design a more efficient Base drive, thus improving the switching performance of the transistors. This is particularly useful for high power converters where the losses in the silicon must be minimized.

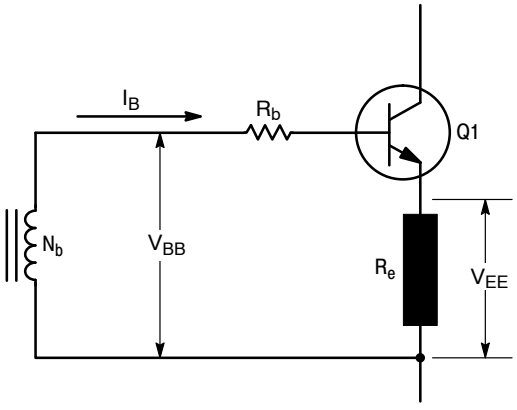


Figure 19. (a) Typical Current Mode Drive

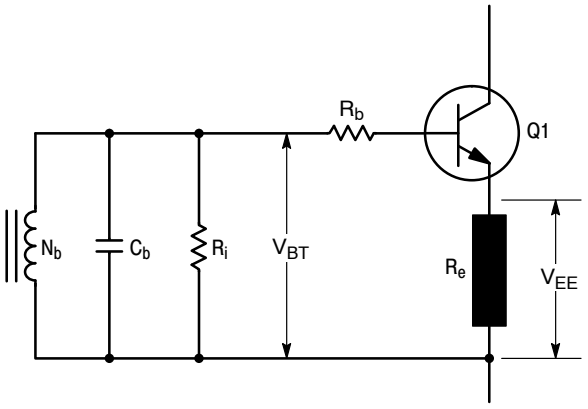


Figure 19.(b) Typical Voltage Mode Drive Circuit

At this point, the oscillator is nearly completed, but it will be necessary to refine the design based on the first results coming from the prototype.

As already stated, the steady state current in the fluorescent tube is limited by the external inductance, L_P. The value of L_P is derived from the impedance one must set in series with the lamp to get the right output power:

$$Z = \frac{V_{CC} - V_{on}}{2 * I_P} \quad (24)$$

$$Z = \frac{310 - 100}{2 * 0.35} = 300\ \Omega$$

This represents the impedance of the R/L/C circuit, according to Equation 11 given on Page 7. Depending upon the values of L and C, assuming the DC resistance R is negligible and the operating frequency is nominal, the current waveform will be truncated at either the peak value of the sine (worst case) or during the negative going slope. Obviously, in the second case, the turn off switching losses will be lower. The dynamic behavior of the transistor must be stable to make sure that the frequency stays within the predicted limits. Consequently, the power semiconductors

must have a tightly specified, low dispersion of the storage time from lot to lot .

Since C3 and C4 are assumed to have a negligible impedance, we can use Z to derive L_P:

$$L_P = \frac{Z}{2 * \pi * F} \quad (25)$$

$$L_P = \frac{300}{2 * \pi * 30000} = 1.60 \text{ mH}$$

On top of limiting the current in steady state, the inductance, associated to the capacitor C_P, builds the resonant circuit during the start−up sequence. Prior to computing the value C_P, one must make two assumptions:

a. The storage time will be shorter during start−up, as a consequence of lower hFE at high current.
b. The toroid will saturate more rapidly due to the higher dI/dt.

Consequently, the operating frequency will be higher, and the resonant network computed accordingly. Assuming that the start−up frequency is 60 kHz, then the value of C_P can be derived by rearranging Equation 8:

$$C_P = \frac{1}{4 * \pi^2 * F^2 * L_P} \quad (26)$$

$$C_P = \frac{1}{4 * \pi^2 * 60000^2 * 1.6 * 10^{-3}} = 4.39 \text{ nF}$$

This value not being standard, we will use 4.7 nF/1000 V. The resonant frequency is then:

$$F = \frac{1}{2 * \pi * \sqrt{(1.6 * 10^{-3} * 4.7 * 10^{-9})}} = 58 \text{ kHz}$$

The capacitors C3 and C4, used to build the passive side of the half−bridge, associated with L_P, must yield a resonant frequency well below the one used in steady state.

Let us make $f_o' < 5*F$, then

$$C = \frac{1}{4 * \pi^2 * f_{o'}^2 * L_P}$$

From an AC point of view, C3 and C4 are in parallel, thus C = C3+C4:

$$C = \frac{1}{4 * \pi^2 * 60000 * 1.6 * 10^{-3}} = 4.39 \text{ nF}$$

We will use the closest normalized value for C3 and C4:

$$C3 = C4 = C/2 = 220 \text{ nF}$$

The start−up network, built around R1/C1/D1/R4, must perform two main functions:

a. Provide enough Base current to Q1 to turn on the transistor.
b. Minimize the losses into this circuit.

To minimize the losses, let R1 = 330 kΩ , yielding 330 mW by Joule's effect into this resistor.

The Base current is given by the discharge of capacitor C1 into the Base/Emitter network. Since this is a low impedance circuit, the capacitor C1 must be sized to yield a pulse width large enough to get a significant current into the primary of T1. As a rule of thumb, the time constant shall be 5% of the ON time, in our case around 500 ns, yielding C1 = 22 nF.

Freewheeling Diodes

Across Q1 and Q2 are the freewheeling diodes D2 and D3. By providing a path for the inductive current, these devices clamp the spike voltage, as stated by the Lenz's law, to V_{CC} + V_F and −V_F when Q1 or Q2 switches off. Of course, since the dV/dt can be pretty high, D2 and D3 must have a fast turn−on time to make sure that the peak voltage will be clamped to a safe value. On the other hand, if these diodes are not used, then the negative going current flows into the Collector/Base junction of Q1/Q2, yielding uncontrolled charges. Moreover, if the voltage drop across the B/E network is higher than the $V_{(BR)EBO}$, the Base/Emitter junction will be avalanched and the associated current will generate extra losses into the silicon as stated by Equation 27:

$$P_B = V_{(BR)EBO} * I_A * dt * F \quad (27)$$

The worst case condition will occur when Q2 switches off. When the voltage at node A (see Figure 6) is negative and the B/E network time constant large enough, the Base/Emitter junction of the top transistor can be forward biased and a short circuit may be generated through Q1/Q2. This instantaneous power can be much higher than the transistors can sustain (the FBSOA characteristic) and both transistors can be destroyed in a few microseconds.

To avoid the risks described above, it is highly recommended that designers use the freewheeling diodes across each transistor.

Safety Circuit

EEC and UL regulations not withstanding, once the converter is running in steady state, the safety circuit can be limited to a single fuse to switch off the line if an overload occurs. A more sophisticated, but much more expensive way, is to use a self resetting thermal switch to open the DC line if the temperature inside the module becomes higher than a safe limit, usually between 85°C to 100°C.

However, during the start−up sequence, one must make sure that the fluorescent tube turns on, otherwise the converter can be damaged by continuously operating in the resonant mode. As stated on Page 7, the current can be very high and the losses in the silicon will rapidly exceed the maximum ratings of the power transistors used in the converter. Of course, a delay must be provided to yield enough time to warm up the filaments and trigger the tube.

Basically, the self oscillant circuit is turned off by grounding the Base drive of the bottom transistor. This is accomplished by using an SCR, or a small signal transistor, to sink the Base current to ground as depicted in Figure 20.

The Base drive can also be disconnected by using an extra winding across the drive transformer (T1, Figure 11), the SCR shunting all of the available current to ground: this technique switches off both Q1 and Q2 and the SCR can

memorize the failure mode until the user switches off the mains (see Figure 21).

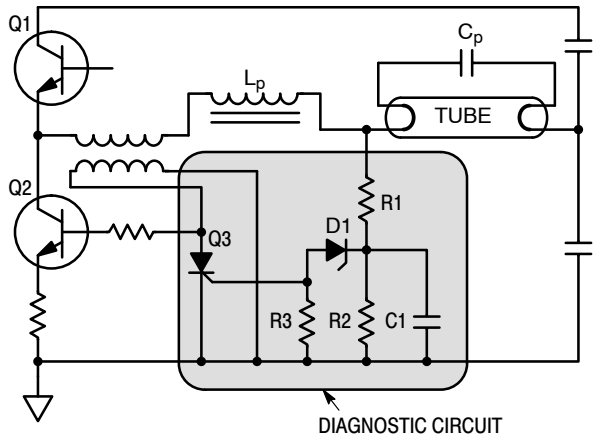


Figure 20. Turning Off the Converter by Sinking the Base Current to Ground

Another way is to open the Emitter to Ground path of the bottom transistor as depicted in Figure 22, but this is relatively complex and not cost effective.

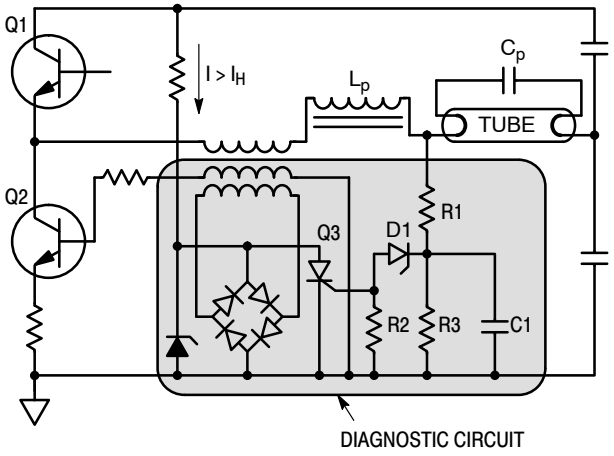


Figure 21. Fault Memorization

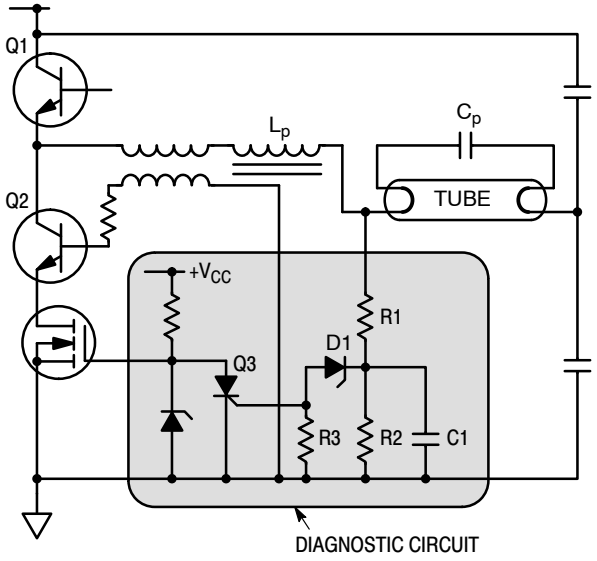


Figure 22. Using the Emitter Switch Off Technique to Stop the Converter

Power Factor Correction

All electronic lamp ballasts use a large bulk reservoir capacitor associated with a bridge rectifier, and therefore, can only draw power from the line when the instantaneous AC voltage exceeds the charge on the capacitor. As a result, the power factor is low (cosΦ around 0.50) and the harmonic content of the input current is very high. The European regulation EEC555−2 specifies both the minimum expected cosΦ value and the maximum harmonic content curve acceptable for any kind of electronic circuit connected to the AC mains. To cope with this regulation, one can use either a passive network (basically a large inductor together with a combination of rectifiers and capacitors) or an active circuit built around a boost converter. The passive Power Factor Correction (PFC) is economical, but bulky (because it operates at line frequency) and not very efficient with a typical cosΦ of 0.80.

Using an active PFC brings, in addition to a high cosΦ and low THD, a constant DC voltage across the electronic ballast which yields a constant power to the load, regardless of the line voltage. For example, let us point out that the European line voltage ranges from 185 V to 265 V, this is a ±15% variation from the nominal values. This can cause a change in light intensity large enough to be sensed by the human eye.

Circuit Description

The proposed PFC circuit is based on the MC34262, a dedicated IC, together with a power switch, in this case a MOSFET, arranged in a boost topology. Of course, the rectified voltage is no longer filtered by a large capacitor, the filter having been designed to damp the high frequency noise from the line (see typical schematic diagram in Figure 23).

This circuit feeds the lamp ballast converter and recharges the reservoir capacitor (i.e., C6, Figure 11). The MC34262 takes care of the 50 Hz signal and controls the MOSFET to make the envelope of the high frequency pulsed current as close as possible to the 50 Hz sinusoidal waveform. On the other hand, the output DC voltage is regulated (sensing is achieved through pin 1) and the current flowing into the power switch is monitored across the sense resistor connected between Source/Ground of Q1.

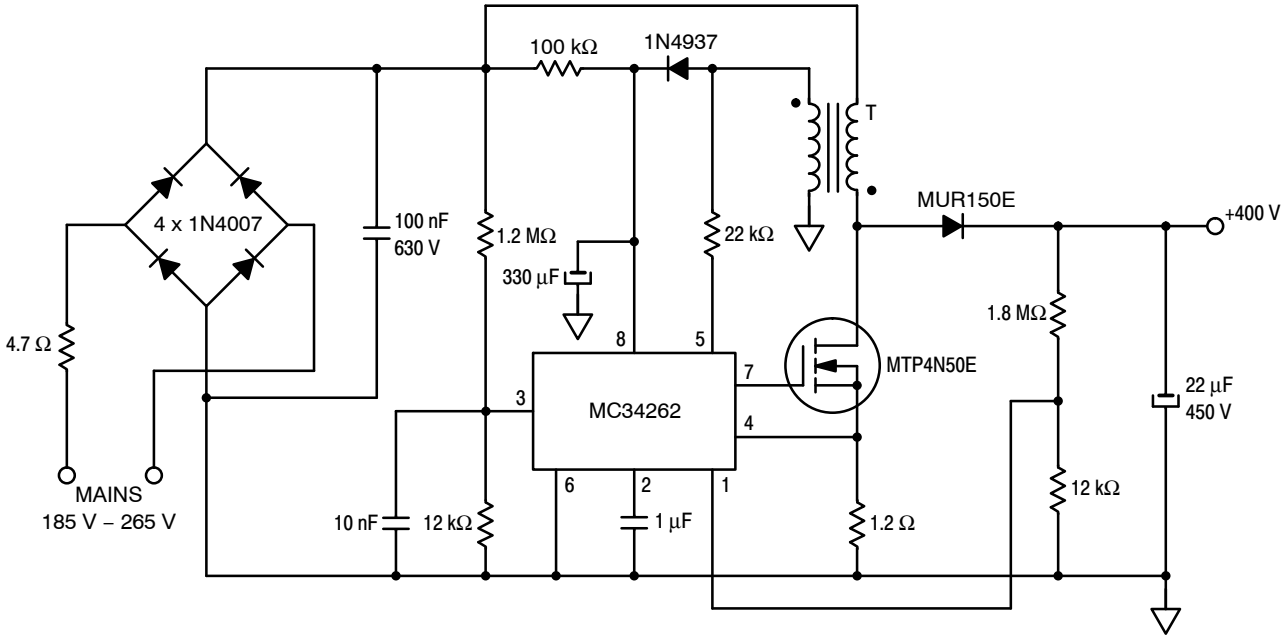


Figure 23. Typical PFC Circuit

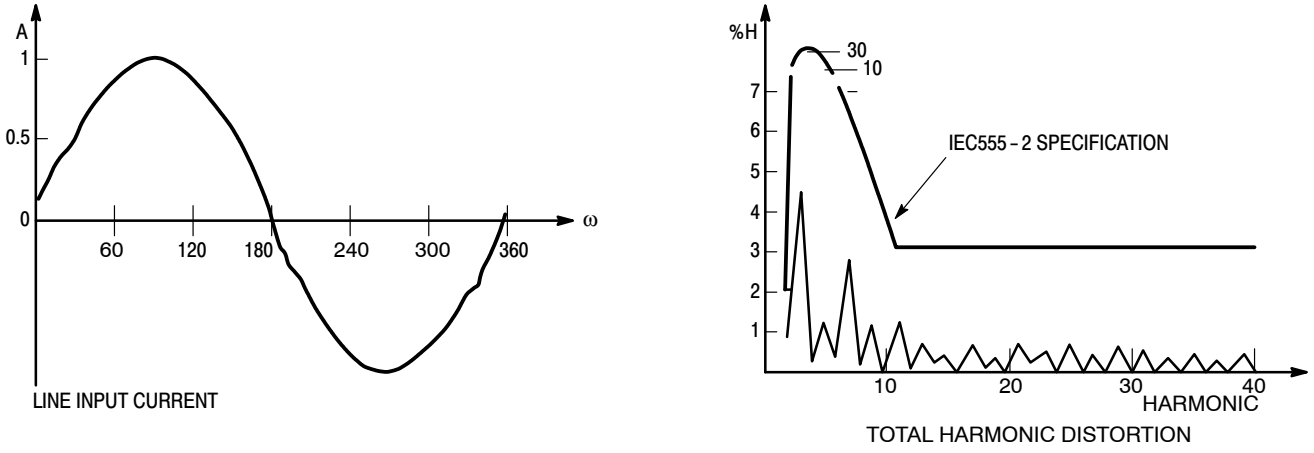


Figure 24. Typical THD of the Evaluation Board

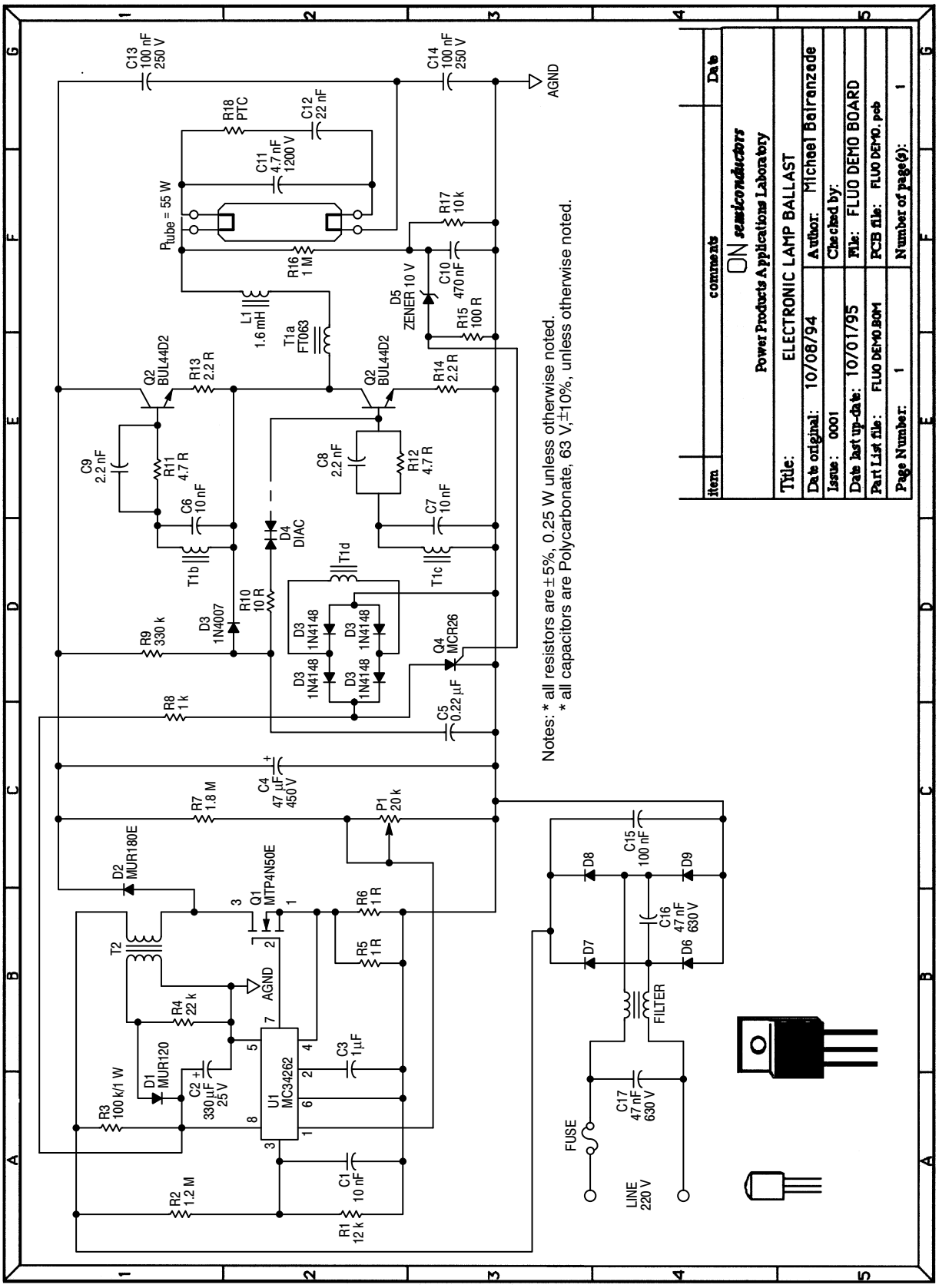


Figure 25. High End Fluorescent Lamp Ballast Demo Board

The performance is outstanding, with a cosΦ = 0.98 and a Total Harmonic Distortion (THD) well within the EEC555−2 regulations.

The MC34262 data sheet and the associated Technical Notes give all the information required to design a PFC loaded by a lamp ballast or any other type of electronic circuit.

In order to make sure that the PFC will not be damaged during the start−up sequence of the lamp ballast, the time constant of R1/C1 delays the operation of the MC34262 about three seconds, thus yielding a safe amount of time to operate both circuits. Of course, the DC voltage will not be constant during the start−up, but this is irrelevant since the converter is not yet running in steady state.

The demo board, designed by ON Semiconductor, includes a PFC circuit which drives the converter with a constant DC voltage. The circuit uses the newly developed BUL44D2 transistors in a standard self oscillant configuration. The performance is summarized below, and the parts list and printed circuit board layout are available in the appendix.

Table 5.Test Results

Nominal Operating Frequency:	40 kHz
Nominal Output Power:	55 W
Power Transistors Case Temperature:	65°C (steady state, free air)
CosΦ:	0.98
Global Efficiency:	85%

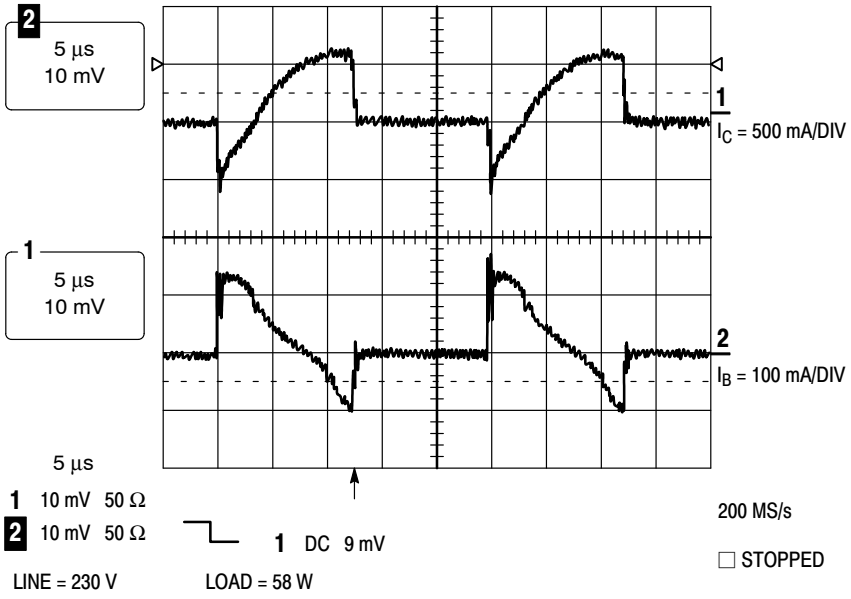


Figure 26. Collector and Base Currents in Steady State

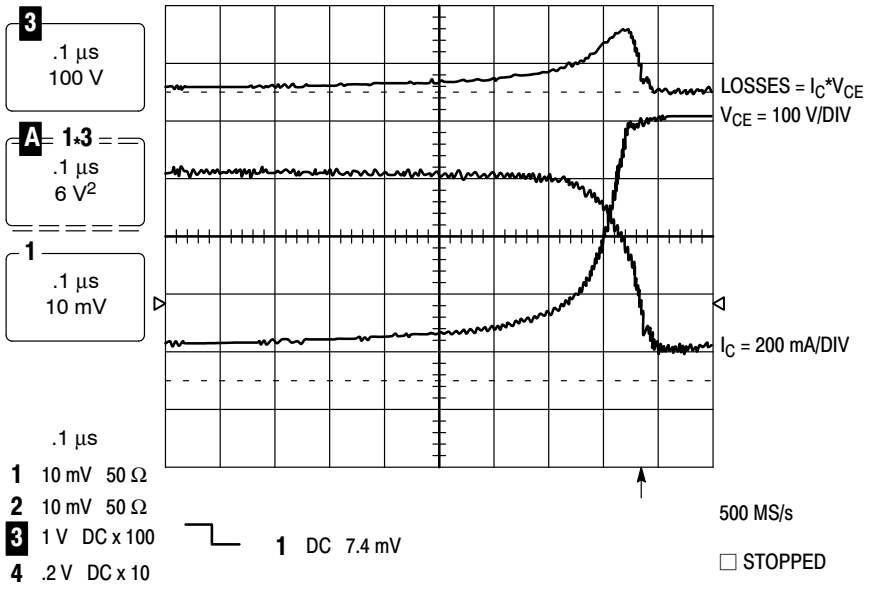


Figure 27. Switching Losses

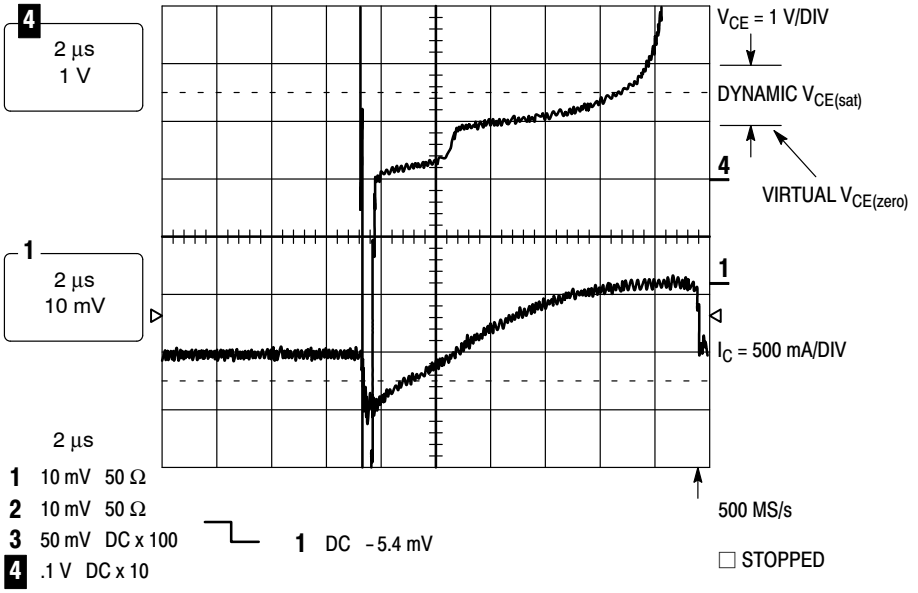


Figure 28. $V_{CE(sat)}$ Losses

Measuring the dynamic $V_{CE(sat)}$, under high V_{CE} value, is not straight forward because the input amplifier of the oscilloscope becomes saturated by the large V_{CE} voltage and cannot accurately sense the low saturation value when the transistor turns on.

For example, setting the oscilloscope to 500 mV/div will yield meaningless results because the instrument will not recover from the +400 V coming from the rail voltage, within less than 10 to 20 µs.

Several techniques exist to overcome this problem. The one used by ON Semiconductor is depicted in Figure 29.

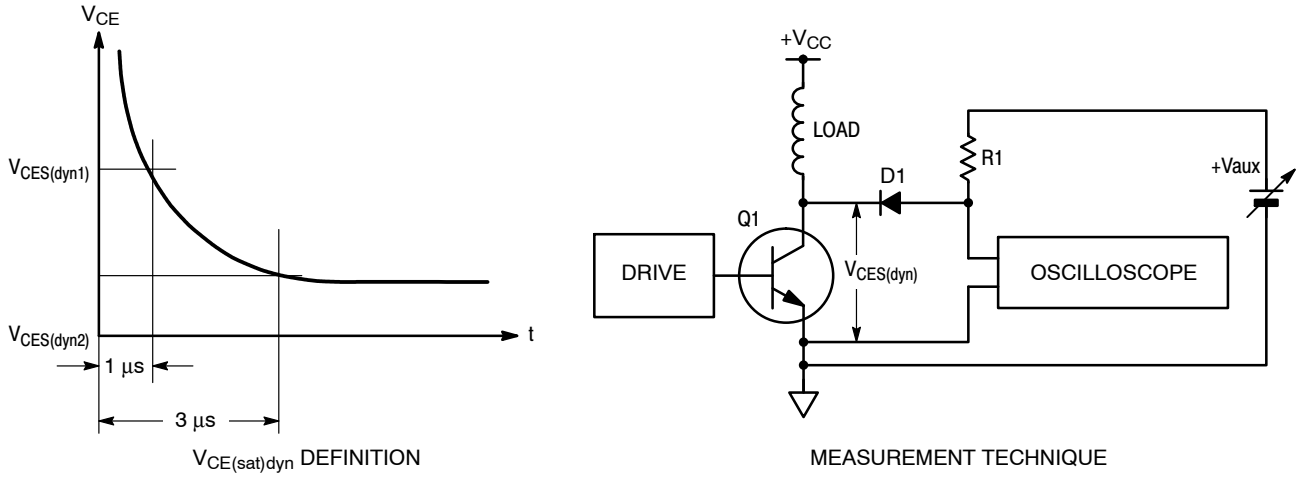


Figure 29. Dynamic $V_{CE(sat)}$

Diode D1 must sustain the peak voltage developed across the device under test (Q1). D1 must also have a very fast turn−on time. The Vaux value is adjusted between 10 to 20 V (depending upon the expected $V_{CE(sat)dyn}$), and the V_F of diode D1 is calibrated at the current forced by resistor R1 (usually I_F = 10 mA).

The $V_{CE(sat)dyn}$ is then calculated by subtracting the forward drop (V_F) from the voltage sensed by the oscilloscope.

The accuracy of this method is good enough to characterize and compare the behavior of several transistors. Additionally, to make this test reproducible, the dynamic $V_{CE(sat)}$ is specified under two timing conditions (see Figure 29): one microsecond and three microseconds after I_{B1} reaches 90% of its end value.

HIGH END DIMMABLE LAMP BALLAST

Since a voltage across the fluorescent tube lower than the V_{on} value would cause the tube to turn off, it's not practical to use the variations of V_{CC} to adjust the output power. In fact, using this basic technique yields a limited span of the dimming effect for the light output of the lamp.

On the other hand, one can use Pulse Width Modulation (PWM) of the current through the tube to dim the light, but care must be taken to balance the magnetic circuit.

Another simple, but efficient solution, is to use a variable frequency (with a constant 50% duty cycle) to drive the converter, keeping the series inductance constant.

Since the impedance of the output network is a function of the frequency (Equation 1), the power can be adjusted from zero to 100% using this technique.

As already stated, the storage time associated with the bipolar transistor is a key parameter for the electronic lamp ballasts. In the case of the dimmable circuits, this parameter is even more important because it will offset the operating frequency by a variable amount. Moreover, since the current varies as the output power is adjusted, the transistor bias varies as well and the Base drive must be designed to automatically compensate these variations.

There are three main keys to solving this problem:

a. Use standard Bipolar transistors with a Baker clamp network.
b. Use high voltage MOSFETs.
c. Use the newly developed H2BIP transistors.

Using the Baker clamp technique is straight forward, as shown by the schematic diagram given in Figure 30, but there are some drawbacks:

- the designer must use at least three fast diodes (two low voltage, one high voltage).
- the ON voltage of the power transistor is no longer the $V_{CE(sat)}$, but increases up to $V_{CE(sat)}$ + $V_{BE(on)}$, yielding much higher ON losses than those generated with a standard circuit.

  For example, the nominal $V_{CE(sat)}$ for a BUL44 is 0.20 V, @ I_C = 1 A, but the ON voltage rises up to 1.0 V when the device is driven with a Baker clamp. It's clear that with five times more power dissipated in steady state, a heatsink is mandatory to cool the transistor.
- the diodes associated with this solution are not free and they occupy space on the printed circuit board.

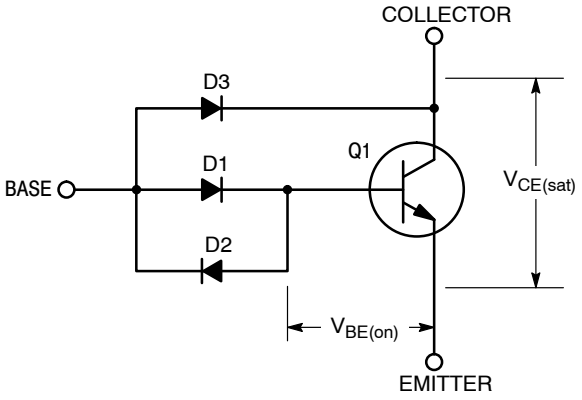


Figure 30. Typical Baker Clamp Circuit

Although this solution is sometimes used, it's not the preferred one to build a dimmable lamp ballast.

The MOSFETs solve all the problems associated with the storage time, even when the operating Drain current varies over a wide range, but the ON losses can be a limiting factor.

The $R_{DS(on)}$ of a MOSFET increases when the breakdown voltage $V_{(BR)DSS}$ increases (for a given chip size). The only way to reduce $R_{DS(on)}$ is to increase the die size, but this also increases the cost, thus limiting the use of MOSFETs to high end applications. Additionally, care must be taken to protect the Gate/Source from voltage spikes over ±20 V.

The H2BIP* device integrates an active anti−sat network into the die of a Bipolar power transistor, together with an antiparallel diode connected across the Collector/Emitter.

The basic concept is twofold:

a. Avoid the hard saturation, thus making the storage time as short as possible.
b. Avoid the storage time variation whatever the operating Collector current is, assuming that the intrinsic h_{FE} is higher than the forced I_C/I_B.

Of course, the t_{si} cannot be zero, but it is small enough to make this new technology a good choice to design an electronic lamp ballast.

Also, the ON voltage is very close to the $V_{CE(sat)}$ (no more than 100 mV are needed to activate the anti−saturation network), keeping the associated losses to a minimum, and the devices can sustain the high voltage needed in these applications.

- H2BIP: see new product paragraph.

Circuit Analysis

To adjust the output power of the fluorescent tube described in the half bridge design example, we will vary the frequency from 20 kHz to 180 kHz. Of course, the circuit can no longer be self oscillant and we'll use an oscillator to drive the power stage as shown in Figure 31.

The oscillator is built with the VCO integrated into U1 to make this module dimmable with a voltage source. The flip−flop U2 provides two out of phase signals to drive the Mosfet Q1 and Q2 which, in turn, control the power stage Q3/Q4. Transistors Q5 and Q6, respectively connected across Gate/Source of Q3/Q4, provide a low impedance path to rapidly discharge the input capacitance of the high voltage devices, avoiding the risk associated with poor drive conditions, particularly when the converter operates at high frequency.

The results of the tests performed in Toulouse are summarized in Table 6.

Table 6.Dimmable Lamp Ballast Test Results

P_{out} min	15 W
P_{out} max	65 W
F_{min}	22 kHz
F_{max}	170 kHz
CosΦ	0.60 (without PFC network)
MTP8N50E	0.98 (with MC33262based PFC)
	T_C = 40°C (steady state, in free air)

The time delays built with $R3/Ciss_{Q1}$, $R4/Ciss_{Q2}$ and $R5/Ciss_{Q3}$, $R6/Ciss_{Q4}$, make sure that none of these circuits will have a cross conduction during the nominal operation. For these reasons, one cannot use bipolar devices for Q1 and Q2.

The design of the series inductance L1 and resonant capacitor C2 is straightforward as already described for the self oscillant circuit. The transformer T1 is built on a T1600A toroid (external diameter 16 mm), the primary inductance being 1 mH. Assuming AL = 1600, the primary and secondary windings are 25 turns each.

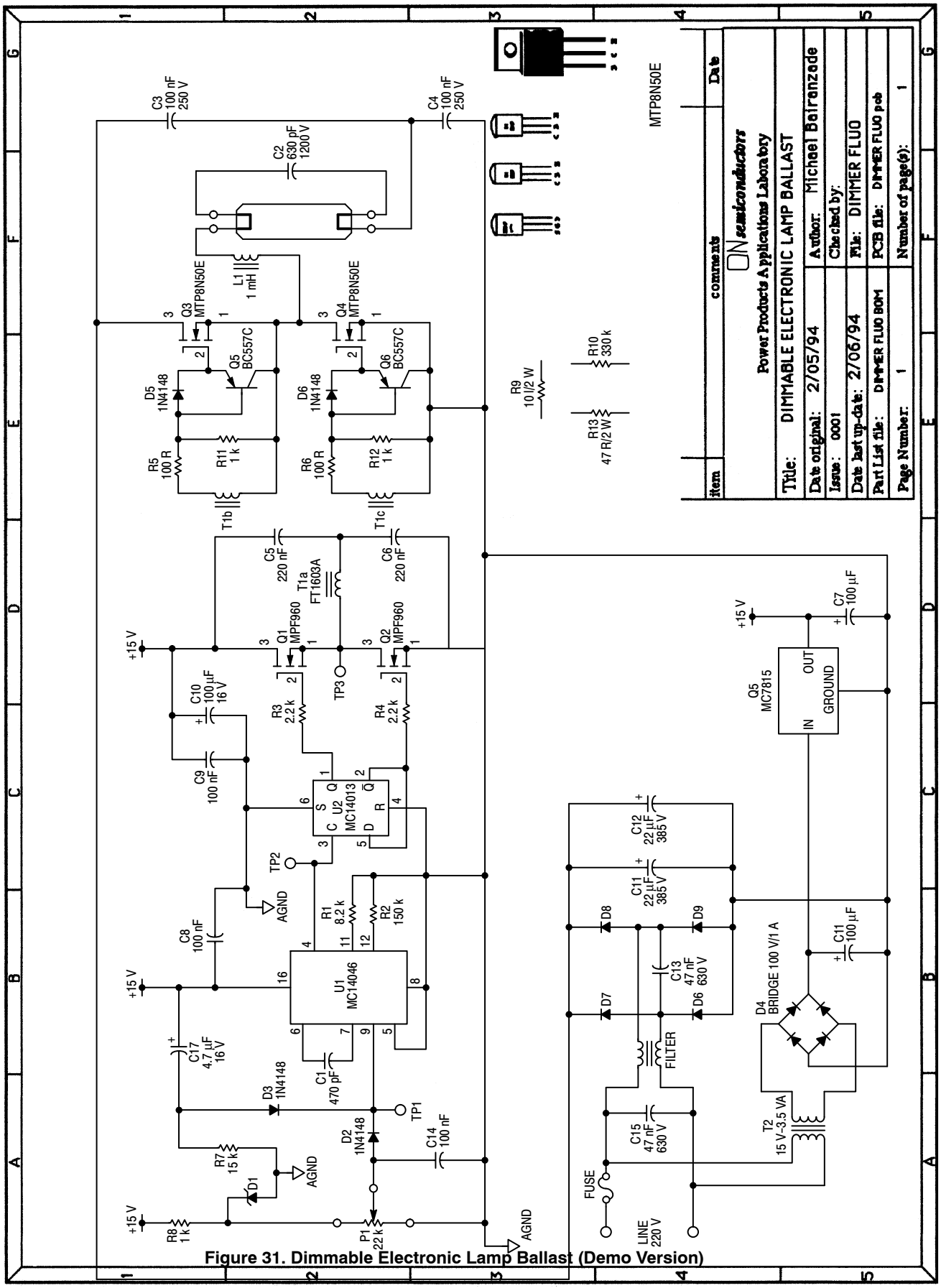


Figure 31. Dimmable Electronic Lamp Ballast (Demo Version)

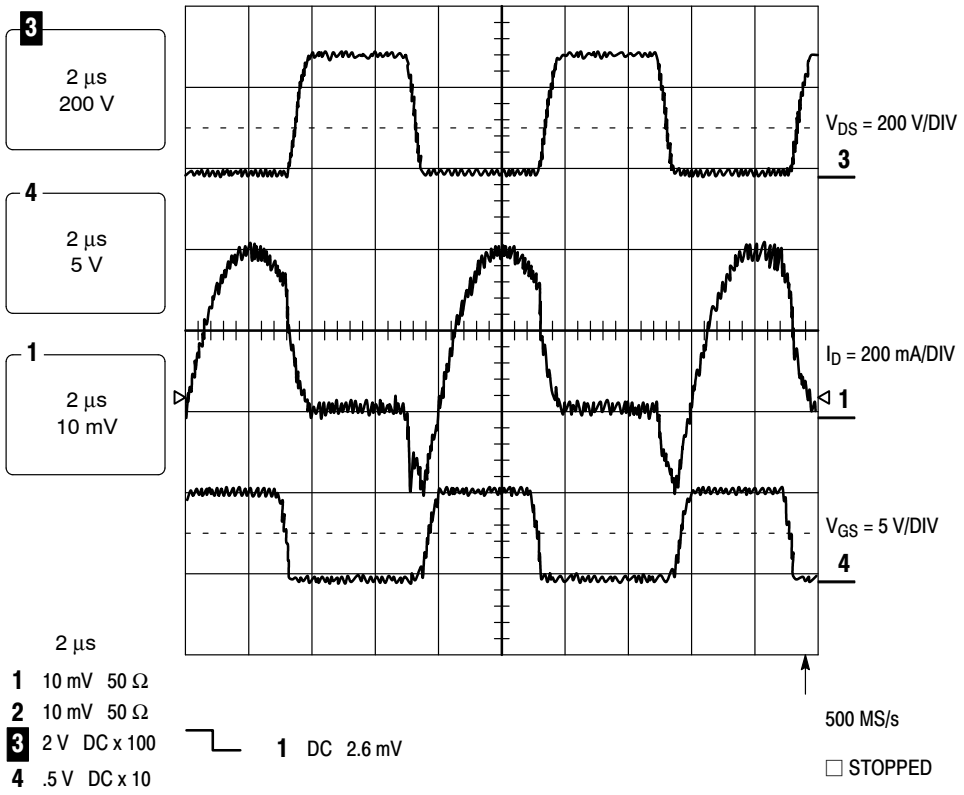


Figure 32. Drain Current and Gate Voltage in Steady State at $P_{out} = P_{max}$

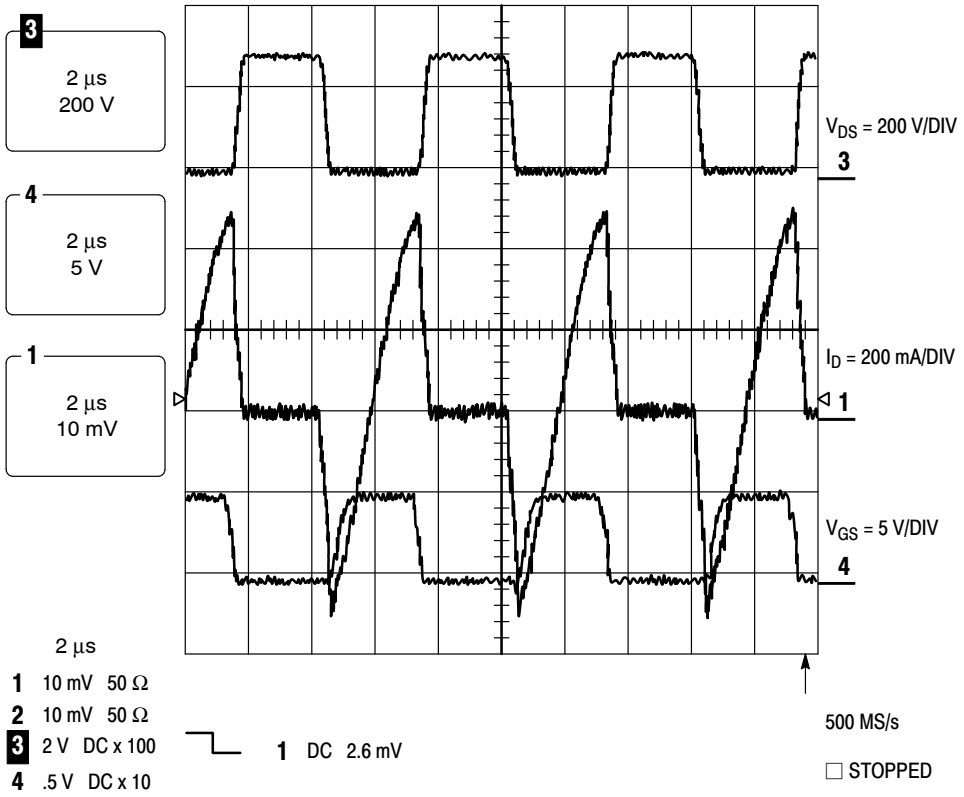


Figure 33. . Drain Current and Gate Voltage in Steady State at $P_{out} = P_{min}$

NEW POWER SEMICONDUCTORS

Integration

Since all of the half bridge based circuits use one freewheeling diode across Collector to Emitter of each power switch, the first step toward the development of new power devices was to integrate this diode into the silicon die of a Bipolar transistor.

Using state of the art technology for the design of power products, ON Semiconductor has taken this opportunity to build in more features, the aim being to make this transistor the best choice for the lamp ballast applications. The basic internal circuit is given in Figure 34a.

This device includes the freewheeling diode and an active anti−saturation network to accurately control the dynamic behavior (particularly the storage time) of the die.

This concept, patented by ON Semiconductor, has been called **H2BIP**, an acronym of **H**igh frequency, **H**igh gain **BIP**olar transistor.

The main features of this high voltage Bipolar transistor are high gain (h_{FE}), short, highly reproducible storage time, and a monolythic Collector/Emitter diode tailored to match the needs of the lamp ballasts.

This new family includes four standard products: BUL44D2, BUL45D2, MJE18004D2 and MJE18604D2, which will be extended to cope with specific requests. There are neither current nor voltage theoretical limits associated with this concept.

Table 7.Preferred H2BIP Devices for Lamp Ballast Applications

Devices	$V_{(BR)CEO}$	$V_{(BR)CBO}$	I_C Nom	I_C Peak
BUL44D2	400 V	700 V	1 A	2 A
BUL45D2	400 V	700 V	2 A	4 A
MJD18002D2	450 V	1000 V	1 A	2 A (under development)
MJE18004D2	450 V	1000 V	2 A	4 A
MJE18604D2	450 V	1600 V	2 A	4 A
MJE18605D2	450 V	1600 V	3 A	5 A

Note: The BUL44D2 is available in DPACK under BUD44D2 name.

These devices can be used either for new designs, or as drop−in replacement parts in current designs. In existing circuits, the designer might have to tune the Base/Emitter network in order to get the full benefit of the H2BIP.

To understand the operation of the H2BIP technique, one must first assume that the forward Base current is large enough to force an equivalent transistor into the saturation region for a given Collector current. As an example, let us assume $I_C = 1$ A, $I_{B1} = I_{B2} = 200$ mA and the intrinsic h_{FE} of the transistor equal to 15 min at $I_C = 1$ A. In this case, a standard transistor will be forced in to hard saturation as a consequence of the large Base current used to bias the junction, yielding a large and uncontrolled storage time. To solve this issue, the H2BIP product will sink to the Emitter node all of the drive current as soon as the voltage difference between Collector/Base of the main transistor is negative enough to forward bias the PNP connected across its Base/Emitter junction. This is depicted in Figure 34b. Using the above bias conditions, $I_B = 1/15 = 66.6$ mA and the PNP will sink to ground the extra 133.4 mA, yielding a mode of operation in the quasi saturation region. This results in the shortest and highly reproducible collector current storage time. Since this mechanism will exist for a Collector current from $I_C = I_{B1}$ up to $I_C = \beta \times I_{B1}$, the dynamic behavior of the transistor will be nearly constant as shown in Figure 35.

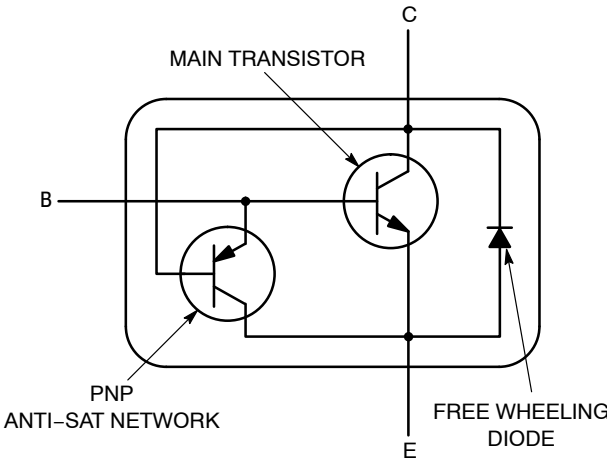


Figure 34. (a) Basic H2BIP Internal Circuit

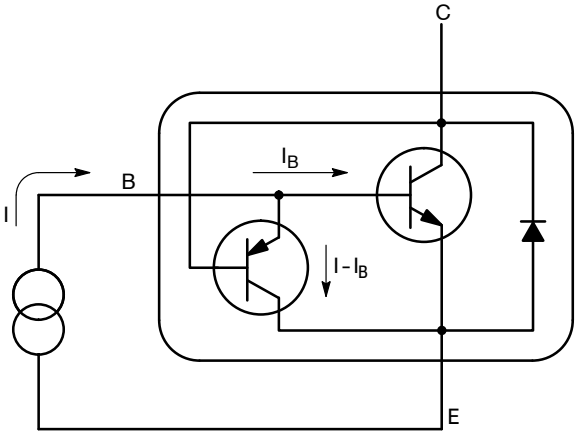


Figure 34.(b) Basic Operation

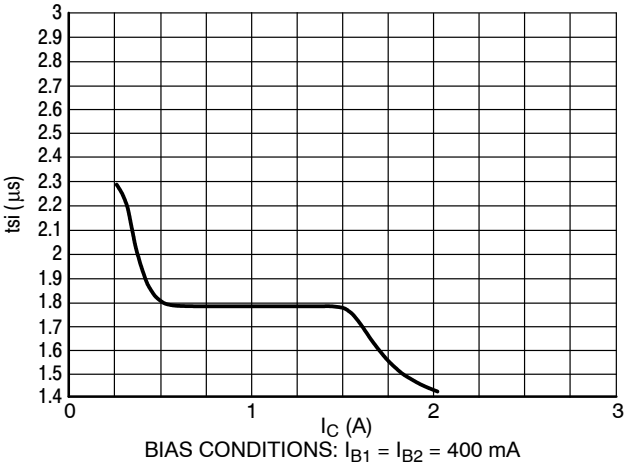


Figure 35. t_{si} = f (I_C) at I_{B1} = I_{B2} = Constant

Using a feedback resistor in the Emitter node of each transistor yields a more stable operation over the operating temperature range as depicted by the curves given in Figure 36.

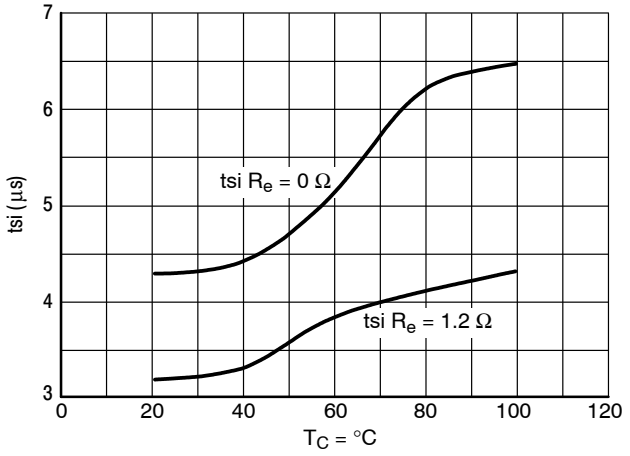


Figure 36. t_{si} = f (T_C) at I_C = Constant

A typical application is demonstrated in Figure 37.

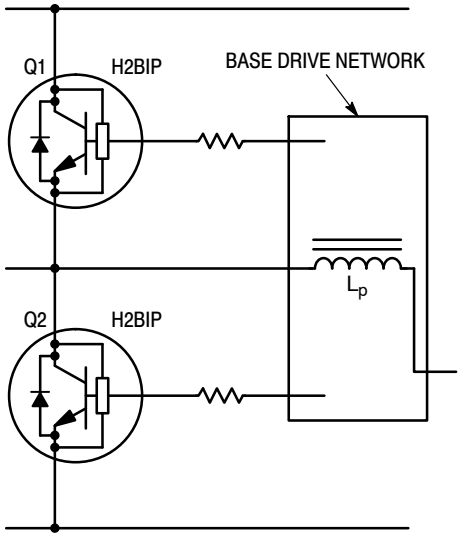


Figure 37. Typical H2BIP Application Circuit

Another possibility is the integration of the R_b resistor, the R_e, or both (see Figure 38). The only problem is the accuracy of any of these resistors. As ON Semiconductor doesn't perform any laser trimming during the wafer processing of power discrete devices (in order to keep the associated costs to a minimum), the accuracy of these resistors is limited to ±30% with a temperature coefficient in the 5000 ppm range. These tolerances are incompatible with electronic lamp ballast applications and, unless the designer accepts the associated drawbacks, no further work will be carried out for these kinds of devices.

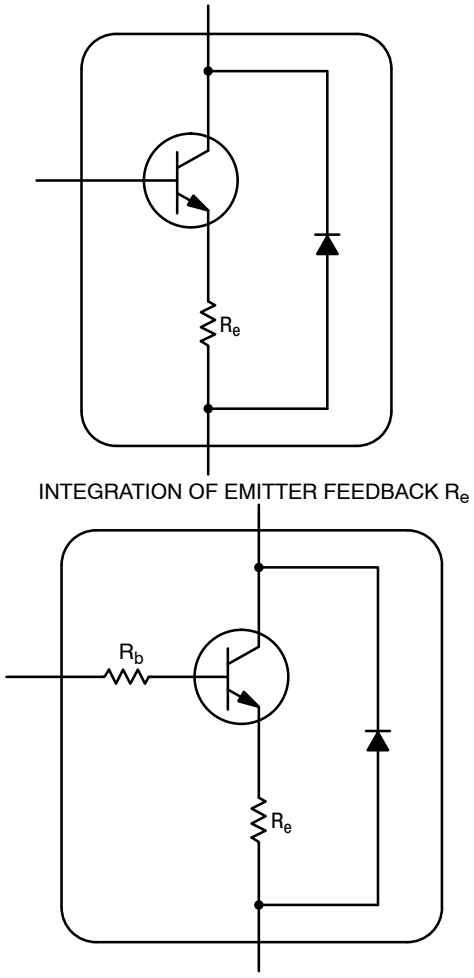


Figure 38. Bias Resistor Integration

The second major integration, already performed by ON Semiconductor, concerns the MOSFET. In a standard converter based on such semiconductors, the designer must provide during the turn−off time a low impedance path to discharge the input capacitance (C_{iss}). Since the global efficiency is expected to be as high as possible, the phase shifter network connected to Gate/Source, usually has a relatively high impedance (several kΩ). The switching performance of the MOSFET might be poor enough to justify the use of extra components to avoid storage time like phenomena and to achieve fast Drain current fall time. See the typical schematic diagram Figure 39.

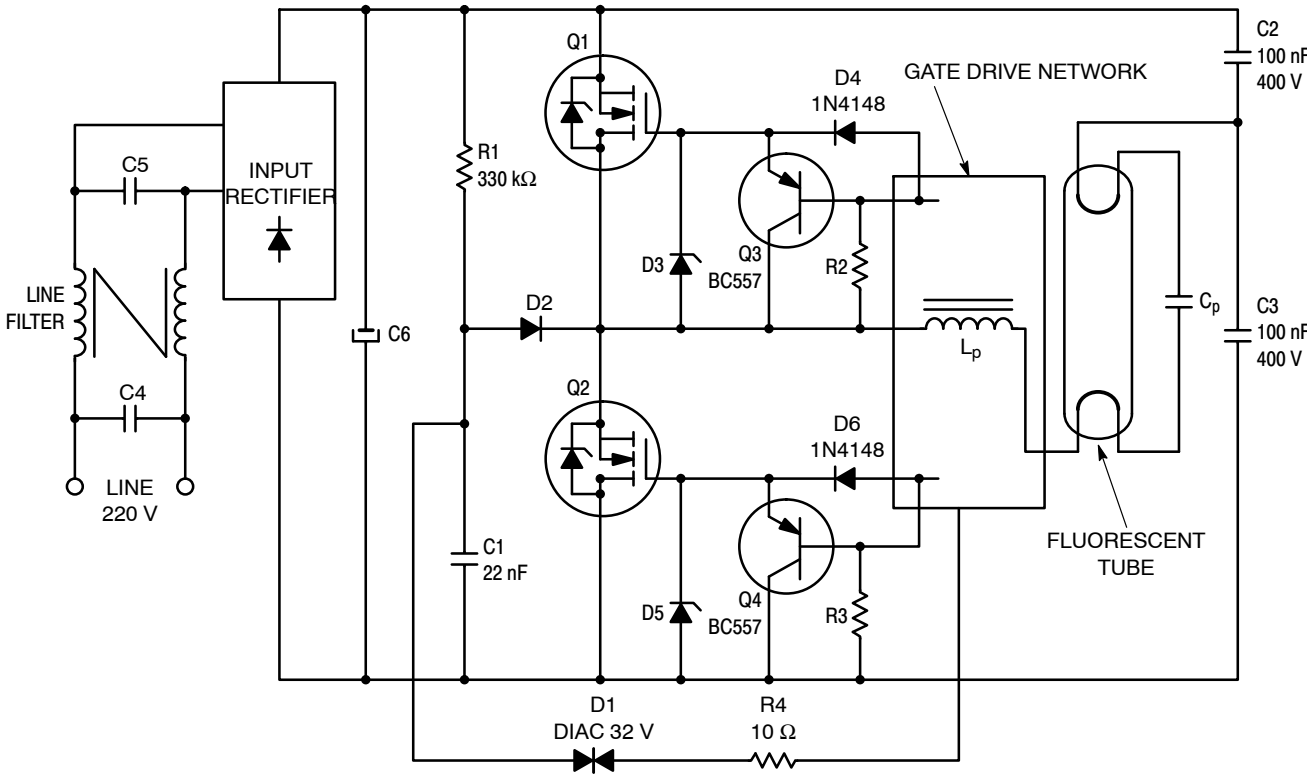


Figure 39. Typical MOSFET Application

This circuit works fine, but the four extra components for each power MOSFET (Q3/D3/D4/R2 for Q1 and Q5/D5/D6/R3 for Q2) take up significant space on the pcb, the total cost is not negligible and, more over, using standard transistors for Q3 and Q4 can lead to uncontrolled operation of the module as a consequence of the very large gain dispersion of these parts.

By using an existing process called Smart Discrete™, ON Semiconductor has integrated this sub circuit into the die of the MOSFET, making the device driveable from high impedance. This family of products is called **ZPCMOS**, an acronym for **Z**ero **P**ower **C**ontrolled **MOS**FET, the basic internal circuit is shown in Figure 40.

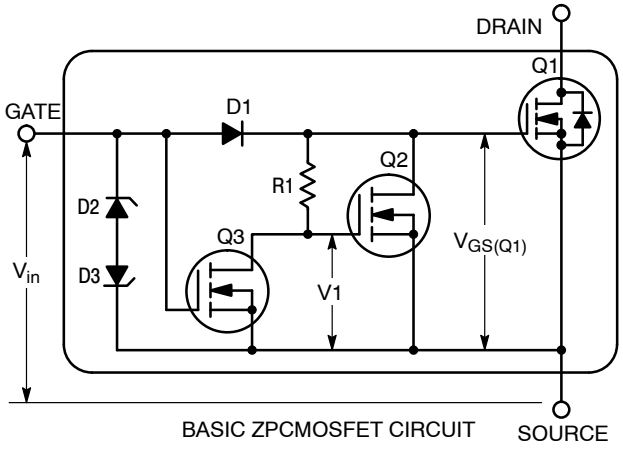


Figure 40. Basic ZPCMOS Internal Circuit

This device can be driven from any network. The turn off time is independent of the impedance connected Gate to Source, the value of resistor R1 being large enough to keep the steady state Igs current below 100 μA. The ZPCMOS can be used in existing circuits, assuming that the electrical parameters are compatible, as a drop−in replacement solution to improve the overall efficiency of a given application. Figure 41 demonstrates the net savings, in terms of component counts, brought by the ZPCMOS in a lamp ballast application.

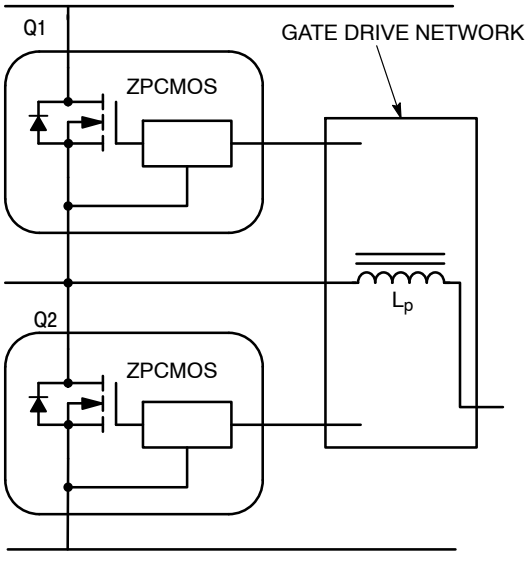


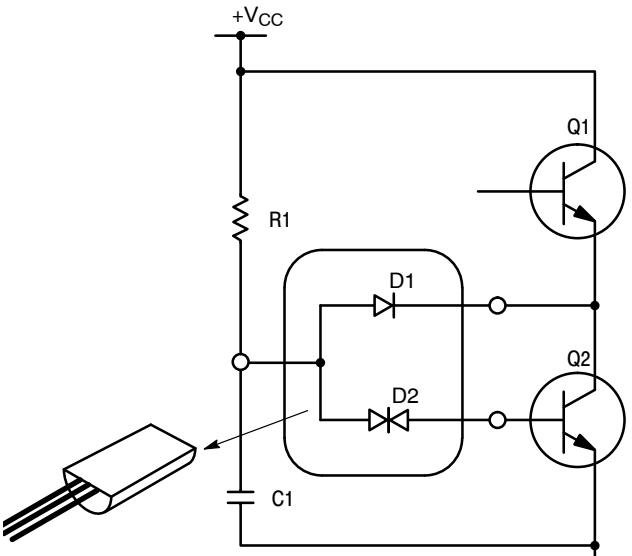
Figure 41. Typical ZPCMOS Drive

The application is assumed to be the same as the one described in Figure 19.

For example, a demo board built with two ZPCMOS is 15% smaller than the circuit using the standard MTD5N25E devices, saving two passive and six active parts in the converter.

Most of the electronic lamp ballasts use a start−up network built around a Diac with associated clamp diode. This circuit is automatically disconnected once the converter is running .

The integration of these two components is now evaluated to bring a simple, low cost TO92 or SMD packaged device to perform this function. Figure 42 gives the typical circuit.



SINGLE TO92 INTEGRATED CIRCUIT
Q1 AND Q2: HALF BRIDGE CONVERTER
D1: 500 V/0.050 A
D2: DIAC 27 TO 32 V
R1: 220 kΩ TO 470 kΩ 1/4 W
C1: 22 nF−100 V

Figure 42. Start−Up Network Integration

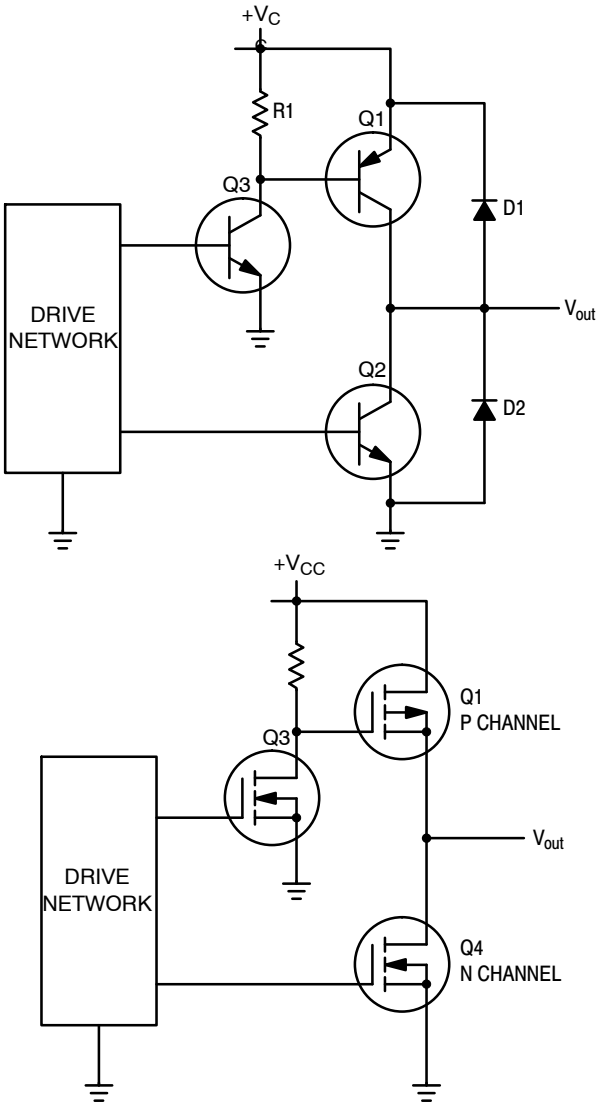


Figure 43. Compound Output Basic Circuits

Other Configurations

The compound circuit described in Figure 43 is an example of how to drive the top transistor in the half bridge topology (the Gate or the Base floats at several hundredths of a volt above ground). Unfortunately, it is much more expensive than the usual network used in electronic lamp ballasts. The reason being, besides the extra transistor, there is a need for a fast, high voltage PNP (or P−channel), a device nearly two times larger than the matched NPNs. This is a consequence of the lower mobility of the carriers into the P material compared to that achieved in the N material (everything else being constant).

Therefore, even if this type of power product is manufacturable, it is unlikely that there will be many chances to develop such devices as the associated cost will not be compatible with the lamp ballast market.

High Voltage Integration

With an end product power range from 5 W to 140 W, it is not possible to design a cost effective circuit with the power transistors built−in, such an I_C would be either over−sized for the low power modules, or marginal for the high end ones.

On the other hand, since the end applications of electronic lamp ballasts can be split into two main families (Compact Fluo and Industrial), a much more flexible solution is to make the driver as intelligent as possible, and leave the power switches outside the silicon.

Although, as already stated, it's probably not a feasible solution to integrate all of the converters for the industrial applications. The low output power together with the strong trend toward miniaturization, make the Compact Fluo Lamp a good candidate to integrate as much as possible of the electronic circuit for this type of product. However, in order

to keep the costs compatible with this market, it is preferable to leave the power switches outside the I_C, the half bridge being built either with two small footprint packages (DPAK, SOT223), or into a single SOIC (assuming that the losses can be held to a minimum, avoiding the risk of high junction temperature).

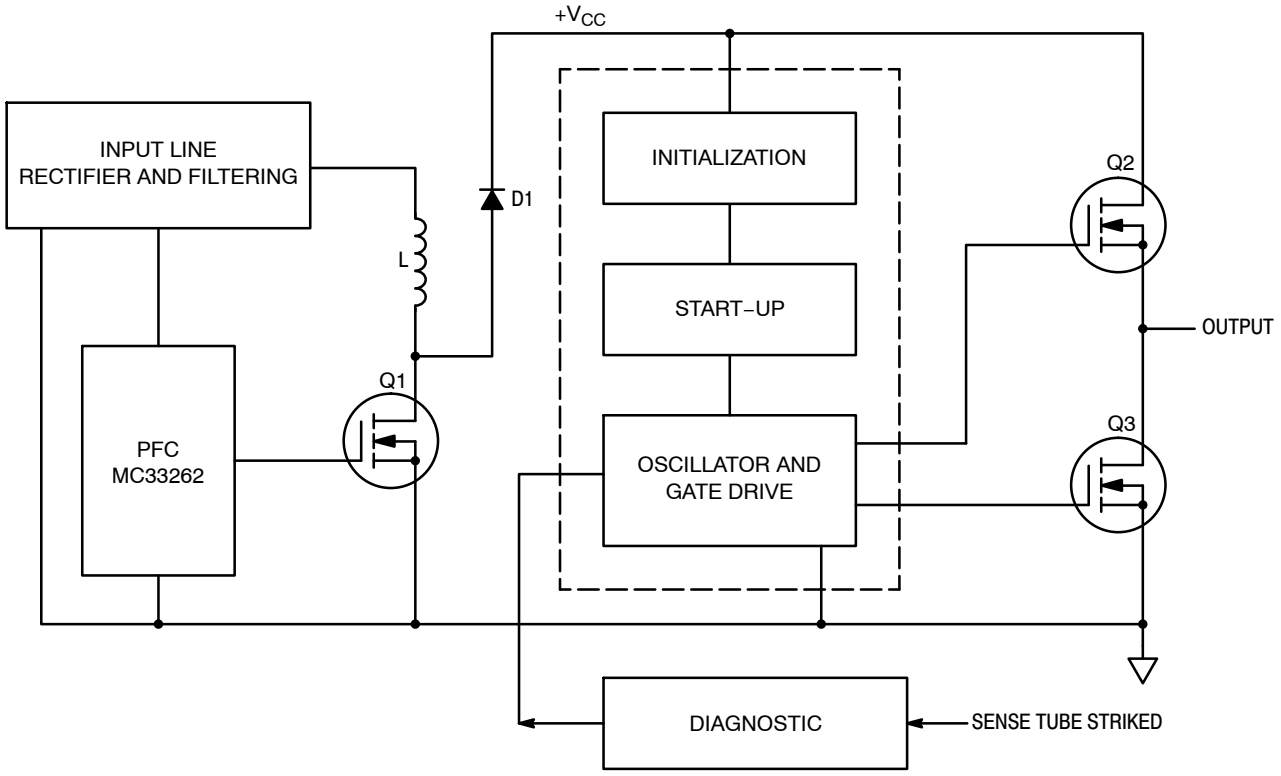


Figure 44. Typical Integrated Version of an Electronic Lamp Ballast

The design of a multi chip package is not as straightforward as it seems at first. It depends greatly on the thermal behavior of the overall system. For example, let the junction to ambient thermal resistance be 150°C/W for a plastic 8 pin SOIC package and the ambient temperature being +60°C. The maximum losses allowable into the silicon are given by Equation 28:

$$P_{max} = \frac{T_J - T_{amb}}{Rth_{ja}} \quad (28)$$

Under the above conditions, $T_J = (150-60)/150 = 600$ mW

This value yields a zero safety margin because it assumes the die is continuously operating at its maximum temperature. The transistor lifetime is highly reduced as a result of Arrhenius's law (the expected life if divided by 1000 when the temperature increases from +40° to +150°).

A more realistic way is to set the junction temperature at +120°C, yielding 400 mW maximum into the silicon under the same ambient conditions. Of course, these losses are equally dissipated in each of the power devices, assuming those in the driver are negligible. For compact fluo lamps in the range of 7 W to 15 W, powered from the 220 V line, the peak current into the switches is around 400 mA and the maximum allowable $R_{DS(on)}$ for the MOSFET is given by Equation 29:

$$R_{DS(on)(max)} = \frac{P}{I_{DRMS}^2} \quad (29)$$

In this example, $R_{DS(on)} = 0.2/((0.4/\sqrt{2})^2) = 2.50\ \Omega$.

Obviously, this is the maximum value at T_J = +120°C, yielding a net 1.60 Ω at T_J = +25°C. The die size of a 500 V rated MOSFET will be 150 x 150 mils, a dimension incompatible with the existing low cost 8 pin SOICs.

The circuit can be either split into two packages (one for the controller, the second for the power stage), or built inside the same SOIC as depicted by the dotted line in Figure 45.

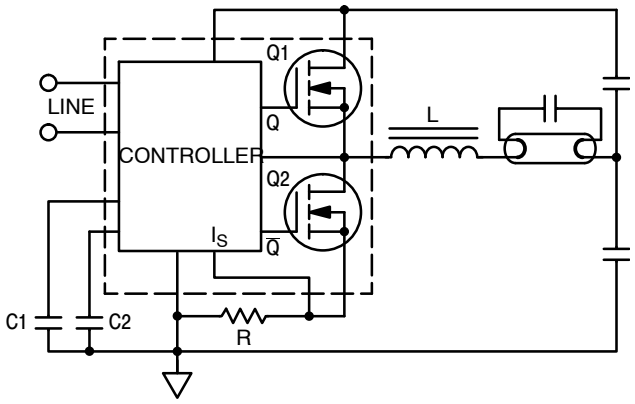


Figure 45. Fully Integrated Low Power Electronic Lamp Ballast

Obviously, the process used to manufacture this type of integrated product must be able to sustain 600 V in order to make it compatible with the EEC and US power requirements.

At the time of this publication, ON Semiconductor is developing such a process and the target specification is already defined to cover the range of power involved in these kinds of applications. The final product will use an existing high voltage technology, developed for line operated battery chargers. However, in order to make such a device as flexible as possible, the power transistors will not be integrated into the structure, giving the designer more flexibility. The lamp ballast road map already includes this development to cope with world wide needs.

EMERGING APPLICATION

High Pressure Fluorescent Lamp

Among the large number of applications being developed in the lighting field, automotive is probably the most promising since it brings more safety to the driver by yielding a much more powerful light without overloading the alternator. This is achieved by using a high pressure lamp, with a white light, to replace the existing incandescent bulbs. With an efficiency about five times higher, a 20 W rated high pressure lamp gives twice the amount of light yielded by the standard halogen bulbs.

The cost of this approach is much higher than the price of a regular bulb, together with the relatively complex circuit needed to ignite and drive the lamp. However, in addition to the higher efficiency, the high pressure lamp brings a lifetime exceeding the expected life time of the car.

Figure 46 gives the typical block diagram for such an application.

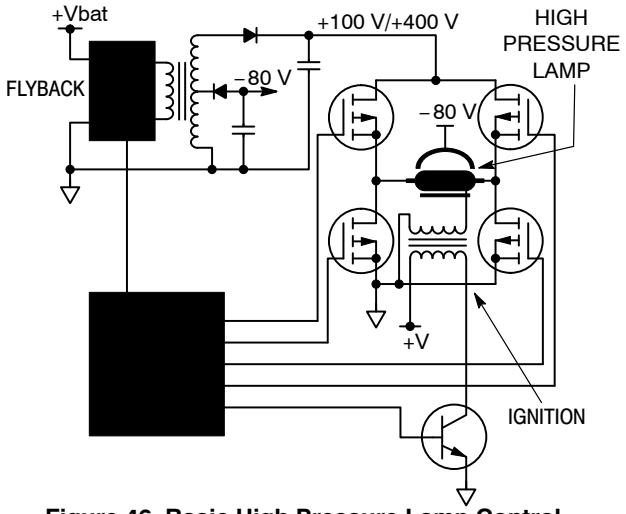


Figure 46. Basic High Pressure Lamp Control Circuit (HID Lamp)

Static Induction Lamp

Using no filament, the **S**tatic **I**nduction **D**ischarge lamp has a 60,000 hour lifetime, far longer than standard fluorescent tubes. Basically, the circuit generates an RF field across the lamp and the plasma is driven by an electromagnetic field instead of an electrostatic one. The SID can be ignited almost instantaneously (there is no need to pre−heat the filaments), and thanks to the high frequencies allowed to control these applications, the circuit can be made smaller than the more conventional ones.

There are, however, a number of drawbacks; the RFI being the most critical since it will not be allowed to pollute the radio frequency bands with thousand of converters operating in the megaHertz range.

The typical schematic diagram is given in Figure 47.

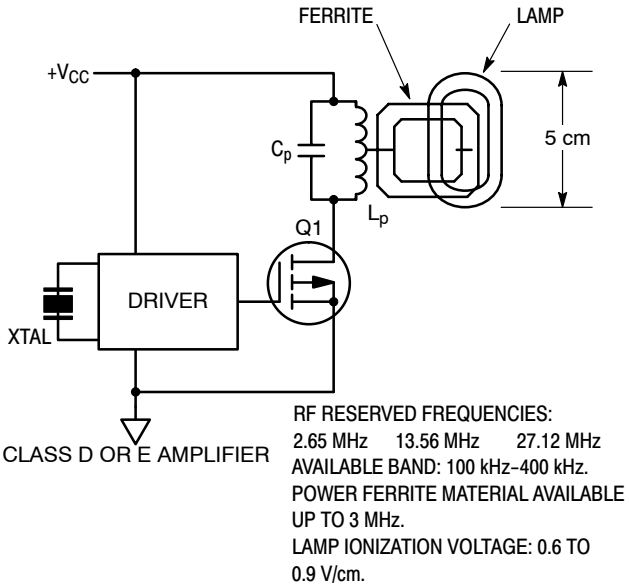


Figure 47. Typical Static Induction Discharge Lamp Application

CONCLUSIONS

Not only does the ELB save a lot of energy, but the miniaturization of the electronic ballasts makes them suitable for small enclosures. The fluorescent lighting market will continue to grow rapidly during the next decade, even replacing the standard incandescent bulbs designed for personal use.

Nowadays, engineers have access to a broad range of semiconductors, from which they can select the best device to match their applications. Power transistors, either Bipolar or MOSFET, are reliable and can run these electronic modules for more than ten years without failure. New technology has only begun to bring more intelligence into the silicon, at an affordable cost, making the lighting systems more rugged, and with features one cannot even imagine with the standard electromechanical ballasts: dimming, remote control, and real time energy saving, just to name a few.

In 1993 the electronic lamp ballast market represented around 50 million Compact Energy Saving lamps, 50 million industrials (two, four and six foot tubes) and 20 million low voltage Halogen lamps, numbers which are expected to more than double within five years. In addition, new applications are emerging, like the high pressure discharge lamps for vehicular and the induction lamps.

As a main supplier of semiconductors, our goal is to develop new products to make sure that any designer in the world will find the optimum solution to cope with his or her own needs: this is the benefit of the electronic lamp ballasts expertise accumulated by ON Semiconductor.

APPENDIX

1. $V_{(BR)CEO}$: Collector to Emitter Breakdown Voltage, Base open. This is the minimum guarantee value for a given transistor. Modern power transistors do not have a wide spread of their electrical parameters and the designer must not rely on some safety margin set by older, non−repetitive, semiconductors.
2. RBSOA: Reverse Bias Safe Operating Area. This parameter specifies the maximum energy the transistor can handle when commutating an inductive load. The RBSOA is a dynamic parameter which is dependent upon the Base reverse voltage bias as specified in the ON Semiconductor designer's data sheets.
3. FBSOA: Forward Bias Safe Operating Area. This parameter specifies the maximum power the transistor can sustain when it is operating in the Forward Base bias mode. The FBSOA is dependent upon the power pulse width and cannot be exceeded under any circumstances.
4. $V_{(BR)CER}$: Collector to Emitter Breakdown Voltage, Base connected to the Emitter via a low impedance.
5. $V_{(BR)CES}$: Collector to Emitter Breakdown Voltage, Base shorted to the Emitter.
6. $V_{(BR)CBO}$: Collector to Base Breakdown Voltage, Emitter open.

SYMBOLS, UNITS AND CONVERSION FACTORS

Parameter	Symbol	SI Units	CGS Units	CGS to SI
Magnetic Flux Density	B	Tesla	Gauss	10^{-4}
Magnetic Field Intensity	H	A−T/m	Oersted	$1000/4\pi$
Permeability (free space)	m_o	$4\pi*10^{-7}$	1	$4\pi*10^{-7}$
Permeability (relative)	m_r			1
Effective Magnetic area	A_e	m^2	cm^2	10^{-4}
Mean Magnetic Path length	l_e	m	cm	10^{-2}
Air Gap length	l_g	m	cm	10^{-2}
Magnetic flux ($\int$BdA)	F	Weber	Maxwell	10^{-3}
Magnetic Potential ($\int$Hdl)	mmf	Amp−Turn	Gilbert	$10/4\pi$
Inductance	L	Henry	Henry	1
Inductance Index	A_L	nH (1 turn)	nH (1 turn)	1
Window Area of core	A_w	m^2	cm^2	10^{-4}
Wire Cross section Area	A_x	m^2	cm^2	10^{-4}
Number of turns	N			1
Mean Length per turn	l_t	m	cm	10^{-2}
Current Density	J	A/m^2	A/cm^2	10^4
Resistivity	r	W−m	W−cm	10^{-2}
Area Product, Aw*Ae	AP	m^4	cm^4	10^{-8}
Energy	W	Joule	Erg	10^{-7}

WIRE TABLE: Copper Wire, Heavy Insulation

AWG	Dia. mm	Area mm^2	Dia. Ins. mm	Area mm^2	Ω/m @ 20°C	Ω/m @ 100°C	Current @ 4.5 A/mm^2 Amps
10	2.59	5.26	2.73	5.85	0.0033	0.0044	23.68A
11	2.31	4.17	2.44	4.67	0.0041	0.0055	18.78A
12	2.05	3.31	2.18	3.73	00.52	0.0070	14.90A
13	1.83	2.62	1.95	2.98	0.0066	0.0088	11.81A
14	1.63	2.08	1.74	2.38	0.0083	0.0111	9.365A
15	1.45	1.65	1.56	1.90	0.0104	0.0140	7.43A
16	1.29	1.31	1.39	1.52	0.0132	0.0176	5.90A
17	1.15	1.03	1.24	1.21	0.0166	0.0176	4.67A
18	1.02	0.82	1.11	0.97	0.0209	0.0280	3.70A
19	0.91	0.65	1.00	0.78	0.0264	0.0353	2.94A
20	0.81	0.52	0.89	0.62	0.0333	0.0445	2.33A
21	0.72	0.41	0.80	0.50	0.0420	0.0561	1.85A
22	0.64	0.32	0.71	0.40	0.0530	0.0708	1.46A
23	0.57	0.26	0.64	0.32	0.0668	0.0892	1.16A
24	0.51	0.20	0.57	0.26	0.0842	0.1125	0.92A
25	0.45	0.16	0.51	0.21	0.1062	0.1419	0.73A
26	0.40	0.13	0.46	0.17	0.1339	0.1789	0.58A
27	0/.36	0.10	0.41	0.13	0.1689	0.2256	0.46A
28	0.32	0.08	0.37	0.11	0.2129	0.2845	0.36A
29	0.29	0.06	0.33	0.08	0.2685	0.3587	0.29A
30	0.25	0.05	0.30	0.07	0.3386	0.4523	0.23A
31	0.23	0.04	0.27	0.06	0.4269	0.5704	0.18A
32	0.20	0.03	0.24	0.04	0.5384	0.7192	0.14A
33	0.18	0.025	0.22	0.037	0.6789	0.9070	0.11A
34	0.16	0.020	0.20	0.300	0.8560	1.1437	0.091A
35	0.14	0.016	0.18	0.024	1.0795	1.4422	0.072A
36	0.13	0.012	0.16	0.019	1.3612	1.8186	0.057A
37	0.11	0.010	0.14	0.016	1.7165	2.2932	0.045A
38	0.10	0.008	0.13	0.013	2.1644	2.8917	0.036A
39	0.09	0.006	0.12	0.011	2.7293	3.6464	0.028A
40	0.08	0.005	0.01	0.008	3.4417	4.5981	0.023A
41	0.07	0.004	0.09	0.007	4.3399	5.7982	0.018A

AWG = American Wire Gauge
Area = $(\pi * D^2)/4$
Copper resistivity at temperature T: $\rho = 1.724*(1 + 0.0042*(T-20))*10^{-6}$ Ω−cm
at T = 20°C: $\rho = 1.724*10^{-6}$ Ω−cm

Current Density Limit:

An rms current density of 4.50 A/mm^2 causes approximately a 30°C temperature increase with natural cooling for a transformer or an inductor whose core area product (AP = Aw*Ae) is 1 cm^4.

With a larger core, the allowable current density decreases because the surface usable to dissipate the heat increases less rapidly than the volume producing the heat:

$$Jmx = 4.5*AP^{-0.125} \quad A/mm^2$$

When the frequency increases, the skin effect becomes dominant and the resistance increases:

$$R_{HF} = \frac{\rho * 1}{2 * \pi * r * a}$$

The thickness (a) is given, by Lord Rayleigh's formula:

$$a = \frac{1}{2 * \pi * \sqrt{((\mu * F * 10^{\boxed{7}})/\rho)}}$$

The RHF value can be derived from Equation 30:

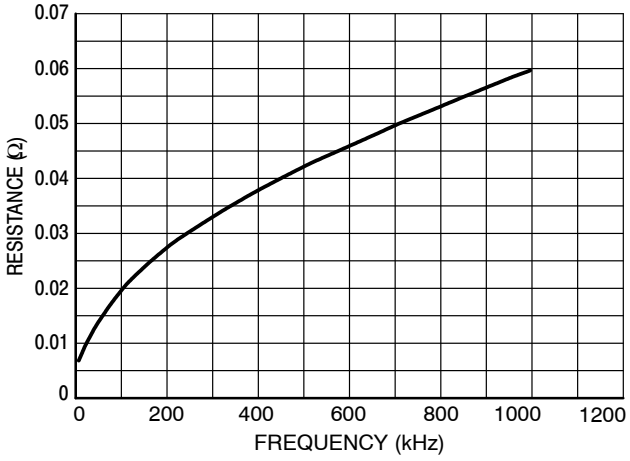
$$R_{HF} = \frac{1 * \sqrt{(8 * \mu * F * \rho * 10^{7})}}{d} \quad (30)$$

with: **F** Hertz **r** resistivity (0.018 for copper)
l meter
d mm μ permeability (1 for copper)

Table 8.Resistance as a Function of the Frequency

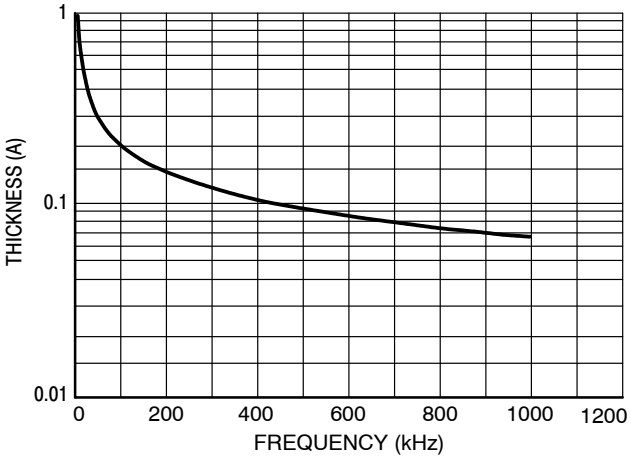
Frequency	Φ 0.50 mm	Φ 1.00 mm	2.00 mm	Thickness a
25kHz	N/A	N/A	0.0094Ω	0.427mm
35kHz	N/A	N/A	0.0112Ω	0.360mm
50kHz	N/	0.0268Ω	0.0134Ω	0.301mm
75kHz	N/A	0.0328Ω	0.0164Ω	0.246mm
100kHz	N/A	0.0379Ω	0.0189Ω	0.213mm
200kHz	0.1073Ω	0.0536Ω	0.0268Ω	0.150mm
300kHz	0.1314Ω	0.0657Ω	0.0328Ω	0.123mm
500kHz	0.1697Ω	0.0848Ω	0.0424Ω	0.095mm
1000kHz	0.2400Ω	0.1200Ω	0.0600Ω	0.067mm

The values are given for a copper of wire of 1 meter long, at the ambient temperature of 25°C.



NOTE: Wire is solid copper, one meter long, diameter 2.00 mm, temperature is +20°C.

Figure 48. Copper Wire Resistance as a Function of the Frequency



NOTE: Curve valid for copper only.

Figure 49. Thickness of the Skin Effect as a Function of Frequency

Table 9.Fluorescent Tube Characteristics

Length ft/mm	Dia. mm/T	Power (W)	Operating Volt/Ampere
8/2400	36/T12	125	152/0.94
8/2400	36/T12	100	128/0.89
6/1800	36/T12	85	123/0.77
6/1800	36/T12	75	131/0.64
6/1800	28/T8	70	128/0.70
5/1500	36/T12	65	113/0.64
5/1500	28/T8	58	113/0.63
4/1200	36/T12	40	104/0.42
4/1200	28/T8	36	104/0.42
3/900	28/T8	30	101/0.36
2/600	36/T12	20	58/0.38
2/600	28/T8	18	58/0.38

Table 10.Preferred Core Suppliers

THOMSON LCC

SIEMENS

PHILIPS

VOGT

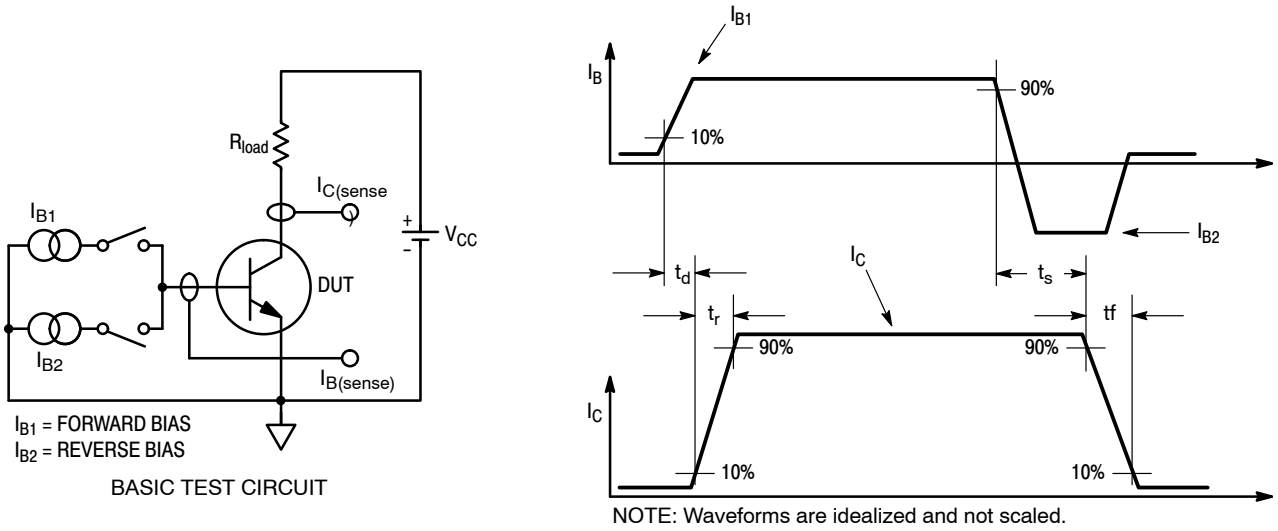


Figure 50. Switching Time Definition

ELECTRONIC LAMP BALLAST PART LIST (Figure 25.)

Index	Value	Comments
C1	10 nF	pitch 200 mils
C2	330 μF/25 V	radial 200 mils
C3	1 μF	pitch 200 mils
C4	47 μF/450 V	radial 300 mils
C5	220 nF/63 V	pitch 200 mils
C6	10 nF/63 V	pitch 200 mils
C7	10 nF/25 V	pitch 200 mils
C8	2.2 nF	pitch 200 mils
C9	2.2 nF	pitch 200 mils
C10	470 nF	pitch 100 mils
C11	4.7 nF/1200 V	pitch 600 mils
C12	22 nF/1200 V	pitch 600 mils
C13	47 nF/630 V	pitch 600 mils
C14	100 nF/250 V	pitch 400 mils
C15	100 nF/630 V	pitch 600 mils
C16	47 nF/630 V	radial 400 mils
C17	47 nF/630 V	radial 400 mils
D1	MUR120	ON Semiconductor
D2	MUR180E	ON Semiconductor
D3	1N4007	ON Semiconductor
D4	DIAC 32 V	ON Semiconductor
D5	Zener 10 V	ON Semiconductor
D6	1N4007	ON Semiconductor
D7	1N4007	ON Semiconductor
D8	1N4007	ON Semiconductor
D9	1N4007	ON Semiconductor
D10	1N4148	
D11	1N4148	
D12	1N4148	
D13	1N4148	
L1	1.6 mH	VOGT
Q1	MTP4N50	ON Semiconductor
Q2	BUL45D2	ON Semiconductor
Q3	BUL45D2	ON Semiconductor
Q4	MCR26	ON Semiconductor
R1	12 kΩ	
R2	1.2 MΩ	
R3	100 kΩ / 1 W	
R4	22 kΩ	
R5	1.0 Ω	
R6	1.0 Ω	
R7	1.8 MΩ	
R8	1 kΩ	
R9	330 kΩ	
R10	10 Ω	
R11	4.7 Ω	
R12	4.7 Ω	
R13	2.2 Ω	
R14	2.2 Ω	
R15	100 Ω	
R16	1 MΩ	
R17	10 kΩ	
U1	MC34262	ON Semiconductor
T1	OSCILLATOR	VOGT

Total Components = 54

Notes: * all resistors are 0.25 W, ±5%, unless otherwise noted
* all capacitors are polycarbonat, 63 V, ±10%, unless otherwise noted

Transformer T1: Core = FT6.3
Ferrite = 4 A
T1A = 1 turn (primary)
T1B = T1C = 5 turns each (secondaries)

Output inductance L1: Core = EF2509
Ferrite = B2 or equivalent (Operating frequency: 150 kHz min)
N = 38 turns, wire dia = 1 mm, preferably Litz type.

DIMMABLE ELECTRONIC LAMP BALLAST PART LIST (Figure 31.)

Index	Value	Comments
ALP	not a component	
C1	470 pF	styroflex, AXIAL
C2	330 pF/1500 V	pitch 600 mils
C2B	330 pF/1500 V	pitch 600 mils
C3	100 nF/400 V	pitch 600 mils
C4	100 nF/400 V	pitch 600 mils
C5	220 nF/63 V	pitch 200 mils
C6	220 nF/63 V	pitch 200 mils
C7	100 μF/25 V	radial 100 mils
C8	100 nF	pitch 200 mils
C9	100 nF	pitch 200 mils
C10	100 μF/16 V	radial 100 mils
C11	22 μF/385 V	radial 300 mils
C12	22 μF/385 V	radial 300 mils
C13	47 nF/630 V	pitch 600 mils
C14	100 nF/63 V	pitch 200 mils
C15	47 nF/630 V	pitch 600 mils
C16	100 μF/25 V	radial 100 mils
C17	4.7 μF/16 V	radial 100 mils
D1	ZENER 10 V	ON Semiconductor
D2	1N4148	
D3	1N4148	
D4	ZENER 18 V	ON Semiconductor
D5	1N4148	
D6	1N4148	
D7	1N4007	ON Semiconductor
D8	1N4007	ON Semiconductor
D9	1N4007	ON Semiconductor
D10	1N4007	ON Semiconductor
DR	100 V/1 A	BRIDGE

Index	Value	Comments
L1	1 mH	EF2509A Core, supplier LCC
Q1	MPF960	ON Semiconductor
Q2	MPF960	ON Semiconductor
Q3	MTP8N50E	ON Semiconductor
Q4	MTP8N50E	ON Semiconductor
Q5	BC557−C	ON Semiconductor
Q6	BC557−C	ON Semiconductor
R1	15 kΩ	
R2	150 kΩ	
R3	4.7 kΩ	
R4	4.7 kΩ	
R5	100 Ω	
R6	100 Ω	
R7	15 kΩ	
R8	1 kΩ	
R9	10 kΩ/2 Ω	
R10	330 kΩ	
R11	1 kΩ	
R12	1 kΩ	
R13	47 Ω/2 W	
TP1	Test Point	VCO voltage
TP2	Test Point	Clock
TP3	Test Point	Drive Voltage
TP4	Test Point	GROUND
U1	MC14046B	ON Semiconductor
U2	MC14013B	ON Semiconductor
T1	DRIVER	T1600A Core, 16 mm, A9, LCC

Total Components = 60

Notes: * all resistors are 0.25 W, ±5%, unless otherwise noted
* all capacitors are polycarbonat, 63 V, ±10%, unless otherwise noted

Transformer T1: Core = FT1600A−M01
Ferrite = A9
T1A = T1B = T1C = 20 turns, wire dia. = 0.2 mm

Output inductance L1: Core = EF2509
Ferrite = B2 or equivalent (Operating frequency: 150 kHz min)
N = 38 turns, wire dia = 1 mm, preferably Litz type.

PUBLICATION ORDERING INFORMATION

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