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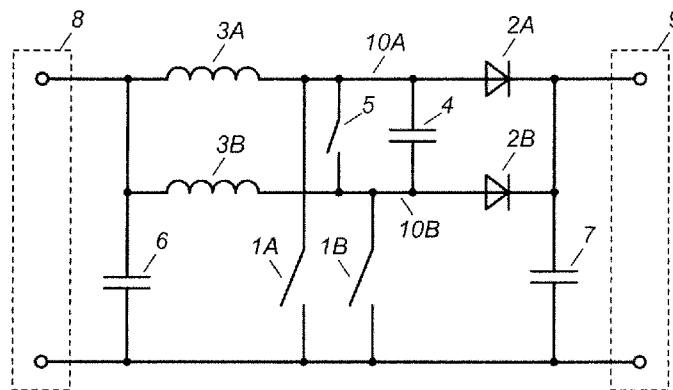


FIG. 1

(57) Abstract: An electronic DC-to-DC converter has a first sub-converter (1A, 2 A, 3 A) having a non-isolated topology, the first sub-converter (1A, 2A, 3 A) is connected with the input connections (8) and with the output connections (9) and has a first inductor (3A), wherein the first end of the first inductor is connected with one of the input connections. The converter further comprises a coupling capacitor (4), a bypass switch (5) and a second sub-converter (1B, 2B, 3B) of the same type as the first sub-converter (1A, 2A, 3 A) having a second inductor (3B) with a first end and a second end. The second sub-converter (1B, 2B, 3B) is provided in parallel to the first sub-converter (1A, 2A, 3 A) between the positive and negative input (8) and the positive and negative output (9), wherein the first sub-converter (1A, 2A, 3 A) and the second sub-converter (1B, 2B, 3B) are connected with the coupling capacitor (4) and with the bypass switch (5). The first end of the coupling capacitor (4) and the first end of the bypass switch (5) are connected to the second end of the first inductor (3 A) of the first sub converter (1A, 2A, 3 A) and the second end of the coupling capacitor (4) and the second end of the bypass switch (5) are connected to the second end of the second inductor (3B) of the second sub converter (1B, 2B, 3B).

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TITLE

DC-TO-DC POWER CONVERTER

TECHNICAL FIELD

5 The present invention relates to a DC-to-DC power converter and a method of controlling it.

PRIOR ART

The prior art knows several types of DC-to-DC power converters. The invention is based on an electronic DC-to-DC converter having a non-isolated topology. Converters having
10 said non-isolated topology are in the group comprising buck converters, boost converters, buck-boost-converters, or bidirectional converters (also known as active or synchronous rectifiers). They all have one inductor.

A buck converter or step-down converter is a DC-to-DC power converter which steps
15 down voltage, while stepping up current, from its input, i.e. supply, to its output, i.e. load. It is a class of switched-mode power supply (SMPS) typically containing at least two semiconductors which can be a diode and a transistor, although other buck converters frequently replace the diode with a second transistor used for synchronous rectification, and at least one energy storage element, a capacitor, inductor, or the two in combination.
20 To reduce voltage ripple, filters made of capacitors, sometimes in combination with inductors, are normally added to such a converter's output as load-side filter and to its input as supply-side filter.

A boost converter or step-up converter is a DC-to-DC power converter which steps up
25 voltage, while stepping down current, from its input to its output. It is a further class of switched-mode power supply with the same components as the buck converter. Similar filters as for the buck converter can be applied to a boost converter.

These switching converters provide much greater power efficiency as DC-to-DC
30 converters than linear regulators, which are simpler circuits that lower voltages by dissipating power as heat, but do not step up output current.

Buck converters can be highly efficient making them useful for tasks such as converting a

computer's main supply voltage, often being 12 V, down to lower voltages needed by USB (as e.g. 5V) or DRAM and the CPU, which work with 1.8 V or less.

Boost converters, on the other side, can use the voltage of e.g. AA or AAA rechargeable
5 cells to convert 1.2 V or 2 times 1.2 V to another voltage as e.g. 9 V.

Due to the limited switching speed of their switching devices, the majority of all switched mode power converters is subject to switching losses. The prior art knows several ways to reduce or eliminate these losses by means of zero-voltage switching (ZVS) and/or zero-
10 current switching (ZCS). The most commonly known method is the use of resonance converters in which the switching devices are turned on and off only at the zero-cross of the voltage or current of a resonant circuit. However, there are also other ways to achieve zero-current and/or zero-voltage switching.

15 Patent application CN 103 095 114 A introduces an active snubber circuit in which a pre-charged capacitor connected to the power switch leads to a low-gradient switching-edge and by this to nearly zero-voltage switching at turn-off of the power switch.

Doo-Yong Jung et al. propose an interleaved soft-switching boost converter for
20 photovoltaic power-generation (IEEE transactions on power electronics, vol. 26, no. 4, April 2011), which adopts a resonant soft-switching method.

Nam-Ju Park and Dong-Seok Hyun propose an interleaved boost converter (IBC) using a single resonant inductor for high-power applications (IEEE transactions on power
25 electronics, vol. 56, no. 5, May 2009).

SUMMARY OF THE INVENTION

Based on this prior art, it is an aim of the present invention to provide a DC-to-DC converter with less switching losses. This is achieved for an electronic DC-to-DC
30 converter having a first sub-converter having a non-isolated topology, wherein the first sub-converter being connected with a positive and negative input connection and with a positive and negative output connection and having a first inductor with a first end and a second end, wherein the first end of the first inductor is connected with one of the input

connections. Then, the converter comprises a coupling capacitor, a bypass switch and a second sub-converter of the same type as the first sub-converter having a second inductor with a first end and a second end. The second sub-converter is provided in parallel to the first sub-converter between the positive and negative input and the positive and negative output, wherein the first sub-converter and the second sub-converter are connected with the coupling capacitor and with the bypass switch, wherein a first end of the coupling capacitor and a first end of the bypass switch are connected to the second end of the first inductor of the first sub converter and wherein a second end of the coupling capacitor and a second end of the bypass switch are connected to the second end of the second inductor of the second sub converter.

The chopper-voltage of the two sub-converters is coupled with said small coupling capacitor, hence the converter is called Capacitive Coupled Pair (CCP) converter. Due to the coupling capacitor and the time difference between the shutdown of the switches, the voltage over the switches has a low gradient and allows the switches to turn off with nearly no losses.

Preferably, the sub-converters having said non-isolated topology are chosen from the group comprising a buck converter, a boost converter, a buck-boost-converter, or a bidirectional converter.

The converter comprises or include a control unit configured to control the switches of the two sub-converters as well as the bypass-switch, wherein the control unit is configured to provide a cycle, comprising two half-cycles, wherein each half-cycle is started with a simultaneous closing of the switches of both sub-converters, wherein the switch of the sub-converter, having at that time of closure of the switch the higher flow of current through the associated inductor, is opened earlier than the switch of the other sub-converter to create a coupling voltage peak within the coupling capacitor. This provides two triangular current curves in the two inductors which have a slightly offset ramp of the current in time. The gradient of the two triangular current curves have essentially the same value, both while in the increasing as well as in the declining part of the ramp. In a different embodiment it is possible to use two different inductors. Then, the gradient of the two inductor currents is not the same.

This is also due to the fact that the starting current of the inductor with the earlier closing switch starts slightly positive and the starting current of the inductor with the later closing switch starts slightly negative. In other words, the absolute difference of the currents provides the time difference when the currents reach their highest value which provides a voltage peak within the coupling capacitor. The sub-converter with the earlier closing switch has a higher current value drop over time, so that the starting current value in the inductors during the transition period (i.e. step 7 as shown in Fig. 3) for the next half-cycle is just inverted compared to the previous half-cycle.

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This enables the converter to switch on the power semiconductors almost currentless and to switch off the power semiconductors almost in zero-voltage state, i.e. free from voltage. This allows to avoid nearly all switching losses. This also enables the circuit to switch the switches comparatively slow compared to the prior art which reduces electromagnetic interferences to a minimum value.

15

This allows within a power supply to dimension a converter having a high efficiency and an excellent electromagnetic compatibility.

The converter can be used in a switched-mode power supply (SMPS), comprising an electronic converter according to the invention having said two CCP-coupled sub-converters.

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Within a method of controlling a converter as mentioned above, the control unit provides a cycle comprising two half-cycles wherein in each half-cycle the switches of the two sub-converters are switched on at the same time, but the current flow through the two inductors start from a small positive and from a small negative value, respectively, wherein the switches of the two sub-converters are switched off at a point of time, when a predetermined current value is reached so that the coupling capacitor reaches a peak voltage within this period of time. At the end of the half-cycle, the current flow through the inductors reaches the same small current flow with an inverse sign compared to the current flow at the begin of the half-cycle.

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Further embodiments of the invention are laid down in the dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

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Preferred embodiments of the invention are described in the following with reference to the drawings, which are for the purpose of illustrating the present preferred embodiments of the invention and not for the purpose of limiting the same. In the drawings,

- 10 Fig. 1 shows a schematic diagram of a DC-to-DC boost converter circuit according to an embodiment of the invention,
Fig. 2A-2N show the schematic diagram of Fig. 1 at different steps during operation,
Fig. 3 shows the evolution of currents in the inductors, the voltage of the coupling capacitor with time in an ideal boost converter according to Fig. 1, operating
15 in non-transient operation;
Fig. 4 shows a schematic inductor current curve over time of an idealised inductor used within the embodiment as shown in Fig. 1;
Fig. 5 shows a schematic diagram of a DC-to-DC buck converter circuit according to an embodiment of the invention,
20 Fig. 6 shows a schematic diagram of a DC-to-DC bidirectional boost converter circuit according to an embodiment of the invention,
Fig. 7 shows a schematic diagram of a DC-to-DC buck-boost converter circuit according to an embodiment of the invention,
Fig. 8A-8G show the schematic diagram of Fig. 5 at different steps during operation,
25 Fig. 9A-9G show the schematic diagram of Fig. 7 at different steps during operation,
Fig. 10 shows a schematic diagram of a DC-to-DC bidirectional buck converter circuit according to an embodiment of the invention, and
Fig. 11 shows a simplified schematic of the sub converters with the control unit.

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DESCRIPTION OF PREFERRED EMBODIMENTS

Fig. 1 shows a schematic diagram of a DC-to-DC boost converter circuit according to an embodiment of the invention. The converter circuit of Fig. 1 comprises two conventional boost sub-converters which are provided in parallel.

The first boost sub-converter comprises a first inductor 3A connecting together with a first diode 2A in series a first contact of input 8 with a first contact of output 9. The second boost sub-converter comprises a second inductor 3B connecting together with a second diode 3A in series the same first contact of input 8 with the same first contact of output 9.

The second contact of input 8 is directly connected with the corresponding second contact of output 9, providing ground. Between the first and second contacts of input 8 is provided an input capacitor 6. On the other side, between the first and second contacts of output 9 is provided an output capacitor 7.

A first switch 1A of the first sub-converter is provided between ground and a contact point between the first inductor 3A and the first diode 2A. A similar third switch 1B of the second sub-converter is provided between ground and a contact point between the second inductor 3B and the second diode 2B.

The two sub-converters, i.e. the components 1A, 2A and 3A, respectively 1B, 2B and 3B, are coupled via a coupling capacitor 4 and a short-circuit switch 5 provided in parallel between the corresponding inductors 3A and 3B and diodes 2A and 2B, respectively.

20

The function of the circuit will be explained under the assumption of ideal components. The switches 1A, 2B and 5 and the diodes 2A and 2B have zero voltage drop when on and zero current flow when off, and the inductors 3A and 3B have zero series resistance. Furthermore, it is assumed that the input and output voltages do not change over the course of a cycle, which implies that the output capacitance is infinite. The stable voltages at input 8 and output 9 provide linear changing currents as explained below.

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Fig. 2A to Fig. 2N show the schematic diagram of Fig. 1 at different steps during operation. Fig. 3 shows the evolution of currents in the inductors, the voltage of the coupling capacitor with time in an ideal boost converter according to Fig. 1, operating in non-continuous conduction mode.

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Fig. 3 shows a complete cycle of operation in fourteen steps 100, marked 1 to 14 in the

boxes in Fig. 3 above the diagrams. Fig. 3 shows there the flow of current 203A in the first inductor 3A, the flow of current 203B in the second inductor 3B, the voltage 204 at the coupling capacitor 4, the status on or off 201A at the first switch 1A, the status on or off 201B at the third switch 1B and the status on or off 205 at the short circuit switch 5.

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Fig. 2A shows step 1 in the non-continuous conduction mode operation. Both sub-converters work “almost” in non-continuous mode which will be explained in connection with step 6 later.

10 This mode of operation already achieves that both switches 1A and 1B close at zero current avoiding losses. Both switches 1A and 1B close at the same time allowing the flow of current according to arrows 101A and 101B in Fig. 2A. The flow of current 203A and 203B as shown in Fig. 3 through the first inductor 3A and through the second inductor 3B, increases over time in step 1. The basis value 2031A of the current flow in the first
15 inductor 3A from the last cycle is slightly positive, the basis value 2031B of the current flow in the second inductor 3B from the last cycle is slightly negative. The maximum value is therefore reached later within the second inductor 3B which will bring us to specific consequences in steps 2 to 4 later on.

20 The value of the voltage 2041 at the coupling capacitor is zero in step 1- It will be shown that it is also zero in steps 5 to 8, and 12 to 14.

As mentioned above the status of first and third switch 1A and 1B are both “on” in step 1.

25 Step 2 is shown in Fig. 2B. At the transition between steps 1 and 2, the first switch 1A opens. The current of inductor 3A is then redirected into the coupling capacitor 4, leading the voltage of coupling capacitor 4 to rise according to arrow 104 with a relatively low gradient. Because of the low voltage gradient, switch 1A turns off at low voltage and therefore with very low switching losses.

30

Step 3 is shown in Fig. 2C. When the coupling capacitor 4 reaches the value of the output voltage according to arrow 104, the first diode 2A becomes conducting and the current from the first inductor 1A flows as current 101A” to output 9. The voltage of the coupling

capacitor 4 in step 3 remains at said voltage 2041'.

Step 4 is shown in Fig. 2D. The third switch 1B is switched off. The current 101B' of the second inductor 3B is used to discharge the coupling capacitor 4 entirely, providing a low
5 gradient drop of voltage 104 to zero. This reduces as in step 2 the losses at the third switch 1B. The switching energy of the second inductor 3B as well as the energy stored within the coupling capacitor 4 are conducted through the first diode 2A into the output 9.

Step 5 is shown in Fig. 2E. When the coupling capacitor 4 is discharged, the second diode
10 2B becomes conducting. Now, the current flowing through both inductors 1A and 1B is directly conducted to output 9. During this time within step 5, the short-circuit switch 5 is being closed as shown in Fig. 2E.

Step 6 is shown in Fig. 2F. Since the first switch 1A was opened earlier than the third
15 switch 1B by the length of steps 2 plus 3, the value of the current of the first inductor 3A is also passing zero before the current of the second inductor 3B. As long as the second diode 2B is conducting, the first inductor 3A is still connected via the short circuit switch 5 with the output voltage. Therefore, the current flow in the first inductor 3A becomes negative in step 6 through a back-flow portion 101X of the current flow 101B''. The short circuit
20 switch 5 avoids that the coupling capacitor 4 is being charged.

Step 7 is shown in Fig. 2G. When the value of the current flow through second inductor
3A'' is reduced to its basic value 2031B, then the entire current is flowing back as flow
portion 101X through the first inductor 1A to input 8. The second diode 2B becomes
25 currentless and blocks. This concludes the first half of the entire cycle.

Step 8 is shown in Fig. 2H. Both switches, the first switch 1A and the third switch 1B are closed at the beginning of this step, whereas the short-circuit switch 5 is turned off.

30 Therefore, the switches 1A and 1B allow the flow of current according to arrows 101A and 101B in Fig. 2H. The flow of current 203A and 203B as shown in Fig. 3 through the first inductor 3A and through the second inductor 3B, increases over time in step 8 with the difference, that the basis value 2031A' of the current flow in the first inductor 3A from the

last cycle is slightly negative, the basis value 2031B' of the current flow in the second inductor 3B is slightly positive. The maximum value is therefore reached later within the first inductor 3A which will bring us to specific consequences in steps 9 to 11.

5 Step 9 is shown in Fig. 2I. Since the second inductor reaches the nominal value earlier, the third switch 1B is switched of earlier at the beginning of step 9. This redirects the inductor current 101B''' into the coupling capacitor 4. The effect is similar to step 2, with the difference, that the coupling capacitor 4 is being charged with opposite polarity. Again, the low voltage gradient caused by the charging of the coupling capacitor reduces switching
10 losses, this time to switch 1B.

In step 10, as shown in Fig. 2J, the coupling capacitor 4 reaches the negative value of the voltage 2041'' and the current from the second inductor 1B flows into output 9. The voltage of the coupling capacitor 4 in step 10 remains at said voltage 2041''.

15

Steps 11 to 14 are identical to steps 4 to 7 with the opposite sequence, i.e. it is the first inductor 3A which reaches a level of slightly positive current whereas it is the second inductor 3B which exhibits a level of slightly negative current of opposite value in the opposite direction of the flow as shown with 101X in Fig. 2F. Therefore, Fig. 2K, 2L, 2M
20 and 2N show a symmetric current flow compared to Fig. 2D, 2E, 2F and 2G.

To achieve optimal performance, steps 3, 7, 10 and 14 have to be kept as short as possible. Also, steps 2, 4, 9 and 11 should not be longer as it is required for the minimization of the switching losses of the switches 1A and 1B. This can be achieved by the right
25 dimensioning of the coupling capacitor 4.

The converter according to Fig. 1 can be dimensioned based on some assumptions. The input and output capacitors 6 and 7 are large enough that the influence of voltage ripples is negligible.

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The present converter comprises a capacitive coupled pair, in short called herein a CCP-converter. The specific principles will be neglected for the following calculations and the two sub-converters will be treated as independent, i.e. the two inductor currents 203A and

203B are zero at the beginning of step 1 and then of equal value. Usually the tolerance of the coil of the inductors is higher than the deviations due to the simplified assumptions.

The example starts with an input voltage at the input 8 of $V_{IN} = 400$ V, and an output
5 voltage at output 9 of $V_{OUT} = 800$ V. The power should be $P_{OUT} = 2$ kW and the frequency $f_{SW} = 50$ kHz which gives a period of $T = 20$ microseconds. Then

$$P_{OUT} = V_{OUT} \cdot I_{OUT} = V_{IN} \cdot I_{IN}$$

$$I_{IN} = \frac{P_{OUT}}{V_{IN}} = \frac{2\text{kW}}{400\text{V}} = \underline{5\text{A}}$$

$$I_{OUT} = \frac{P_{OUT}}{V_{OUT}} = \frac{2\text{kW}}{800\text{V}} = \underline{2.5\text{A}}$$

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Fig. 4 shows a schematic inductor current curve over time of an idealised inductor used within the embodiment as shown in Fig. 1; The current ripple within the inductors 3A and 3B is triangular. During the ON-time t_{ON} of the switches 1A and 1B, the current raises from zero to the maximal value I_P , which is followed by the time of demagnetization t_{DEM}
15 within which the currents in the inductors are going down in a linear relationship over time to zero. This is followed by the dead time t_T within which the inductors 3A and 3B do not conduct any current.

With the definition of T as:

20

$$T = t_{ON} + t_{DEM} + t_T$$

t_{ON} is based on the duty cycle D as

$$t_{ON} = D \cdot T$$

During t_{ON} the inductor has the input voltage V_{IN} so that the maximum value of the inductor current I_P of the storage choke L can be calculated based on

25

$$I_P = \frac{t_{ON} \cdot V_{IN}}{L} = \frac{D \cdot T \cdot V_{IN}}{L}$$

During demagnetisation time, the difference between input and out voltage $V_{OUT} - V_{IN}$ is identical to the voltage of the inductor. This achieves

$$t_{DEM} = \frac{L \cdot I_P}{V_{OUT} - V_{IN}} = \frac{L \cdot \frac{D \cdot T \cdot V_{IN}}{L}}{V_{OUT} - V_{IN}} = D \cdot T \cdot \frac{V_{IN}}{V_{OUT} - V_{IN}}$$

The charge Q_{IN} received by the inductor is proportional to the area under the curve of Fig.

4. This allows to calculate the charge as

$$Q_{IN} = \frac{(t_{ON} + t_{DEM}) \cdot I_P}{2} = \frac{\left(D \cdot T + D \cdot T \cdot \frac{V_{IN}}{V_{OUT} - V_{IN}}\right) \cdot \frac{D \cdot T \cdot V_{IN}}{L}}{2} = \frac{D^2 \cdot T^2 \cdot V_{OUT} \cdot V_{IN}}{2 \cdot L \cdot (V_{OUT} - V_{IN})}$$

5 In order to obtain the average input current of the circuit, the charge has to be multiplied by 2, since there are two sub-converters in parallel and divided by the period time T .

$$I_{IN} = \frac{2 \cdot Q_{IN}}{T} = \frac{D^2 \cdot T \cdot V_{OUT} \cdot V_{IN}}{L \cdot (V_{OUT} - V_{IN})}$$

This allows to calculate the output current as well as follows:

$$I_{OUT} = I_{IN} \cdot \frac{V_{IN}}{V_{OUT}} = \frac{D^2 \cdot T \cdot V_{IN}^2}{L \cdot (V_{OUT} - V_{IN})}$$

10 Therefore, a relationship is established having two degrees of freedom with D and L allowing to choose specific relationships between t_{ON} , t_{DEM} , and t_T vis-à-vis T .

It has to be avoided to use values where the inductor current cannot fall down to zero.

Therefore, an activity relationship A is created with:

$$15 \quad A = \frac{t_{ON} + t_{DEM}}{T} = \frac{D \cdot T + D \cdot T \cdot \frac{V_{IN}}{V_{OUT} - V_{IN}}}{T} = D \cdot \frac{V_{OUT}}{V_{OUT} - V_{IN}}$$

With the expression solved for D , it is obtained:

$$D = A \cdot \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

And the output current is calculated as:

$$I_{OUT} = \frac{D^2 \cdot T \cdot V_{IN}^2}{L \cdot (V_{OUT} - V_{IN})} = \frac{\left(A \cdot \frac{V_{OUT} - V_{IN}}{V_{OUT}}\right)^2 \cdot T \cdot V_{IN}^2}{L \cdot (V_{OUT} - V_{IN})} = \frac{A^2 \cdot T \cdot V_{IN}^2 \cdot (V_{OUT} - V_{IN})}{L \cdot V_{OUT}^2}$$

20 All variables are known beside L . L can be calculated by solving the expression for L :

$$L = \frac{A^2 \cdot T \cdot V_{IN}^2 \cdot (V_{OUT} - V_{IN})}{I_{OUT} \cdot V_{OUT}^2}$$

To obtain an improved efficiency rate, the inductors are to be charged and discharged most of the time, i.e. the dead time t_T should be rather small. This is equivalent to choose A as a high value but $A < 1$. With $A = 0.9$, L can be calculated as:

$$L = \frac{A^2 \cdot T \cdot V_{IN}^2 \cdot (V_{OUT} - V_{IN})}{I_{OUT} \cdot V_{OUT}^2} = \frac{0.9^2 \cdot 20\mu s \cdot (400V)^2 \cdot (800V - 400V)}{2.5A \cdot (800V)^2} = \underline{648\mu H}$$

The duty cycle D is:

$$D = A \cdot \frac{V_{OUT} - V_{IN}}{V_{OUT}} = 0.9 \cdot \frac{800V - 400V}{800V} = \underline{0.45}$$

And the maximum value of the inductor current is:

$$5 \quad I_P = \frac{D \cdot T \cdot V_{IN}}{L} = \frac{0.45 \cdot 20\mu s \cdot 400V}{648\mu H} = \underline{5.5A}$$

The above calculation also applies to interleaved boost converters. The specific impact of the couple capacitor is taken into account as follows. The dimension shall allow that the change of charge takes longer than the switch-off time or fall time t_F of the transistor used.

A usual fall time is $t_F = 50ns$ - The time to change the charge of the coupling capacitor 4 is roughly

$$t_{CHARGE} \approx 10 \cdot t_F = 10 \cdot 50ns = \underline{500ns}$$

This is the time within which the capacitor has to be charged from zero to the output voltage V_{OUT} . Since the time of change of the charge is very short compared to the period T , the current can be assumed to be constant. This value is the peak value of the coil current I_P , which gives us the formula for the capacitance of the capacitor 4

$$C_C = \frac{I_P \cdot t_{CHARGE}}{U_{OUT}} = \frac{5.5A \cdot 500ns}{800V} = 3.472nF (\approx \underline{3.3nF})$$

This capacitance may be too high, due to the fact that the factor 10 for the time of change of charge is quite generous. However, the semiconductors used may have parasitic capacitances which could be seen as parallel capacitances for the coupling capacitor 4.

The coupling capacitor 4 receives per cycle one time the peak value of the current to charge and discharge the coils of the inductors 3A and 3B. Therefore, during the charge time, the effective current can be calculated as

$$25 \quad I_{C_C-RMS} = \sqrt{\frac{1}{T} \cdot \int_0^{2 \cdot \frac{C_C \cdot U_{OUT}}{I_P}} I_P^2 dt} = \sqrt{\frac{2 \cdot C_C \cdot I_P \cdot U_{OUT}}{T}} = \sqrt{\frac{2 \cdot 3.3nF \cdot 5.5A \cdot 800V}{20\mu s}}$$

$$= \underline{1.211A}$$

which leads to a current value above 1 Ampère which is a high value for a 3.3nF capacitor 4. Therefore, it should have a small ESR. This can be a foil capacitor or a ceramic

capacitor.

Fig. 5 shows a schematic diagram of a DC-to-DC buck converter circuit according to an embodiment of the invention. Same features have received identical reference numerals.

5 The same principle applies as for the boost converter of Fig. 1. Fig. 8A to 8G show the first half-cycle of operation of the DC-to-DC buck converter in the same manner as Fig. 2A to 2G show the first half-cycle of the boost converter. The reference numerals for components 1A, 1B, 2A, 2B, 3A, 3B, 4, 5, 6, 7, 8 and 9 have been omitted for better visibility of the current flow and voltage indication. The second half-cycle is identical to the first half-
10 cycle, but with swapped roles of the switches and inductors. The timing diagram of buck and buck-boost converters according to embodiments of the invention is similar to the timing diagram of the boost converter in Fig. 3.

Fig. 6 shows a schematic diagram of a DC-to-DC bi-directional boost converter circuit
15 (also known as active or synchronous rectifier) according to an embodiment of the invention. Here, the difference is the exchange of diodes 2A and 2B through use of transistor switches 2A' and 2B'. The bi-directional converter can work as a boost converter as shown in Fig. 1. In this mode, switches 1A', 1B' and 5 are being controlled in the same way as the switches 1A and 1B as shown in Fig. 1. The switches 2A' and 2B' are being
20 controlled to take on the function of the diodes 2A and 2B in Fig. 1, meaning, they have to be turned on whenever the diodes in Fig. 1 are conducting. When working in the opposite direction – that is when the converted energy flows from the output 9 to the input 8 – the bi-directional converter actually works as buck converter as shown in Fig. 5 but drawn mirrored and with swapped input and output ports. In this mode of operation, switches 2A'
25 and 2B' in Fig. 6 take on the role of the switches 1A and 2A in Fig. 5 and switches 1A' and 1B' in Fig. 6 take on the role of the diodes 2A and 2B in Fig. 5. In other words, the bi-directional converter can work as both boost converter transferring energy from input to output as well as buck converter transferring energy from output to input.

30 Fig. 10 shows a schematic diagram of a DC-to-DC bi-directional buck converter circuit according to an embodiment of the invention. Like with the bi-directional boost converter in Fig. 6, bi-directional operation is achieved by replacement of the diodes 2A and 2B through use of switches 2A' and 2B'. Basically, the converter of Fig. 10 is identical to the

converter of Fig. 6, but with swapped input and output as well as different referencing of the components.

Fig. 7 shows a schematic diagram of a DC-to-DC buck-boost converter circuit or inverting
 5 converter according to an embodiment of the invention. Fig. 9A to 9G show the first half-cycle of operation of the DC-to-DC buck-boost converter in the same manner as Fig. 2A to 2G show the first half-cycle of the boost converter. The second half-cycle is identical to the first half-cycle, but with swapped roles of the switches and inductors. The signals shown in Fig. 3 also apply for the buck-boost converter.

10

Fig. 11 shows a simplified schematic diagram of any of the DC-to-DC converters from figures 1, 5, 6, 7 or 10 including the control unit required for operation. The first sub converter 11A and the second sub converter 11B are connected in parallel to a common input terminal 8 with the input capacitor 6 and to a common output 9 with the output
 15 capacitor 7. Furthermore, the sub converters are connected with the coupling capacitor 4 in parallel to the bypass switch 5. The control unit 12 generates the necessary control signals 13 to control the switches in the described way.

The switches are typically chosen as to be MOSFET, IGBT or BJT.

20

LIST OF REFERENCE SIGNS

1A	first switch	6	input capacitor
1B	third switch	7	output capacitor
2A	first diode	8	input
2B	second diode	9	output
2A'	second switch	10A	first common node
2B'	fourth switch	10B	second common node
3A	first inductor	11A	first sub converter
3B	second inductor	11B	second sub converter
4	coupling capacitor	12	control unit
5	short circuit switch / bypass switch	13	control signals
		100	steps

101A	flow of current in steps 1, 8 and 9 (boost converter)	204	voltage at the coupling capacitor
101A'	flow of current in step 2 (boost converter)	205	status of the short circuit switch
101A''	flow of current in steps 3, 4 5, 12 and 13 (boost converter)	2031A	basic current flow before step 1
101A'''	flow of current in step 11 (boost converter)	2031A'	basic current flow before step 8
101B	flow of current in steps 1, 2, 3 and 8 (boost converter)	2031B	basic current flow before step 1
101B'	flow of current in step 4 (boost converter)	2031B'	basic current flow before step 8
101B''	flow of current in steps 5, 6, 10, 11 and 12 (boost converter)	2041	voltage value of coupling capacitor in steps 1, 5 to 8 and 12 to 14
101B'''	flow of current in step 9 (boost converter)	2041'	voltage value of coupling capacitor in step 3
101X	back flow current in steps 6 and 7 (boost converter)	2041''	voltage value of coupling capacitor in step 10
101X'	back flow current in steps 13 and 14 (boost converter)	301A	flow of current in steps 1, 8 and 9 (buck converter)
104	voltage over coupling capacitor in steps 3 and 4 (boost converter)	301A'	flow of current in step 2 (buck converter)
104'	voltage over coupling capacitor in steps 10 and 11 (boost converter)	301A''	flow of current in steps 3, 4 5, 12 and 13 (buck converter)
201A	status of the first switch	301A'''	flow of current in step 11 (buck converter)
201B	status of the third switch	301B	flow of current in steps 1, 2, 3 and 8 (buck converter)
203A	flow of current in the first inductor	301B'	flow of current in step 4 (buck converter)
203B	flow of current in the second inductor	301B''	flow of current in steps 5, 6, 10, 11 and 12 (buck

	converter)		(buck-boost converter)
301B'''	flow of current in step 9 (buck converter)	401B	flow of current in steps 1, 2, 3 and 8 (buck-boost converter)
301X	back flow current in steps 6 and 7 (buck converter)	401B'	flow of current in step 4 (buck-boost converter)
301X'	back flow current in steps 13 and 14 (buck converter)	401B''	flow of current in steps 5, 6, 10, 11 and 12 (buck-boost converter)
304	voltage over coupling capacitor in steps 3 and 4 (buck converter)	401B'''	flow of current in step 9 (buck-boost converter)
304'	voltage over coupling capacitor in steps 10 and 11 (buck converter)	401X	back flow current in steps 6 and 7 (buck-boost converter)
401A	flow of current in steps 1, 8 and 9 (buck-boost converter)	401X'	back flow current in steps 13 and 14 (buck-boost converter)
401A'	flow of current in step 2 (buck-boost converter)	404	voltage over coupling capacitor in steps 3 and 4 (buck-boost converter)
401A''	flow of current in steps 3, 4 5, 12 and 13 (buck-boost converter)	404'	voltage over coupling capacitor in steps 10 and 11 (buck-boost converter)
401A'''	flow of current in step 11		

CLAIMS

1. Electronic power converter having a first sub converter (11A) comprising a first switching device (1A), a second switching device (2A or 2A') and a first inductor (3A) connected to a first common node (10A), wherein the first sub converter has the topology of a buck converter, a boost converter, a buck-boost-converter or a bidirectional converter, also known as active or synchronous rectifier, further having a second sub converter (11B) comprising a third switching device (1B), a fourth switching device (2B or 2B') and a second inductor (3B) connected to a second common node (10B), where the second sub converter has the same topology as the first sub converter, where both sub converters are connected to a common input (8) and a common output (9), further having a coupling capacitor (4) with a first end and a second end, where the first end of the coupling capacitor is connected to the first common node (10A) and the second end of the coupling capacitor is connected to the second common node (10B), characterized in that the converter further comprises a control unit (12) providing the control signals (13) to control the first (1A) and, if the second switching device (2A or 2A') not being a diode, the second (2A or 2A') switching device of the first sub-converter (11A) and to control the third (1B) and, if the fourth switching device (2B or 2B') not being a diode, the fourth (2B or 2B') switching device of the second sub-converter (11B), wherein the control signals (13) control the first, second, third and fourth switching devices in a way that leads to zero-current or nearly zero-current switching at turn-on of the first (1A) and third (1B) switching device as well as to zero-voltage or nearly zero-voltage switching at turn-off of the first (1A) and third (1B) switching device.

2. Converter according to claim 1, wherein the first sub-converter and the second sub-converter are also connected with an additional bypass switch (5) in parallel to the coupling capacitor (4), especially wherein a first end of the bypass switch (5) is connected to the second end of the first inductor (3A) of the first sub converter and wherein a second end of the bypass switch (5) is connected to the second end of the second inductor (3B) of the second sub converter to prevent unwanted charging of the coupling capacitor.

3. Converter according to any one of claims 1 or 2, wherein the control unit is

configured to provide a cycle, comprising two half-cycles, wherein each half-cycle is started with a simultaneous closing of the switches (1A and 1B, or 2A' and 2B') of both sub-converters, wherein at the end of each half-cycle the switch (1A, 1B; 1A', 1B', 2A', 2B';) of one sub-converter is opened earlier than the switch (1A, 1B; 1A', 1B', 2A', 2B';) of the other sub-converter.

4. Converter according to claim 3, wherein the first switching device (1A) and the third switching device (1B) are turned-off in the order in which the respective switching device, whose associated inductor's (3A, 3B) current has the higher instantaneous value, is turned-off earlier than the other switching device.

5. Method of controlling a converter according to any one of claims 1 to 5, wherein the control unit provides a cycle comprising two half cycles, where in both half cycles the first switching device (1A) and the third switching device (1B) are being turned on simultaneously, leading the currents in inductors (3A, 3B) of both sub-converters to rise, where in the first half cycle the first switching device (1A) is being turned off as soon as the current in the first inductor (3A) of the first sub-converter reaches a predetermined value and the third switching device (1B) is being turned off a predetermined time delay after the first switching device (1A) has been turned off, where in the second half cycle the third switching device (1B) converter is being turned off as soon as the current in the second inductor (3B) of the second sub converter reaches a predetermined value and the first switching device (1A) is being turned off a time delay after the third switching device (1B) has been turned off, where said time delay is chosen to be long enough to allow the voltage of the coupling capacitor (4) after turn-off of the first and third switching device to settle on a stationary value with the aim to redirect the currents of both inductors (3A, 3B) after turn-off of their associated switches (1A, 1B) into the coupling capacitor with the effect that the charging and discharging of the coupling capacitor leads to a low-gradient switching slope allowing near zero-voltage switching at the turn-off of the first and third switching device (1A, 1B).

6. Method of controlling a converter according to claim 5, wherein the point in time at which the switches (1A, 1B) of the two sub-converters are switched off is chosen, when a predetermined current value is reached in the inductors (3A, 3B), so that the coupling

capacitor (4) reaches a peak voltage (2041', 2041'') within this period of time and the current flow through the inductors (3A, 3B) reaches the same small current flow at the end of the half-cycle with an inverse sign compared to the current flow at the begin of the half-cycle.

7. Method according to claim 6, wherein the dead time between the two half-cycles is configured to be a predetermined value.

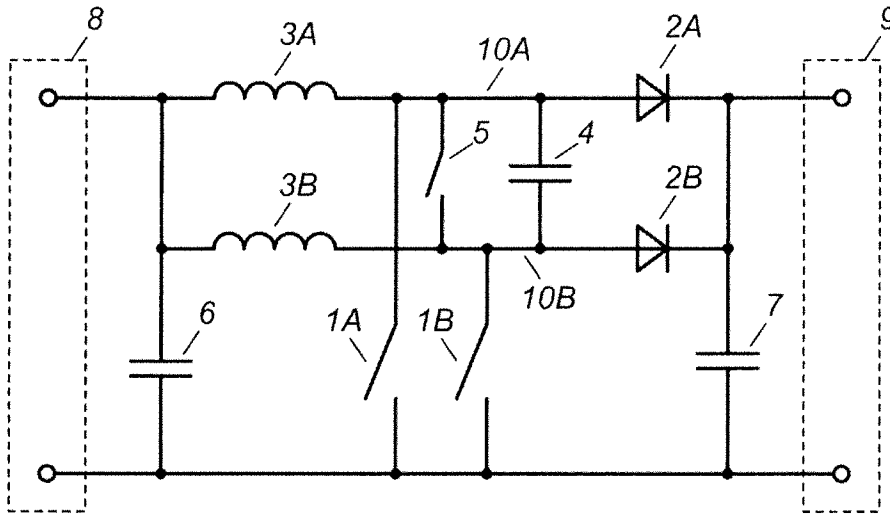


FIG. 1

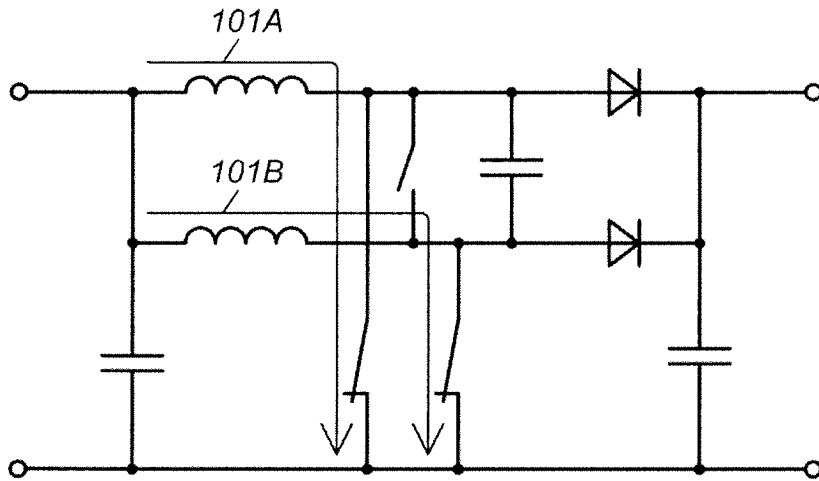


FIG. 2A

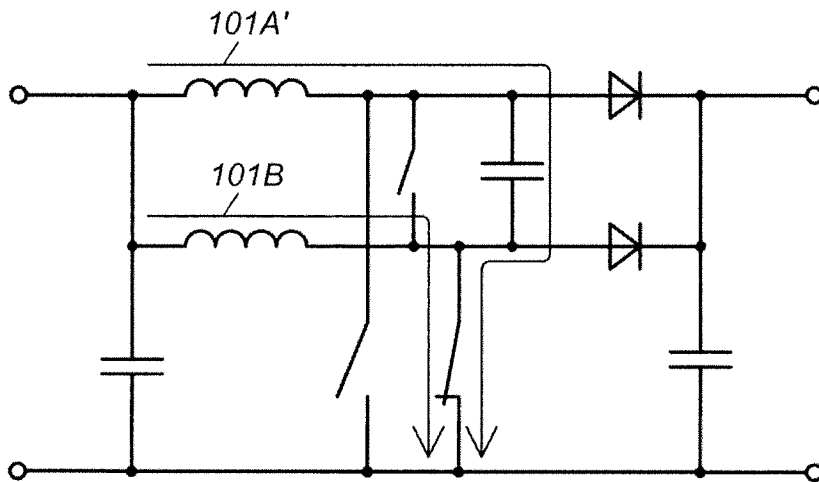


FIG. 2B

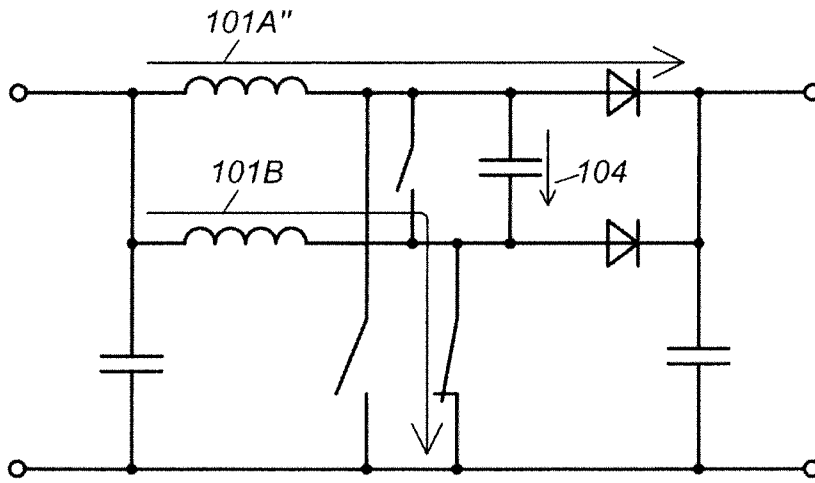


FIG. 2C

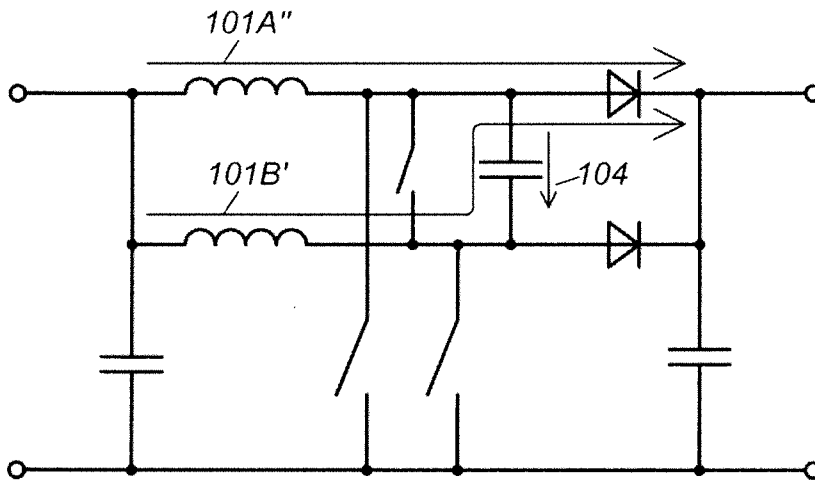


FIG. 2D

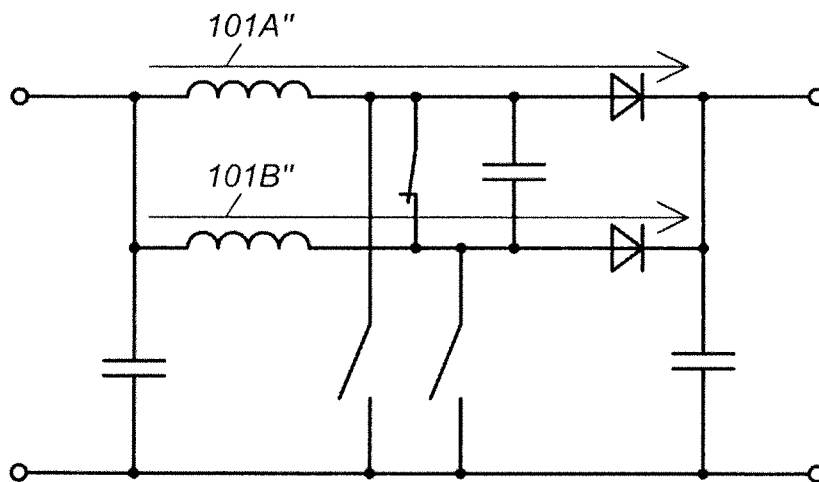


FIG. 2E

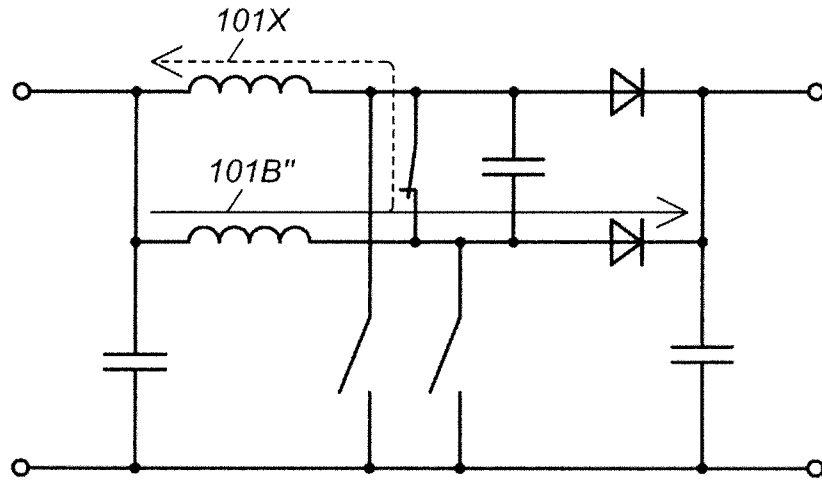


FIG. 2F

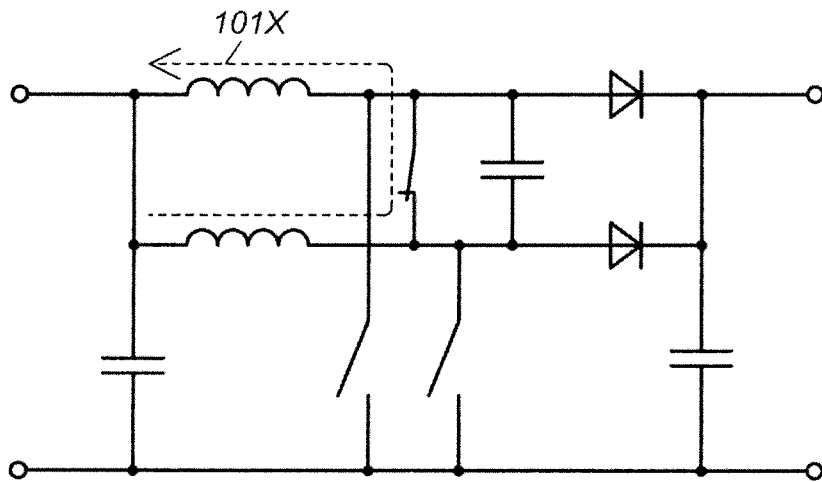


FIG. 2G

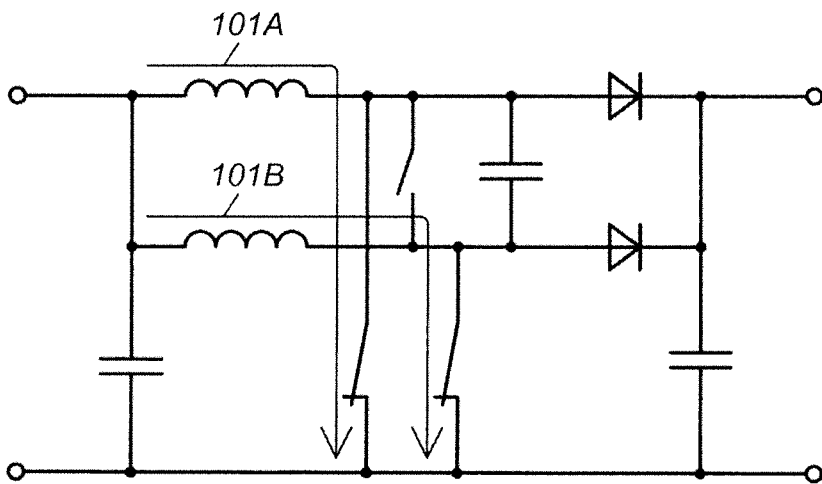


FIG. 2H

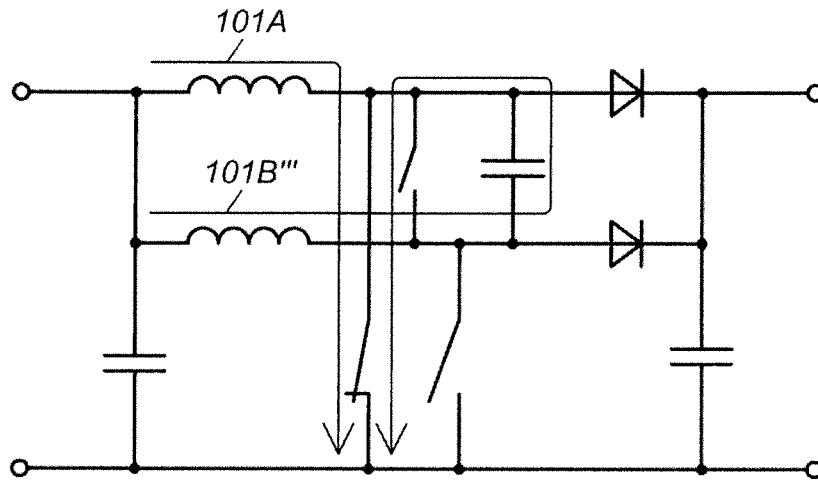


FIG. 2I

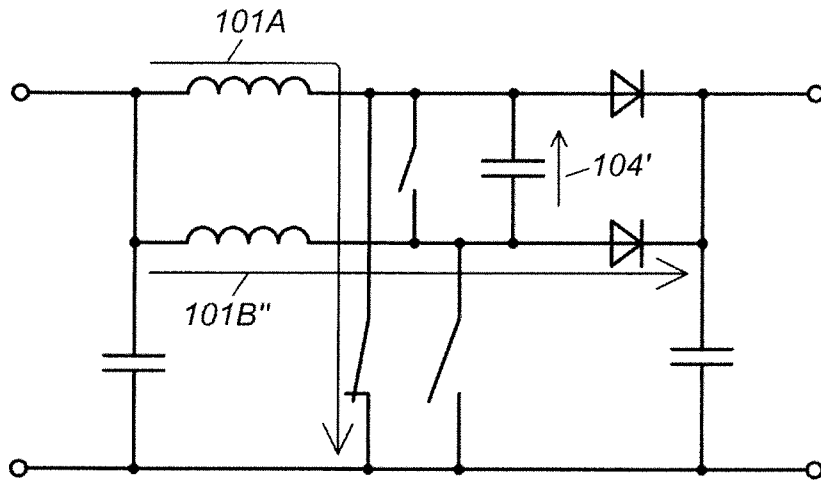


FIG. 2J

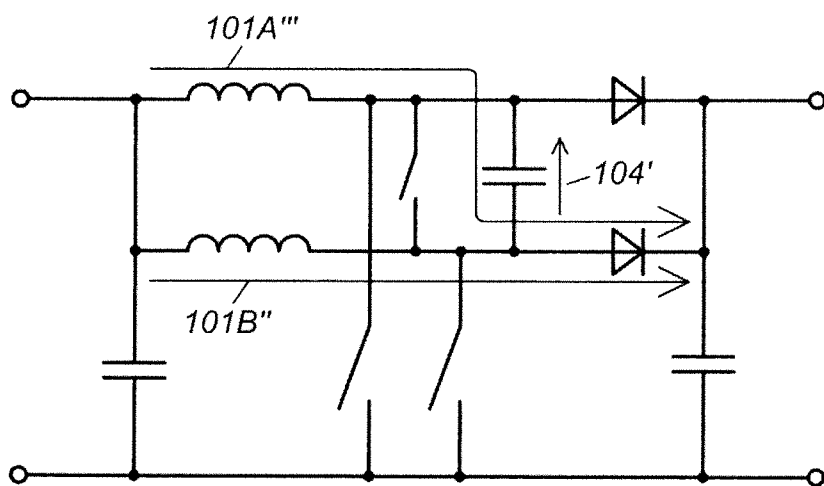


FIG. 2K

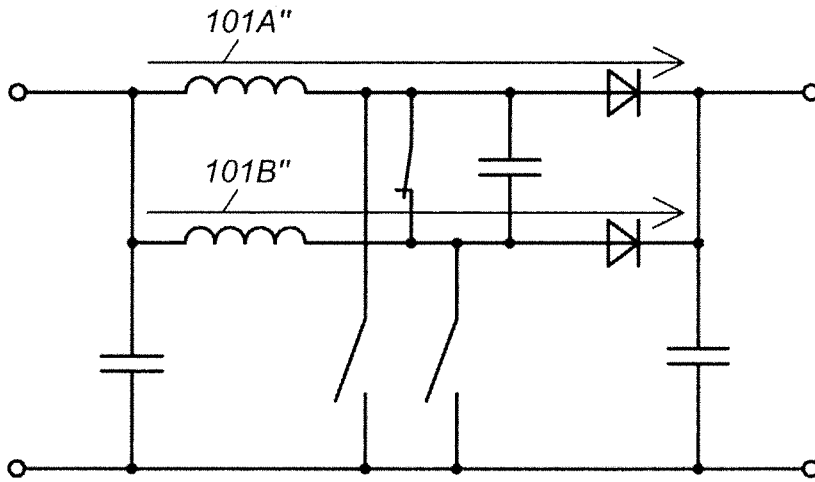


FIG. 2L

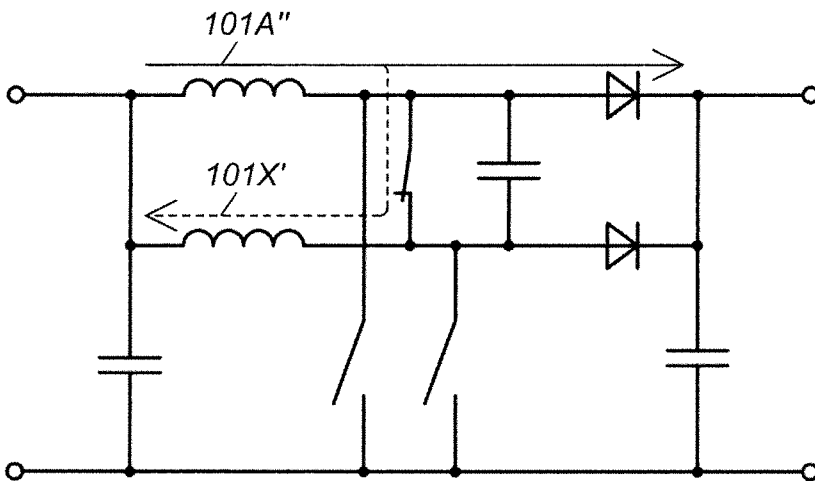


FIG. 2M

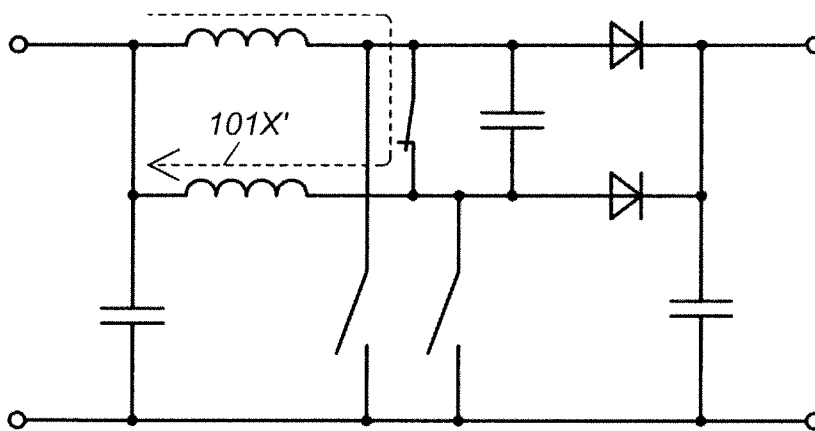


FIG. 2N

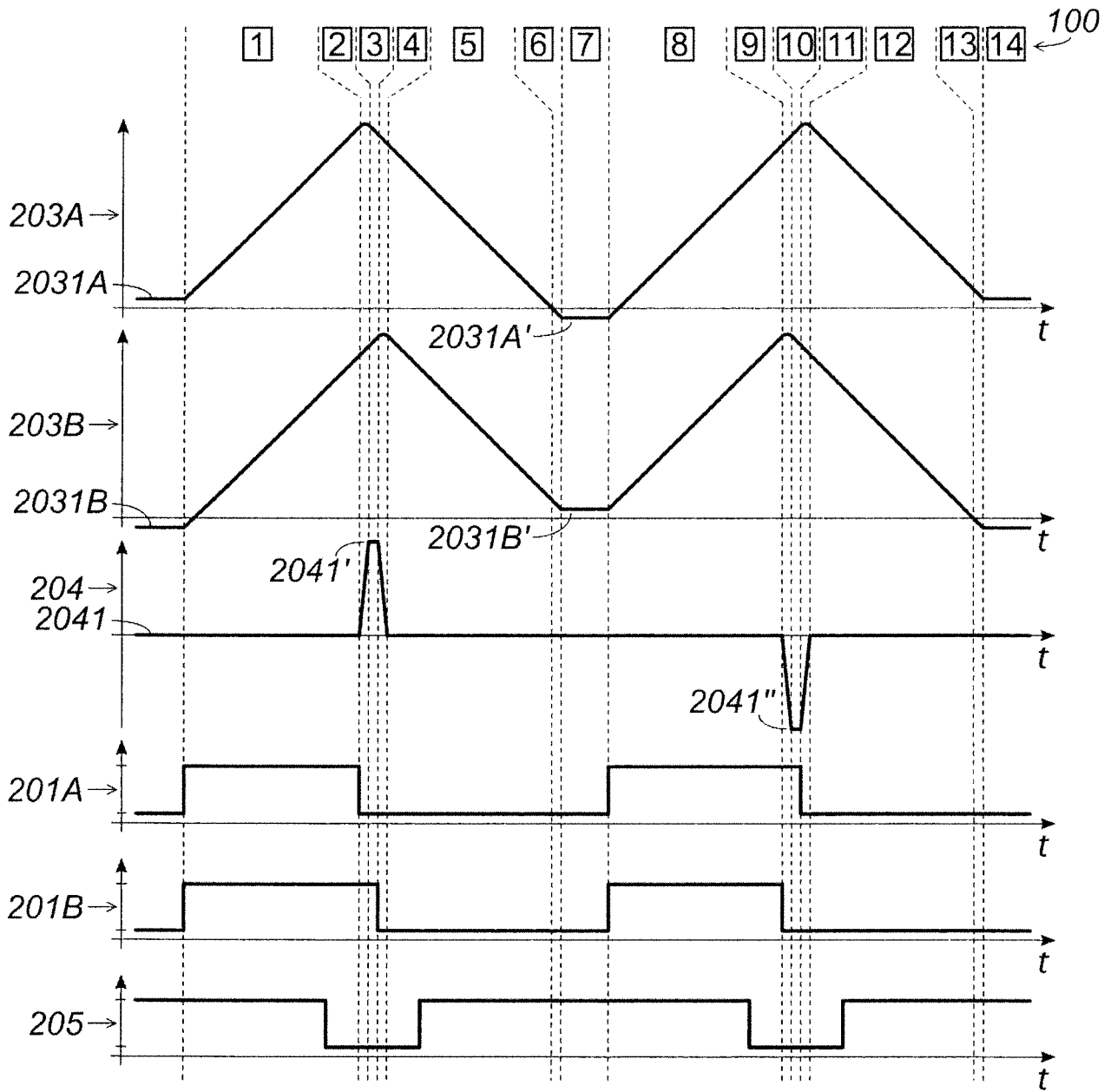


FIG. 3

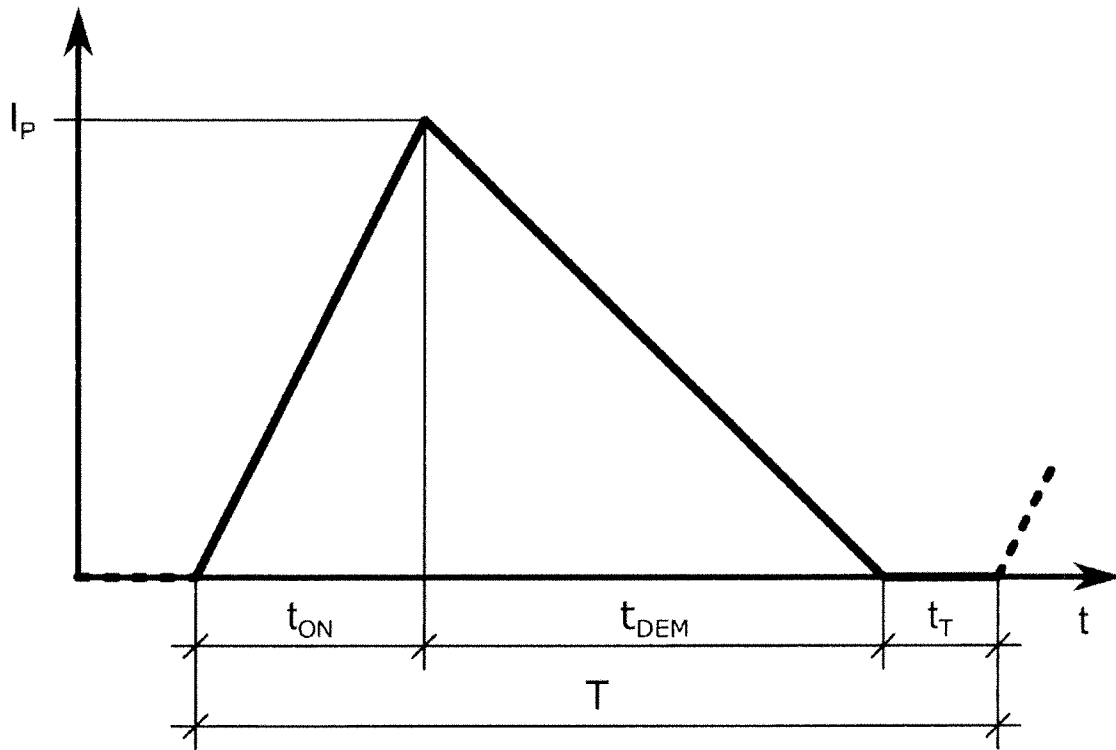


FIG. 4

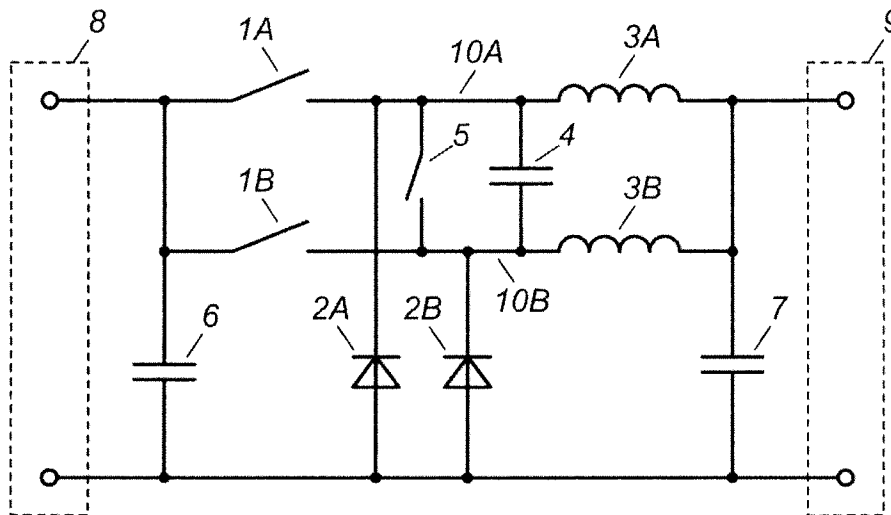


FIG. 5

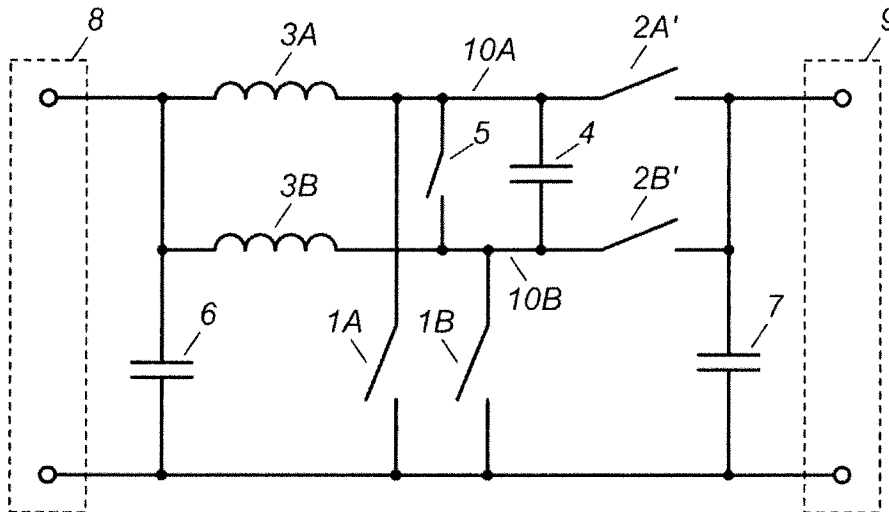


FIG. 6

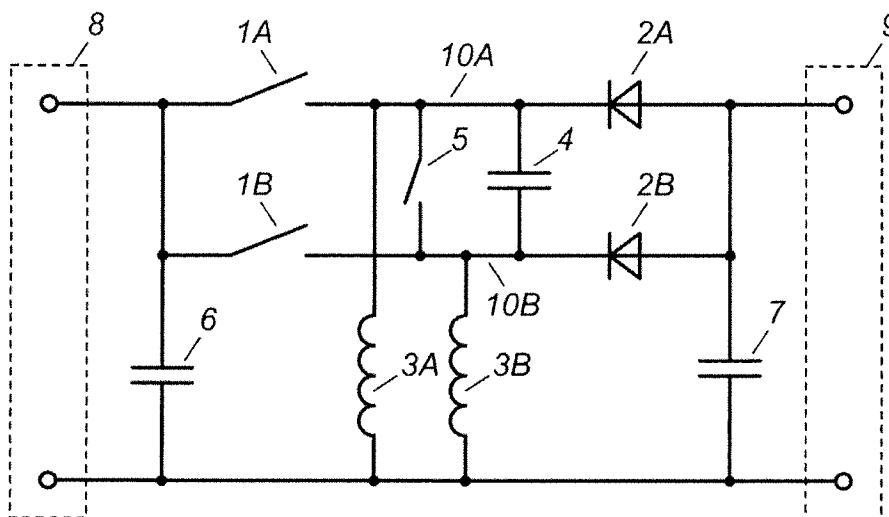


FIG. 7

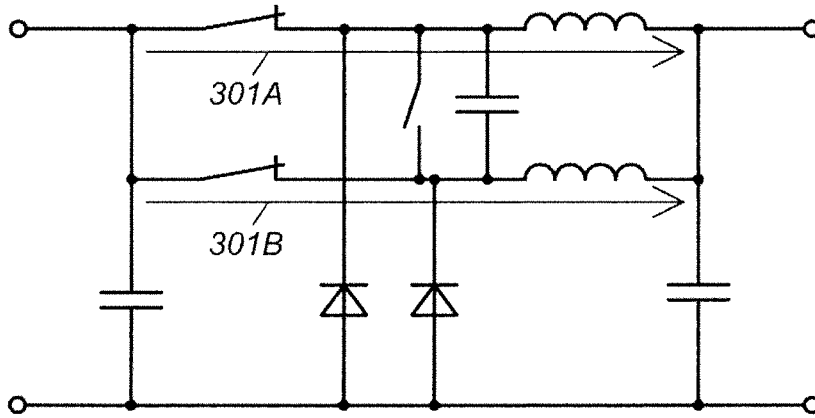


FIG. 8A

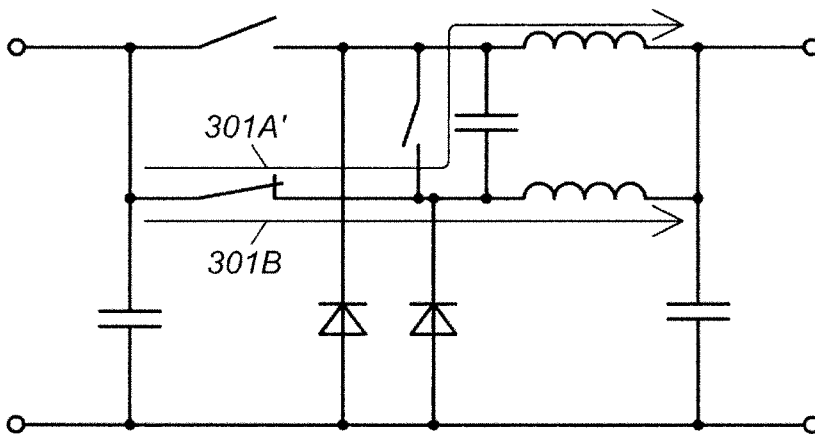


FIG. 8B

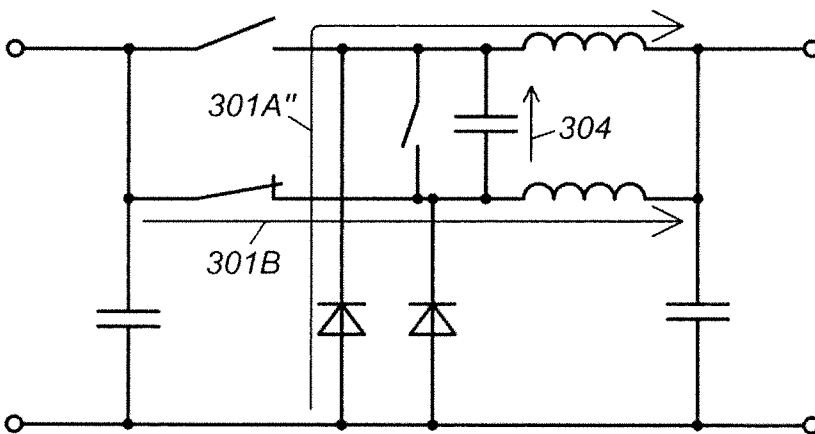


FIG. 8C

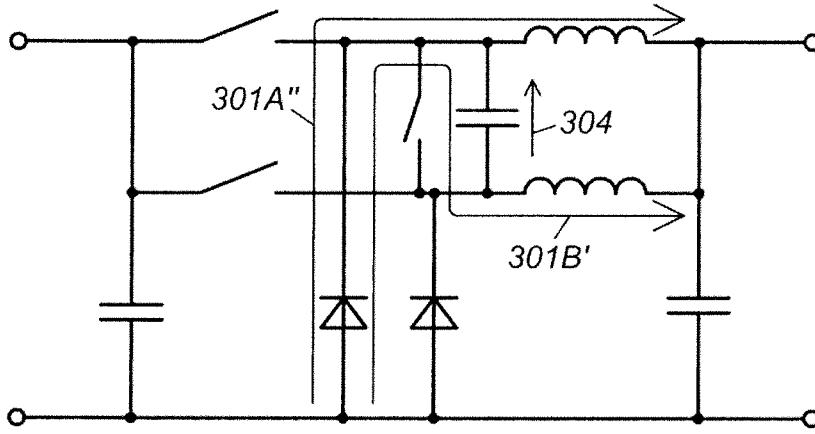


FIG. 8D

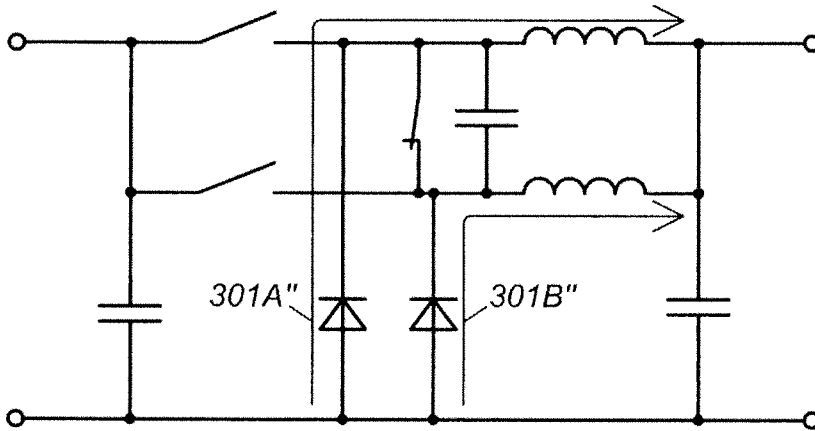


FIG. 8E

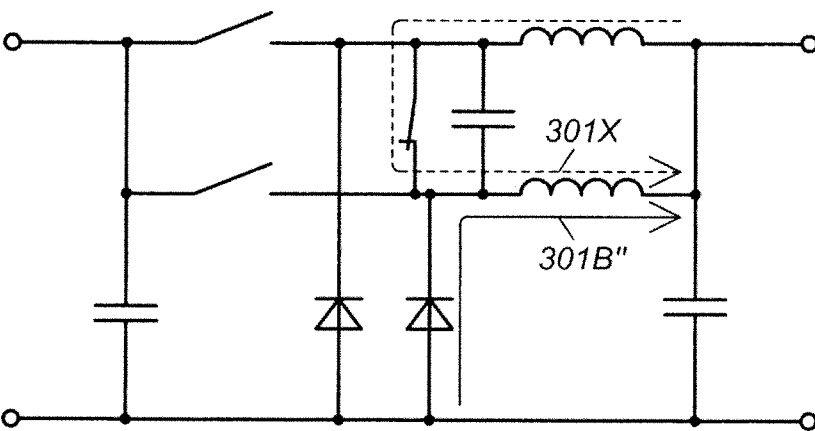


FIG. 8F

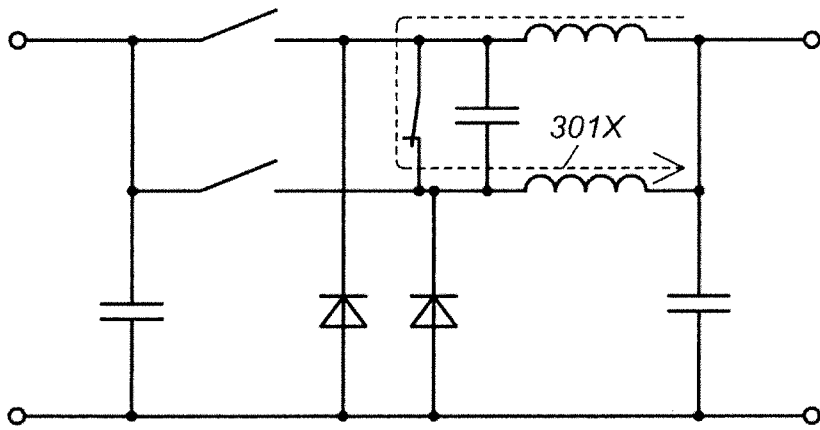


FIG. 8G

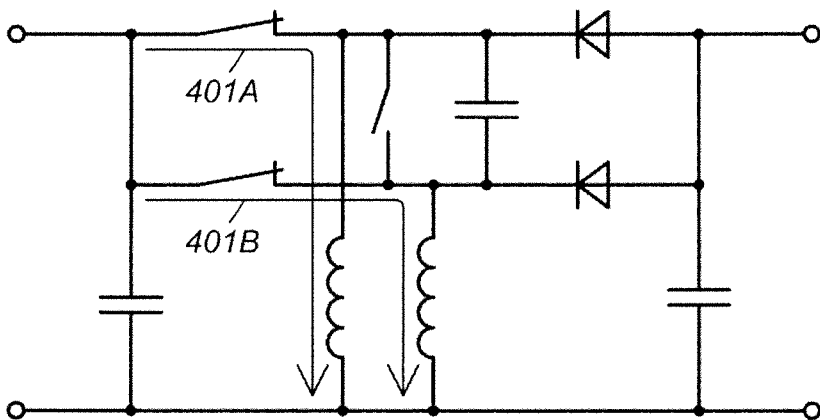


FIG. 9A

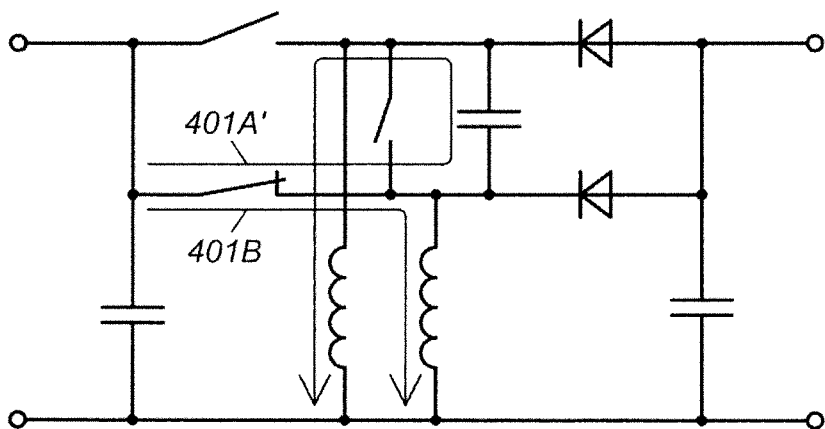


FIG. 9B

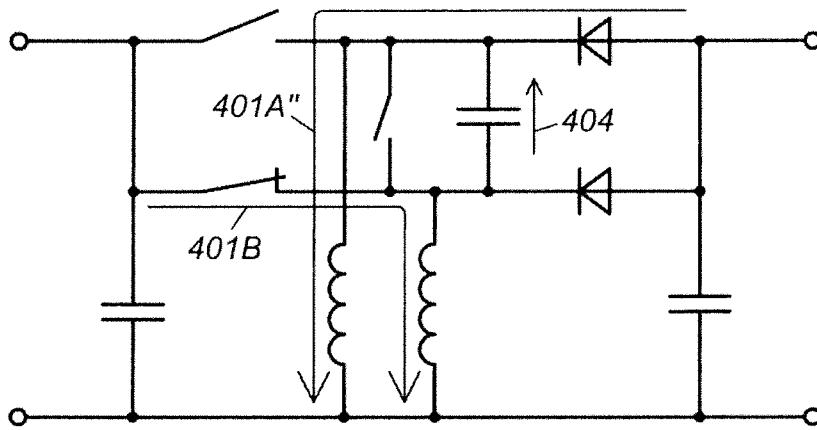


FIG. 9C

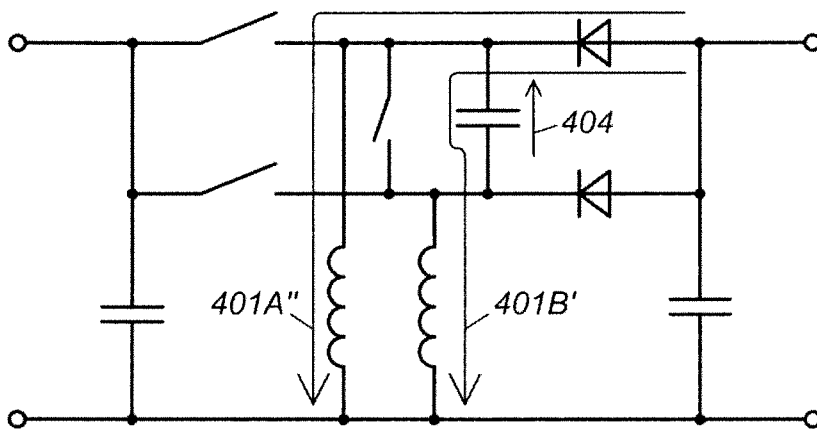


FIG. 9D

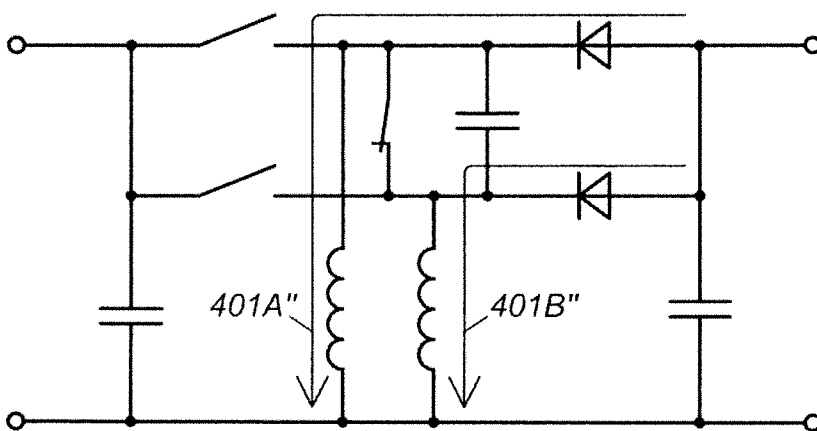


FIG. 9E

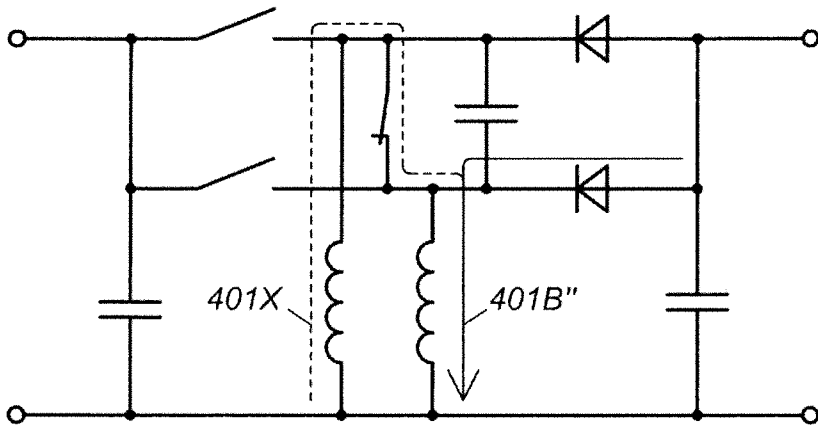


FIG. 9F

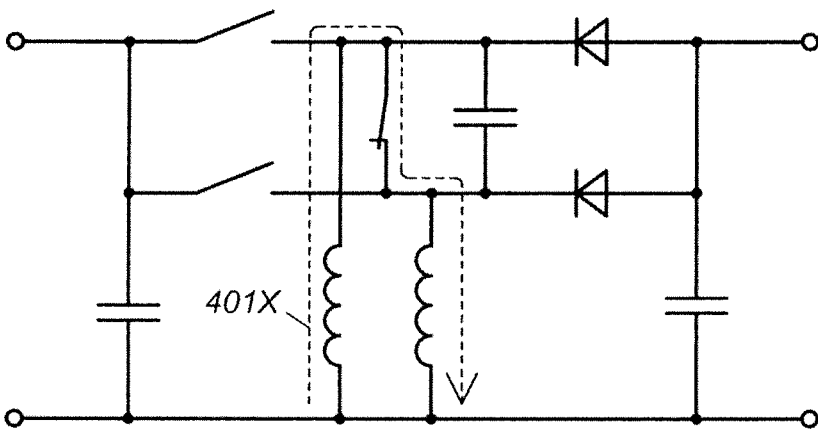


FIG. 9G

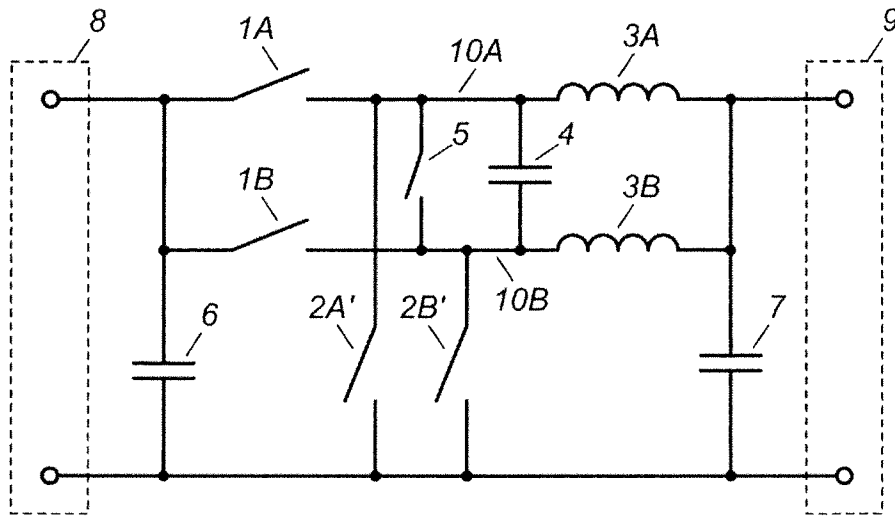


FIG. 10

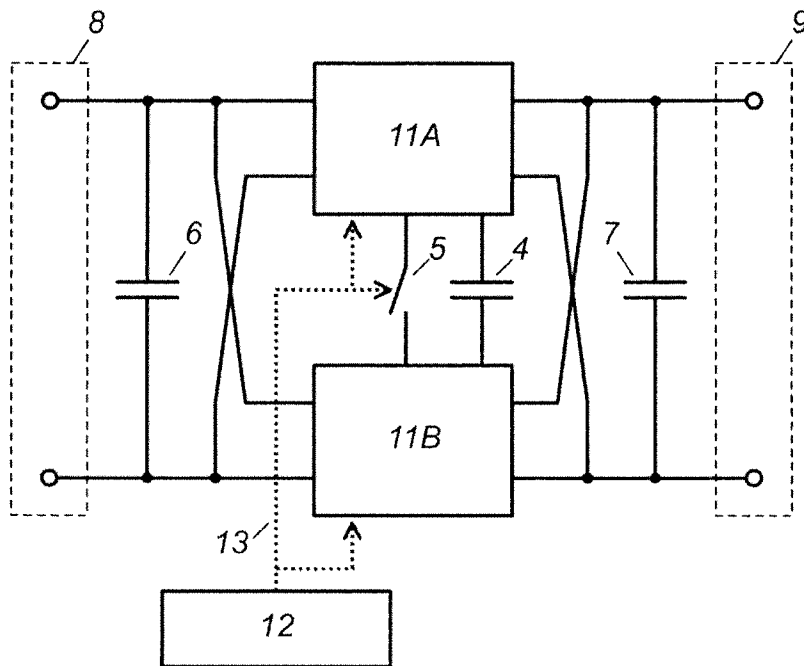


FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/068415

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/158
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/262752 A1 (GAIKWAD KHANDERAO MADHAV [PH] ET AL) 15 November 2007 (2007-11-15) figure 2	1-4
A	----- figure 2	5-7
X	CN 103 095 114 B (UNIV CHONGQING) 2 March 2016 (2016-03-02) figure 2	1
	----- -/--	

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
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- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search 17 September 2019	Date of mailing of the international search report 25/09/2019
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Gotzig, Bernhard

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/068415

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>NAM-JU PARK ET AL: "IBC Using a Single Resonant Inductor for High-Power Applications", IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 56, no. 5, 1 May 2009 (2009-05-01), pages 1522-1530, XP011249050, ISSN: 0278-0046 figure 3</p> <p style="text-align: center;">-----</p>	1-4
X	<p>DOO-YONG JUNG ET AL: "Interleaved Soft-Switching Boost Converter for Photovoltaic Power-Generation System", IEEE TRANSACTIONS ON POWER ELECTRONICS, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, USA, vol. 26, no. 4, 1 April 2011 (2011-04-01), pages 1137-1145, XP011355384, ISSN: 0885-8993, DOI: 10.1109/TPEL.2010.2090948 figure 1</p> <p style="text-align: center;">-----</p>	1
X	<p>XUDONG HUANG ET AL: "Parasitic ringing and design issues of high power interleaved. boost converters", POWER ELECTRONICS SPECIALISTS CONFERENCE; [ANNUAL POWER ELECTRONICS SPECIALISTS CONFERENCE],, vol. 1, 23 June 2002 (2002-06-23), pages 30-35, XP010596061, ISBN: 978-0-7803-7262-7 figure 4</p> <p style="text-align: center;">-----</p>	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2019/068415

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		DE 112007001127 T5	02-07-2009
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		WO 2007132345 A2	22-11-2007

CN 103095114	B	02-03-2016	NONE
