

ICs for Consumer Electronics MEGATEXT

Getting Started

MEGATEXT® Getting Started	
Revision History: 10.94	
Previous Releases: 08.93, 02.94	
Page	Subjects (changes since last revision)

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25\text{ °C}$ and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about “**Processing Guidelines**” and “**Quality Assurance**” for ICs, see our “**Short Form Catalog**”.

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1 Introduction

MEGATEXT® is a high sophisticated system with respect to feature content and flexibility. This paper shows an easy way

- to get familiar with MEGATEXT
 - by naming the most important features and modes of operation
 - by naming the documents that give you more detailed information
- to get quick first results in an application
 - by naming the favorite operation modes
 - by naming available development tools

2 Important MEGATEXT Documents

The following list shows some important documents and their roll in understanding and using MEGATEXT.

N = for novices

D = for display designers

P = for programmers

H = for hardware developers

A complete list of available MEGATEXT documents and their contents is available on request.

Document	Contents/Comment
Feature Presentation	
● System Overview (N)	Feature Highlights
Getting Familiar with MEGATEXT	
● Getting Started (N)	Index of Basic MEGATEXT Items, (Megatext reference documents have their own index)
● Index (N)	
Some More Details	
● Hardware Functions (H,P)	Description of Basic Chip and Block Structures and Functions
● Firmware Overview (P)	Overview on Tasks of the RISC, Principle of Acquisition

Document	Contents/Comment
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Application Hardware

- | | |
|------------------|--|
| ● Data Sheet (H) | Package, Pinning, Pin Specification
(level, timing)
Waveforms, Application Circuit Diagram |
|------------------|--|

Programmers Reference Document

Manuals with complete information of software controllable chip functions

- | | |
|------------------------------|--|
| ● M3L-Bus Registers (H,P) | List and Description of all M3L-Bus Registers |
| ● Display Functions (D) | Description of all Display Functions |
| ● Display Registers (D) | List of all Display Registers,
Quick Reference for the Experienced User |
| ● Acquisition Reference (P) | Description of Acquisition Operation Modes |
| ● Megatext Command Interface | List and Description of all MEGATEXT
Commands |

Application Notes

Application notes are accomplished by and by. The following items application notes are available or in preparation:

- Acquisition Application Note
- Bus Application Note
- Crystal Application Note
- Display Application Note
- Initialization Application Note
- Software Application Note
- Synchronization Application Note

3 Application Board and Periphery

3.1 Reset

There are three ways to reset the MEGATEXT chip:

- Power-on reset (reset by low supply voltage)
- Pin_reset (reset by an external reset signal connected to pin RES)
- Software reset (software reset via M3L-bus command)

The power-on reset condition is derived from the generation of the substrate bias voltage V_{BB} . The negative value of V_{BB} follows the supply voltage with a certain delay. If V_{BB} has reached approximately -2.6 V , the power-on reset is switched off and V_{BB} rises to approximately -2.0 V .

The pin RES can be used to guarantee a power-on reset in cases where the supply voltage rise is so slow that the internal power-on reset may not work reliably. A simple RC combination connected to pin RES will help. RES can also be used to reset MEGATEXT by an external controller.

The external controller may also use a M3L-bus subaddress to reset MEGATEXT. The M3L-interface itself recognizes the subaddress as an reset command and initiates a chip reset. The PU is not involved.

After all types of reset conditions are over the PU starts an initialization routine of approximately 2 ms duration. During the initialization SCL is forced to ground. When SCL is released, MEGATEXT is ready for commands via serial bus.

Related Documents

- SDA 5273 Data Sheet, Characteristics
- Hardware Functions
- M3L-Bus Registers, R255

3.2 Serial Bus

All communication with MEGATEXT is done via a 3 pin serial bus port consisting of the signals I²CEN, SCL, SDA. Via the serial bus an external controller can read or write data from/to MEGATEXT, i.e. MEGATEXT is a slave bus transmitter/receiver. The bus gives access to:

- to the MEGATEXT registers
- to the internal or external DRAM by using the data port registers

The bus can be operated in I²C or M3L mode. M3L stands for "MEGATEXT 3 line" and is specified in accordance with the USART interface of 8051 based micro controllers. The maximum clock rate is 1 MHz. Under certain conditions megatext may force the bus transfer to pause by holding down the SCL line (wait condition).

Relevant Documents

- SDA 5273 Data Sheet
- Hardware Functions
- Bus Application Note
- M3L-Bus Registers

3.3 Crystal/Resonator

The crystal frequency defines the lock range of the internal PLLs and the freerun frequency. The ratio between crystal frequency and nominal system clock is 20.48 MHz/24 MHz. Because MEGATEXT needs no special accuracy of the crystal frequency a ceramic resonator can also be used.

The center frequency of the horizontal PLL is proportional to the crystal frequency. In PAL mode the center frequency is 15.625 kHz for the typical crystal frequency of 20.48 MHz. Deviations from the typical crystal frequency will shift the range of the horizontal frequencies where the PLL is able to lock.

Relevant Documents

- SDA 5273 Data Sheet
- Crystal Application Note

3.4 Clocks

MEGATEXT has three Independent Clock Systems on Chip

- The acquisition clock (typ. 24 MHz)
generated by the acquisition PLL
- The display clock (typ. 24 MHz for 4:3 displays,
typ. 25.5 MHz for 16:9 displays)
generated by the display PLL
- The crystal clock

The acquisition clock is locked to the CVBS input signal. The ADC and the slicer use this clock.

The display clock can be in free run mode or can be locked to an external horizontal sync signal. Most parts of MEGATEXT use this clock. E.g. the RISC (PU), the display generator, the DRAM etc.

In 16:9 mode a special pixel clock is activated that accelerates the pixel rate from 25.5 MHz to 32 MHz. In 4:3 mode the pixel clock is identical to the display clock. The chip can be forced to a completely synchronous operation, i.e. acquisition clock and display clock are identical. As master clock source can be selected the acquisition clock (locked on CVBS), the display clock (in freerun or locked on external H) or an external clock supplied to pin CLK_ IO. If an external clock is used MEGATEXT has to be in freerun mode. Otherwise the PU may "run away" and DRAM data transfers will go wrong. Clock source selection is done by R112.

The acquisition clock and the display clock are generated by a voltage controlled oscillator (VCO). The range of the VCO that generates the display clock has to be adjusted to the application (R85).

Relevant Documents

- M3L-Bus Registers (R82, R85, R112, R113)
- Sync Application Note

3.5 Display Synchronization

MEGATEXT is prepared for PAL/NTSC/SECAM 1F_H or 2F_H displays.
MEGATEXT can be sync master or sync slave.

As *sync master*, MEGATEXT generates sync signals in a freerun mode or can follow sync signals separated from the CVBS input. The pins HS, VS and TCSQ deliver the sync output signals. A TV and a VCR time constant is selectable to adjust the horizontal PLL that locks on the CVBS. Also some vertical processing functions are available to stabilize the V output of weak CVBS signals. Several freerun modes (525/625 lines, non-interlace, etc.) are available. Their timing is derived from the 20.48 MHz crystal.

As *sync slave*, the display PLL of MEGATEXT follows an external horizontal sync signal HS. In this case the pins HS and/or VS/VCS work as sync inputs. For 2f_H input signals a prescaler (divider by 2) has to be activated.

Sync input/output selection is done in R82.
Sync mode selection is done in R113, R114.

Relevant Documents

- M3L-Bus Registers (R96, 98, 112 ... 117)
- Sync Application Note
- Hardware Functions

3.6 RGB

MEGATEXT has RGB outputs with internal load resistors of typical 270 Ω connected to the pin RGB_GND. The output signal has two components: a horizontal sync pulse and the RGB display signal.

The horizontal sync pulse changes from clamp level (= ground) during horizontal flyback period to black level during the rest of the line. The width and the position of the sync pulse (= clamp period) is selectable by R11x. The black level can be changed from 0 V to 0.9 V in seven steps by R83. This corresponds to a *brightness control* of the RGB output. The RGB display signal is added to the black level of the sync pulse. It is zero in the clamp period. Its peak to peak amplitude can be changed in 31 steps from 0 to 1.3 V by R83. This corresponds to a *contrast control* of the RGB output. The *resolution of the RGB display* signal is 4 bit / 4096 colors independent of the contrast control.

Relevant Documents

- Hardware Functions
- SDA 5273 Data Sheet

3.7 Internal DRAM

The internal DRAM has a size of 24 Kbyte. The memory organization can be described as 6 DRAMs of 4 Kbyte each, organized 4K x 8 bits. The 6 DRAMs are addressed in parallel and one byte is selected by defining one of the byte positions 0 ... 5. The DRAM address can be in binary or in row/column format.

The row/column address format divides the IRAM into 4 blocks, each block into 25.6 rows and each row into 40 columns.

The *allocation of the IRAM* for different functions is flexible.

Block 0, row 0 ... 8 and row 24, 25 is reserved as PU workspace.

Block 0, row 9 ... 23 can be used as PCS and/or RISC program memory.

Block 1 can be used to store 6 teletext pages.

Alternatively it can be used for pixel graphics and/or RISC programs.

Block 2 can be used as a first display memory and page memory.

Alternatively it can be used for pixel graphics and/or RISC programs.

Block 3 can be used as a second display memory and page memory.

Alternatively it can be used for pixel graphics and/or RISC programs.

Type of Data	Organization of IRAM Area
Display words for full performance	<ul style="list-style-type: none"> – block 2 and/or 3 – rows and columns corresponding to the display positions on the screen – bytepositions 1 to 5 – byteposition 6 is free
Display words for reduced performance	<ul style="list-style-type: none"> – block 2 and/or 3 – rows and columns corresponding to the display positions on the screen – bytepositions 1 to n, n = 2, 3, 4 – byteposition n + 1 to 5 are free
PCS pixel information	<ul style="list-style-type: none"> – block 0, row 8 to 23 – byteposition 1 to 6
Graphics	<ul style="list-style-type: none"> – blocks and rows: please refer to the "Display Functions" reference manual – byteposition 1 to 6
RISC programs	<ul style="list-style-type: none"> – any contiguous binary IRAM address range – byteposition 1 to 6
Teletext pages in transmitted format (i.e. not converted for display)	<ul style="list-style-type: none"> – any block except block 0 – any byteposition: one byteposition for 1 Kbyte (basic page)
Multi purpose RAM area for the external controller	<ul style="list-style-type: none"> – any address range except for areas in block 0 reserved for the PU

The M3L-bus gives bitwise access to the IRAM via data ports. Each data port consists of several registers to define the type of access, the type of address, the address increment mode, the address itself and one byte of data. For more information how to *access the IRAM* via bus, please refer to the document "M3L-bus registers", R48 ff.

Relevant Documents

- Hardware Functions
- M3L-Bus Registers, R48 ff.
- Display Functions
- Acquisition Reference

3.8 External DRAM

The use of an external DRAM is optional.

Megatext expects one external DRAM with an organization $x \ 4$ bit. The maximum DRAM size is $4M \times 4$ bit. The data access time from CAS has to be at least 60 ns. MEGATEXT can be adopted to different refresh requirements. The refresh period can be varied in a wide range by a MCI command.

The external DRAM can be accessed by the M3L bus via register data ports. The external DRAM can be used to store any type of data. It can be used to store

- a large number of teletext pages
- display data like graphics or menus
- downloadable character sets
- RISC programs.

The transfer of data from the external DRAM to the internal DRAM (IRAM) is supported by PU commands and is very fast.

Relevant Documents

- SDA 5273 Data Sheet
- Megatext Command Interface (software refresh)

3.9 CVBS

MEGATEXT separates teletext and other data services from the CVBS signal. It also separates the sync information from the CVBS. The CVBS may be a PAL or a NTSC signal.

The CVBS is ac coupled to MEGATEXT and digitized by a 7 bit ADC. At the beginning of a new synchronization up or down pulses pull the CVBS into the ADC range. The sync level of the CVBS is automatically clamped to ground as soon as the CVBS_PLL has locked.

The ADC range is proportional to V_{REF} and typically $1.9 V_{pp}$ (Volt peak to peak) for $V_{REF} = 3.0 V$. For optimum resolution the maximum peak level of teletext data should be 1.8 V above sync level. The white level of video information may exceed the ADC range. The teletext slicing level is restricted to a range from 0.25 to 0.75 of the ADC range. This gives a lower limit for the CVBS amplitude.

Relevant Documents

- SDA 5273 Data Sheet

4 Editing the Display

The easiest way to create a display with MEGATEXT is to use the MEGATEXT display editor "DEDITOR" running on a PC and a monitor interface to the MEGATEXT IC that downloads online the PC display. A TV screen connected to MEGATEXT will give you a realistic impression of your display design.

It is also possible to convert data from Bildschirmtext (Viewdata) to the *SDO format*. SDO files can be downloaded into the MEGATEXT display memory. Pictures can be scanned and downloaded as graphic data.

In general the display data within MEGATEXT defines a virtual display. In some applications all display information is visible simultaneously on the screen. In other applications the virtual display can be scrolled vertically and/or horizontally behind the visible screen window to make all display information visible.

The MEGATEXT Display Consists of 3 Layers

- The character position oriented **display area**
stored in the display memory areas of the IRAM
- The **graphics**
stored in the graphic memory areas of the IRAM
- The **pixel cursors**
stored in a special ROM

Display Area

The MEGATEXT display area is defined by the data of the display memory and the contents of the display registers, both registers and display memory located in the IRAM. For each character position a display data word is stored in the display memory. The display data word defines the shape and all attributes of a character. The character shape can be a character from the **character ROM** or a downloaded **PCS character** from the PCS memory area in block 0 or an overlay of ROM and PCS characters.

The display memory is split into two sub areas: one in IRAM block 2 and one in block 3. Each display area consists of the address range:

row 0 to 23,
column 0 to 39 and
byteposition 0 to 5.

By use of mask registers parts of the display memory areas, e.g. the higher bytepositions or some rows, can be replaced by register data. The memory area disabled for display by mask registers can be used for other purposes e.g. bytepositions 4 and 5 as two chapters of teletext page memory.

The two display areas can be used independently from each other as an inner screen display area for a central text display of max. 24 rows/40 columns or as an outer screen display area outside a box of 24 rows/40 columns. The inner and outer screen display area together form a display of 32 rows/64 columns.

In double scan applications the two display areas can be placed above each other resulting in a text display of 48 rows/40 columns. The two display areas can be placed beside each other resulting in a text display of 24 rows/80 columns (80 character mode).

The 80 characters can be made visible in $1f_H$ applications by choosing a pixel rate of 24 MHz (double speed). In $2f_H$ applications with a typical pixel rate of 24 MHz only appr. 52 of the 80 characters are visible simultaneously on the screen. The others are hidden but can be scrolled into the visible area.

Graphics

The graphics are processed independently of the display memory. They can be positioned by the user. Graphic memory areas can be defined in IRAM blocks 1, 2 and/or 3 depending on the size of the graphic.

Pixelrate

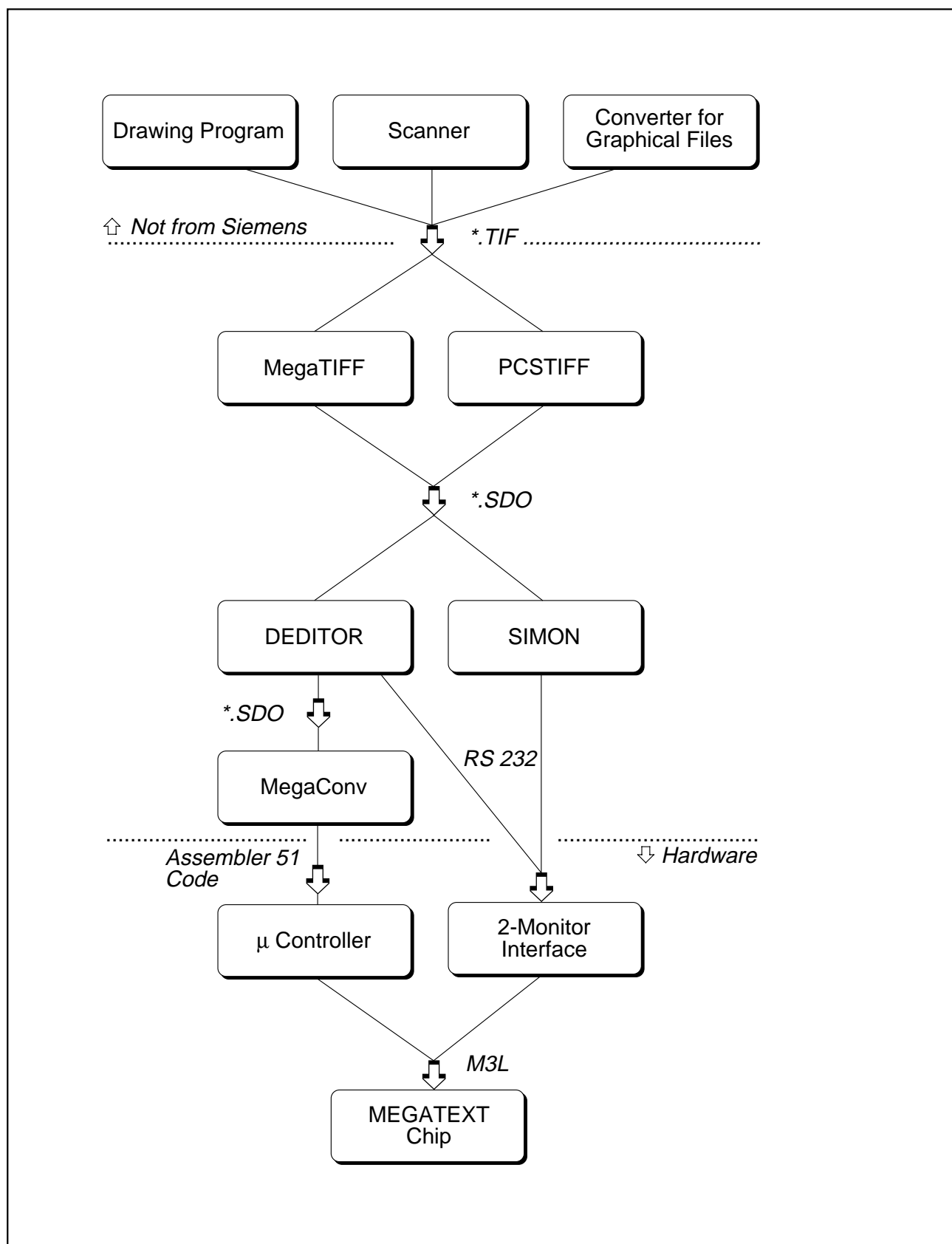
In 16:9 mode a FIFO is used to accelerate the pixel rate by a factor of 1.33. The FIFO can store a maximum of 64 characters. The margin area outside the 64 characters is filled with the repetition of the first respectively the last of 64 characters.

The document "DEDITOR" describes the installation and use of the DEDITOR. The document "Display Functions" explains how to invoke the different display features.

Relevant Documents

- System Overview: Display Features
- Synchronization Application Note
- Display Functions
- Display Registers
- M3L-Bus Registers, Pixelrate: R114

Display Development Tools



Drawing Program:	For the design of graphical elements. We recommend the "DESIGNER" from Micrografx.
Scanner:	To generate pixel graphics (e.g. from photos). We recommend the model 256 from LOGITECH. (Gray scale handy scanner)
Converter:	To convert TIFF files from other sources. We recommend the Graphic Workshop (Shareware).
MegaTIFF:	Converts Pixel oriented TIFF files into MEGATEXT SDO format. Uses the graphic mode.
PCSTIFF:	Converts Pixel oriented TIFF files into MEGATEXT SDO format. Generates arrangements of programmable character (PCS).
DEDITOR:	Display Editor for MEGATEXT Displays. Generates SDO files.
SIMON:	For editing and controlling MEGATEXT Registers; downloading of SDO files.
MegaConv:	Converts SDO files to Assembler 51 code.

5 Acquisition

5.1 Acquisition and Display of Teletext Data

The slicer separates teletext data from the CVBS. The slicer can operate in two different modes. The first mode is active during the data entry window defined in R96, 97, the second mode is active during a single line defined in R98. The two mode have different framing codes and clock rates. The first mode is used to acquire normal teletext data, the single data line is used to acquire data from services like VPS.

The RISC (PU) checks, selects and stores the data requested. For this task the PU needs a memory buffer of typically 1 Kbyte allocated in the IRAM. The teletext pages are stored in chapters of 1 Kbyte. If stored in the IRAM each chapter fills one byte position of a block. In an external 4M x 4 bit DRAM 2048 chapters can be used. To display a received teletext page the teletext data has to be translated into character display words of the display memory. That means for level 1 teletext essentially a conversion of serially transmitted attributes into parallel attributes of the character display words. This serial parallel conversion (SPC) is also done by the PU.

An example of how to initialize the MEGATEXT acquisition in an easy application is available in the application note "acquisition". After having gone through the other relevant documents it may be a good basis to get the acquisition working.

Relevant Documents

- Specification of World Standard Teletext
- Firmware Overview
- Acquisition Reference
- Application Note Acquisition Software
- MEGATEXT Command Interface (MCI)

5.2 Acquisition of VPS Data

MEGATEXT is able to receive VPS data as transmitted in Germany as VCR programming service. The data is checked by the PU and stored in the DRAM.

VPS data can be received if MEGATEXT acquisition is in PAL mode (R109, D5) and the special data line acquisition (R98) is activated.

Relevant Documents

- Specification of VPS
- MEGATEXT Command Interface (MCI)

5.3 Signal Quality

MEGATEXT can collect some information about the quality of the CVBS. This information is derived from the state of the CVBS-PLL and from the teletext data error rate. A special MCI command starts the signal quality analysis. The information can be read out of registers located in the IRAM.

Relevant Documents

- Hardware Functions
- MEGATEXT Command Interface (MCI)

6 Downloadable RISC Software

... is not really an item for a paper titled "**Getting Started**".

Nevertheless: It is possible to add new or modified commands to the MCI by writing special RISC routines. This software can be stored in the ROM of the external controller and has to be downloaded into the internal RAM. The RISC is a special Siemens development for MEGATEXT and not compatible with any standard RISC you will find on the market. To write RISC software you need a complete MEGATEXT development environment including an emulator and detailed know how about the RISC and the MEGATEXT firmware. The documentation is in preparation and only available on special request.