

## ICs for Consumer Electronics MEGATEXT

Hardware Functions

<b>MEGATEXT® Hardware Functions</b>	
<b>Revision History: 10.94</b>	
Previous Releases: 08.93, 02.94	
Page	Subjects (changes since last revision)

## Data Classification

### Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

### Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25\text{ °C}$  and the given supply voltage.

### Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about “**Processing Guidelines**” and “**Quality Assurance**” for ICs, see our “**Short Form Catalog**”.

### Edition 10.94

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## 1 Chip Overview

The block diagram shows the main circuit blocks of the MEGATEXT<sup>®</sup> chip:

CVBS A/D Converter

CVBS Sync Slicer and Timing

Teletext Data Slicer

Acquisition Interface

Processing Unit (RISC)

Internal Memory (IRAM)

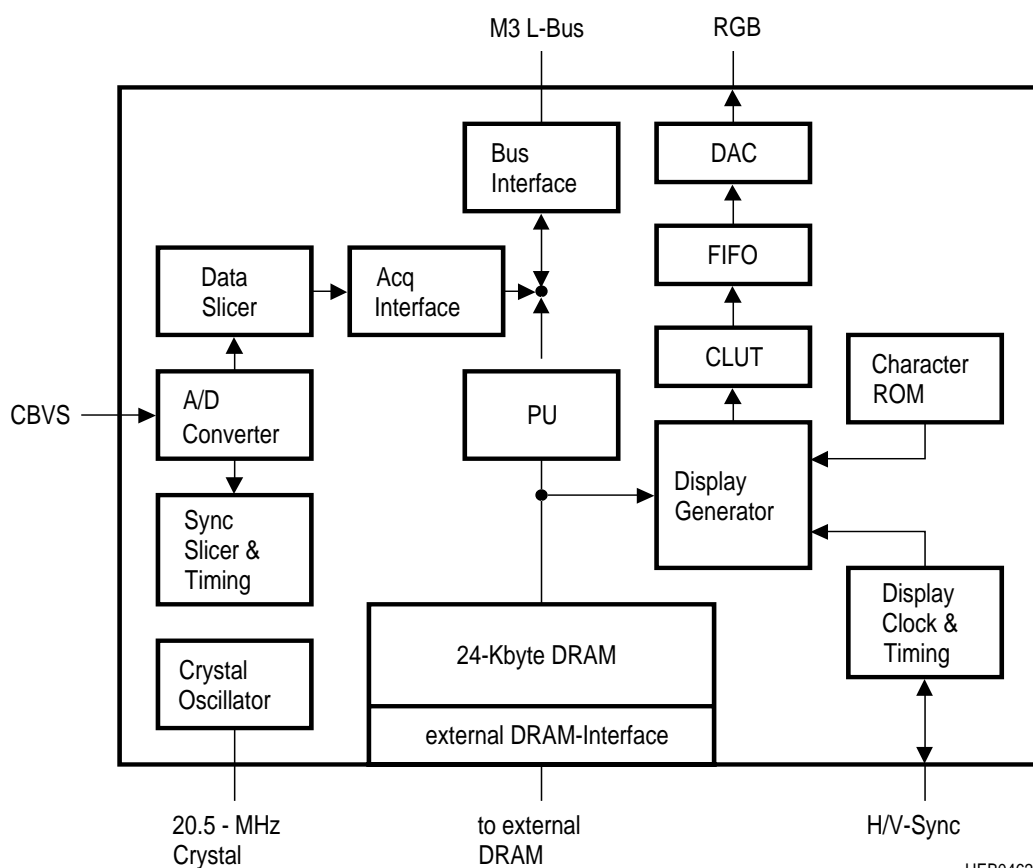
Display Generator with Character ROM and CLUT

Display PLL and Timing

16:9 FIFO

RGB D/A Converter

M3L-Bus Interface



**Figure 1**  
**Block Diagram**

Although mainly digital the chip circuitry comprises analog functions like ADC, DAC and PLL and a 24-Kbyte DRAM. The chip is processed in Siemens 1M DRAM technology. This is a 0.9  $\mu\text{m}$  triple poly CMOS n-tub technology with substrate bias voltage. The substrate bias voltage generator is on-chip. The digital circuits use generally dynamic precharge logic.

The chip needs a single 5-V supply. The supply pins are divided into analog and digital supply pins. The printed circuit board layout should take this into account. MEGATEXT needs also a 3-V reference voltage. The range of the ADC for the CVBS input and the RGB output signals are proportional to this voltage. A substrate bias voltage of typ. – 2.5 V is generated on-chip.

The package is a P-SDIP-52 or but a preliminary version SDA 5273 without the 16:9 feature is only available in P-LCC-68. The bondout version for the MEGATEXT emulator is housed in a C-PGA-120 package.

### Clock System

The chip has three independent clock systems:

- the acquisition clocks TA24 (typ. 24 MHz) and TA12 (typ. 12 MHz) normally locked to the CVBS,
- the display clocks TD24 (typ. 24 MHz) and TD12 (typ. 12 MHz) normally locked to external H/V sync or in freerun mode,
- the pixel clock TA32 (typ. 24 MHz for 4:3 display and typ. 32 MHz for 16:9 displays) locked on the display clock.

It is also possible to lock the display clock to an external 6-MHz, 24-MHz or 27-MHz clock or to use an external 24-MHz master clock.

### Power-Up & Reset

There are three ways to reset the MEGATEXT chip:

- |  |                  |
|--|------------------|
| – reset by low supply voltage                            | : power-up reset |
| – reset by an external reset signal connected to pin RES | : pin reset      |
| – software reset via M3L-Bus command                     | : software reset |

The name of the reset signifies the reset initiation and not the reset function. The three types will reset

- all hardware registers to their default values,
- the clock system,
- the PU program.

After hardware reset the PU sets all registers which are not yet set to defined values to their default values. This concerns especially the registers located in the internal DRAM.

The power-up reset condition is derived from the value of the substrate bias voltage. The value of the internally generated substrate bias voltage depends on the value of the supply voltage. The substrate voltage will follow the supply voltage with a certain delay. If the substrate bias voltage is too high, a hardware reset is produced. This is necessary to prevent chip latch-up, which otherwise might be caused by processes in the internal DRAM during supply voltage rise. A very short dip of the supply voltage does not disturb the substrate bias voltage and will not cause a reset, but may

lead to an undefined state of the internal processing unit. For more details please refer to the MEGATEXT IC specification.

The pin RES can be used to guarantee a power-up reset in cases where the supply voltage rise is so slow that the internal power-up reset may not work reliably. A simple RC combination connected to pin RES will help. RES can also be used to reset MEGATEXT by an external controller.

In the case of the software reset the external controller uses an M3L-Bus telegram instead of a special wire to reset MEGATEXT. The M3L-interface itself recognizes the reset command and initiates a chip reset. The PU is not involved, so this reset mode works even when the PU software is upset.

## 2 A/D Converter

Before conversion, the analog CVBS signal is clamped in a two-step process to its sync level. First the signal offset is adjusted until the sync pulse lies within the converter range. In step two, a pulse from the HPLL is used for clamping the sync level finally to ground.

The flash converter converts the clamped signal to its 7-bit binary coded digital equivalent. The performance of the ADC fulfills all requirements for succeeding sync separation and digital WST data-slicing functions.

Sample rate	24 MHz (nominal)
Digital resolution	7 bits, 1 LSB = 15 mV (typ.)
Integral nonlinearity	4 LSB (typ.) monotone
ADC input voltage range	$0.66 \times V_{REF} = 2 \text{ V}$ (typ.)
Input capacitance	30 pF
Ext. coupling capacitor	100 nF recommended
Sync amplitude	0.1 V min – 1 V max
Teletext data amplitude	0.3 V min – 1.8 V max

## 3 Sync Slicer and Clock (HPLL)

The HPLL and SYNC processing circuit generates a line-locked 24-MHz acquisition clock and separates the horizontal and vertical synchronization out of the digitized CVBS signal. The highly sophisticated H-signal processing allows use of the acquisition clock as a stable display clock.

To reach the greatest possible signal/noise ratio, the digitized CVBS signal is lowpass filtered. The sync separation establishes the sync bottom, the black level and right between the two of them a sync threshold. Every time the CVBS signal decides to cross the sync threshold, an HS pulse is released to the horizontal phase-locked loop. If CVBS not only crosses the sync threshold but stays for a longer time below the threshold, a vertical sync pulse is detected.

The core of the HPLL is basically a digital PLL consisting of a phase detector, a second-order low-pass and a DTO. The art of phase detection in the HPLL is a very elaborate one, evaluating a fine and a coarse phase difference between the sync-separated HS and the PLL HS. The fine phase difference is computed by integrating samples of the filtered CVBS signal on the leading edge of the

sync pulse. The coarse one is determined by counting just the clock periods between the PLL HS and the sync-separated HS. Like in any other PLL, the phase difference gets some filtering and is at least translated into an increment for the DTO. The DTO cruises at a crystal frequency of 20.5 MHz to avoid problems caused by harmonics. The sawtooth output of the DTO is converted to a 6-MHz trapezoidal signal. This is a line-locked signal. An analog PLL multiplies the 6 MHz by 4 to get the 24-MHz acquisition clock.

The line-position counter of the HPLL is operated with the 24-MHz acquisition clock. In fact it is this counter that is locked to the sync-separated HS. The PLL HS is simply derived by decoding the zero crossings of the line position counter. All other signals that have to be locked to the horizontal period of the CVBS are decoded from this counter.

#### 4 Data Slicer

The all-digital slicer is capable of processing all digital TV data services.

This includes:

- 6.9375 Mbit/s World System Teletext (WST, 625 lines)
- 5.7272 Mbit/s WST, 525 lines
- 2.5 Mbit/s Video Program System
- 503.496 kbit/s Telecaption

The data slicer consists of four main building blocks related to the basic functions it has to perform:

- Slicing-level generation
- Frequency compensation
- Separation of the data clock
- Data separation

The operation of these blocks is supported by a timing and control unit, providing also a programmer's interface.

The A/D-converted CVBS signal is first fed into the slicing-level generation circuit. The slicing level is calculated by lowpass filtering the CVBS input during the clock run-in. Two different modes for filtering can be selected via the M3L-Bus. In the first mode the slicing level is obtained by lowpass filtering during the clock run-in sequence. The second mode uses samples from clock run-in sequences of eight consecutive lines for slicing-level generation.

After subtraction of the slicing level, distortions caused by the not so perfect transmission channels can be compensated by applying either a lowpass or highpass filter. The optimum filter can be determined by the slicer or can be selected by programming the corresponding M3L-Bus register.

Separation of the data clock is achieved by feeding the zero crossings of the frequency-compensated signal to the clock PLL. The zero-crossing information is used to synchronize the DTO to the incoming data. The PLL filter coefficients during the clock run-in are hardwired, whereas adjustment after the clock run-in can be selected via the M3L-Bus. Decoding of the DTO delivers the data clock.

To enhance the distinction between a data 0 and a data 1, a pair of filters (a lowpass and a bandpass) is employed. A comparator compares the outputs of these two filters.

### 5 Acquisition Interface (AI)

The acquisition interface processes the serial data from the slicer. It does some easy but time critical jobs and leaves the more intelligent acquisition tasks to the PU.

Functions of the AI:

- byte synchronization
- bit-serial to byte-parallel conversion
- framing-code detection (VPS or WST)
- error tolerance for framing code
- status information about errors and type of data (WST, VPS, e.g.)
- data synchronization from acquisition clock to display clock (= PU clock)
- buffer for one line of text data

The AI is connected to the PU by a data bus and interrupt lines. The AI gives an interrupt to the PU when a valid teletext format is detected. A second interrupt may follow if the data buffer of the AI is read out too fast. In addition to the acquired data, the AI transmits a byte with status information about the error situation and type of data (VPS, WST) to the PU.

### 6 Processing Unit

The internal processing unit is the central data turntable between acquisition, memory, display and bus interface. It performs the main acquisition functions (including page selection, memory management and parity, hamming, cyclic redundancy checks), serial-to-parallel attribute conversion to build up a basic display from a received page, selects the language table automatically, and executes ROM stored subroutines for the support of higher teletext levels, TOP and FLOP. Further tasks are register and memory initialization after power-on or at external command and watchdog timer management. The PU can also execute user-defined subroutines stored in the internal DRAM.

The processing unit has been designed in RISC (Reduced Instruction Set Computer) architecture, thus allowing complete operations to be executed in a single 12-MHz cycle. The data and the command word width is 24 bit. The command word is divided into a 6-bit operation code, two 6-bit source addresses, and a 6-bit destination address. The command words are stored in a ROM organized as  $8\text{ K} \times 24\text{ bit}$ . The 64 registers of the processing unit are realized separately, whereas the working memory is part of the internal memory. The following list shows some characteristics of the PU.

#### Main Characteristics of the MEGATEXT Processing Unit (PU)

- 24-bit RISC processor
- 1-stage pipeline
- 32 basic instructions
- table addressing in ROM
- READ ROM instruction
- support of row/column or binary addressing in internal or external RAM
- executable code in ROM and/or internal RAM
- 4 Kwords ROM code
- 3-address machine
- 32 triple-port general-purpose registers



- 24 multiple-port special-purpose registers
- 18 constant registers
- 40-bit interrupt handling
- 8-level interrupt priority logic
- reentrant interrupts possible
- enable bits for each interrupt request and each process
- serial interface for sampling 7-bit status information and 5-bit interrupt requests from chip (maximum interrupt response time = 12 cycles)
- eight fast interrupt requests (interrupt response time = 2 cycles)
- interrupt output to external controller
- fast hardware stack (16 words) in PU for subroutine calls, data push and interrupt return addresses (level 2-7)
- automatic stack overflow/underflow handling (per interrupt)
- software-configurable RAM stack
- additional scratch register for M3L and stack interrupt return addresses (level 0,1)
- direct or indirect jumps
- 90 different jump conditions
- interface with M3L-Bus or acquisition interface (AI)
- interface with CRC logic
- watchdog timer

To understand the operation mode of the PU, some terms have to be defined. Although the PU is able to execute one instruction in one system cycle, one has to distinguish between one cycle and one instruction. One system cycle normally takes 83 ns (12 MHz). This frequency can vary from 11.16 MHz to 12.8 MHz. In normal cases one instruction is evaluated in one cycle, in some exceptions (no acknowledge from memory) there may be wait cycles.

The PU is a three-address machine, meaning that it reads two independent operands from the PU register set, executes an arithmetic or logic operation, and saves the result in a third independent register within one cycle. All this information is given in one instruction word (see instruction format).

Parallel to this data processing, the program counter is incremented and the next instruction is fetched from ROM. Because this takes two cycles, a one-stage pipeline technique is used. In a linear program this is not visible for the user. However, the PC always points to the instruction  $i + 2$ , if the instruction is just executed. This results in the fact that the instruction after a jump is always executed. The suppression of this execution is intentionally resigned to increase the performance of the PU.

Dependent on 90 different jump conditions, it is possible to execute direct or indirect branches, subroutine calls, subroutine returns, and returns from interrupt. The decision whether a branch is executed or ignored is dependent on the result of the last instruction.

Another possibility for branching in a program is the use of an implemented table instruction. With this instruction it is possible to execute exactly one arbitrarily pointed instruction. The pointer corresponds to the contents of any PU register. This instruction has nearly the same function as a subroutine call with automatic return. If the pointed instruction is a branch instruction, you have an easy and very fast realization of the well-known “case” instruction of higher program languages.

The READ ROM instruction has nearly the same function, but the pointed word is always interpreted as a data word and will be stored in a CFC (Constant Form Code) register.

There is a fast hardware stack with a depth of 16 words in which the return addresses of calls and interrupts are stored as well as any pushed data words. In case of overflow (underflow) this stack is automatically swapped to the internal MEGATEXT RAM. This feature is handled with a special interrupt service routine.

8-level interrupt priority logic controls the choice of the right interrupt if more than one is requested. It is possible to evaluate 40 different interrupt requests. They are attached to eight different process levels. Each of these requests and processes can be disabled independently. With this feature it is possible to program reentrant interrupt routines.

A read-only peripheral status register collects status information from the rest of the chip.

There are also 18 hardware-programmed read-only constant registers for fast access of often used constants.

Data access to RAM is realized by indirect addressing. The address can be computed in any of the PU work registers and then be written to the address port. The write or read access is then controlled by hardware. If RAM accesses do not succeed each other too quickly, the ROM program execution becomes independent of the speed of the RAM, because the ROM-program execution may continue, although the memory interface is waiting for bus access.

Programs may be executed from ROM or internal MEGATEXT RAM. They are always addressed by the program counter.

By use of reserved PU register addresses it is possible to move data from PU to additional hardware and vice versa, for example to the M3L-Bus or the hamming-check logic block. These hardware blocks work in parallel and independently of the PU program.

Object code must be generated with the ASM5273 assembler. Predefined symbols are given in file ASM5273.EQU.

## **7 I<sup>2</sup>C / M3L-Bus Interface**

There are only four possible interconnections for communication between the external controller and the MEGATEXT IC. The I<sup>2</sup>C/M3L-interface with two or three pins and the interrupt pin.

The I<sup>2</sup>C-Bus uses two connections, the pins SDA (data) and SCL (clock), and operates according to the I<sup>2</sup>C-Bus specifications, which limits the maximum transfer rate at 100 kbit/s. MEGATEXT can handle the I<sup>2</sup>C protocol at a maximum transfer rate of 1 Mbit/s.

The M3L-Bus (MEGATEXT 3-Line-Bus) uses the same two pins SDA and SCL and in addition the pin I<sup>2</sup>CEN. The transfer rate is max. 1 Mbit/s.

Microcontrollers from the Siemens range are available with suitable hardware interfaces for either the I<sup>2</sup>C-Bus or the M3L-Bus.

MEGATEXT always operates in the slave mode: either as receiver or transmitter. It has the chip select address MSB 0010001 LSB in I<sup>2</sup>C-Bus mode. The MSB is transmitted first.

In M3L-Bus mode the LSB is transmitted first and the chip select address is MSB 1000100 LSB.

### Abbreviations

START	Start conditions: I <sup>2</sup> C: See I <sup>2</sup> C-Bus technical description M3L: Falling edge of I <sup>2</sup> CEN
STOP	Stop conditions: I <sup>2</sup> C: See I <sup>2</sup> C-Bus technical description M3L: Rising edge of I <sup>2</sup> CEN
A	Acknowledge
A*	The acknowledge of the last byte in a read must be High
W	Write
R	Read
SLAVE ADR	7-bit MEGATEXT chip select address
SUB ADR	8-bit internal subaddress

### I<sup>2</sup>C-Bus Mode

The serial port is in I<sup>2</sup>C-Bus mode when the input pin I<sup>2</sup>CEN is High. The I<sup>2</sup>C-Bus interface operates with all clock frequencies between 0 Hz and 1 MHz. The MEGATEXT chip may slow down the transmission rate by holding the clock line Low after a byte transmission is terminated by an acknowledge bit. Input filters in the SDA and SCL pins suppress high-frequency interference.

The standard I<sup>2</sup>C-Bus is specified for frequencies up to 100 kHz. For higher frequencies a special specification applies.

### The following protocols are supported:

Clock frequency  $0 < f_{SCL} < 100 \text{ kHz}$ :

Writing to the SDA 5273 followed by a read:

START	SLAVE ADR	W	A	SUB ADR	A	DATA	A	DATA	A	...	START	SLAVE ADR	R	A	DATA	A	DATA	A*	...	STOP
-------	-----------	---	---	---------	---	------	---	------	---	-----	-------	-----------	---	---	------	---	------	----	-----	------

START	SLAVE ADR	W	A	SUB ADR	A	DATA	A	DATA	A	...	STOP	START	SLAVE ADR	R	A	DATA	A	DATA	A*	...	STOP
-------	-----------	---	---	---------	---	------	---	------	---	-----	------	-------	-----------	---	---	------	---	------	----	-----	------

Reading from the SDA 5273 (using a previously defined subaddress):

START	SLAVE ADR	R	A	DATA	A	DATA	A*	...	STOP
-------	-----------	---	---	------	---	------	----	-----	------

Clock frequency  $0 < f_{SCL} < 1 \text{ MHz}$ :

Writing to the SDA 5273:

START	SLAVE ADR	W	A	SUB ADR	A	DATA	A	DATA	A	...	STOP
-------	-----------	---	---	---------	---	------	---	------	---	-----	------

Reading from the SDA 5273 (using a previously defined subaddress):

START	SLAVE ADR	W	A	SUB ADR	A	START	SLAVE ADR	R	A	DATA	A	DATA	A*	...	STOP
-------	-----------	---	---	---------	---	-------	-----------	---	---	------	---	------	----	-----	------

START	SLAVE ADR	W	A	SUB ADR	A	STOP	START	SLAVE ADR	R	A	DATA	A	DATA	A*	...	STOP
-------	-----------	---	---	---------	---	------	-------	-----------	---	---	------	---	------	----	-----	------

### M3L-Mode

The serial port is in M3L-Bus mode when the input pin I<sup>2</sup>CEN is Low.

The M3L-Bus uses the three pins I<sup>2</sup>CEN, SDA and SCL.

The M3L-Bus interface operates with all clock frequencies between 0 Hz and 1 MHz. The MEGATEXT chip may occasionally slow down the transmission rate by holding the clock line Low.

The SDA 5273 only ever holds the eighth clock pulse of a byte and only if the internal processing is blocked by worst-case realtime acquisition and display functions.

Input filters in the SDA and SCL pins suppress high-frequency interference.

Data change when the SCL line is High.

A data packet is defined by a frame start and a frame end.

The frame start is a High to Low change at the I<sup>2</sup>CEN pin. The frame end is a Low to High change at the I<sup>2</sup>CEN pin. This stop condition may not occur within 2.3 μs of the last edge of the last clock pulse. The data inside a frame are transmitted in 8-bit words. The least significant bit is transmitted first.

The word transfer timing is compatible with an 8051 controller in mode 0.

### The following protocols are supported:

Clock frequency  $0 < f_{SCL} < 1 \text{ MHz}$ :

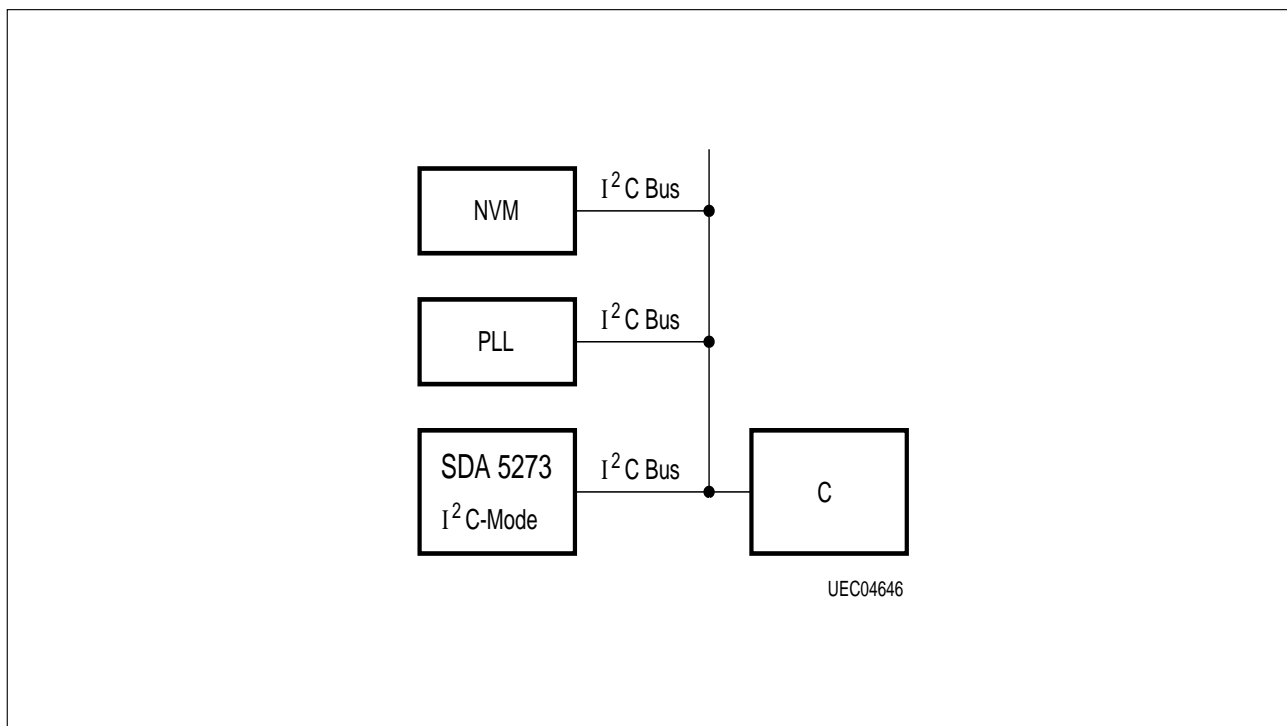
Writing to the SDA 5273:

START	SLAVE ADR	W	SUB ADR	DATA	DATA	...	STOP
-------	-----------	---	---------	------	------	-----	------

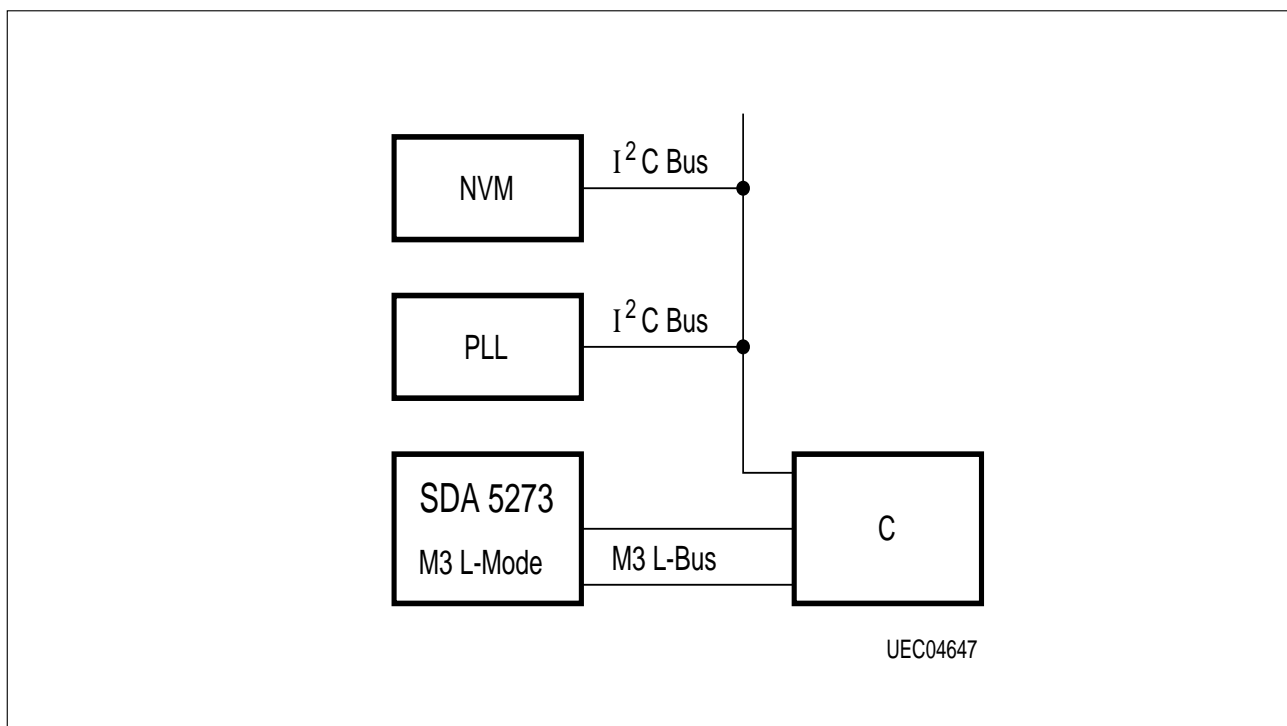
Reading from the SDA 5273 (using a transmitted subaddress):

START	SLAVE ADR	W	SUB ADR	STOP	START	SLAVE ADR	R	DATA	DATA	...	STOP
-------	-----------	---	---------	------	-------	-----------	---	------	------	-----	------

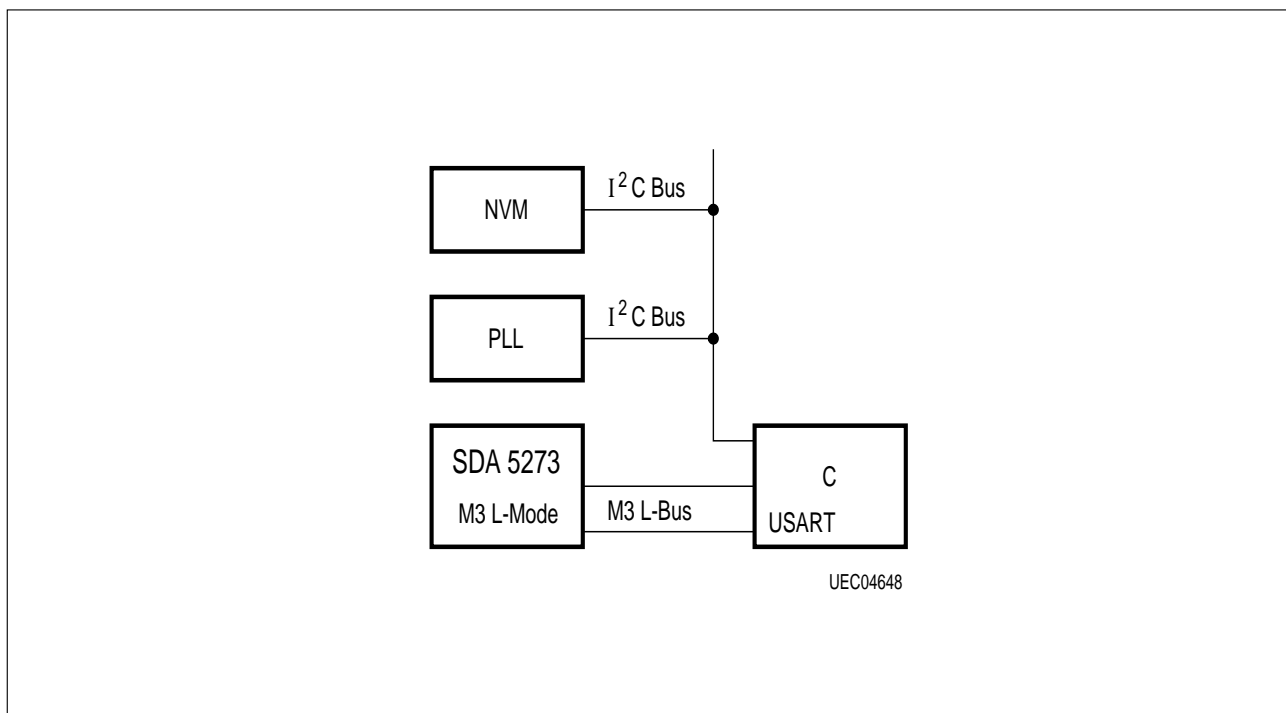
## Bus Application Examples



**Figure 2**  
**Bus Configuration for Slow Data Transfer with Hardware or Software Driven I<sup>2</sup>C-Bus**



**Figure 3**  
**Bus Configuration for Slow Data Transfer with Software Driven I<sup>2</sup>C and M3L-Bus**



**Figure 4**  
**Bus Configuration for Fast Data Transfer with Software I²C-Bus and Hardware M3L-Bus**

## 8 Internal DRAM (IRAM)

The organization of the internal memory (=IRAM) was chosen to achieve a very high data rate that is necessary to display pixel graphics parallel to acquisition and other high-priority tasks of the PU. The data unit accessible by one IRAM access cycle is 48 bits in 166 ns, resulting in a maximum data rate of 288 Mbit/s or 36 Mbyte/s.

The memory organization can be described as six DRAMs of 4 Kbytes each, organized 4 K x 8 bits. They are addressed in parallel. The data ports are connected to the 48-bit MEGATEXT data bus via multiplexer 6:n, which makes it possible to access one or more bytes of the 6 bytes instead of accessing all of them. The selection is done by six byte select bits. For more detailed information please refer to the M3L-Bus register reference, R48 ff.

10 bits of the 12 IRAM address bits are connected to the internal MEGATEXT data bus via a row/column-to-binary address converter. Character-position-related functions like page acquisition and display need the row/column address format, whereas PU programs use the binary address format. Address conversion is enabled by a row/column select bit.

The row/column address format divides

- the IRAM into 4 blocks,
- each block into 25.6 rows,
- each row into 40 columns.

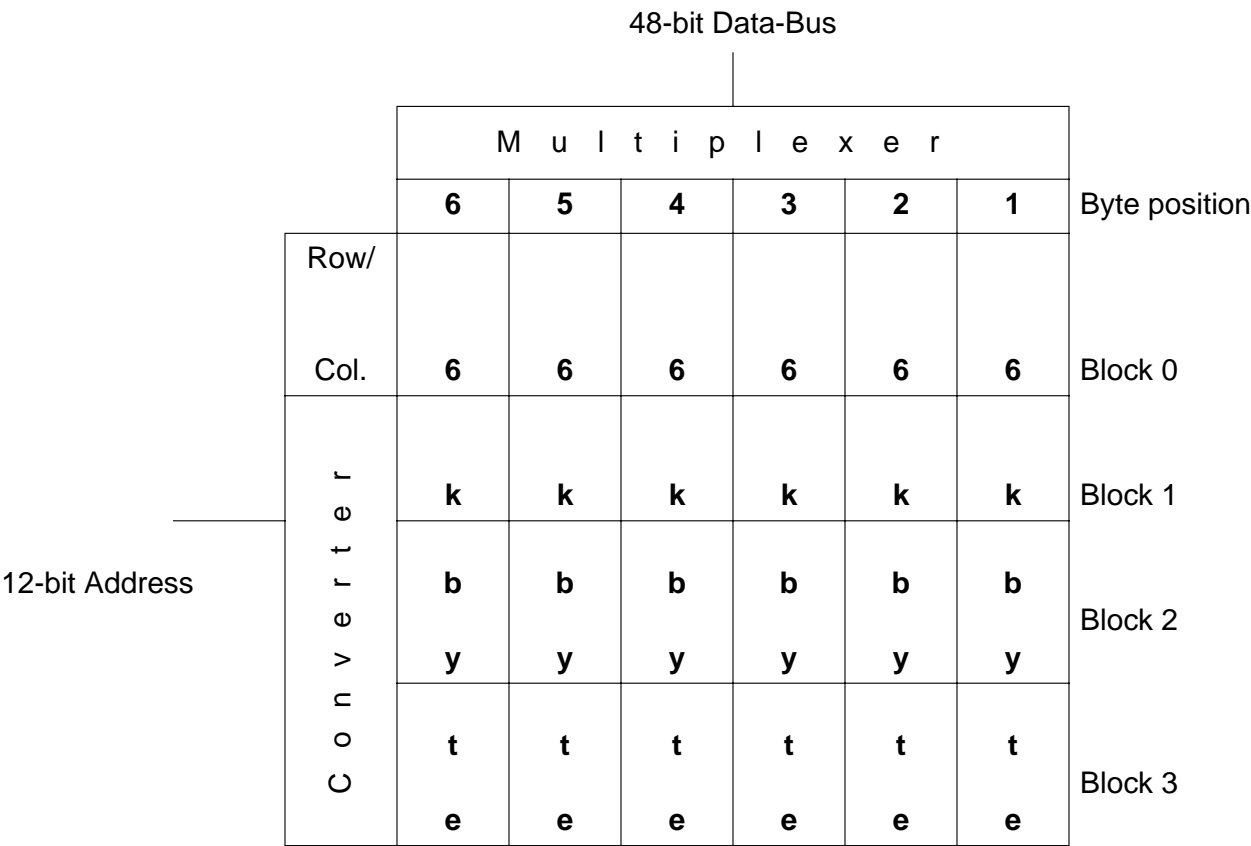
The row address consists of 5 bits. The row address range is 0 to 25 decimal.

The column address consists of 6 bits. The column address range is 0 to 39 decimal.

An address range overflow occurs for addresses greater than row 25/ column 24 and is not checked by the address converter. It has to be avoided.

To save chip area the IRAM was chosen to be a dynamic RAM. Its memory cell and the CMOS process is derived from the Siemens 1M DRAM generation. The necessary refresh is done automatically once per display line initiated by the display generator.

IRAM Organization



Different types of data need differently organized IRAM areas. Except for binary addressed RISC programs, the applications use all columns of a row. The following table give an overview of the different IRAM applications.

### Use of IRAM

Type of Data	Organization of IRAM Area
Display words for full performance	<ul style="list-style-type: none"> <li>– block 2 and/ or 3</li> <li>– rows and columns corresponding to the display positions on the screen</li> <li>– byte positions 1 to 5</li> <li>– byte position 6 is free</li> </ul>
Display words for reduced performance	<ul style="list-style-type: none"> <li>– blocks 2 and/ or 3</li> <li>– rows and columns corresponding to the display positions on the screen</li> <li>– byte positions 1 to n, n = 2, 3, 4</li> <li>– byte positions n + 1 to 5 are free</li> </ul>
PCS pixel information	<ul style="list-style-type: none"> <li>– block 0, row 8 to 23</li> <li>– byte position 1 to 6</li> </ul>
Graphics	<ul style="list-style-type: none"> <li>– blocks and rows: please refer to the display reference manual</li> <li>– byte position 1 to 6</li> </ul>
RISC programs	<ul style="list-style-type: none"> <li>– any contiguous binary IRAM address range</li> <li>– byte position 1 to 6</li> </ul>
Teletext pages in transmitted format (i.e. not converted for display)	<ul style="list-style-type: none"> <li>– any block except block 0</li> <li>– any byte position: one byte position for 1 Kbyte (basic page)</li> </ul>
Multipurpose RAM area for external controller	<ul style="list-style-type: none"> <li>– any address range except for areas in block 0 reserved for the PU</li> </ul>



### Conversion of Row/ Column Addresses into Binary Addresses

Address in Row / Column Mode	Address Bits Row Column	Address in Binary Mode (decimal)	Address Bit Binary
0/ 0 to 31	00000 000000 00000 011111	0 to 31	00000 00000 to 00000 11111
1/ 0 to 31	00001 000000 00001 011111	32 to 63	00001 00000 to 00001 11111
.			
24/ 0 to 31	11000 000000 11000 011111	768 to 799	11000 00000 to 11000 11111
25/ 0 to 23	11001 000000 11001 010111	800 to 823	11001 00000 to 11001 10111
0/ 32 to 39	00000 100000 00000 100111	1016 to 1023	11111 11000 to 11111 11111
1/ 32 to 39	00001 100000 00001 100111	1008 to 1015	11111 10000 to 11111 10111
.			
24/ 32 to 39	11000 100000 11000 100111	824 to 831	11001 11000 to 11001 11111

Row/ column to binary conversion algorithm:

a) Column address 0 to 31

B9 B8 B7 B6 B5	_ B4 B3 B2 B1 B0	binary address bits
R4 R3 R2 R1 R0	0 C4 C3 C2 C1 C0	row/ column address bits

b) Column address 32 to 39

1 1 B7 B6 B5 B4 B3	_ _ _ B2 B1 B0	binary address bits
_ _ R4 R3 R2 R1 R0	1 0 0 C2 C1 C0	row/ column address bits

## 9 Display Generator (DG)

The display generator is a very complex circuit. That is why this paper does not show a DG block diagram. Most of the functions that have to be performed by the DG can be understood better by studying the control bits of the display word. Some main functions are listed below.

### Functions of the display generator:

- Control of data transfer IRAM to DG
  - reading control data and CLUT
  - reading inner screen display words
  - reading outer screen display words
  - reading pixel information (DRCS, graphics) as requested by control information and display words
- Decoding of display words
  - reading character pixels from the character ROM
  - color control
  - flash modes
  - display masks
  - overlay control (transparent, cursor, accents, etc.)
  - size control (double height, width, etc.)
- Display format control
  - speed control (pixel rate, double scan, etc.)
  - position of frame, text areas, cursor and graphics
- Special cursor generation
- Start of IRAM refresh

The display word consists of 5 bytes and contains all display information about a character position of the display screen areas except for graphics. For displays that do not need the full MEGATEXT display performance, it is possible to set the higher bytes to default values by using mask registers. This is a convenient method to economize on internal DRAM area. For a level 1 teletext display, for example, only a 3-byte display word is necessary, so 3 Kbytes are left in the display IRAM block (block 2 or 3) for the storage of transmitted teletext pages (please refer to chapter 8, IRAM).

### Bits of Character Display Word

Byte Pos.	Bit	Name	Function	Remarks
0	0	B0	ROM character select	Each character is defined by a 12 × 10 pixel matrix
	1	B1		
	2	B2		
	3	B3		
	4	B4		
	5	B5		
	6	B6		
	7	B7		
1	8	B8		
	9	US	Underline / separate graphics	Function depends on special character
	10	UH	Upper half double height	
	11	DH	Double height	
	12	DW	Double width	Marks the left half of the character
	13	CO	Conceal / reveal	
	14	TRB	Transparent background	Video picture visible
	15	TRF	Transparent foreground	
2	16	BX	Box mode	
	17	BC0	Selection of eight background colors	Inside selected CLUT
	18	BC1		
	19	BC2		
	20	FC0	Selection of eight foreground colors	Inside selected CLUT
	21	FC1		
	22	FC2		
	23	F0	Control of flash modes	
3	24	F1		
	25	F2		
	26	F3		
	27	IC	Inverse colors	May be used as cursor
	28	BC3	CLUT select for background color	
	29	BC4		
	30	FC3	CLUT select for foreground color	
	31	FC4		

### Bits of Character Display Word (cont'd)

Byte Pos.	Bit	Name	Function	Remark
4	32	DD0	Multimode bits – Addressing of accents – Addressing of PCS memory – Selection of DRCS mode	
	33	DD1		
	34	DD2		
	35	DD3		
	36	DD4		
	37	DM0	Display mode selection	
	38	DM1		
	39	UC	User CLUT select	Selects CLUT 0 : 3 or CLUT 4 : 7

### 10 Display Sync and Timing

A digital display PLL (DPLL) generates the horizontal timing signals for the display and a line locked display clock. It works similarly to the HPLL but the input is only a digital horizontal pulse. The acquisition PLL or the pins HS or VCS (for composite sync signals) can be selected as horizontal input sources. The display PLL is restricted to lock on horizontal frequencies of 15.625 kHz  $\pm$ 10%. To lock on double scan signals a prescaler 2:1 can be activated.

MEGATEXT can be display sync master or display sync slave. For sync master modes the DPLL has to be switched to a freerun mode or to the acquisition PLL and HS/VS pins or the TCSQ pin are used as sync outputs.

#### MEGATEXT as Display Sync Slave

For standard sync input signals supported by freerun modes the flywheel can be used for vertical stabilization. For non-standard sync input signals vertical filter circuits have to be adjusted or switched off. TCSQ is only valid for standard signals supported by freerun modes. In other cases TCSQ contains no vertical component. Duplication of the vertical display frequency (sync mode SL3) is possible only for 50/60 Hz sync formats supported by MEGATEXT freerun modes (e.g. 50 Hz/15.6 kHz input, 100 Hz/31.2 kHz display).

### Sync Slave Modes

Mode	Vertical Display Frequency	Horiz. Display Frequency	Lines per Field
Sync input is H/V:			
SL1-HV	Like VS	Like HS	Like VS
Sync input is VCS:			
SL1-VCS	Like VCS	Like VCS	Like VCS
For double line displays:			
SL2-HV	Like VS	2 × HS	Like VS
For double field displays:			
SL3-HV	2 × VS	2 × HS	2 × VS

### Freerun Modes

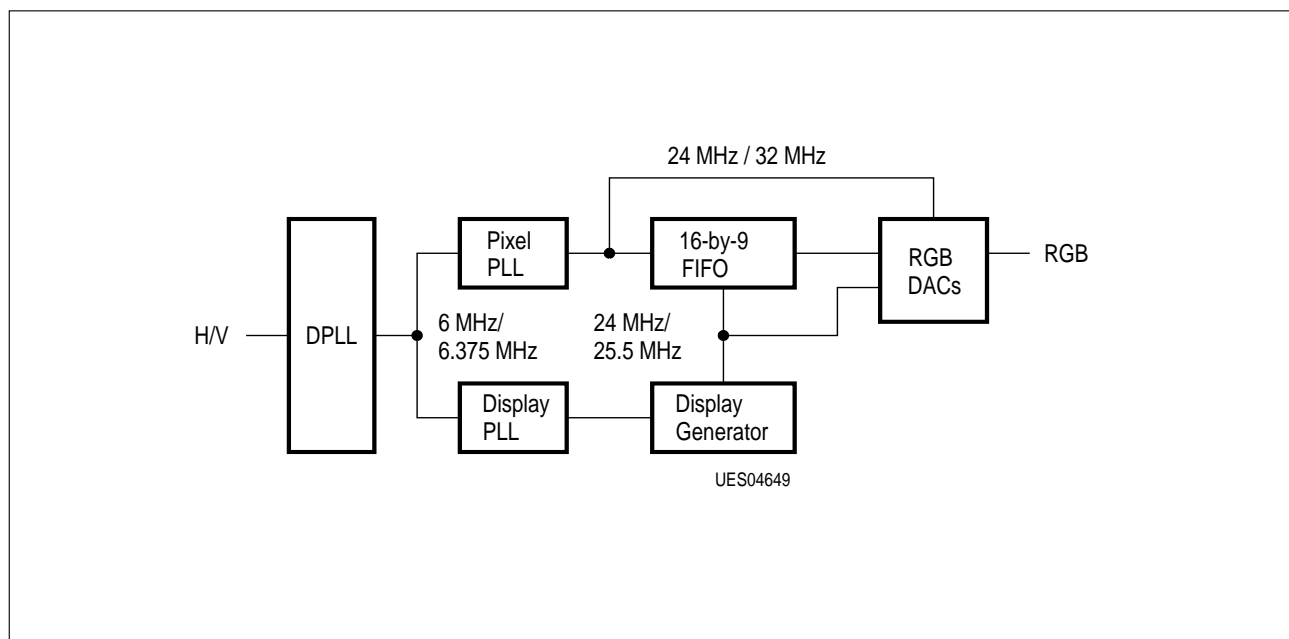
Freerun Mode	Vertical Output Frequency	Horiz. Output Frequency	Lines per Field
F1	50 Hz	15.6 kHz	313/312
F1N	60 Hz	15.6 kHz	263/262
F2	50 Hz	15.6 kHz	312/312
F2N	60 Hz	15.6 kHz	262/262
F3	50 Hz	15.6 kHz	312.5/312.5
F3N	60 Hz	15.6 kHz	262.5/262.5
F4	100 Hz	31.2 kHz	313/312
F4N	120 Hz	31.2 kHz	263/262
F5	100 Hz	31.2 kHz	312/312
F5N	120 Hz	31.2 kHz	262/262
F6	100 Hz	31.2 kHz	312.5/312.5
F6N	120 Hz	31.2 kHz	262.5/262.5
F7	50 Hz	31.2 kHz	625/625
F7N	60 Hz	31.2 kHz	525/525

### 11 16 by 9 FIFO

To display text or graphics on a 16:9 screen with undistorted geometry it is necessary to accelerate the pixel rate from normally 24 MHz to 32 MHz. In 16 by 9 mode 64 characters have to be displayed in 26  $\mu$ s assuming a horizontal period of 32  $\mu$ s. Because the internal DRAM cannot handle the necessary data rate, the display data are fetched from the DRAM during the whole horizontal period with a system clock of 25.5 MHz. The data are processed by the display generator and the resulting pixel data are stored in a FIFO. The FIFO readout is done with 32 MHz.

In 4 by 3 mode the FIFO is simply bypassed and the pixel clock frequency is the same as the display clock frequency (typ. 24 MHz).

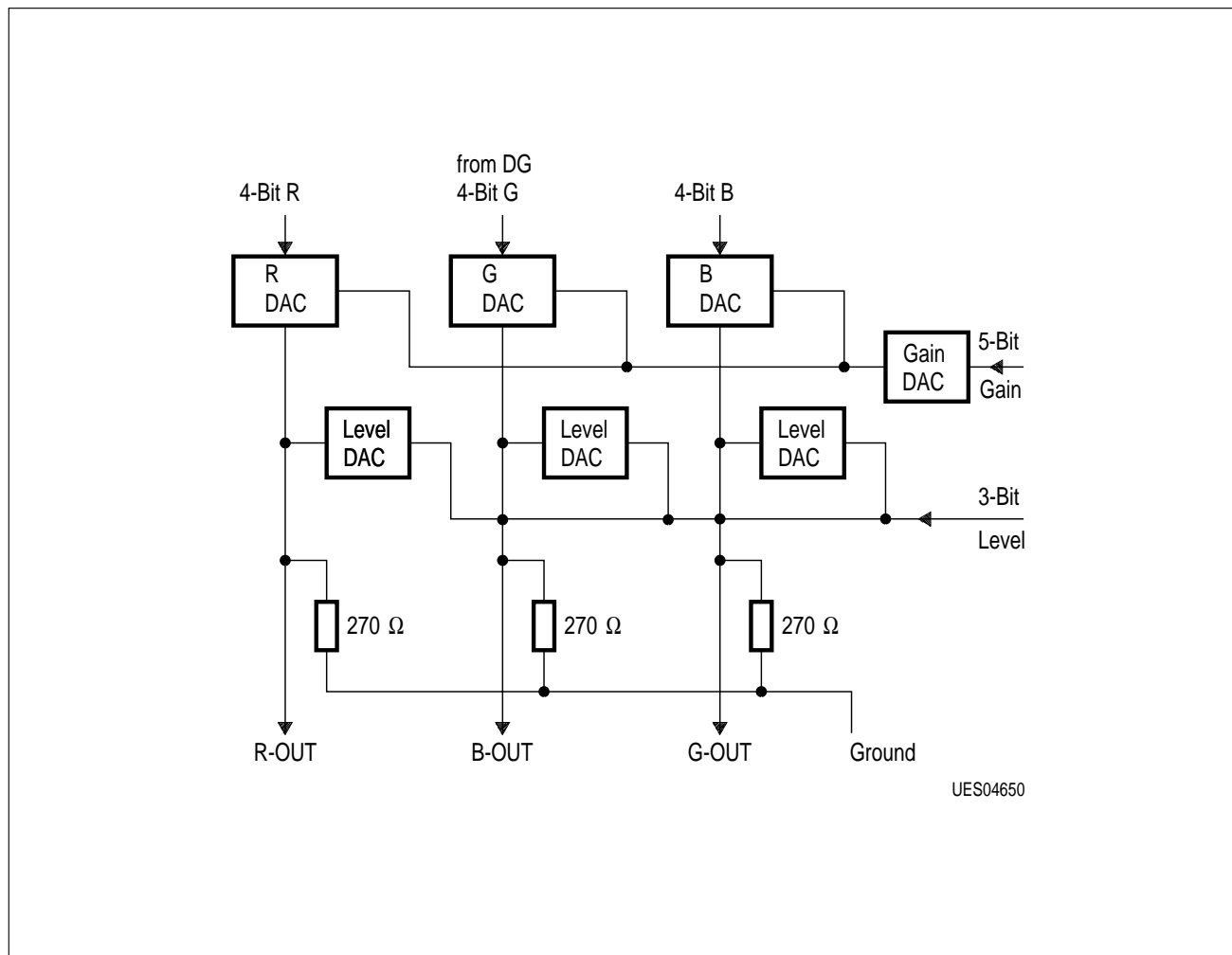
The display and pixel clocks are generated by analog PLLs. Both PLLs lock on the same 6-MHz signal, which is normally generated by the digital display PLL (DPLL). The division ratio of the pixel clock PLL can be selected as 4:1 or 5:1. The output signal of the DPLL can be selected as typ. 6 MHz or typ. 6.375 MHz.



**Figure 5**  
**MEGATEXT Display Function Blocks for 16 by 9**

## 12 RGB Outputs

The display generator produces pixel data with 4 bit resolution for each of the color signals R,G and B. Three D/A converters produce the analog RGB output signals. The DACs are digital controlled current sources with internal load resistors of typically  $270\ \Omega$ . The load resistors have a common ground pin separated from the  $V_{SS}$  and  $V_{SSA}$  pins. The output of the DACs is proportional to a reference current.



**Figure 6**  
**RGB Outputs**