

ICs for Consumer Electronics MEGATEXT

M3L-Bus Registers

MEGATEXT® M3L-Bus Registers	
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Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25\text{ °C}$ and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about “**Processing Guidelines**” and “**Quality Assurance**” for ICs, see our “**Short Form Catalog**”.

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1 Introduction

This manual is written to support the SDA 5273 programmer in using the M3L-Bus registers. M3L-Bus registers are the key to communication with SDA 5273. To access them it is necessary to send a subaddress. Successive data can be read or written.

M3L-Bus registers are classified as follows:

- PU software control registers
- MCI registers
- Address pointer and data-port registers
- Hardware control registers
- Reserved registers

PU software control registers are used as program input parameters to configure the multifunction RAM.

MCI registers are divided into parameter registers and a special command register. PU command functions will be evoked by writing a command number into the command register. Each command has several input parameters and return values. All available commands are explained in document “MCI Description”.

Address pointer and data-port registers are used to transfer data byte-wise between the MEGATEXT® controller and the internal or external RAM.

Hardware control registers give direct control to special hardware functions like slicer, acquisition, timing, synchronization and RGB output settings. These registers are marked with an “(H)” in section “Register Quick Reference”.

Reserved registers and bits must not be used by the SDA 5273 programmer. They are reserved for future applications.

2 Description of M3L-Bus Registers

In this section the M3L-Bus registers are described. Each of these registers has 8 bits. In general they are named D0 to D7. D0 is the LSB and D7 the MSB. The M3L-Bus registers can be read and/or written by an external microcontroller via the M3L-Bus interface or by the internal processing unit (PU). Reading or writing the M3L-Bus registers via the M3L-Bus interface is controlled by the PU.

Autoincrement of M3L register subaddresses:

M3L-Bus registers are functionally packed in 16 internal memory doublewords (one doubleword consists of 6 bytes numbered 5, 4, 3, 2, 1, 0). Each byte of such a doubleword is addressed via the M3L Bus with its M3L-Bus register subaddress. Subaddress range is from 0 to 127 except the values $(n \times 8) - 1$ and $(n \times 8) - 2$ ($n = 1$ to 16). A special subaddress 255 acts to generate a power-on reset. Subaddresses 128 to 254 are not allowed.

After a read or write access to a M3L-Bus register the subaddress will be incremented automatically if it does not correspond with byte 0 of an internal memory doubleword. In case of byte 0 the subaddress is set to byte 5 of the actual memory doubleword. In other words the subaddress is incremented and byte number decremented modulo 6. Exceptions for subaddress autoincrement are made for the DATA_PORT registers.

After an access to undefined subaddresses $(n \times 8) - 1$ and $(n \times 8) - 2$ ($n = 1$ to 16), autoincrement works as follows:

- after access to subaddress = $(n \times 8) - 2 \rightarrow (n \times 8) - 1$
- after access to subaddress = $(n \times 8) - 1 \rightarrow (n \times 8)$.

This subaddress corresponds to byte 5 of the memory doubleword with block/row/column/byte position = 0/00/n – 1/5.

Subaddress 255 does not address a register but is used to generate a power-on reset.

Note: The most significant bit of the subaddress is ignored by the M3L interface.

For each register the following features are explained:

- symbolic name of the M3L-Bus register
- symbolic name of the bits
- position of the bits in the register
- the register subaddress
- the register block/row/column/byte address
- the register default value after hardware power-on reset or software reset
- access operation read and/or write
- autoincrement of the subaddress
- function of the register
- interpretation of the bits

Chip-select address:

The chip-select address for SDA 5273 is:

In the I²C mode of the M3L Bus: MSB 0010001R/W LSB. The MSB is transmitted first.

In the 3L mode of the M3L Bus: MSB R/W1000100 LSB. The LSB is transmitted first.

2.1 Packet Buffer Registers: R0, R1, R2, R3, R4, R5

The packet buffer registers will be used to configure the packet buffer start address and length. It is always addressed using the binary address scheme.

R0 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D7 – D0 Not used. D7 – D0 must be 0.

Subaddress 00000000 b

Block/row/column/byte position 0/00/00/5

Power-on reset initialization 00000000 b

Data dispatched to hardware register No

Subaddress autoincrement Yes

R1 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D7 – D0 Not used. D7 – D0 must be 0.

Subaddress 00000001 b

Block/row/column/byte position 0/00/00/4

Power-on reset initialization 00000000 b

Data dispatched to hardware register No

Subaddress autoincrement Yes

R2 PB_LENGTH

PB_L_07	PB_L_06	PB_L_05	PB_L_04	PB_L_03	PB_L_02	PB_L_01	PB_L_00
---------	---------	---------	---------	---------	---------	---------	---------

Referenced registers: PB_ADR_2, PB_ADR_1, PB_ADR_0.

PB_LENGTH: Length of the packet buffer. The packet buffer with length = 1 has 43 bytes which can store one TTX or VPS packet.

PB_L_07 – PB_L_00 Range of PB_LENGTH is $1 \leq \text{PB_LENGTH} \leq 23$.

Subaddress 00000010 b

Block/row/column/byte position 0/00/00/3

Power-on reset initialization 0

Data dispatched to hardware register No

Subaddress autoincrement Yes

R3**PB_ADR_2**

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

Referenced registers: PB_ADR_1, PB_ADR_0, PB_LENGTH.

PB_ADR_2 is the most significant byte of the packet buffer **binary** start address.

BYT_5 – BYT_2

Four most significant bits of the byte position of an internal memory doubleword. For instance: to address byte 3 of a doubleword, BYT_3 has to be 1.

For EXT_MEM = 0 these bits select the corresponding byte of an internal memory doubleword.

For EXT_MEM = 1 see the description for CHP_10 – CHP_5 bits.

Warning: It is not allowed to set more than one byte address bit simultaneously!

CHP_10 – CHP_5

Seven most significant bits of the external memory chapter address.

For EXT_MEM = 1 these bits select a chapter of the external memory. 0 ≡ chapter address ≡ 2047.

For EXT_MEM = 0 see the description for BYT_5 – BYT_2 bits.

EXT_MEM

In the 1 condition of the EXT_MEM bit the address pointers are related to the external memory.

In the 0 condition of the EXT_MEM bit the address pointers are related to the internal memory.

Subaddress	00000011 b
Block/row/column/byte position	0/00/00/2
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R4

PB_ADR_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	BI_ADR_10	BI_ADR_9	BI_ADR_8
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

Referenced registers: PB_ADR_2, PB_ADR_0, PB_LENGTH.

PB_ADR_1 is the middle byte of the packet buffer **binary** start address.

CHP_4 – CHP_0

Five least significant bits of the external memory chapter address.
For EXT_MEM = 1 these bits select a chapter of the external memory.
 $0 \leq \text{chapter address} \leq 2047$.
For EXT_MEM = 0 see the description for BLK_2 – BLK_0 and BYT_1, BYT_0 bits.

BLK_2 – BLK_0

For EXT_MEM = 0 these bits select the block of the internal memory.
 $0 \leq \text{block address} \leq 7$.
For EXT_MEM = 1 see the description for CHP_4 – CHP_0 bits.

BYT_1, BYT_0

Two least significant bits of the byte position of an internal memory doubleword.
For EXT_MEM = 0 these bits select the corresponding byte of an internal memory doubleword. The internal memory doubleword is addressed by the BI_ADR_10 – BI_ADR_1 bits.
For EXT_MEM = 1 see the description for CHP_4 – CHP_0.

Warning: It is not allowed to set more than one byte address bit simultaneously!

BI_ADR_10 – BI_ADR_0 Binary address bits

With register PB_ADR_0 the binary address range is:
 $0 \leq \text{BI_ADR_10} - \text{BI_ADR_1} \leq 2^{10} - 1$.

Subaddress	00000100 b
Block/row/column/byte position	0/00/00/1
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R5

PB_ADR_0

BI_ADR_7	BI_ADR_6	BI_ADR_5	BI_ADR_4	BI_ADR_3	BI_ADR_2	BI_ADR_1	BI_ADR_0
----------	----------	----------	----------	----------	----------	----------	----------

Referenced registers: PB_ADR_2, PB_ADR_1, PB_LENGTH.

PB_ADR_0 is the least significant byte of the packet buffer start address.
For the bit description see register PB_ADR_1.

Subaddress	00000101 b
Block/row/column/byte position	0/00/00/0
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Next subaddress is R0

2.2 MCI Parameter Registers: R8 to R36

MCI parameter registers input or return values to or from the called function.

The command input parameters specify the function of a command given in the M3L register “MCI_COMMAND” and must be set before executing the command.

The command return values return the function results.

For more details of command parameters see document “MCI Description”.

2.2.1 MCIO Registers: R8 to R13

R8

MCIO_5

MCIO_5_7	MCIO_5_6	MCIO_5_5	MCIO_5_4	MCIO_5_3	MCIO_5_2	MCIO_5_1	MCIO_5_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCIO_5_7 – MCIO_5_0

See document “MCI Description”.

Subaddress	00001000 b
Block/row/column/byte position	0/00/01/5
Power-on reset initialization	month tens (ASCII) of firmware date code
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R9

MCIO_4

MCIO_4_7	MCIO_4_6	MCIO_4_5	MCIO_4_4	MCIO_4_3	MCIO_4_2	MCIO_4_1	MCIO_4_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCIO_4_7 – MCIO_4_0

See document “MCI Description”.

Subaddress	00001001 b
Block/row/column/byte position	0/00/01/4
Power-on reset initialization	month units (ASCII) of firmware date code
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R10

MCIO_3

MCIO_3_7	MCIO_3_6	MCIO_3_5	MCIO_3_4	MCIO_3_3	MCIO_3_2	MCIO_3_1	MCIO_3_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCIO_3_7 – MCIO_3_0

See document “MCI Description”.

Subaddress	00001010 b
Block/row/column/byte position	0/00/01/3
Power-on reset initialization	day tens (ASCII) of firmware date code
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R11

MCIO_2

MCIO_2_7	MCIO_2_6	MCIO_2_5	MCIO_2_4	MCIO_2_3	MCIO_2_2	MCIO_2_1	MCIO_2_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCIO_2_7 – MCIO_2_0

See document “MCI Description”.

Subaddress	00001011 b
Block/row/column/byte position	0/00/01/2
Power-on reset initialization	day units (ASCII) of firmware date code
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R12

MCIO_1

MCIO_1_7	MCIO_1_6	MCIO_1_5	MCIO_1_4	MCIO_1_3	MCIO_1_2	MCIO_1_1	MCIO_1_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCIO_1_7 – MCIO_1_0

See document “MCI Description”.

Subaddress	00001100 b
Block/row/column/byte position	0/00/01/1
Power-on reset initialization	year tens (ASCII) of firmware date code
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R13

MCIO_0

MCIO_0_7	MCIO_0_6	MCIO_0_5	MCIO_0_4	MCIO_0_3	MCIO_0_2	MCIO_0_1	MCIO_0_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCIO_0_7 – MCIO_0_0

See document “MCI Description”.

Subaddress	00001101 b
Block/row/column/byte position	0/00/01/0
Power-on reset initialization	year units (ASCII) of firmware date code
Data dispatched to hardware register	No
Subaddress autoincrement	Next subaddress is R8

2.2.2 MCI1 Registers: R16 to R21

R16

MCI1_5

MCI1_5_7	MCI1_5_6	MCI1_5_5	MCI1_5_4	MCI1_5_3	MCI1_5_2	MCI1_5_1	MCI1_5_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI1_5_7 – MCI1_5_0

See document “MCI Description”.

Subaddress	00010000 b
Block/row/column/byte position	0/00/02/5
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R17

MCI1_4

MCI1_4_7	MCI1_4_6	MCI1_4_5	MCI1_4_4	MCI1_4_3	MCI1_4_2	MCI1_4_1	MCI1_4_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI1_4_7 – MCI1_4_0

See document “MCI Description”.

Subaddress	00010001 b
Block/row/column/byte position	0/00/02/4
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R18

MCI1_3

MCI1_3_7	MCI1_3_6	MCI1_3_5	MCI1_3_4	MCI1_3_3	MCI1_3_2	MCI1_3_1	MCI1_3_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI1_3_7 – MCI1_3_0

See document “MCI Description”.

Subaddress	00010010 b
Block/row/column/byte position	0/00/02/3
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R19

MCI1_2

MCI1_2_7	MCI1_2_6	MCI1_2_5	MCI1_2_4	MCI1_2_3	MCI1_2_2	MCI1_2_1	MCI1_2_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI1_2_7 – MCI1_2_0

See document “MCI Description”.

Subaddress	00010011 b
Block/row/column/byte position	0/00/02/2
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R20

MCI1_1

MCI1_1_7	MCI1_1_6	MCI1_1_5	MCI1_1_4	MCI1_1_3	MCI1_1_2	MCI1_1_1	MCI1_1_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI1_1_7 – MCI1_1_0

See document “MCI Description”.

Subaddress	00010100 b
Block/row/column/byte position	0/00/02/1
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R21

MCI1_0

MCI1_0_7	MCI1_0_6	MCI1_0_5	MCI1_0_4	MCI1_0_3	MCI1_0_2	MCI1_0_1	MCI1_0_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI1_0_7 – MCI1_0_0

See document “MCI Description”.

Subaddress	00010101 b
Block/row/column/byte position	0/00/02/0
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Next subaddress is R16

2.2.3 MCI2 Registers: R24 to R29

R24

MCI2_5

MCI2_5_7	MCI2_5_6	MCI2_5_5	MCI2_5_4	MCI2_5_3	MCI2_5_2	MCI2_5_1	MCI2_5_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI2_5_7 – MCI2_5_0

See document “MCI Description”.

Subaddress	00011000 b
Block/row/column/byte position	0/00/03/5
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R25

MCI2_4

MCI2_4_7	MCI2_4_6	MCI2_4_5	MCI2_4_4	MCI2_4_3	MCI2_4_2	MCI2_4_1	MCI2_4_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI2_4_7 – MCI2_4_0

See document “MCI Description”.

Subaddress	00011001 b
Block/row/column/byte position	0/00/03/4
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R26

MCI2_3

MCI2_3_7	MCI2_3_6	MCI2_3_5	MCI2_3_4	MCI2_3_3	MCI2_3_2	MCI2_3_1	MCI2_3_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI2_3_7 – MCI2_3_0

See document “MCI Description”.

Subaddress	00011010 b
Block/row/column/byte position	0/00/03/3
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R27

MCI2_2

MCI2_2_7	MCI2_2_6	MCI2_2_5	MCI2_2_4	MCI2_2_3	MCI2_2_2	MCI2_2_1	MCI2_2_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI2_2_7 – MCI2_2_0

See document “MCI Description”.

Subaddress	00011011 b
Block/row/column/byte position	0/00/03/2
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R28

MCI2_1

MCI2_1_7	MCI2_1_6	MCI2_1_5	MCI2_1_4	MCI2_1_3	MCI2_1_2	MCI2_1_1	MCI2_1_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI2_1_7 – MCI2_1_0

See document “MCI Description”.

Subaddress	00011100 b
Block/row/column/byte position	0/00/03/1
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R29

MCI2_0

MCI2_0_7	MCI2_0_6	MCI2_0_5	MCI2_0_4	MCI2_0_3	MCI2_0_2	MCI2_0_1	MCI2_0_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI2_0_7 – MCI2_0_0

See document “MCI Description”.

Subaddress	00011101 b
Block/row/column/byte position	0/00/03/0
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Next subaddress is R24

2.2.4 MCI3 Registers: R32 to R36

R32

MCI3_5

MCI3_5_7	MCI3_5_6	MCI3_5_5	MCI3_5_4	MCI3_5_3	MCI3_5_2	MCI3_5_1	MCI3_5_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI3_5_7 – MCI3_5_0

See document “MCI Description”.

Subaddress	00100000 b
Block/row/column/byte position	0/00/04/5
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R33

MCI3_4

MCI3_4_7	MCI3_4_6	MCI3_4_5	MCI3_4_4	MCI3_4_3	MCI3_4_2	MCI3_4_1	MCI3_4_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI3_4_7 – MCI3_4_0

See document “MCI Description”.

Subaddress	00100001 b
Block/row/column/byte position	0/00/04/4
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R34

MCI3_3

MCI3_3_7	MCI3_3_6	MCI3_3_5	MCI3_3_4	MCI3_3_3	MCI3_3_2	MCI3_3_1	MCI3_3_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI3_3_7 – MCI3_3_0

See document “MCI Description”.

Subaddress	00100010 b
Block/row/column/byte position	0/00/04/3
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R35

MCI3_2

MCI3_2_7	MCI3_2_6	MCI3_2_5	MCI3_2_4	MCI3_2_3	MCI3_2_2	MCI3_2_1	MCI3_2_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI3_2_7 – MCI3_2_0

See document “MCI Description”.

Subaddress	00100011 b
Block/row/column/byte position	0/00/04/2
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R36**MCI3_1**

MCI3_1_7	MCI3_1_6	MCI3_1_5	MCI3_1_4	MCI3_1_3	MCI3_1_2	MCI3_1_1	MCI3_1_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI3_1_7 – MCI3_1_0

See document “MCI Description”.

Subaddress	00100100 b
Block/row/column/byte position	0/00/04/1
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

2.2.5 MCI Command Register**R37****MCI_COMMAND**

CMD_7	CMD_6	CMD_5	CMD_4	CMD_3	CMD_2	CMD_1	CMD_0	
-------	-------	-------	-------	-------	-------	-------	-------	--

Referenced bits: CMD_RUN.

CMD_7 – CMD_0

MCI commands are used to call firmware subroutines. Each subroutine is related to a function. Every time the MEGATEXT controller writes a command to M3L-register MCI_COMMAND causes a MCI_INT interrupt request. The MCI_INT interrupt service routine then will execute the function. The CMD_RUN bit should be used to handshake command transfers from MEGATEXT controller to M3L-register MCI_COMMAND. Before giving a MCI command, the CMD_RUN bit must be set by the external controller. As long as the CMD_RUN bit is in the one condition, the function is in execution. After finishing the function, the CMD_RUN bit will be cleared automatically.

Function input parameters will be taken from the command parameter registers MCI0_0 to MCI3_1. They must be set before giving a command. Function return values will be send to the command parameter registers MCI0_0 to MCI3_1.

For details of command parameters see document “MCI description”.

Remark: A MCI_INT interrupt will be generated after a direct write access to the MCI_COMMAND register. The MCI_INT interrupt will be not generated after a write access to the MCI_COMMAND register over any DATA_PORT register.

Subaddress	00100101 b
Block/row/column/byte position	0/00/04/0
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Next subaddress is R32

2.3 Free CHAP Chain Control Registers: R40, R41, R42, R43, R44, R45

R40

FFP_CHAP_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

Referenced registers: FFP_CHAP_1, FFP_CHAP_0.

This register is byte 2 of the first free pointer to the free chap chain.

The first chapter element of the free chap chain is at the address given by FFP_CHAP_2, FFP_CHAP_1 and FFP_CHAP_0. The next chapter elements are located at consecutive ascending chapter addresses.

The interpretation of the bits is the same as explained for the “ADDRESS_POINTER_0_2” register.

Subaddress	00101000 b
Block/row/column/byte position	0/00/05/5
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R41

FFP_CHAP_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	0	0	0
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

Referenced registers: FFP_CHAP_2, FFP_CHAP_0.

This register is byte 1 of the first free pointer to the free chap chain.

The interpretation of the bits is the same as explained for the “ADDRESS_POINTER_0_1” register.

Subaddress	00101001 b
Block/row/column/byte position	0/00/05/4
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R42

FFP_CHAP_0

0	0	0	0	0	0	0	NIL
---	---	---	---	---	---	---	-----

Referenced registers: FFP_CHAP_2, FFP_CHAP_1.

This register is byte 0 of the first free pointer to the free chap chain.

NIL 1: End of chain. The pointer does not point to any chain element.
0: The pointer points to the first element of the chain.

Subaddress	00101010 b
Block/row/column/byte position	0/00/05/3
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R43 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D7 – D0 Not used. D7 – D0 must be 0.

Subaddress 00101011 b
 Block/row/column/byte position 0/00/05/2
 Power-on reset initialization 00000000 b
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

R44 NF_CHAP_1

D7	D6	D5	D4	NF_C_11	NF_C_10	NF_C_9	NF_C_8
----	----	----	----	---------	---------	--------	--------

Referenced register: NF_CHAP_0.

Actual number of free elements of the free chap chain.

After power-on reset this is the maximum number of chap elements which are available for chap chain allocation.

D7 – D4 Not used. D7 – D4 must be 0.

NF_C_11 – NF_C_8 With NF_C_7 – NF_C_0 in register NF_CHAP_0 these bits define the number of free elements of the free chap chain.
 $0 < \text{NF_C_12} - \text{NF_C_0} < 2065$.

Remark: 2066 = 2048 external memory + 18 internal memory.

Subaddress 00101100 b
 Block/row/column/byte position 0/00/05/1
 Power-on reset initialization 00000000 b
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

R45 NF_CHAP_0

NF_C_7	NF_C_6	NF_C_5	NF_C_4	NF_C_3	NF_C_2	NF_C_1	NF_C_0
--------	--------	--------	--------	--------	--------	--------	--------

Referenced register: NF_CHAP_1.

Number of free elements of the free chap chain.

For the bit description see register “NF_CHAP_1”.

Subaddress 00101101 b
 Block/row/column/byte position 0/00/05/0
 Power-on reset initialization 00000000 b
 Data dispatched to hardware register No
 Subaddress autoincrement Next subaddress is R40

2.4 Address Pointer and Data-Port Registers

The address pointer registers are used to address the internal and external memory to read or write data via the M3L Bus. Two data ports can be used to transfer data. A data port is an M3L-Bus register which can be read or written by addressing it with its subaddress. In the case of a write to a data port, the data memory destination address is defined by the address pointer registers and, in the case of a read from a data port, the data memory source address is defined by the address pointer registers. For each data port three address pointer registers forming a 24 bit address word are available. Therefore it is possible to make very fast access to two different memory source or destination addresses.

All addresses in the address pointer registers are interpreted as row/column addresses. The address pointers for internal RAM however can be switched between row/column and binary addressing scheme with the BI_ADR bit. Binary addressing is useful to download program code into internal RAM.

Warning: Data transmission to registers which are labeled with “(H)” in section “Register Quick Reference” through data ports does not update the corresponding hardware registers. Only direct write access to these registers updates the corresponding hardware registers.

2.4.1 Data Port 0 Related Registers

2.4.1.1 Address Pointer: R48, R49, R50

R48

ADDRESS_POINTER_0_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

BYT_5 – BYT_2

Four most significant bits of the byte position of an internal memory doubleword. For instance: to address byte 3 of a doubleword, BYT_3 has to be 1.

For EXT_MEM = 0 these bits select the corresponding byte of an internal memory doubleword.

For EXT_MEM = 1 see the description for CHP_10 – CHP_5 bits.

Warning: It is not allowed to set more than one byte address bit simultaneously!

CHP_10 – CHP_5

Seven most significant bits of the external memory chapter address. For EXT_MEM = 1 these bits select a chapter of the external memory. $0 \leq \text{chapter address} \leq 2047$.

For EXT_MEM = 0 see the description for BYT_5 – BYT_2 bits.

EXT_MEM

In the 1 condition of the EXT_MEM bit the address pointers are related to the external memory.

In the 0 condition of the EXT_MEM bit the address pointers are related to the internal memory.

Subaddress	00110000 b
Block/row/column/byte position	0/00/06/5
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R49

ADDRESS_POINTER_0_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	ROW_4	ROW_3	ROW_2
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

ROW_4 – ROW_2

Three most significant bits of the memory row address.
 $0 \leq \text{row address} \leq 25$.

CHP_4 – CHP_0

Five least significant bits of the external memory chapter address.
 For EXT_MEM = 1 these bits select a chapter of the external memory.
 $0 \leq \text{chapter address} \leq 2047$.
 For EXT_MEM = 0 see the description for BLK_2 – BLK_0 and
 BYT_1, BYT_0 bits.

BLK_2 – BLK_0

For EXT_MEM = 0 these bits select the block of the internal memory.
 $0 \leq \text{block address} \leq 7$.
 For EXT_MEM = 1 see the description for CHP_4 – CHP_0 bits.

BYT_1, BYT_0

Two least significant bits of the byte position of an internal memory
 doubleword.

For EXT_MEM = 0 these bits select the corresponding byte of an
 internal memory doubleword. The internal memory doubleword is
 addressed by the ROW and COL bits.

For EXT_MEM = 1 see the description for CHP_4 – CHP_0.

Warning: It is not allowed to set more than one byte
 address bit simultaneously!

Subaddress	00110001 b
Block/row/column/byte position	0/00/06/4
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R50

ADDRESS_POINTER_0_0

ROW_1	ROW_0	COL_5	COL_4	COL_3	COL_2	COL_1	COL_0
-------	-------	-------	-------	-------	-------	-------	-------

COL_5 – COL_0

Memory column address

For $0 \leq \text{row address} \leq 24$ $0 \leq \text{column address} \leq 39$.
 For row address = 25 $0 \leq \text{column address} \leq 23$.

ROW_1, ROW_0

Two least significant bits of the memory row address.
 $0 \leq \text{row address} \leq 25$.

Subaddress	00110010 b
Block/row/column/byte position	0/00/06/3
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

2.4.1.2 Data Port 0: R51

R51

DATA_PORT_0

DATA_P_07	DATA_P_06	DATA_P_05	DATA_P_04	DATA_P_03	DATA_P_02	DATA_P_01	DATA_P_00	
-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	--

DATA_P_07 – DATA_P_00

These bits are the data to transfer to or from the selected memory address.

Any write or read to or from DATA_PORT_0 activates the autoincrement functions in the corresponding address pointer registers.

The autoincrement functions are working as follows:

RWINC_OFF	CLINC_OFF	Explanation			
0	0	increment	column	row	row is incremented if column overflows from 39 to 0
0	1	increment		row	column remain unchanged
1	0	increment	column		row remain unchanged
1	1	no increment			

Autoincrement Overflow Behavior

Column autoincrement:

For $0 \leq \text{row} \leq 25$, the column address is autoincremented until column address = 39. After a data port access on column = 39, the column address overflows to 0.

Warning: In row 25 only column addresses ≤ 23 are single value related to memory doubleword addresses. It is recommended not to use column addresses > 23 in row 25.

Row autoincrement:

For each chapter the row address is autoincremented up to row address = 24 if RWINC_OFF = 0. After a data port access on row = 24 and column = 39, the row address overflows to 0.

After a data port access on row = 25 and column = 23, the row address overflows to 0.

Subaddress	00110011 b
Block/row/column/byte position	0/00/06/2
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	No

R52**RESERVED**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D7 – D0 Not used. D7 – D0 must be 0.

Subaddress 00110100 b
 Block/row/column/byte position 0/00/06/1
 Power-on reset initialization 00000000 b
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

2.4.1.3 Port 0 Control: R53**R53****PORT_0_CONTROL**

D7	D6	BRC_INC_5	BRC_INC_4	BRC_INC_ON	BI_ADR	RWINC_OFF	CLINC_OFF
----	----	-----------	-----------	------------	--------	-----------	-----------

CLINC_OFF

Autoincrement control for column address pointer COL_5 – COL_0 in ADDRESS_POINTER_0_0 register.

In the 0 condition of the CLINC_OFF bit the autoincrement function for the column address pointer is switched on. If RWINC_OFF = 0 then column increment is done to column 39 before the row is incremented.

In the 1 condition of the CLINC_OFF bit the autoincrement function for the column address pointer is switched off. Autoincrement overflow behavior: see the description for register “DATA_PORT_0”.

The CLINC_OFF bit does not affect column autoincrement behavior if the BRC_INC_ON or BI_ADR bit is 1.

RWINC_OFF

Autoincrement control for row address pointer ROW_4 – ROW_0 in “ADDRESS_POINTER_0_1” and “ADDRESS_POINTER_0_0” registers.

In the 0 condition of the RWINC_OFF bit the autoincrement function for the row address pointer is switched on. If CLINC_OFF = 0 then column increment is done to column 39 before the row is incremented.

In the 1 condition of the RWINC_OFF bit the autoincrement function for the row address pointer is switched off. Autoincrement overflow behavior: see the description for register “DATA_PORT_0”.

The RWINC_OFF bit does not affect row autoincrement behavior if the BRC_INC_ON or BI_ADR bit is 1.

BI_ADR

This bit is used to select binary or row/column addressing scheme.

0: Row/column addressing scheme is selected.

The description for RWINC_OFF and CLINC_OFF bits is the same as explained above.

1: Binary addressing scheme is selected.

The function of bits RWINC_OFF and CLINC_OFF is no longer valid. The address bits ROW_4 – ROW_2 in register “ADDRESS_POINTER_0_1” and ROW_1 – COL_0 in “ADDRESS_POINTER_0_0” are interpreted as a binary address. Data transfer begins at the address which corresponds to the marked BYT bit.

After each data-port access the autoincrement works as follows:

Start with BYT_2, BYT_1, BYT_0, BYTE_5, BYTE_4, BYT_3, row/column binary increment or start with BYTE_5, BYTE_4, BYT_3, row/column binary increment, BYT_2, BYT_1, BYT_0.

Binary autoincrement can be used to load RAM programs or access consecutive bytes of a word.

Warning: No binary address overflow check is supported.

BRC_INC_ON

This bit is used to select byte position with row/column autoincrement. It only affects autoincrement behavior if the BI_ADR bit is 0.

0: Byte position with row/column autoincrement is switched off.

The description for RWINC_OFF and CLINC_OFF bits is the same as explained above.

1: Byte position with row/column autoincrement is switched on.

The RWINC_OFF and CLINC_OFF bits do not affect autoincrement behavior. Row and column autoincrement works as explained for RWINC_OFF = CLINC_OFF = 0. The address bits are given in registers “ADDRESS_POINTER_0_1” and “ADDRESS_POINTER_0_0”. Data transfer begins at the address which corresponds to the marked BYT bit. The byte position autoincrement overflow value can be chosen by the BRC_INC_4 or BRC_INC_5 bits.

After each data-port access the autoincrement works as follows:

(Please see next page)

Byte position with row/column autoincrement can be used to speed up data transmission to and from internal RAM words, doublewords or consecutive 5 byte memory units as in the display memory segments.

Warning: No chapter row/column end address overflow check is supported.

BRC_INC_5	BRC_INC_4	BYT Position before Transmission	BYT Position after Transmission	Row/Column Autoincrement
0	0	0	1	No
0	0	1	2	No
0	0	2	0	Yes
0	0	3	0	Yes
0	0	4	0	Yes
0	0	5	0	Yes
0	1	0	1	No
0	1	1	2	No
0	1	2	3	No
0	1	3	4	No
0	1	4	0	Yes
0	1	5	0	Yes
1	x	0	1	No
1	x	1	2	No
1	x	2	3	No
1	x	3	4	No
1	x	4	5	No
1	x	5	0	Yes

BRC_INC_4

This bit is used to select the byte position autoincrement overflow value, with row/column autoincrement. It only affects the byte position with row/column autoincrement mode (BRC_INC_ON = 1).

0: The byte position autoincrement overflow value is byte position 2. Autoincrement behavior is as explained in the table above.

1: The byte position autoincrement overflow value is byte position 4. Autoincrement behavior is as explained in the table above.

BRC_INC_5

This bit is used to select the byte position autoincrement overflow value, with row/column autoincrement. It only affects the byte position with row/column autoincrement mode (BRC_INC_ON = 1).

0: The byte position autoincrement overflow value is given by bit BRC_INC_4. Autoincrement behavior is as explained in the table above.

1: The byte position autoincrement overflow value is byte position 5. Autoincrement behavior is as explained in the table above.

D7, D6

Reserved. D7, D6 must be 0.

Subaddress	00110101 b
Block/row/column/byte position	0/00/06/0
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Next subaddress is R48

2.4.2 Data Port 1 Related Registers

2.4.2.1 Address Pointer: R56, R57, R58

R56

ADDRESS_POINTER_1_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

The interpretation of the following bits is the same as explained for the “ADDRESS_POINTER_0_2” register.

BYT_5 – BYT_2

CHP_10 – CHP_5

EXT_MEM

Subaddress	00111000 b
Block/row/column/byte position	0/00/07/5
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R57

ADDRESS_POINTER_1_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	ROW_4	ROW_3	ROW_2
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

The interpretation of the following bits is the same as explained for the “ADDRESS_POINTER_0_1” register.

ROW_4 – ROW_2

BLK_2 – BLK_0

BYT_1, BYT_0

CHP_4 – CHP_0

Subaddress	00111001 b
Block/row/column/byte position	0/00/07/4
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R58**ADDRESS_POINTER_1_0**

ROW_1	ROW_0	COL_5	COL_4	COL_3	COL_2	COL_1	COL_0	
-------	-------	-------	-------	-------	-------	-------	-------	--

The interpretation of the following bits is the same as explained for the “ADDRESS_POINTER_0_0” register.

COL_5 – COL_0
ROW_1, ROW_0

Subaddress	00111010 b
Block/row/column/byte position	0/00/07/3
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

2.4.2.2 Data Port 1: R59**R59****DATA_PORT_1**

DATA_P_17	DATA_P_16	DATA_P_15	DATA_P_14	DATA_P_13	DATA_P_12	DATA_P_11	DATA_P_10	
-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	--

The interpretation of the following bits is the same as explained for the “DATA_PORT_0” register.

DATA_P_17 – DATA_P_10

Subaddress	00111011 b
Block/row/column/byte position	0/00/07/2
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	No

R60**RESERVED**

D7	D6	D5	D4	D3	D2	D1	D0	
----	----	----	----	----	----	----	----	--

D7 – D0
Not used. D7 – D0 must be 0.

Subaddress	00111100 b
Block/row/column/byte position	0/00/07/1
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

2.4.2.3 Port 1 Control: R61

R61		PORT_1_CONTROL						
D7	D6	BRC_INC_5	BRC_INC_4	BRC_INC_ON	BI_ADR	RWINC_OFF	CLINC_OFF	

The interpretation of the following bits is the same as explained for the “PORT_0_CONTROL” register.

CLINC_OFF
RWINC_OFF
BI_ADR
BRC_INC_ON
BRC_INC_4

D7, D6 Reserved. D7, D6 must be 0.

Subaddress	00111101 b
Block/row/column/byte position	0/00/07/0
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Next subaddress is R56

2.5 Free p80 Chain Control Registers: R64, R65, R66, R67, R68, R69

R64

FFP_P80_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

Referenced registers: FFP_P80_1, FFP_P80_0.

This register is byte 2 of the first free pointer to the free p80 chain.

The ROW bits must be 0 if the p80 chain starts in a chapter. They must have the P80_ROW_0 row value if the p80 chain is in IRAM block 0.

The first p80 element of the free p80 chain is at the address given by FFP_P80_2, FFP_P80_1, and FFP_P80_0. The next p80 elements are located at consecutive ascending p80 addresses.

The interpretation of the bits is the same as explained for the “ADDRESS_POINTER_0_2” register.

Subaddress	01000000 b
Block/row/column/byte position	0/00/08/5
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R65

FFP_P80_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	ROW_4	ROW_3	ROW_2
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

Referenced registers: FFP_P80_2, FFP_P80_0.

This register is byte 1 of the first free pointer to the free p80 chain.

The interpretation of the bits is the same as explained for the “ADDRESS_POINTER_0_1” register.

Subaddress	01000001 b
Block/row/column/byte position	0/00/08/4
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R66 FFP_P80_0

ROW_1	ROW_0	0	0	0	0	0	NIL
-------	-------	---	---	---	---	---	-----

Referenced registers: FFP_P80_2, FFP_P80_1.

This register is byte 0 of the first free pointer to the free p80 chain.

NIL 1: End of chain. The pointer does not point to any chain element.
0: The pointer points to the first element of the chain.

ROW_1, ROW_0 The interpretation of the bits is the same as explained for the "ADDRESS_POINTER_0_0" register.

Subaddress 01000010 b
Block/row/column/byte position 0/00/08/3
Power-on reset initialization 00000000 b
Data dispatched to hardware register No
Subaddress autoincrement Yes

R67 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D7 – D0 Not used. D7 – D0 must be 0.

Subaddress 01000011 b
Block/row/column/byte position 0/00/08/2
Power-on reset initialization 00000000 b
Data dispatched to hardware register No
Subaddress autoincrement No

R68 NF_P80_1

NF_8_15	NF_8_14	NF_8_13	NF_8_12	NF_8_11	NF_8_10	NF_8_9	NF_8_8
---------	---------	---------	---------	---------	---------	--------	--------

Referenced register: NF_P80_0.

This register is byte 1 of the number of free elements of the free p80 chain.

After power-on reset this is the maximum number of p80 elements which are available for p80 chain allocation.

NF_8_15 – NF_8_0 These bits define the number of free elements of the free p80 chain. For the maximum number of p80 elements see description in document "ACQ Reference".

Subaddress 01000100 b
Block/row/column/byte position 0/00/08/1
Power-on reset initialization 00000000 b
Data dispatched to hardware register No
Subaddress autoincrement Yes

R69**NF_P80_0**

NF_8_7	NF_8_6	NF_8_5	NF_8_4	NF_8_3	NF_8_2	NF_8_1	NF_8_0	
--------	--------	--------	--------	--------	--------	--------	--------	--

Referenced register: NF_P80_0.

This register is byte 0 of the number of free elements of the free p80 chain.

Subaddress	01000101 b
Block/row/column/byte position	0/00/08/0
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Next subaddress is R64

2.6 Free p40 Chain Control Registers: R72, R73, R74, R75, R76, R77

R72**FFP_P40_2**

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

Referenced registers: FFP_P40_1, FFP_P40_0.

This register is byte 2 of the first free pointer to the free p40 chain.

The ROW bits always must be 0 if set by the user. That means a p40 chain always starts at row 0. The first p40 element of the free p40 chain is at the address given by FFP_P40_2, FFP_P40_1, and FFP_P40_0. The next p40 elements are located at consecutive ascending p40 addresses.

The interpretation of the bits is the same as explained for the "ADDRESS_POINTER_0_2" register.

Subaddress	01001000 b
Block/row/column/byte position	0/00/09/5
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R73

FFP_P40_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	ROW_4	ROW_3	ROW_2
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

Referenced registers: FFP_P40_2, FFP_P40_0.

This register is byte 1 of the first free pointer to the free p40 chain.

The interpretation of the bits is the same as explained for the “ADDRESS_POINTER_0_1” register.

Subaddress	01001001 b
Block/row/column/byte position	0/00/09/4
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R74

FFP_P40_0

ROW_1	ROW_0	0	0	0	0	0	NIL
-------	-------	---	---	---	---	---	-----

Referenced registers: FFP_P40_2, FFP_P40_1.

This register is byte 0 of the first free pointer to the free p40 chain.

NIL 1: End of chain. The pointer does not point to any chain element.
0: The pointer points to the first element of the chain.

ROW_1, ROW_0 The interpretation of the bits is the same as explained for the “ADDRESS_POINTER_0_0” register.

Subaddress	01001010 b
Block/row/column/byte position	0/00/09/3
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R75

RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D7 – D0 Not used. D7 – D0 must be 0.

Subaddress	01001011 b
Block/row/column/byte position	0/00/09/2
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	No

R76

NF_P40_1

NF_4_15	NF_4_14	NF_4_13	NF_4_12	NF_4_11	NF_4_10	NF_4_9	NF_4_8	
---------	---------	---------	---------	---------	---------	--------	--------	--

Referenced register: NF_P40_0.

Number of free elements of the free p40 chain.

After power-on reset this is the maximum number of p40 elements which are available for p40 chain allocation.

NF_4_15 – NF_4_8 With NF_4_7 – NF_4_0 in register NF_P40_0 these bits define the number of free elements of the free p40 chain.
 $0 < \text{NF_C_15} - \text{NF_C_0} < 51650$.
Remark: $51650 = 25 \times 2048$ external memory + 25×18 internal memory.

Subaddress	01001100 b
Block/row/column/byte position	0/00/09/1
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R77

NF_P40_0

NF_4_7	NF_4_6	NF_4_5	NF_4_4	NF_4_3	NF_4_2	NF_4_1	NF_4_0	
--------	--------	--------	--------	--------	--------	--------	--------	--

Referenced register: NF_P40_1.

Number of free elements of the free p40 chain.

For the bit description see register “NF_P40_1”.

Subaddress	01001101 b
Block/row/column/byte position	0/00/09/0
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Next subaddress is R72

2.7 Hardware Control Registers

2.7.1 Input/Output Control Registers: R80, R81, R82, R83, R84, R85

R80

RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D7 – D0 Not used. D7 – D0 must be 0.

Subaddress 01010000 b
 Block/row/column/byte position 0/00/10/5
 Power-on reset initialization 00000000 b
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

R81

SLICER_CONTROL

D7	D6	SLC_WD	PFC_1	PFC_0	FQC_1	FQC_0	MCC
----	----	--------	-------	-------	-------	-------	-----

MCC

Mode of clock run-in level calculation

Slicing level control. Switches between two generation techniques for the slicing level. Set to 0 for normal slicer operation.

Slicing level calculation mode:

MCC = 0: the slicing level is calculated from the clock run-in of each teletext line.

MCC = 1: the slicing level is calculated from the clock run-in of eight subsequent teletext lines.

FQC_1 – FQC_0

Frequency compensation of the CVBS channel

These bits can be used to compensate distortions of the CVBS signal.

The following characteristics can be adjusted:

FQC_1	FQC_0	
0	0	Automatic frequency compensation
0	1	Lowpass characteristic
1	0	Highpass characteristic
1	1	No frequency compensation

Set FQC_1, FQC_0 to 0,0 for normal slicer operation.

PFC_1 – PFC_0**PLL filter coefficient after clock run-in**

Selects the post adjustment after “clock run-in” teletext clock regeneration. The following characteristics can be adjusted:

PCF_1	PCF_0	
0	0	Middle
0	1	Weak
1	0	Strong
1	1	None

D7, D6

Not used. D7, D6 must be 0.

SLC_WD**Slicer watchdog control**

1: The slicer restarts the slicing level search if 16 frames without framing code are detected.

0: Framing code detection does not affect the slicing level search.
Set to 1 for normal slicer operation.

Subaddress	01010001 b
Block/row/column/byte position	0/00/10/4
Power-on reset initialization	00000000 b
Data dispatched to hardware register	Yes
Subaddress autoincrement	Yes

R82**OUTPUT_PIN_CONTROL**

CLK_OUT	GPOC_1	GPOC_0	TCS_FLD_2	TCS_FLD_1	TCS_FLD_0	HS_OUT	VS_OUT	
---------	--------	--------	-----------	-----------	-----------	--------	--------	--

VS_OUT**VS pin output enable**

0: Input for vertical sync or composite sync pulse.

1: Output for display vertical sync pulse.

HS_OUT**HS pin output enable**

0: Input for horizontal sync pulse.

1: Output for display horizontal sync pulse.

TCS_FLD_2 – TCS_FLD_0 Text composite sync field selection

The following table shows the signal selection with
TCS_FLD_2 – TCS_FLD_0 bits at TCSQ pin.

TCS_FLD_2	TCS_FLD_1	TCS_FLD_0	Signal at TCSQ
0	0	0	High-impedance output
0	0	1	Display coupled TCS at output
0	1	0	Display even field signal at output (display frame indicator)
0	1	1	Acquisition even field signal at output (ACQ frame indicator)
1	0	0	CVBS signal at CVBS is taken to TCSQ pin
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

GPOC_1, GPOC_0**General-purpose output control**

GPO pin is general-purpose and burst gate pulse output.

GPOC_1	GPOC_0	Signal at GPO Pin
0	0	High-impedance output
0	1	High
1	0	Low
1	1	Burst gate pulse

CLK_OUT**CLK pin output**

Switches CLK pin as input or output.

0: CLK pin is an input for external 24-MHz clock.

1: CLK pin outputs internal 24-MHz clock.

Subaddress	01010010 b
Block/row/column/byte position	0/00/10/3
Power-on reset initialization	00000000 b
Data dispatched to hardware register	Yes
Subaddress autoincrement	Yes

R83

RGB_CONTROL

RGB_GAIN_4	RGB_GAIN_3	RGB_GAIN_2	RGB_GAIN_1	RGB_GAIN_0	RGB_LVL_2	RGB_LVL_1	RGB_LVL_0	
------------	------------	------------	------------	------------	-----------	-----------	-----------	--

RGB_LVL_2 – RGB_LVL_0

RGB level adjustment

Superposes DC level to RGB signals except for black level clamp period (see register BLACK_LEVEL_CLAMP).

$0 \leq \text{RGB_LVL_2} - \text{RGB_LVL_0} \leq 7$.

RGB_GAIN_4 – RGB_GAIN_0

RGB gain adjustment

Controls amplitude of RGB signals.

$0 \leq \text{RGB_GAIN_4} - \text{RGB_GAIN_0} \leq 31$.

Remark: In MEGATEXT silicon versions B and the bondout version a42, bit RGB_GAIN_4 does not work. Bit RGB_LVL_0 acts as most significant bit for RGB gain adjustment as well as least significant bit for RGB level adjustment. So if maximum RGB gain is required, RGB_LVL_0 must be 1. From MEGATEXT silicon versions C on, the meaning of these bits is as described above.

Subaddress 01010011 b

Block/row/column/byte position 0/00/10/2

Power-on reset initialization 00000000 b

Data dispatched to hardware register Yes

Subaddress autoincrement Yes

R84

RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D7 – D0

Not used. D7 – D0 must be 0.

Subaddress 01010100 b

Block/row/column/byte position 0/00/10/1

Power-on reset initialization 00000000 b

Data dispatched to hardware register No

Subaddress autoincrement Yes

DISPLAY_VCO

D7	D6	D5	D4	D_VCO_3	D_VCO_2	D_VCO_1	D0
----	----	----	----	---------	---------	---------	----

D0 Reserved. D0 must be 0.

D_VCO_3 – D_VCO_1	Display VCO frequency-range adjustment For the use of this register refer to the MEGATEXT Application Notes.
-------------------	--

As a recommendation set D_VCO to:

D_VCO_3 – D_VCO_1	Explanation
100	For 24-MHz display clock
110	For 25.5-MHz display clock (16:9-display mode)

D7 – D4 Reserved. D7 – D4 must be 0.

Subaddress	01010101 b
Block/row/column/byte position	0/00/10/0
Power-on reset initialization	IRAM: 00000000 b Hardware: 00000100 b
Data dispatched to hardware register	Yes
Subaddress autoincrement	Next subaddress is R80

2.8 Memory Allocation Registers: R88, R89, R90, R91, R92, R93

Each bit of the memory allocation registers allocates 1 Kbyte of internal or external RAM memory. Such allocated memory cannot be used by any free chain. A default allocation setting is done during software initialization after power-on reset.

The external controller however can reconfigure these register settings for its own requirements. After reconfiguration a complete new allocation of free memory chains must be initiated by the external controller.

R88

IAT_2

ABLK_3_5	ABLK_3_4	ABLK_3_3	ABLK_3_2	ABLK_3_1	ABLK_3_0	ABLK_2_5	ABLK_2_4	
----------	----------	----------	----------	----------	----------	----------	----------	--

Referenced registers: IAT_1, IAT_0.

Internal memory allocation table.

ABLK_3_5 – ABLK_2_4 Each bit ABLK_X_Y corresponds to a 1 Kbyte internal memory byte segment of block X.
 1: Memory segment is allocated.
 0: Memory segment is not allocated.

Subaddress 01011000 b
 Block/row/column/byte position 0/00/11/5
 Power-on reset initialization See following table
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

The bit setting of the IAT registers after power-on reset is shown in the following table:

IAT_2	0, 3/5	0, 3/4	0, 3/3	0, 3/2	0, 3/1	0, 3/0	0, 2/5	0, 2/4
IAT_1	0, 2/3	0, 2/2	0, 2/1	0, 2/0	0, 1/5	0, 1/4	0, 1/3	0, 1/2
IAT_0	0, 1/1	0, 1/0	0, 0/5	0, 0/4	0, 0/3	0, 0/2	0, 0/1	0, 0/0

Meaning of bit description: bit setting, assignment of bit to IRAM address notified as block/byte position, use.

R89

IAT_1

ABLK_2_3	ABLK_2_2	ABLK_2_1	ABLK_2_0	ABLK_1_5	ABLK_1_4	ABLK_1_3	ABLK_1_2	
----------	----------	----------	----------	----------	----------	----------	----------	--

Referenced registers: IAT_2, IAT_0.

Internal memory allocation table.

ABLK_2_3 – ABLK_1_2 Each bit ABLK_X_Y corresponds to a 1 Kbyte internal memory byte segment of block X.
 1: Memory segment is allocated.
 0: Memory segment is not allocated.

Subaddress 01011001 b
 Block/row/column/byte position 0/00/11/4
 Power-on reset initialization See register “IAT_2”
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

R90

IAT_0

ABLK_1_1	ABLK_1_0	ABLK_0_5	ABLK_0_4	ABLK_0_3	ABLK_0_2	ABLK_0_1	ABLK_0_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

Referenced registers: IAT_2, IAT_1.

Internal memory allocation table.

ABLK_1_1 – ABLK_0_0 Each bit ABLK_X_Y corresponds to a 1 Kbyte internal memory byte segment of block X.
 1: Memory segment is allocated.
 0: Memory segment is not allocated.

Subaddress 01011010 b
 Block/row/column/byte position 0/00/11/3
 Power-on reset initialization See register “IAT_2”
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

R91

XAT_2

ACHP_23	ACHP_22	ACHP_21	ACHP_20	ACHP_19	ACHP_18	ACHP_17	ACHP_16	
---------	---------	---------	---------	---------	---------	---------	---------	--

Referenced registers: XAT_1, XAT_0.

External memory allocation table.

ACHP_23 – ACHP_16 Each bit ACHP_X corresponds to a 1 Kbyte external memory byte segment (chapter) with chapter address X.
 1: Memory segment is allocated.
 0: Memory segment is not allocated.

Subaddress	01011011 b
Block/row/column/byte position	0/00/11/2
Power-on reset initialization	See following table
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

The bit setting of the XAT registers after power-on reset is shown in the following table:

XAT_2	0, 23	0, 22	0, 21	0, 20	0, 19	0, 18	0, 17	0, 16
XAT_1	0, 15	0, 14	0, 13	0, 12	0, 11	0, 10	0, 9	0, 8
XAT_0	0, 7	0, 6	0, 5	0, 4	0, 3	0, 2	0, 1	0, 0

Meaning of bit description: bit setting, assignment of bit to XRAM address notified as chapter, use.

R92

XAT_1

ACHP_15	ACHP_14	ACHP_13	ACHP_12	ACHP_11	ACHP_10	ACHP_9	ACHP_8	
---------	---------	---------	---------	---------	---------	--------	--------	--

Referenced registers: XAT_2, XAT_0.

External memory allocation table.

ACHP_15 – ACHP_8 Each bit ACHP_X corresponds to a 1 Kbyte external memory byte segment (chapter) with chapter address X.
 1: Memory segment is allocated.
 0: Memory segment is not allocated.

Subaddress	01011100 b
Block/row/column/byte position	0/00/11/1
Power-on reset initialization	See register “XAT_2”
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R93

XAT_0

ACHP_7	ACHP_6	ACHP_5	ACHP_4	ACHP_3	ACHP_2	ACHP_1	ACHP_0	
--------	--------	--------	--------	--------	--------	--------	--------	--

Referenced registers: XAT_2, XAT_1.

External memory allocation table.

ACHP_7 – ACHP_0 Each bit ACHP_X corresponds to a 1 Kbyte external memory byte segment (chapter) with chapter address X.
 1: Memory segment is allocated.
 0: Memory segment is not allocated.

Subaddress	01011101 b
Block/row/column/byte position	0/00/11/0
Power-on reset initialization	See register “XAT_2”
Data dispatched to hardware register	No
Subaddress autoincrement	Next subaddress is R88

2.9 Hardware Control Registers

2.9.1 Data Line Selection Registers: R96, R97, R98, R99, R100, R101

R96 DEW_START_LINE

D7	D6	D5	DEW_STR_LN_4	DEW_STR_LN_3	DEW_STR_LN_2	DEW_STR_LN_1	DEW_STR_LN_0
----	----	----	--------------	--------------	--------------	--------------	--------------

Referenced bits: DEW_END_LN_4 – DEW_END_LN_0.

DEW_STR_LN_4 – DEW_STR_LN_0 **Data entry window start line**
 $0 \leq \text{DEW_STR_LN_4} - \text{DEW_STR_LN_0} \leq 31$.
The acquisition data entry window starts at the beginning of the line named in this register. Line counting is related to fields.
For $\text{DEW_STR_LN_4} - \text{DEW_STR_LN_0} = 0$ the data entry window is always closed.
 $\text{DEW_STR_LN_4} - \text{DEW_STR_LN_0} = \text{DEW_END_LN_4} - \text{DEW_END_LN_0}$ is not allowed.

D7 – D5 Not used. D7 – D5 must be 0.

Subaddress 01100000 b
Block/row/column/byte position 0/00/12/5
Power-on reset initialization 00000000 b
Data dispatched to hardware register Yes
Subaddress autoincrement Yes

R97 DEW_END_LINE

D7	D6	D5	DEW_END_LN_4	DEW_END_LN_3	DEW_END_LN_2	DEW_END_LN_1	DEW_END_LN_0
----	----	----	--------------	--------------	--------------	--------------	--------------

Referenced bits: DEW_STR_LN_4 – DEW_STR_LN_0.

DEW_END_LN_4 – DEW_END_LN_0 **Data entry window end line**
 $0 \leq \text{DEW_END_LN_4} - \text{DEW_END_LN_0} \leq 31$.
The acquisition data entry window ends at the beginning of the line named in this register. Line counting is related to fields.
For $\text{DEW_END_LN_4} - \text{DEW_END_LN_0} = 0$ the data entry window is always open.
 $\text{DEW_STR_LN_4} - \text{DEW_STR_LN_0} = \text{DEW_END_LN_4} - \text{DEW_END_LN_0}$ is not allowed.

D7 – D5 Not used. D7 – D5 must be 0.

Subaddress 01100001 b
Block/row/column/byte position 0/00/12/4
Power-on reset initialization 00000000 b
Data dispatched to hardware register Yes
Subaddress autoincrement Yes

R98

SINGLE_DATA_LINE

D7	D6	D5	SNG_LN_4	SNG_LN_3	SNG_LN_2	SNG_LN_1	SNG_LN_0
----	----	----	----------	----------	----------	----------	----------

SNG_LN_4 – SNG_LN_0

Single data line selection for the videorecorder program service VPS data line

$1 \leq \text{SNG_LN_4} - \text{SNG_LN_0} \leq 31$.

For $\text{SNG_LN_4} - \text{SNG_LN_0} = 0$ no line of a field is checked for valid VPS data.

D7 – D5

Reserved. D7 – D5 must be 0.

Subaddress 01100010 b

Block/row/column/byte position 0/00/12/3

Power-on reset initialization 00000000 b

Data dispatched to hardware register Yes

Subaddress autoincrement Yes

R99

TTX_FRAMING_WINDOW

TFW_END_3	TFW_END_2	TFW_END_1	TFW_END_0	TFW_STR_3	TFW_STR_2	TFW_STR_1	TFW_STR_0
-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------

Referenced bits: DEW, SNG_LN.

TFW_STR_3 – TFW_STR_0

These bits define the teletext framing window start position for the lines defined in R96, 97.

Each step has a resolution of $0.67 \mu\text{s}$.

$0 \leq \text{TFW_STR_3} - \text{TFW_STR_0} \leq 15$.

TFW_END_3 – TFW_END_0

These bits define the teletext framing window end position for the lines defined in R96, 97.

Each step has a resolution of $0.67 \mu\text{s}$.

$0 \leq \text{TFW_END_3} - \text{TFW_END_0} \leq 15$.

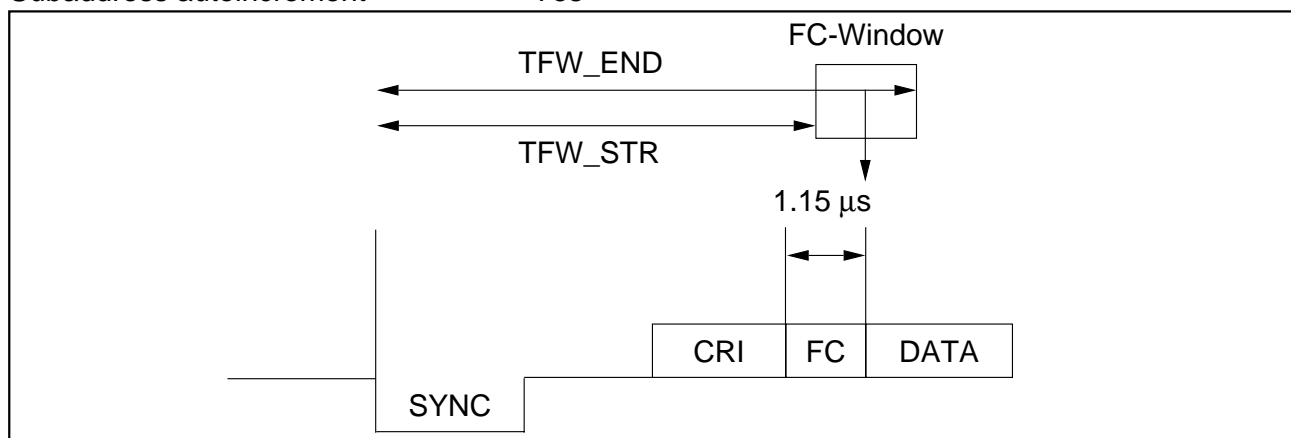
Subaddress 01100011 b

Block/row/column/byte position 0/00/12/2

Power-on reset initialization 00000000 b

Data dispatched to hardware register Yes

Subaddress autoincrement Yes



For TTX_FRAMING_WINDOW selection, SNGLN must be inactive and DEW must be active. Otherwise the EXTRA_FRAMING_WINDOW may be selected.

TFW_STR	Window Start Position Relative to H Sync of CVBS Signal
0	10.75 μ s
1	11.42 μ s
2	12.09 μ s
3	12.76 μ s
4	13.43 μ s
5	14.10 μ s
6	14.77 μ s
7	15.44 μ s
8	16.11 μ s
9	16.78 μ s
10	17.45 μ s
11	18.12 μ s
12	18.79 μ s
13	19.46 μ s
14	20.13 μ s
15	–

TFW_END	Window End Position Relative to H Sync of CVBS Signal
0	–
1	10.95 μ s
2	11.62 μ s
3	12.29 μ s
4	12.96 μ s
5	13.63 μ s
6	14.30 μ s
7	14.97 μ s
8	15.64 μ s
9	16.31 μ s
10	16.98 μ s
11	17.65 μ s
12	18.32 μ s
13	18.99 μ s
14	19.66 μ s
15	66.83 μ s

R100

EXTRA_FRAMING_WINDOW

XFW_END_3	XFW_END_2	XFW_END_1	XFW_END_0	XFW_STR_3	XFW_STR_2	XFW_STR_1	XFW_STR_0	
-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	--

Referenced bits: ACQ_NTSC, SNG_LN.

The extra framing window is the framing window for VPS (ACQ_NTSC = 0) or for TV caption lines (ACQ_NTSC = 1).

XFW_STR_3 – XFW_STR_0 These bits define the extra framing window start position. Each step has a resolution of 0.6666 μ s.
 $0 \leq \text{XFW_STR_3} - \text{XFW_STR_0} \leq 15$.

XFW_END_3 – XFW_END_0 These bits define the extra framing window end position. Each step has a resolution of 0.6666 μ s.
 $0 \leq \text{XFW_END_3} - \text{XFW_END_0} \leq 15$.

For EXTRA_FRAMING_WINDOW selection, SNG_LN must be active. Otherwise the TTX_FRAMING_WINDOW may be selected.

XFW_STR	Window Start Position Relative to H Sync of CVBS Signal
0	10.75 μ s
1	11.42 μ s
2	12.09 μ s
3	12.76 μ s
4	13.43 μ s
5	14.10 μ s
6	14.77 μ s
7	15.44 μ s
8	16.11 μ s
9	16.78 μ s
10	17.45 μ s
11	18.12 μ s
12	18.79 μ s
13	19.46 μ s
14	20.13 μ s
15	–

XFW_END	Window End Position Relative to H Sync of CVBS Signal
0	–
1	10.95 μs
2	11.62 μs
3	12.29 μs
4	12.96 μs
5	13.63 μs
6	14.30 μs
7	14.97 μs
8	15.64 μs
9	16.31 μs
10	16.98 μs
11	17.65 μs
12	18.32 μs
13	18.99 μs
14	19.66 μs
15	66.83 μs

Subaddress01100100 b

Block/row/column/byte position0/00/12/1

Power-on reset initialization00000000 b

Data dispatched to hardware registerYes

Subaddress autoincrementYes

R101RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D7 – D0

Not used. D7 – D0 must be 0.

Subaddress01100101 b

Block/row/column/byte position0/00/12/0

Power-on reset initialization00000000 b

Data dispatched to hardware registerNo

Subaddress autoincrementNext subaddress is R96

2.9.2 Acquisition Control Registers: R104, R105, R106, R107, R108, R109

R104**RESERVED**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D7 – D0 Not used. D7 – D0 must be 0.

Subaddress 01101000 b
 Block/row/column/byte position 0/00/13/5
 Power-on reset initialization 00000000 b
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

R105**RECEPTION_THRESHOLD**

HCB_CHECK	ACQR_HEAD	ACQR_MGRW	FC_ERR_1	MAG_ERR_2	MAG_ERR_1	ROW_ERR_2	ROW_ERR_1
-----------	-----------	-----------	----------	-----------	-----------	-----------	-----------

The acquisition discards packets with bit errors relating to the reception_threshold register bits.

FC_ERR_1**Framing code one error**

1: Framing code 1 bit error check enabled
 0: Framing code 1 bit error check disabled

MAG_ERR_2**Magazine number two errors**

1: Magazine number 2 bit error check enabled
 0: Magazine number 2 bit error check disabled

MAG_ERR_1**Magazine number one error**

1: Magazine number 1 bit error check enabled
 0: Magazine number 1 bit error check disabled

ROW_ERR_2**Row number two errors**

1: Row number 2 bit error check enabled
 0: Row number 2 bit error check disabled

ROW_ERR_1**Row number one error**

1: Row number 1 bit error check enabled
 0: Row number 1 bit error check disabled

HCB_CHECK**Header control byte check**

1: Hamming check of the last two hamming coded header bytes is switched off.
 0: Hamming check of the last two hamming coded header bytes is switched on.

ACQR_HEAD**Header related acquisition reset**

1: If, in the hamming coded header bytes, at least one non-correctible hamming error is detected, the actual packet will be discarded and the ACQ will be reset.

The ACQ reset is like:

- Reset of the Active_Header_ID's.
- The bits PBR and FIRST of the TTX data destination chapter will be set to 0.

0: If, in the hamming coded header bytes, at least one non-correctible hamming error is detected, the actual packet will be discarded without resetting the ACQ.

ACQR_MGRW**Magazine and row related acquisition reset**

1: If, in the hamming coded magazine number or row number bytes, one non-correctible hamming error is detected, the actual packet will be discarded and the ACQ will be reset.

The ACQ reset is like:

- Reset of the Active_Header_ID's.
- The bits PBR and FIRST of the TTX data destination chapter will be set to 0.

0: If, in the hamming coded magazine number or row number bytes, one non-correctible hamming error is detected, the actual packet will be discarded without resetting the ACQ.

Subaddress	01101001 b
Block/row/column/byte position	0/00/13/4
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R106**PSEUDO_PACKET_ENABLE**

0	0	0	0	EN_X_28	EN_X_27	EN_X_26	EN_X_25
---	---	---	---	---------	---------	---------	---------

The acquisition stores only pseudopackets which are selected by the PSEUDO_PACKET_ENABLE bits.

EN_X_28 – EN_X_25

Each bit is associated with the pseudopacket number given in its symbol.

1: Acquisition of associated packet is enabled.

0: Acquisition of associated packet is disabled.

Subaddress	01101010 b
Block/row/column/byte position	0/00/13/3
Power-on reset initialization	00000000 b
Data dispatched to hardware register	No
Subaddress autoincrement	Yes

R107**RESERVED**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D7 – D0

Not used. D7 – D0 must be 0.

Subaddress 01101011 b

Block/row/column/byte position 0/00/13/2

Power-on reset initialization 00000000 b

Data dispatched to hardware register No

Subaddress autoincrement Yes

R108**ACQUISITION_TIMING_1**

D7	D6	EXT_AD	CLMP_DIS	D3	D2	ASF_SRC	VSA_SRC
----	----	--------	----------	----	----	---------	---------

VSA_SRC**Source selection for vertical sync analysis**

The V pulse is analyzed with respect to lines per frame (S525) and signal quality (V_FINE).

0: Input is CVBS signal.

1: Input is VS pin.

ASF_SRC**Acquisition start of field source**

0: ACQ V sync processing is made with ACQ V sync.

1: ACQ V sync processing is made with display V sync.

Set to 0 for normal text acquisition modes.

D3, D2

Reserved. D3, D2 must be 0.

CLMP_DIS**CVBS clamp circuit disable**

For test purposes only. Set to 0.

0: Clamp circuit for CVBS input signal is switched on.

1: Clamp circuit for CVBS input signal is switched off.

EXT_AD**External analog/digital converter selection**

For test purposes only. Set to 0.

0: The on-chip ADC is switched on. An external ADC cannot be connected.

1: The on-chip ADC is switched off and an external ADC can be connected.

D6, D7

Reserved. D6, D7 must be 0.

Subaddress 01101100 b

Block/row/column/byte position 0/00/13/1

Power-on reset initialization 00000000 b

Data dispatched to hardware register Yes

Subaddress autoincrement Yes

R109

ACQUISITION_TIMING_0

RST_SYN	FRZ_INC	ACQ_NTSC	VCRQ/TV	V_THRE	VSAW_WDTH	AVFW_WDTH	AFDM	
---------	---------	----------	---------	--------	-----------	-----------	------	--

AFDM**Acquisition field detection mode**

A field suppression circuit can suppress all V pulses that appear in the second half of a line. With standard signals having interlaced sync the V pulse of the second field is suppressed.

0: Suppression active.

1: No suppression.

The acquisition flywheel needs only a V trigger for the first field. For standard signals this bit should be set to 0.

AVFW_WDTH**Acquisition V-sync distortion filter window width**

0: Small window.

1: Broad window.

The acquisition V-sync signal is accepted only if it is inside the window. A broad window should be used for VCR applications.

The small window suppresses distortion in the V-sync signal until line 312 of each field in 625-line mode or 262 of each field in 525-line mode.

The broad window suppresses distortion in the V-sync signal until line 300 of each field in 625-line mode or 250 of each field in 525-line mode.

VSAW_WDTH**V sync analysis distortion filter window width**

0: Small window.

1: Broad window.

The selected V-sync signal is accepted only if it is inside the window. The broad window should be used for VCR applications.

The small window suppresses distortion in the V-sync signal until line 312 of each field in 625-line mode or 262 of each field in 525-line mode.

The broad window suppresses distortion in the V-sync signal until line 300 of each field in 625-line mode or 250 of each field in 525-line mode.

Referenced bit: VSA_SRC.

V_THRE**Vertical sync pulse threshold**

Switches the time length which detects the V sync pulse of the CVBS signal. In case of noisy CVBS signals V_THRE = 1 can be used.

1: Time length is 13.3 μ s.

0: Time length is 22.6 μ s.

VCRQ/TV**HPLL time constant selection**

HPLL means acquisition PLL.

0: HPLL time constant has a small value (VCR mode).

1: HPLL time constant has a large value (TV mode).

ACQ_NTSC

Acquisition standard

ACQ_NTSC controls the number of lines per frame (625/525) and the TTX bit rate and format.

0: Acquisition works in PAL mode.

1: Acquisition works in NTSC mode.

FRZ_INC

Freeze acquisition PLL increment value

Opens acquisition PLL and freezes the current frequency value.

1: Frequency is frozen.

0: Frequency follows horizontal input frequency.

RST_SYN

Restart acquisition sync processing

After changing the CVBS source it is advisable to restart the sync processing for a faster lock.

Writing a 1 in this bit position holds the sync processing in the reset mode. Setting the bit back to the 0 condition deactivates the reset mode and starts new sync processing.

Subaddress	01101101 b
Block/row/column/byte position	0/00/13/0
Power-on reset initialization	00000000 b
Data dispatched to hardware register	Yes
Subaddress autoincrement	Next subaddress is R104

2.9.3 Clock and Sync Control Registers: R112, R113, R114, R115, R116, R117

R112 SYSTEM_CLOCK_CONTROL

D7	D6	D5	27_TO_24	CLK_EXT	ADP_PLLQ	TD_TO_TA	TA_TO_TD
----	----	----	----------	---------	----------	----------	----------

Display clock selection overview:

27_TO_24	EXT_PLL	CLK_EXT	ADP_PLLQ	TA_TO_TD	Input at Pin CLK	Output of Analog Display PLL	Display Clock Frequency (4:3 mode)	Display Clock Source
x	x	0	0	0	Not used	24 MHz	24 MHz	Int./Display
0	0	1	0	0	24 MHz	24 MHz	24 MHz	Ext./anl. PLL
1	0	1	0	0	27 MHz	24 MHz	24 MHz	Ext./anl. PLL
x	1	1	0	0	6 MHz	24 MHz	24 MHz	Ext./anl. PLL
x	x	x	1	0	24 MHz	Not used	24 MHz	Ext./direct
x	x	x	x	1	Not used	Not used	24 MHz	Int./acqu.

TA_TO_TD

1: Acquisition clock feeds the display clock.

0: Display clock comes from external clock or from the display PLL.

Referenced bits: ADP_PLLQ, CLK_EXT.

TD_TO_TA

1: Display clock feeds the acquisition clock.

0: Acquisition clock comes from the acquisition PLL.

ADP_PLLQ**Analog display PLL selection**

0: Analog display PLL is active.

1: Analog display PLL is bypassed.

The analog display PLL multiplies the frequency of its input signal (typ. 6 MHz) by 4 and delivers a typ. 24-MHz output frequency. If the analog display PLL is bypassed, the external clock is directly used as the display clock if the external clock source is selected.

Referenced bits: CLK_EXT, 27_TO_24, EXT_PLL.

CLK_EXT**System clock from external source at CLK pin**

0: System clock is internal.

1: System clock is external.

Referenced bits: TA_TO_TD, TD_TO_TA, ADP_PLLQ.

27_TO_24**External clock frequency division control 1**

This bit controls the frequency of the input signal of the analog display PLL. This signal is derived from the external clock and may be divided by 1, 4 or by 4.5.

Referenced bits: EXT_PLL, ADP_PLLQ.

D7 – D5

Not used. D7 – D5 must be 0.

Subaddress	01110000 b
Block/row/column/byte position	0/00/14/5
Power-on reset initialization	IRAM: 00000000 b, Hardware: 00000010 b
Data dispatched to hardware register	Yes
Subaddress autoincrement	Yes

R113**SYNC_SOURCE_SELECTION**

D7	DLC_CTRQ	D5 = 0	EXT_PLL	DSF_SRC_1	DSF_SRC_0	DSL_SRC_1	DSL_SRC_0	
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DSL_SRC_1, DSL_SRC_0**Display start of line source**

The sequence of setting or resetting these bits is important when changing from lock_mode to freerun or vice versa. The function of these bits depends also on the DPLL_LOCK bit as shown in the following table. Please refer to the hardware application note "sync".

DPLL_LOCK	DSL_SRC_1	DSL_SRC_0	Horizontal Display Sync Source
0	0	0	Freerun
0	0	1	CVBS (set R112, D0: = 1) ^{*)}
1	0	0	HS
1	0	1	VCS
1	1	1	CVBS PLL feeds display PLL

^{*)} please refer to the application note sync

Referenced bit: DPLL_LOCK.

DSF_SRC_1, DSF_SRC_0**Display start of field source**

The following table shows the source selection with DSF_SRC_1 and DSF_SRC_0 bits to generate internal start of display field.

DSF_SRC_1	DSF_SRC_0	Source
0	0	CVBS pin
0	1	Reserved
1	0	VS pin (without internal V integration)
1	1	VCS pin (with internal V integration)

D4

Reserved. D4 must be 0.

EXT_PLL**External clock frequency division control**

Refer to R112: Display clock selection overview.

D5

Reserved. D5 must be 0.

DLC_CTRQ**Display line counter clock control**

V pulses – if not suppressed by bit DFDM (R116) – reset the line counter to line 1 of a field. The reset may be delayed to the start of the next line for V pulses appearing in the second half of a line indicating the start of the second field. This is necessary for counting correct line numbers of standard interlaced sync signals. For other signals this feature may be switched off.

0: Line counter reset delay active in the second field.

1: V resets line counter immediately.

D7

Not used. D7 must be 0.

Subaddress 01110001 b

Block/row/column/byte position 0/00/14/4

Power-on reset initialization 00000000 b

Data dispatched to hardware register Yes

Subaddress autoincrement Yes

R114**DISPLAY_PLL_CONTROL**

HALF_DLC	DPLL_2HS	100 Hz	DLP	DPLL_LOCK	16_BY_9	HS_HALF	DPLL_FRQ_0
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The horizontal display PLL has a period of typically 1536 display clocks or 64 μ s. The PLL output signals can be generated with a period of

1536 clocks/64 μ s for normal displays or

768 clocks/32 μ s for double scan displays.

To lock the PLL on an external 31.25 kHz horizontal pulse from a double scan source, a divider 1:2 has to be activated. For progressive scan or 100/120-Hz display the display line counter has to be adjusted.

MEGATEXT display freerun modes:

16_BY_9	DLP	DPLL_FRQ_0	Display Clock	Pixel Rate (double speed)	Display Standard
0	0	0	24.0 MHz	24.0 MHz	4:3 PAL
0	0	1	24.192 MHz	24.192 MHz	4:3 NTSC
0	1	0	25.5 MHz	25.5 MHz	–
0	1	1	25.704 MHz	25.704 MHz	–
1	1	0	25.5 MHz	31.875 MHz	16:9 PAL
1	1	1	25.704 MHz	32.130 MHz	16:9 NTSC

MEGATEXT display PLL lock modes:

16_BY_9	DLP	HS Input	Display Clock	Pixel Rate (double speed)	Display Standard
0	0	15.625 kHz	24.0 MHz	24.0 MHz	4:3 PAL
0	0	15.500 kHz	24.192 MHz	24.192 MHz	4:3 NTSC
0	1	15.625 kHz	25.5 MHz	25.5 MHz	–
0	1	15.500 kHz	25.704 MHz	25.704 MHz	–
1	1	15.625 kHz	25.5 MHz	31.875 MHz	16:9 PAL
1	1	15.500 kHz	25.704 MHz	32.13 MHz	16:9 NTSC

DPLL_FRQ_0**Display PLL freerun selection**

0: 64.0 μ s horizontal period for PAL.

1: 63.5 μ s horizontal period for NTSC.

HS_HALF

This bit activates a prescaler which divides a double scan H-sync input to a 15.6-kHz signal to enable the DPLL to lock.

0: Prescaler not active.

1: Prescaler active.

Remark: This bit works only in MEGATEXT versions C. In the MEGATEXT emulator version the function of HS_HALF is attached to the bit 100 Hz.

16_BY_9**Pixel rate selection**

This bit controls the function of a FIFO which is placed in front of the RGB DACs and can accelerate the pixel rate from typ. 12/24 MHz to 16/32 MHz. It also controls the analog PLL which derives the 24/32-MHz pixel clock from the display clock.

0: FIFO bypassed, ratio pixel rate/display clock is 1.

1: FIFO active, ratio pixel rate/display clock is 1.25.

Remark: This bit works only in MEGATEXT versions C.

DPLL_LOCK**Display PLL lock mode selection**

For description of this bit see bits DSL_SRC_1 and DSL_SRC_0 in register "SYNC_SOURCE_SELECTION".

DLP**Display PLL control for clocks per line selection**

0: 1536 clocks per line for 4:3 display mode.

1: 1632 clocks per line for 16:9 display mode.

100 Hz**100/120-Hz display and sync control**

This bit has to be set for 100/120-Hz display generation and sync processing. The period of all DPLL output signals is reduced by 2 to generate a 100-Hz display and sync timing.

0: 50/60-Hz display and sync.

1: 100/120-Hz display and sync.

(In the emulator version of MEGATEXT this bit has also the function of "HS_HALF" in the same register.)

DPLL_2HS

Double scan display control

This bit can be used to generate a 50/60-Hz double scan display. In this case the DPLL generates double scan timing for the display generator. DPLL_2HS does not affect vertical processing.

0: Normal scan DPLL output signals.

1: Double scan DPLL output signals.

HALF_DLC

Display line counter prescaler control

The display line counter counts the line pulses of the display PLL output.

0: Prescaler disabled for

100/120-Hz double scan displays or

50/60-Hz normal scan displays.

1: Prescaler active for

50/60-Hz double scan displays (progressive scan mode).

Subaddress

01110010 b

Block/row/column/byte position

0/00/14/3

Power-on reset initialization

00000000 b

Data dispatched to hardware register

Yes

Subaddress autoincrement

Yes

R115

BLACK_LEVEL_CLAMP

CW1	CW0	CC5	CC4	CC3	CC2	CC1	CC0	
-----	-----	-----	-----	-----	-----	-----	-----	--

Referenced bits: 100 Hz, DLP.

This register allows programmable control of the display D/A converter switch-off time during the black level sync pulse shoulder.

CC5 – CC0

Clamp count bits

The value of CC is proportional to the time delay from DSOL (display start of line) on, after which the DAC will be switched off.

The range is: $0 \leq CC \leq 63$.

The delay time t_{delay} is calculated as follows:

$t_{\text{delay}} = 0.25 \mu\text{s} + (n \times (1 \mu\text{s} + CC \mu\text{s}))$ with n as given in the following table:

n	100 Hz	DLP
0.5	1	0
1.0	1	1
1.0	0	0
2.0	0	1

CW1, CW0

Clamp width bits

The value of CW is proportional to the switch-off time of the D/A converter.

The range is: $0 \leq CW \leq 3$.

The switch-off time is given in the following table:

$t_{\text{switch OFF}}$	CW
$4 \mu\text{s} \times m$	0
$4 \mu\text{s} \times m$	1
$8 \mu\text{s} \times m$	2
$12 \mu\text{s} \times m$	3

with m as given in the following table:

m	100 Hz
1	0
0.5	1

Subaddress	01110011 b
Block/row/column/byte position	0/00/14/2
Power-on reset initialization	00000000 b
Data dispatched to hardware register	Yes
Subaddress autoincrement	Yes

R116

DISPLAY_TIMING

DFRE_RUNQ	DFRE_MOD_2	DFRE_MOD_1	DFRE_MOD_0	DV_DIS	DV_FILTQ	DVFW_WDTH	DFDM	
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DFDM

Display field detection mode

A field suppression circuit can suppress all V pulses that appear in the second half of a line. If the V delay is correct, the pulses of the second field are suppressed.

0: Suppression active.

1: No suppression.

The flywheel needs only a V trigger for the first field. When flywheel is used, this bit should be set to 0.

DVFW_WDTH

Display V-sync distortion filter window width

0: Small window.

1: Broad window.

The display V-sync signal is accepted only if it is inside the window. The broad window should be used for VCR applications.

The small window suppresses distortion in the V-sync signal until line
312 of each field in 625-line mode or
262 of each field in 525-line mode.

The broad window suppresses distortion in the V-sync signal until line
300 of each field in 625-line mode or
250 of each field in 525-line mode.

DV_FILTQ Display V-sync distortion filter disable

0: V-sync distortion filter enable.
 1: V-sync distortion filter disable.

DV_DIS External display V-sync disable

This bit is for test purposes only. Set to 0.

0: V-sync selected by sync source selection bits is processed for display V-sync generation.

1: Display V-sync is generated only by the display line counter (flywheel or counter overflow).

Referenced bit: VS_OUT_EN.

DFRE_MOD_2 – Display raster selection**DFRE_MOD_0**

These bits affect:

- the sync pulses of the TCS signal which is available at TCSQ pin,
- the VS signal which is available at VS pin (interlaced/non interlaced),
- V-sync distortion filter window (50/60 Hz).

The possible raster selections are:

- 625 lines interlace,
- 625 lines non-interlace,
- 525 lines interlace,
- 525 lines non-interlace.

They are listed in the following table:

DFRE_MOD_2.1.0	Raster	Lines in Field 1/Field 2
000	Non-interlaced	313 / 312 (text mode 50/100 Hz)
001	Non-interlaced	312 / 312 (terminal mode 50/100 Hz)
010	Interlaced	313 / 312 (mix mode 50/100 Hz)
011	Non-interlaced	625 / 625 (progressive scan mode 50 Hz)
100	Non-interlaced	263 / 262 (text mode 60/120 Hz)
101	Non-interlaced	262 / 262 (terminal mode 60/120 Hz)
110	Interlaced	263 / 262 (mix mode 60/120 Hz)
111	Non-interlaced	525 / 525 (progressive scan mode 60 Hz)

Remark: The TCS signal at TCSQ pin is only for normal scan mode.

Referenced bit: DFRE_RUNQ.

DFRE_RUNQ Display V-sync flywheel control

0: Display V-sync flywheel enable. Display V-sync is processed with flywheel.

1: Display V-sync flywheel disable. Display V-sync is processed without flywheel.

Subaddress	01110100 b
Block/row/column/byte position	0/00/14/1
Power-on reset initialization	00000000 b
Data dispatched to hardware register	Yes
Subaddress autoincrement	Yes

R117

V_DELAY_SETTING

D7	CLKSYM	DPLL_RESP	DV_DLY_4	DV_DLY_3	DV_DLY_2	DV_DLY_1	DV_DLY_0
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DV_DLY_4 – DV_DLY_0

Display vertical sync delay for out of standard signals

The display vertical sync signal is delayed from 0 up to 62 μ s.

Delay resolution is 2 μ s.

$0 \leq DV_DLY_4 - DV_DLY_0 \leq 31$.

To detect the right frame information of non-standard signals, the display vertical sync has to be shifted to the right position in the line by delay. Note that the display line counter may be affected by this delay.

DPLL_RESP

Selection of a faster or slower response of the display PLL

0: KP = 4 faster response.

1: KP = 2 slower response.

CLKSYM

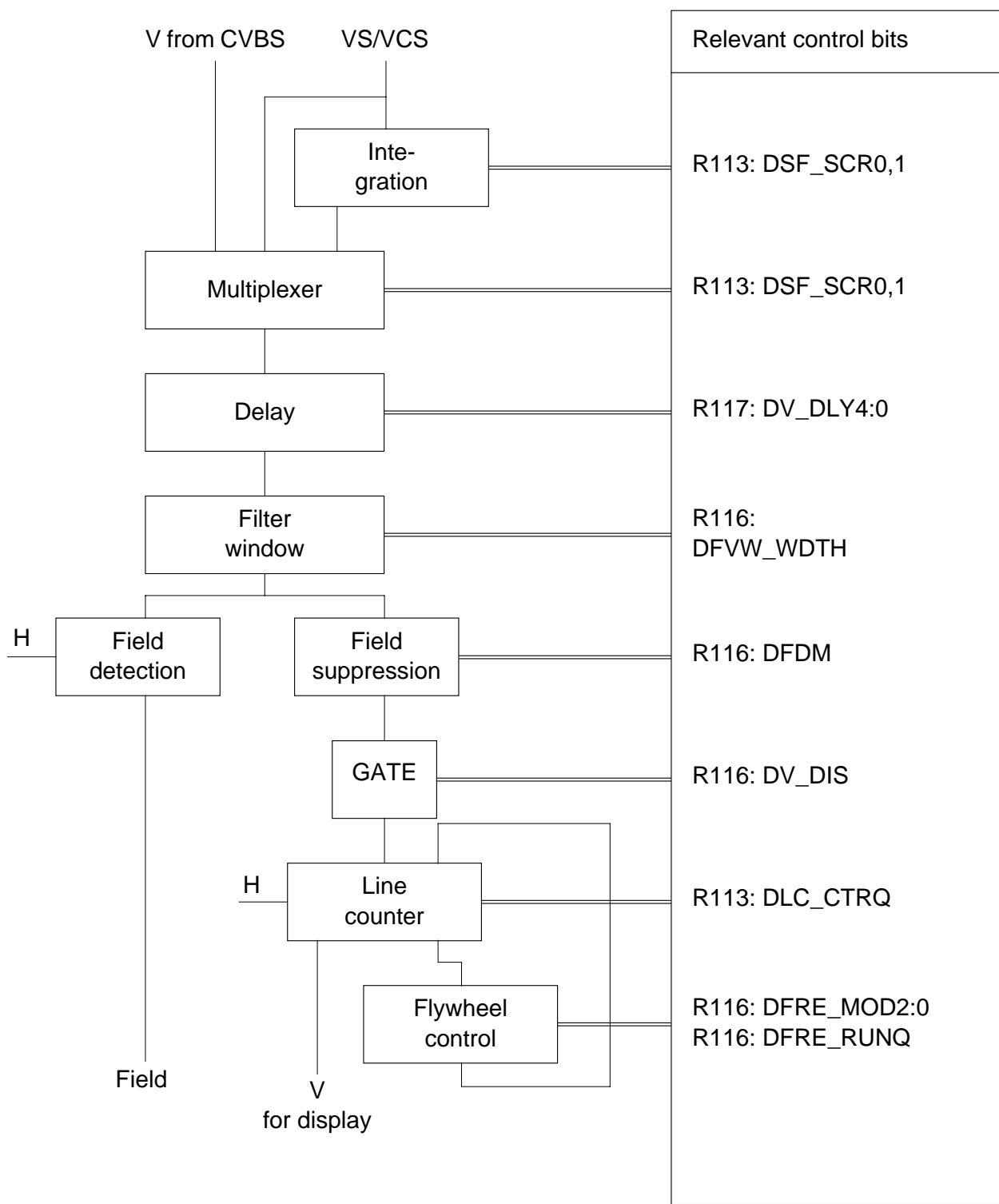
Display Clock Symmetrie adjustment must be 0

D7

Not used. D7 must be 0.

Subaddress	01110101 b
Block/row/column/byte position	0/00/14/0
Power-on reset initialization	00000000 b
Data dispatched to hardware register	Yes
Subaddress autoincrement	Next subaddress is R104

Flow Chart of Vertical Processing for Display
(influence of control bits)



2.10 TOP_COM_BAS Registers: R120, R121, R122

The TOP_COM_BAS registers are used to configure the compressed linked basic TOP tables start address.

R120

TOP_COM_BAS_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

Referenced registers: TOP_COM_BAS_1, TOP_COM_BAS_0.

The interpretation of the bits is the same as explained for the “ADDRESS_POINTER_0_2” register.

Subaddress 01111000 b
 Block/row/column/byte position 0/00/15/5
 Power-on reset initialization 00000000 b
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

R121

TOP_COM_BAS_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	0	0	0
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

Referenced registers: TOP_COM_BAS_2, TOP_COM_BAS_0.

The interpretation of the bits is the same as explained for the “ADDRESS_POINTER_0_1” register.

Subaddress 01111001 b
 Block/row/column/byte position 0/00/15/4
 Power-on reset initialization 00000000 b
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

R122

TOP_COM_BAS_0

0	0	0	0	0	0	0	NIL
---	---	---	---	---	---	---	-----

Referenced registers: TOP_COM_BAS_2, TOP_COM_BAS_1.

NIL

1: No table allocated.
 0: TOP_COM_BAS_2 – TOP_COM_BAS_0 point to the start address of the compressed linked basic TOP table.

Subaddress 01111010 b
 Block/row/column/byte position 0/00/15/3
 Power-on reset initialization 00000000 b
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

2.11 Page Trace Registers: R123, R124, R125

The page trace registers are used to configure the page trace memory start address.

R123 PT_ADR_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

Referenced registers: PT_ADR_1, PT_ADR_0.

The interpretation of the bits is the same as explained for the “PB_ADR_2” register.

Subaddress 01111011 b
 Block/row/column/byte position 0/00/15/2
 Power-on reset initialization 00000000 b
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

R124 PT_ADR_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	0	0	0
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

Referenced registers: PT_ADR_2, PT_ADR_0.

The interpretation of the bits is the same as explained for the “PB_ADR_1” register.

Subaddress 01111100 b
 Block/row/column/byte position 0/00/15/1
 Power-on reset initialization 00000000 b
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

R125 PT_ADR_0

0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

Referenced registers: PT_ADR_2, PT_ADR_1.

The interpretation of the bits is the same as explained for the “PB_ADR_0” register.

Subaddress 01111101 b
 Block/row/column/byte position 0/00/15/0
 Power-on reset initialization 00000000 b
 Data dispatched to hardware register No
 Subaddress autoincrement Yes

R255 POWER_ON_RESET

Register is not implemented.

Subaddress 11111111 b
 Writing this subaddress to SDA 5273 generates a power on reset.

3 Register Quick Reference

This chapter gives a survey of all M3L-Bus registers. It includes their subaddress, symbolic names of registers and bits. Data written to subaddresses which are labeled with “(H)” are dispatched to corresponding hardware registers.

Packet Buffer Registers

R0 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

R1 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

R2 PB_LENGTH

PB_L_07	PB_L_06	PB_L_05	PB_L_04	PB_L_03	PB_L_02	PB_L_01	PB_L_00
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R3 PB_ADR_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

R4 PB_ADR_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	BI_ADR_10	BI_ADR_9	BI_ADR_8
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

R5 PB_ADR_0

BI_ADR_7	BI_ADR_6	BI_ADR_5	BI_ADR_4	BI_ADR_3	BI_ADR_2	BI_ADR_1	BI_ADR_0
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MCI Parameter Registers

R8 MCI0_5

MCI0_5_7	MCI0_5_6	MCI0_5_5	MCI0_5_4	MCI0_5_3	MCI0_5_2	MCI0_5_1	MCI0_5_0	
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R9 MCI0_4

MCI0_4_7	MCI0_4_6	MCI0_4_5	MCI0_4_4	MCI0_4_3	MCI0_4_2	MCI0_4_1	MCI0_4_0	
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R10 MCI0_3

MCI0_3_7	MCI0_3_6	MCI0_3_5	MCI0_3_4	MCI0_3_3	MCI0_3_2	MCI0_3_1	MCI0_3_0	
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R11 MCI0_2

MCI0_2_7	MCI0_2_6	MCI0_2_5	MCI0_2_4	MCI0_2_3	MCI0_2_2	MCI0_2_1	MCI0_2_0	
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R12 MCI0_1

MCI0_1_7	MCI0_1_6	MCI0_1_5	MCI0_1_4	MCI0_1_3	MCI0_1_2	MCI0_1_1	MCI0_1_0	
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R13 MCI0_0

MCI0_0_7	MCI0_0_6	MCI0_0_5	MCI0_0_4	MCI0_0_3	MCI0_0_2	MCI0_0_1	MCI0_0_0	
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R16 MCI1_5

MCI1_5_7	MCI1_5_6	MCI1_5_5	MCI1_5_4	MCI1_5_3	MCI1_5_2	MCI1_5_1	MCI1_5_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

R17 MCI1_4

MCI1_4_7	MCI1_4_6	MCI1_4_5	MCI1_4_4	MCI1_4_3	MCI1_4_2	MCI1_4_1	MCI1_4_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

R18 MCI1_3

MCI1_3_7	MCI1_3_6	MCI1_3_5	MCI1_3_4	MCI1_3_3	MCI1_3_2	MCI1_3_1	MCI1_3_0	
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R19 MCI1_2

MCI1_2_7	MCI1_2_6	MCI1_2_5	MCI1_2_4	MCI1_2_3	MCI1_2_2	MCI1_2_1	MCI1_2_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

R20 MCI1_1

MCI1_1_7	MCI1_1_6	MCI1_1_5	MCI1_1_4	MCI1_1_3	MCI1_1_2	MCI1_1_1	MCI1_1_0	
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R21 MCI1_0

MCI1_0_7	MCI1_0_6	MCI1_0_5	MCI1_0_4	MCI1_0_3	MCI1_0_2	MCI1_0_1	MCI1_0_0	
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MCI Parameter Registers (cont'd)

R24 MCI2_5

MCI2_5_7	MCI2_5_6	MCI2_5_5	MCI2_5_4	MCI2_5_3	MCI2_5_2	MCI2_5_1	MCI2_5_0	
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R25 MCI2_4

MCI2_4_7	MCI2_4_6	MCI2_4_5	MCI2_4_4	MCI2_4_3	MCI2_4_2	MCI2_4_1	MCI2_4_0	
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R26 MCI2_3

MCI2_3_7	MCI2_3_6	MCI2_3_5	MCI2_3_4	MCI2_3_3	MCI2_3_2	MCI2_3_1	MCI2_3_0	
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R27 MCI2_2

MCI2_2_7	MCI2_2_6	MCI2_2_5	MCI2_2_4	MCI2_2_3	MCI2_2_2	MCI2_2_1	MCI2_2_0	
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R28 MCI2_1

MCI2_1_7	MCI2_1_6	MCI2_1_5	MCI2_1_4	MCI2_1_3	MCI2_1_2	MCI2_1_1	MCI2_1_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

R29 MCI2_0

MCI2_0_7	MCI2_0_6	MCI2_0_5	MCI2_0_4	MCI2_0_3	MCI2_0_2	MCI2_0_1	MCI2_0_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

R32 MCI3_5

MCI3_5_7	MCI3_5_6	MCI3_5_5	MCI3_5_4	MCI3_5_3	MCI3_5_2	MCI3_5_1	MCI3_5_0	
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R33 MCI3_4

MCI3_4_7	MCI3_4_6	MCI3_4_5	MCI3_4_4	MCI3_4_3	MCI3_4_2	MCI3_4_1	MCI3_4_0	
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R34 MCI3_3

MCI3_3_7	MCI3_3_6	MCI3_3_5	MCI3_3_4	MCI3_3_3	MCI3_3_2	MCI3_3_1	MCI3_3_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

R35 MCI3_2

MCI3_2_7	MCI3_2_6	MCI3_2_5	MCI3_2_4	MCI3_2_3	MCI3_2_2	MCI3_2_1	MCI3_2_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

R36 MCI3_1

MCI3_1_7	MCI3_1_6	MCI3_1_5	MCI3_1_4	MCI3_1_3	MCI3_1_2	MCI3_1_1	MCI3_1_0	
----------	----------	----------	----------	----------	----------	----------	----------	--

MCI Command Register

R37 MCI_COMMAND

CMD_7	CMD_6	CMD_5	CMD_4	CMD_3	CMD_2	CMD_1	CMD_0	
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Free CHAP Chain Control Registers

R40 FFP_CHAP_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

R41 FFP_CHAP_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	0	0	0
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

R42 FFP_CHAP_0

0	0	0	0	0	0	0	NIL
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R43 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
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R44 NF_CHAP_1

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

R45 NF_CHAP_0

NF_C_7	NF_C_6	NF_C_5	NF_C_4	NF_C_3	NF_C_2	NF_C_1	NF_C_0
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Address Pointer and Data-Port Registers

R48 ADDRESS_POINTER_0_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

R49 ADDRESS_POINTER_0_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	ROW_4	ROW_3	ROW_2
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

R50 ADDRESS_POINTER_0_0

ROW_1	ROW_0	COL_5	COL_4	COL_3	COL_2	COL_1	COL_0
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R51 DATA_PORT_0

DATA_P_07	DATA_P_06	DATA_P_05	DATA_P_04	DATA_P_03	DATA_P_02	DATA_P_01	DATA_P_00
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R52 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
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R53 PORT_0_CONTROL

D7	D6	BRC_INC_5	BRC_INC_4	BRC_INC_ON	BI_ADR	RWINC_OFF	CLINC_OFF
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R56 ADDRESS_POINTER_1_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

R57 ADDRESS_POINTER_1_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	ROW_4	ROW_3	ROW_2
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

R58 ADDRESS_POINTER_1_0

ROW_1	ROW_0	COL_5	COL_4	COL_3	COL_2	COL_1	COL_0
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R59 DATA_PORT_1

DATA_P_17	DATA_P_16	DATA_P_15	DATA_P_14	DATA_P_13	DATA_P_12	DATA_P_11	DATA_P_10
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R60 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

R61 PORT_1_CONTROL

D7	D6	BRC_INC_5	BRC_INC_4	BRC_INC_ON	BI_ADR	RWINC_OFF	CLINC_OFF
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Free p80 Chain Control Registers

R64 FFP_P80_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

R65 FFP_P80_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	ROW_4	ROW_3	ROW_2
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

R66 FFP_P80_0

ROW_1	ROW_0	0	0	0	0	0	NIL
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R67 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

R68 NF_P80_1

NF_8_15	NF_8_14	NF_8_13	NF_8_12	NF_8_11	NF_8_10	NF_8_9	NF_8_8
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R69 NF_P80_0

NF_8_7	NF_8_6	NF_8_5	NF_8_4	NF_8_3	NF_8_2	NF_8_1	NF_8_0
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Free p40 Chain Control Registers

R72 FFP_P40_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

R73 FFP_P40_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	ROW_4	ROW_3	ROW_2
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

R74 FFP_P40_0

ROW_1	ROW_0	0	0	0	0	0	NIL
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R75 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

R76 NF_P40_1

NF_4_15	NF_4_14	NF_4_13	NF_4_12	NF_4_11	NF_4_10	NF_4_9	NF_4_8
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R77 NF_P40_0

NF_4_7	NF_4_6	NF_4_5	NF_4_4	NF_4_3	NF_4_2	NF_4_1	NF_4_0
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Hardware Control Registers

Input/Output Control Registers

R80 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0	
----	----	----	----	----	----	----	----	--

R81 (H) SLICER_CONTROL

D7	D6	SLC_WD	PFC_1	PFC_0	FQC_1	FQC_0	MCC	
----	----	--------	-------	-------	-------	-------	-----	--

R82 (H) OUTPUT_PIN_CONTROL

CLK_OUT	GPOC_1	GPOC_0	TCS_FLD_2	TCS_FLD_1	TCS_FLD_0	HS_OUT	VS_OUT	
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R83 (H) RGB_CONTROL

RGB_GAIN_4	RGB_GAIN_3	RGB_GAIN_2	RGB_GAIN_1	RGB_GAIN_0	RGB_LVL_2	RGB_LVL_1	RGB_LVL_0	
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R84 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0	
----	----	----	----	----	----	----	----	--

R85 (H) DISPLAY_VCO

D7	D6	D5	D4	D_VCO_3	D_VCO_2	D_VCO_1	D0	
----	----	----	----	---------	---------	---------	----	--

Memory Allocation Registers

R88 IAT_2

ABLK_3_5	ABLK_3_4	ABLK_3_3	ABLK_3_2	ABLK_3_1	BLK_3_0	ABLK_2_5	ABLK_2_4	
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R89 IAT_1

ABLK_2_3	ABLK_2_2	ABLK_2_1	ABLK_2_0	ABLK_1_5	ABLK_1_4	ABLK_1_3	ABLK_1_2	
----------	----------	----------	----------	----------	----------	----------	----------	--

R90 IAT_0

ABLK_1_1	ABLK_1_0	ABLK_0_5	BLK_0_4	ABLK_0_3	ABLK_0_2	ABLK_0_1	ABLK_0_0	
----------	----------	----------	---------	----------	----------	----------	----------	--

R91 XAT_2

ACHP_23	ACHP_22	ACHP_21	ACHP_20	ACHP_19	ACHP_18	ACHP_17	ACHP_16	
---------	---------	---------	---------	---------	---------	---------	---------	--

R92 XAT_1

ACHP_15	ACHP_14	ACHP_13	ACHP_12	ACHP_11	ACHP_10	ACHP_9	ACHP_8	
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R93 XAT_0

ACHP_7	ACHP_6	ACHP_5	ACHP_4	ACHP_3	ACHP_2	ACHP_1	ACHP_0	
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Data Line Selection Registers

R96 (H) DEW_START_LINE

D7	D6	D5	DEW_STR_LN_4	DEW_STR_LN_3	DEW_STR_LN_2	DEW_STR_LN_1	DEW_STR_LN_0
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R97 (H) DEW_END_LINE

D7	D6	D5	DEW_END_LN_	4	DEW_END_LN_3	DEW_END_LN_2	DEW_END_LN_1
----	----	----	-------------	---	--------------	--------------	--------------

R98 (H) SINGLE_DATA_LINE

D7	D6	D5	SNG_LN_4	SNG_LN_3	SNG_LN_2	SNG_LN_1	SNG_LN_0
----	----	----	----------	----------	----------	----------	----------

R99 (H) TTX_FRAMING_WINDOW

TFW_END_3	TFW_END_2	TFW_END_1	TFW_END_0	TFW_STR_3	TFW_STR_2	TFW_STR_1	TFW_STR_0
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R100 (H) EXTRA_FRAMING_WINDOW

XFW_END_3	XFW_END_2	XFW_END_1	XFW_END_0	XFW_STR_3	XFW_STR_2	XFW_STR_1	XFW_STR_0
-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------

R101 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Acquisition Control Registers

R104 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

R105 RECEPTION_THRESHOLD

HCB_CHECK	ACQR_HEAD	ACQR_MGRW	FC_ERR_1	MAG_ERR_2	MAG_ERR_1	ROW_ERR_2	ROW_ERR_1
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R106 PSEUDO_PACKET_ENABLE

0	0	0	0	EN_X_28	EN_X_27	EN_X_26	EN_X_25
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R107 RESERVED

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

R108 (H) ACQUISITION_TIMING_1

D7	D6	EXT_AD	CLMP_DIS	D3	D2	ASF_SRC	VSA_SRC
----	----	--------	----------	----	----	---------	---------

R109 (H) ACQUISITION_TIMING_0

RST_SYN	FRZ_INC	ACQ_NTSC	VCRQ/TV	V_THRE	VSAW_WDTH	AVFW_WDTH	AFDM
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Clock and Sync Control Registers

R112 (H) SYSTEM_CLOCK_CONTROL

D7	D6	D5	27_TO_24	CLK_EXT	ADP_PLLQ	TD_TO_TA	TA_TO_TD	
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R113 (H) SYNC_SOURCE_SELECTION

D7	DLC_CTRQ	D5 = 0	EXT_PLL	DSF_SRC_1	DSF_SRC_0	DSL_SRC_1	DSL_SRC_0	
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R114 (H) DISPLAY_PLL_CONTROL

HALF_DLC	DPLL_2HS	100 Hz	DLP	DPLL_LOCK	16_BY_9	HS_HALF	DPLL_FRQ_0	
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R115 (H) BLACK_LEVEL_CLAMP

CW1	CW0	CC5	CC4	CC3	CC2	CC1	CC0	
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R116 (H) DISPLAY_TIMING

DFRE_RUNQ	DFRE_MOD_2	DFRE_MOD_1	DFRE_MOD_0	DV_DIS	DV_FILTQ	DVFW_WIDTH	DFDM	
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R117 (H) V_DELAY_SETTING

D7	D6	DPLL_RES0	DV_DLY_4	DV_DLY_3	DV_DLY_2	DV_DLY_1	DV_DLY_0	
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TOP_COM_BAS Registers

R120 TOP_COM_BAS_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

R121 TOP_COM_BAS_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	0	0	0
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

R122 TOP_COM_BAS_0

0	0	0	0	0	0	0	NIL
---	---	---	---	---	---	---	-----

Page Trace Registers

R123 PT_ADR_2

EXT_MEM = 0	0	0	1	BYT_5	BYT_4	BYT_3	BYT_2
EXT_MEM = 1	0	CHP_10	CHP_9	CHP_8	CHP_7	CHP_6	CHP_5

R124 PT_ADR_1

BYT_1	BYT_0	BLK_2	BLK_1	BLK_0	0	0	0
CHP_4	CHP_3	CHP_2	CHP_1	CHP_0			

R125 PT_ADR_0

0	0	0	0	0	0	0	0
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4 Glossary

BDM	Basic Display Memory. 3 to 5 chapters of internal RAM memory used exclusively to store display characters and attributes for the inner screen area.
Block	Internal memory segment of 1024 consecutive doublewords. The first doubleword of a block starts at row/column address 0/0.
Chapter	Internal or external memory of 1024 consecutive bytes aligned to row/column = 0/0.
Displayed page memory	Page memory which is actually converted by S/P-C into basic display memory.
Display word (DPWORD)	Word length = 24 to 48 bits. Depending on the selected display mask registers.
Doubleword	Word length = 48 bits.
DPLL	Display PLL.
EDM	Extended display memory. 5 chapters of internal RAM memory used exclusively to store display characters and attributes for the outer screen area.
HPLL	Acquisition PLL.
IRAM5273.PDF	Program definition file in ASM5273 source code for PU programs. Defines memory mapping.
MEGATEXT controller	Microcontroller connected via M3L Bus with SDA 5273.
MCI	MEGATEXT command interface. Commands for the PU can be given over the MCI. MCI comprises the M3L registers "MCI_COMMAND", "MCI0_5" to "MCI3_1", the M3L bit CMD_RUN and the interrupt signal at INTQ pin.
Page memory	Internal or external memory segment reserved for storing TTX data.
Page request data	Page-related information bits as defined in the world system teletext specification.
PRQ	Page request bits or packet request bits.
PU	Processing unit. On-chip SDA 5273 RISC processor.
S/P-C	Serial-to-parallel attribute conversion, realized with firmware.
Trace memory	Stores traced basic page numbers of the incoming teletext data and a flag which indicates the presence of related subpages.
Word	Word length = 24 bits.

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