

# SIEMENS

## ICs for Consumer Electronics

### MEGATEXT

Serial Bus Interface

Edition 10.94

<b>MEGATEXT® Serial Bus Interface</b>	
<b>Revision History:                      Original Version 10.94</b>	
Previous Releases:	
Page	Subjects (changes since last revision)

## Data Classification

## Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

## Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25\text{ °C}$  and the given supply voltage.

## Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about “**Processing Guidelines**” and “**Quality Assurance**” for ICs, see our “**Short Form Catalog**”.

## Edition 10.94

This edition was realized using the software system FrameMaker®.

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Contents	Page
Introduction . . . . .	4
Documents . . . . .	4
Abbreviations . . . . .	5
I <sup>2</sup> C Bus Mode . . . . .	5
M3L-Mode . . . . .	6
Wait Condition . . . . .	6
Read/Write/Chip Address . . . . .	7
Comparison between I <sup>2</sup> C- and M3L-Mode . . . . .	7
Autoincrement of Bus Registers . . . . .	8
Protocol Examples . . . . .	10

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### Introduction

There are four possible interconnections for communication between the external controller and the MEGATEXT IC: The serial bus port with 2 or 3 pins and the interrupt pin.

All communication with MEGATEXT is done via the serial bus port consisting of the signals I<sup>2</sup>CEN, SCL, SDA. The use of this interface depends on 3 basic parameters:

- I<sup>2</sup>C-protocol / M3L-protocol
- read mode / write mode
- register access / DRAM-access

The I<sup>2</sup>C Bus uses two connections, the pins SDA (data) and SCL (clock), and operates according to the I<sup>2</sup>C Bus specifications which limits the maximum transfer rate at 100 kbit/s. MEGATEXT can handle the I<sup>2</sup>C protocol at a maximum transfer rate of 1 Mbit/s.

The M3L-bus (MEGATEXT 3 Line bus) uses the same two pins SDA and SCL and in addition the pin I<sup>2</sup>CEN. The transfer rate is max. 1 Mbit/s. Microcontrollers from the Siemens range are available with suitable hardware interfaces for either the I<sup>2</sup>C Bus or the M3L-bus.

MEGATEXT always operates in the slave mode; either as receiver or transmitter. It has the chip select address MSB 0010001x LSB in I<sup>2</sup>C Bus mode. The MSB is transmitted first. In M3L-bus mode the LSB is transmitted first and the chip select address is LSB 00100001x MSB.

### Documents

The timing relations and levels of the signals "I<sup>2</sup>CEN, SCL, SDA" are specified under "characteristics" of the MEGATEXT data sheet.

The protocol of the bus transfer is specified:

- for M3L-mode in this document
- for I<sup>2</sup>C-mode in

"SIEMENS I<sup>2</sup>C Bus Technical Description".

### Abbreviations

START	Start conditions: I <sup>2</sup> C: See I <sup>2</sup> C Bus Technical description M3L: Falling edge of I <sup>2</sup> CEN
STOP	Stop conditions: I <sup>2</sup> C: See I <sup>2</sup> C Bus Technical description M3L: Rising edge of I <sup>2</sup> CEN
A	Acknowledge
A*	The acknowledge of the last byte in a read must be high
W	Write
R	Read
SLAVE ADR	7-bit MEGATEXT chip select address
SUB ADR	8-bit internal subaddress

### I<sup>2</sup>C Bus Mode

The serial port is in I<sup>2</sup>C Bus mode when the input pin I<sup>2</sup>CEN is high. The I<sup>2</sup>C Bus interface operates with all clock frequencies between 0 Hz and 1 MHz. The MEGATEXT chip may slow down the transmission rate by holding the clock line low after a byte transmission is terminated by an acknowledge bit. Input filters in the SDA and SCL pins suppress high frequency interference.

The following protocols are supported:

Clock frequency  $0 < f_{SCL} < 1 \text{ MHz}$ :

Writing to the SDA 5273:

START	SLAVE ADR	W	A	SUB ADR	A	DATA	A	DATA	A	...	STOP
-------	-----------	---	---	---------	---	------	---	------	---	-----	------

Read from the SDA 5273:

START	SLAVE ADR	W	A	SUB ADR	A	START	SLAVE ADR	R	A	DATA	A	DATA	A*	...	STOP
-------	-----------	---	---	---------	---	-------	-----------	---	---	------	---	------	----	-----	------

START	SLAVE ADR	W	A	SUB ADR	A	STOP	START	SLAVE ADR	R	A	DATA	A	DATA	A*	...	STOP
-------	-----------	---	---	---------	---	------	-------	-----------	---	---	------	---	------	----	-----	------

Read from the SDA 5273 using a subaddress generated by autoincrement or a subaddress previously transmitted:

START	SLAVE ADR	R	A	DATA	A	DATA	A*	...	STOP
-------	-----------	---	---	------	---	------	----	-----	------

### M3L-Mode

The serial port is in M3L-bus mode when the input pin I<sup>2</sup>CEN is low. The M3L-bus uses the three pins I<sup>2</sup>CEN, SDA and SCL. The M3L-Bus interface operates with all clock frequencies between 0 Hz and 1 MHz. MEGATEXT may occasionally slow down the transmission rate by holding the clock line low. The SDA 5273 only ever holds the eighth clock pulse of a byte and only if the internal processing is blocked by worst case real time acquisition and display functions. Input filters in the SDA- and SCL-pins suppress high frequency interference. Data changes when the SCL-line is high.

A data packet is defined by a frame start and a frame end.

The frame start is a high to low change at the I<sup>2</sup>CEN-pin. The frame end is a low to high change at the I<sup>2</sup>CEN-pin. This stop condition may not occur within 400 ns after the rising edge of the last clock pulse. The data inside a frame are transmitted in 8-bit words. The least significant bit is transmitted first.

The word transfer timing is compatible to an 8051 controller in mode 0.

#### The following protocols are supported:

Clock frequency  $0 < f_{SCL} < 1 \text{ MHz}$ :

Writing to the SDA 5273:

START	SLAVE ADR	W	SUB ADR	DATA	DATA	...	STOP
-------	-----------	---	---------	------	------	-----	------

Read from the SDA 5273:

START	SLAVE ADR	W	SUB ADR	STOP	START	SLAVE ADR	R	DATA	DATA	...	STOP
-------	-----------	---	---------	------	-------	-----------	---	------	------	-----	------

Read from the SDA 5273 using a subaddress generated by autoincrement or a subaddress previously transmitted:

START	SLAVE ADR	R	DATA	DATA	...	STOP
-------	-----------	---	------	------	-----	------

### Wait Condition

If teletext acquisition is active the PU has to do some real time processing that may delay the serial bus processing. To force the external controller to stop the transmission sequence until MEGATEXT is ready for more data, MEGATEXT can force down SCL after the transmission of a complete byte, i.e. in M3L-mode after the rising SCL edge of the last data bit, in I<sup>2</sup>C-mode after the acknowledge bit.

Before the transmission of a new byte the external controller has to check SCL. If SCL is held low the controller has to switch its SCL-output to high impedance and check the state of SCL until it is high again. In I<sup>2</sup>C-mode the SDA-line has to be set to the value of the first bit of the data byte to be transmitted next **before** the controller looks for SCL high level because in I<sup>2</sup>C-mode the rising edge of SCL defines the first bit.

### Read/Write/Chip Address

The last bit of the first transmitted byte following the start condition defines the type of access: 0 = write, 1 = read. The other bits of this byte form the chip address and define which slave IC is accessed by the bus master. The MEGATEXT chip address is 0010 001x (MSB ... LSB) in I<sup>2</sup>C-mode and x100 0100 (MSB ... LSB) in M3L-mode.

Immediately after the transmission of a complete read address the SDA-pin changes from input to output.

### Comparison between I<sup>2</sup>C- and M3L-Mode

Changing from I<sup>2</sup>C- to M3L-mode or vice versa is allowed whenever a bus transfer is completed, i.e. that the wait condition has to be checked after the transmission of the last byte to/from MEGATEXT. The wait condition has to be finished before starting an other bus transfer.

### Characteristics of the I<sup>2</sup>C-Mode

The signal I<sup>2</sup>CEN has to be high to select the I<sup>2</sup>C-mode but is otherwise not part of the I<sup>2</sup>C-protocol. The standard I<sup>2</sup>C Bus is specified for a maximum clock rate of 100 kHz. MEGATEXT allows also clock rates up to 1 MHz with the same protocol but a special timing.

In I<sup>2</sup>C-mode it is possible to skip the stop condition if it is followed by a new start condition.

The MSB of each byte is transmitted first.

Each byte is followed by an acknowledge bit (activ low).

The last acknowledge bit of a read sequence has to be high.

The high level of SCL defines the valid data.

### Characteristics of the M3L-Mode

The M3L-mode is specified for maximum frequencies up to 1 MHz. The signal I<sup>2</sup>CEN defines the start and stop of a M3L-data transfer. The M3L-bus is specified in accordance with mode 0 of the standard USART-interface of the 8051 based micro controller SDA 30C162.

The LSB of each byte is transmitted first.

There is no acknowledge bit defined in M3L-mode.

The low level of SCL defines the valid data.

### Autoincrement of Bus Registers

Autoincrement modes are described on the first pages of the document “M3L-Bus Registers Programmers Reference”.

The addresses of MEGATEXT registers are automatically incremented for maximum 6 subsequent data accesses in a modulo 6 cycle by a hardware increment. Registers with addresses of  $(n \times 8) + 6$  and  $(n \times 8) + 7$ ,  $n = 0, 1, \dots$ , do not exist and are skipped by the autoincrement. If these addresses are transmitted in spite the autoincrement sequence behaves like shown below.

### Autoincrement Address Sequence for Common Registers

Formula	n = 0	1	2	3	4	5	10	11	12	13	14
$(n \times 8) + 6$	–	06	14	22	30	38	78	86	94	102	110
$(n \times 8) + 7$	–	07	15	23	31	39	79	87	95	103	111
$(n \times 8)$	00	08	16	24	32	40	80	88	96	104	112
$(n \times 8) + 1$	01	09	17	24	33	41	81	89	97	105	113
$(n \times 8) + 2$	02	10	18	25	34	42	82	90	98	106	114
$(n \times 8) + 3$	03	11	19	26	35	43	83	91	99	107	115
$(n \times 8) + 4$	04	12	20	27	36	44	84	92	100	108	116
$(n \times 8) + 5$	05	13	21	28	37	45	85	93	101	109	117
$(n \times 8)$	00	08	16	24	32	40	80	88	96	104	112
.											
.											
.											

A special autoincrement sequence was implemented for data port 0. This sequence is also useful for data port 1. For reasons of chip development history this increment sequence applies also for registers number 64 ... 79.

For data ports the increment follows the following scheme:

- port control register (defining the address mode)
- DRAM address pointer registers
- data port register (no further increment)



### Autoincrement Address Sequence for Registers 48 to 79

Formula	n = 6	7	8	9
$(n \times 8) + 5$	53	61	69	77
$(n \times 8)$	48	56	64	72
$(n \times 8) + 1$	49	57	65	73
$(n \times 8) + 2$	50	58	66	74
$(n \times 8) + 3$	51	59	67	75
$(n \times 8) + 3$	51	59	67	75
.				
.				
.				
or				
$(n \times 8) + 6$	54	62	70	76
$(n \times 8) + 7$	55	63	71	77
$(n \times 8)$	48	56	64	72
$(n \times 8) + 1$	49	57	65	73
$(n \times 8) + 2$	50	58	66	74
$(n \times 8) + 3$	51	59	67	75
$(n \times 8) + 3$	51	59	67	75
.				
.				
.				

### Autoincrement of DRAM Addresspointers

The data ports are used to access the internal DRAM or an optional external DRAM. Making use of the register autoincrement it is easy to load down a DRAM-start address followed by a sequence of data bytes for incremented DRAM-addresses. The DRAM-address itself is incremented by firmware. The increment mode for the DRAM-addresses can be selected in register 53 for data port 0 and register 61 for data port 1. DRAM-addresses can be in binary or in row/column format. E.g. in binary mode the increment is byte-by-byte with the byte position sequence 3, 2, 1, 6, 5, 4 and then incrementing the word address. The firmware autoincrement changes the contents of the data port registers. The current address can be checked by reading the data port registers. For more information please refer to the M3L-register reference.

### Protocol Examples

#### Writing data into registers

- start condition
- chip address WRITE
- subaddress of register n
- data for register n
- data for incr. register
- data for incr. register
- ...
- stop condition

#### Writing data into DRAM via data port 0

- start condition
- chip address WRITE
- subaddress of address mode register 53
- address mode data for register 53
- DRAM-address data for register 48
- DRAM-address data for register 49
- DRAM-address data for register 50
- data for DRAM-address to register 51
- data for incremented DRAM-address to register 51
- ...
- stop condition

#### Reading data registers

- start condition
- chip address WRITE
- subaddress of register n
- stop condition (optional in I<sup>2</sup>C-mode)
- start condition
- chip address READ
- data from register n
- data from incr. register
- data from incr. register
- ...
- stop condition

### Reading data from DRAM via data port 0

- start condition
- chip address WRITE
- subaddress of address mode register 53
- address mode data for register 53
- DRAM-address data for register 48
- DRAM-address data for register 49
- DRAM-address data for register 50
- stop condition (optional in I<sup>2</sup>C-mode)
- start condition
- chip address READ
- data from DRAM-address via register 51 to serial bus interface
- data from incremented DRAM-address via register 51 to serial bus interface
- . . .
- stop condition

### Writing data into registers and reading back

- start condition
- chip address WRITE
- subaddress of register n
- data for register n
- data for incr. register
- data for incr. register
- . . .
- stop condition (optional in I<sup>2</sup>C-mode)
- start condition
- chip address WRITE
- subaddress of register n
- stop condition (optional in I<sup>2</sup>C-mode)
- start condition
- chip address READ
- data from register n
- data from incr. register
- data from incr. register
- . . .
- stop condition

### Writing data to DRAM via data port 0 and reading back

- start condition
- chip address WRITE
- subaddress of address mode register 53
- address mode data for register 53
- DRAM-address data for register 48
- DRAM-address data for register 49
- DRAM-address data for register 50
- data for DRAM-address to register 51
- data for incremented DRAM-address to register 51
- ...
- stop condition (optional in I<sup>2</sup>C-mode)
  
- start condition
- chip address WRITE
- subaddress of address mode register 53
- address mode data for register 53
- DRAM-address data for register 48
- DRAM-address data for register 49
- DRAM-address data for register 50
- stop condition (optional in I<sup>2</sup>C-mode)
  
- start condition
- chip address READ
- data from DRAM-address via register 51 to serial bus
- data from incr. DRAM-address via register 51 to serial bus
- ...
- stop condition

If some of the DRAM-address data is already defined the unchanged data need not be transmitted again. For example:

- start condition
- chip address WRITE
- subaddress of address mode register 49
- DRAM-address data for register 49
- DRAM-address data for register 50

In this example the registers 53 and 48 have already been loaded with the right data.

In I<sup>2</sup>C-mode it is possible to skip the stop condition if it is followed by a new start condition.

Changing from I<sup>2</sup>C- to M3L-mode or vice versa is allowed whenever a bus transfer is completed. I.e. that the wait condition has to be checked after the transmission of the last byte to/from MEGATEXT. The wait condition has to be finished before starting an other bus transfer.